MN3665A

10000-Bit High-Resolution CCD Linear Image Sensor

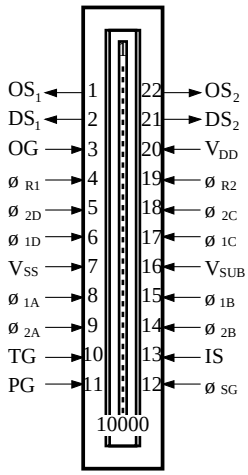
■ Overview

The MN3665A is a high-speed high-resolution CCD linear image sensor having low dark output floating photodiodes in the photodetector region and CCD analog shift registers for read out.
It provides large output at a high S/N ratio for visible light inputs over a wide range of wavelength.

■ Features

- 10000 floating photodiodes and n-channel buried type CCD shift registers for read out are integrated in a single chip.
- An A3 size document can be read with a high resolution of 800dpi.
- Permits high speed scanning of a data rate of 6MHz.
- High blue responsivity of a maximum responsivity ratio of 60% (typ.) at 400nm, and smooth spectral response over the entire visible region.
- Large signal output of 1.6V (typ.) at saturation can be obtained.
- Since a compensation output pin (DS) is provided in addition to the signal output pin (OS), it is possible to obtain a signal with a high S/N ratio by carrying out differential amplification of the OS and DS outputs.
- Operation with a single +12V positive power supply.

■ Pin Assignments

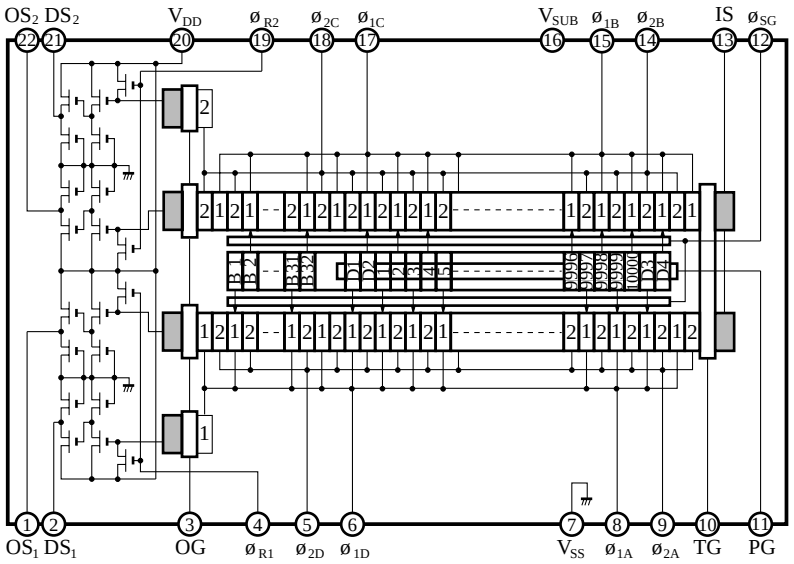


(Top View)
(C23) WDIP022-C-0400D

■ Application

- Graphic and character read out in fax machines, image scanners, etc.

■ Block Diagram



B1 to B32 : Black reference pixels
D1 to D 4 : Dummy invalid pixels

■ Absolute Maximum Ratings (Ta=25˚C, V_{SS}=0V)

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	– 0.3 to +17	V
	V_{SUB}	– 0.3 to +17	V
	V_{IS}	– 0.3 to +17	V
	V_{OG}	– 0.3 to +17	V
	V_{PG}	– 0.3 to +17	V
Input pin voltage	V_I	– 0.3 to +17	V
Output pin voltage	V_O	– 0.3 to +17	V
Operating temperature range	T_{opr}	–20 to + 60	˚C
Storage temperature range	T_{stg}	–40 to +100	˚C

■ Operating Conditions

• Voltage conditions (Ta=–20 to + 60˚C, V_{SS}=0V)

Parameter	Symbol	Condition	min	typ	max	Unit
Power supply voltage	V_{DD}		11.5	12.0	12.5	V
IS test pin voltage	V_{IS}	$V_{IS}=V_{DD}$	11.5	12.0	12.5	V
Substrate voltage	V_{SUB}	$V_{SUB}=V_{DD}$	11.5	12.0	12.5	V
Output gate voltage	V_{OG}	V_{DD}=12V	4.2	4.5	4.8	V
Photo storage gate voltage	V_{PG}	$V_{PG}=V_{OG}$	4.2	4.5	4.8	V
TG test pin voltage	V_{TG}	$V_{TG}=V_{SS}$	0	0	0.3	V
CCD shift register clock High level	$V_{øH}$		9.0	10.0	V_{DD}	V
CCD shift register clock Low level	$V_{øL}$		0	0.5	0.8	V
Shift gate clock High level	V_{SH}		V_{DD} –1	V_{DD}	V_{DD}	V
Shift gate clock Low level	V_{SL}		0	0.5	0.8	V
Reset gate clock High level	V_{RH}		V_{DD} –1	V_{DD}	V_{DD}	V
Reset gate clock Low level	V_{RL}		0	0.5	0.8	V

• Timing conditions (Ta=–20 to + 60˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock frequency	f_C	$f_C=f_R$=1/2T	0.1	1.0	3.0	MHz
Reset clock frequency	f_R		0.1	1.0	3.0	MHz
Shift register clock rise time	t_{Cr}	See timing diagram	0	20	50	ns
Shift register clock fall time	t_{Cf}		0	20	50	ns
Shift clock rise time	t_{Sr}	See timing diagram	0	15	50	ns
Shift clock fall time	t_{Sf}		0	15	50	ns
Shift clock set up time	t_{Ss}		250	400	1000	ns
Shift clock pulse width	t_{Sw}		1.0	1.8	10	µs
Shift clock hold time	t_{Sh}		0	0.5	1	µs
Reset clock rise time	t_{Rr}	See timing diagram	0	10	20	ns
Reset clock fall time	t_{Rf}		0	10	20	ns
Reset clock set up time	t_{Rs}		0.7T	—	—	ns
Reset clock pulse width	t_{Rw}		20	30	—	ns
Reset clock hold time	t_{Rh}		5	10	—	ns

■ Electrical Characteristics

• Clock input capacitance (Ta=–20 to + 60˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock input capacitance	C_{1A}, C_{2A} C_{1B}, C_{2B}	V_{IN}=12V f=1MHz	—	600	750	pF
Reset clock input capacitance	C_R		—	15	30	pF
Shift clock input capacitance	C_S		—	250	300	pF

*$ø_{1A}$, $ø_{2A}$, $ø_{1B}$, and $ø_{2B}$ are respectively connected to $ø_{1D}$, $ø_{2D}$, $ø_{1C}$, and $ø_{2C}$ internally.

• DC characteristics

Parameter	Symbol	Condition	min	typ	max	Unit
Power supply current	I_{DD}	V_{DD}=+12V	—	20	50	mA
IS test pin leak current	I_{IS}		—	0.1	1	mA
Photo storage gate leak current	I_{PG}	V_{DD}=+5V	—	5	50	µA
Output gate pin leak current	I_{OG}		—	5	50	µA

• AC characteristics

Parameter	Symbol	Condition	min	typ	max	Unit
Signal output set up time *	t_{OS}	See timing diagram	—	30	—	ns
Signal output hold time	t_{OW}		—	30	—	ns

* OS output level: =500mV

■ Optical Characteristics

<Inspection conditions>

- Ta=25˚C, standard operating condition, f_C=f_R=1MHz, T_{int} (accumulation time)=10ms
- Light source: Daylight type fluorescent lamp
- Optical system: A slit with an aperture dimensions of 20mm × 20mm is used at a distance of 200mm from the sensor (equivalent to F=10).
- This parameters are inspected by signal multiplex with channels 1 and 2 which correspond to the output of both OS_1 and DS_1 (channel 1) and the output of both OS_2 and DS_2 (channel 2) respectively. Before multiplex the channels 1 and 2, the OS and DS signals should be respectively through unity gain differential amplifiers with input impedances of 100k Ohms or more, carrying out zero level DC clamping of each channel.
- These specifications apply to the 10000 valid pixels excluding the dummy pixels D1 to D4.

Parameter	Symbol	Condition	min	typ	max	Unit
Responsivity	R	Note 1	1.3	1.8	2.3	V/lx· s
Photo response non-uniformity	PRNU	Note 2	—	—	10	%
Bit non-uniformity	BNU	Note 3	—	—	±8	%
Saturation output voltage	V_{SAT}	Note 4	1.00	1.60	—	V
Saturation exposure	SE	Note 5	0.43	0.89	—	lx· s
Dark signal output voltage	V_{DRK}	Dark condition, see Note 6	—	0.5	3.0	mV
Dark signal output non-uniformity	DSNU	Dark condition, see Note 7	—	0.2	2.0	mV
Shift register total transfer efficiency	STTE	Note 8	92	—	—	%
Dynamic range	DR	Note 9	—	3200	—	
Modulation transfer function	MTF_R	Note 10	—	65	—	%

* The definitions of the parameters are given in Note 1) to Note 10) on the following page.

■ Optical Characteristics (continued)

Note 1) Responsivity (R)

This is the value obtained by dividing the average output voltage (V) of the 10000 valid pixels by the exposure (lx·s).
The exposure (lx·s) is the product of the illumination intensity (lx) and the accumulation time (s).
Since the responsivity changes with the spectral distribution of the light source used, care should be taken when using a light source other than the daylight type fluorescent lamp specified in the inspection conditions.

Note 2) Photo response non-uniformity (PRNU)

The photo response non-uniformity (PRNU) is defined by the following equation, where X_{ave} is the average output voltage of the valid 10000 pixels and Δx is the absolute value of the difference between the maximum and minimum voltage, when the surface of the photo-sites is illuminated with light having a uniform distribution over the entire surface.

$$PRNU = \frac{\triangle x}{X_{ave}} \times 100\ (\%)$$

The incident light intensity shall be 50% of the standard saturation llight intensity.

Note 3) Bit non-uniformity (BNU)

This is defined by the following equation where the output voltage of each pixel among the 10000 pixels is denoted by Xi (i = 1 to 10000) when the photodetector region is illuminated by a light of uniform illumination intensity distribution, and the average output voltage of the pixels near the ith pixel is denoted by $X_{local\text{-}ave.}$ (a total of 20 pixels with 10 pixels before and 10 pixels after that pixel). Here, the max. operation consists of comparing with the absolute value and assigning the sign of the numerator.

$$BNU = \max.\ \left(\frac{Xi - X_{local\text{-}ave.}}{X_{local\text{-}ave.}} \right) \times 100\ (\%)$$

The incident light intensity shall be 50% of the standard saturation llight intensity.

Note 4) Saturation output voltage (V_{SAT})

This is the output voltage at the point beyond which it is not possible to maintain the linearity of the photoelectric conversion characteristics as the exposure is increased. (The exposure at this point is called the saturation exposure.)

Note 5) Saturation Exposure (SE)

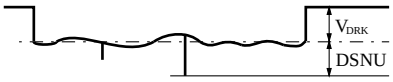
This is the exposure beyond which it is not possible to maintain the linearity of the output voltage as the exposure is increased. When designing the equipment using these devices, make sure that the incident light exposure is set with sufficient margin so that the CCD never gets saturated.

Note 6) Dark signal output voltage (V_{DRK})

This is defined as the average of the output from the 10000 active pixels in the dark condition at Ta=25˚C, T_{int}=10ms. Since normally the dark signal output voltage gets doubled for every 8 to 10˚C increase in Ta and is proportional to T_{int}, it is necessary to convert the value if Ta andT_{int} are different from the inspection conditions given above. (See the figure below.)

Note 7) Dark signal non-uniformity (DSNU)

This is defined as the difference between the maximum value among the output voltages from the 10000 valid pixels at Ta=25˚C and T_{int}=10ms and V_{DRK}. (See the figure below.)



Note 8) Shift register total transfer efficiency (STTE)

This is given by the following equation where the average output voltage of all the 10000 pixels is denoted by $X_{ave.}$ and the larger of the output voltages of the 2 dummy pixels following the dummy pixel D4 is denoted by X_r when the photodetector region is illuminated by a light of uniform illumination intensity distribution.

$$STTE = \frac{X_{ave.} - X_r}{X_{ave.}} \times 100\ (\%)$$

Note 9) Dynamic range (DR)

This is defined by the following equation.

$$DR = \frac{V_{SAT}}{V_{DRK}}$$

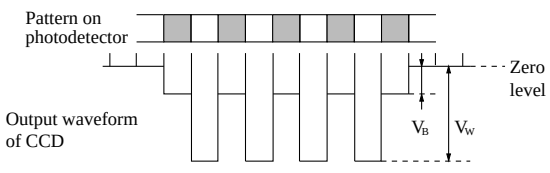
Since the dark signal output voltage is proportional to the accumulation time, the dynamic range becomes wider when the accumulation time is shorter. This value is not a guaranteed value, but is merely a reference value.

Note 10) Modulation transfer function (MTF_R)

This is defined by the following equation where the average output voltages of the pixels with the white pattern and the pixels with the black pattern are respectively denoted by V_W and V_B when a black and white stripe pattern (in which the black and white patterns alternate at every pixel) is projected on the photodetector region in phase (equivalent to the Nyquist spatial frequency).

$$MTF_R = \frac{V_W - V_B}{V_W + V_B} \times 100\ (\%)$$

This value is a measure of resolution of the sensor. This parameter is not a guaranteed value but is merely a reference value.



■ Pin Descriptions

Pin No.	Symbol	Pin name	Condition
1	OS_1	Signal output 1	Odd-number pixel output
2	DS_1	Compensation output 1	
3	OG	Output gate	
4	$ø_{R1}$	Reset clock	
5	$ø_{2D}$	CCD shift register clock	
6	$ø_{1D}$	CCD shift register clock	
7	V_{SS}	Ground	
8	$ø_{1A}$	CCD shift register clock	Internally connected to $ø_{1D}$.
9	$ø_{2A}$	CCD shift register clock	Internally connected to $ø_{2D}$.
10	TG	Test pin	Connect externally to V_{SS}.
11	PG	Photo storage gate	
12	$ø_{SG}$	Shift clock gate	
13	IS	Test pin	Connect externally to V_{DD}.
14	$ø_{2B}$	CCD shift register clock	Internally connected to $ø_{2C}$.
15	$ø_{1B}$	CCD shift register clock	Internally connected to $ø_{1C}$.
16	$ø_{SUB}$	Substrate	Connect externally to V_{DD}.
17	V_{1C}	CCD shift register clock	
18	$ø_{2C}$	CCD shift register clock	
19	$ø_{R2}$	Reset clock	
20	V_{DD}	Power supply	
21	DS_2	Compensation output 2	
22	OS_2	Signal output 2	Even-number pixel output

■ Construction of the Image Sensor

The MN3665A can made up of into the three sections of—a) photo detector region, b) CCD transfer region (shift register), and c) output region.

a) Photo detector region

- The photoelectric conversion device consists of a 5µm floating photodiode and a 2µm channel stopper for each pixel, and 10000 of these devices are linearly arranged side by side at a pitch of 7µm.
- The photo detector's windows are 7µm × 7µm squares and light incident on areas other than these windows is optically shut out.
- The photo detector is provided with 32 optically shielded pixels which serve as the black reference.

b) CCD Transfer region (shift register)

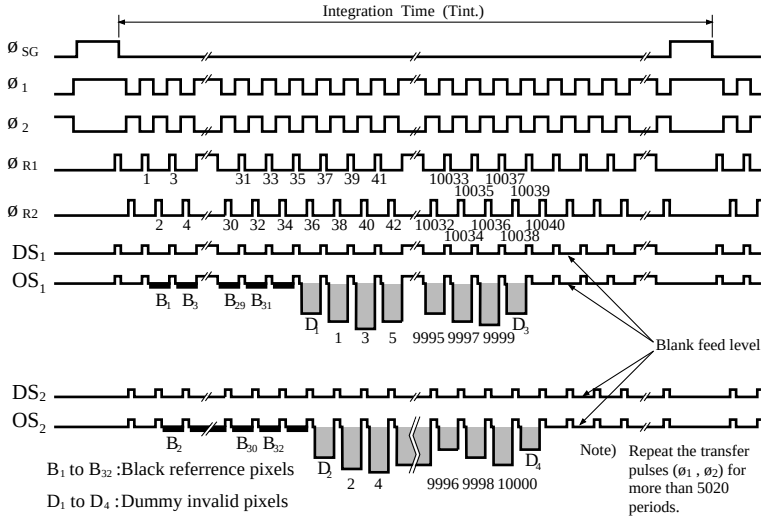
- The light output that has been photoelectrically converted is transferred to the CCD transfer for each odd and even pixel at the timing of the shift clock ($ø_{SG}$). The optical signal electric charge transferred to this analog shift register is successively transferred out and guided to the output region.
- A buried type CCD that can be driven by a two phase clock ($ø_1$, $ø_2$) is used for the analog shift register.

c) Output region

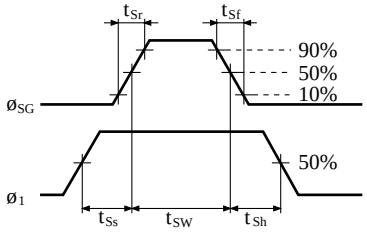
- The signal charge that is transferred to the output region is sent to the detector where impedance transformation is done using two source follower stages.
- The DC level component and the clock noise component not containing optical signals are output from the DS pin.
- By carrying out differential amplification of the two outputs OS and DS externally, it is possible to obtain an output signal with a high S/N ratio by reducing the clock noise, etc.

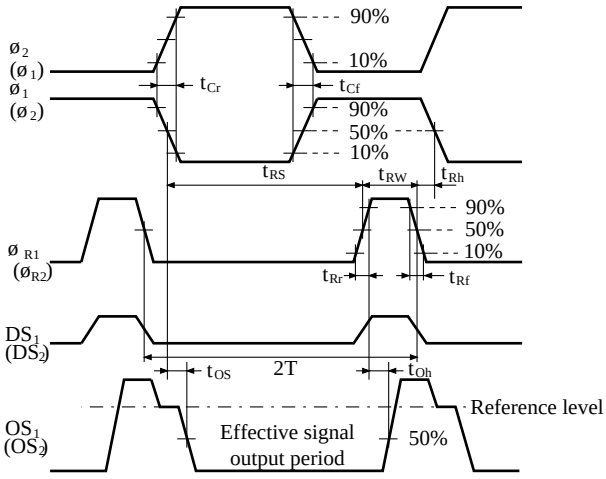
■ Timing Diagram

(1) I/O timing



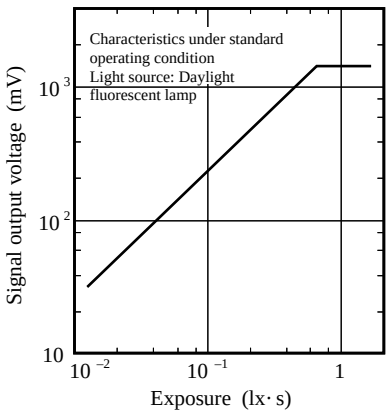
(2) Drive timing



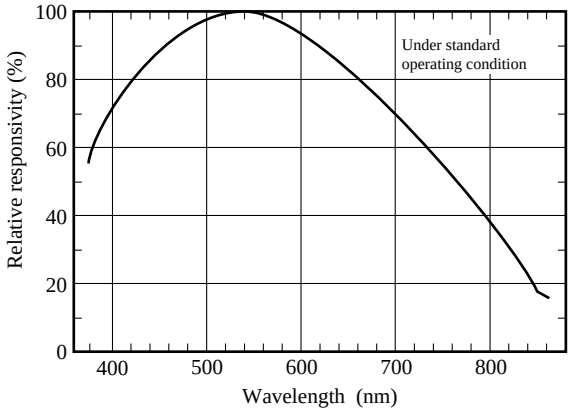


■ Graphs and Characteristics

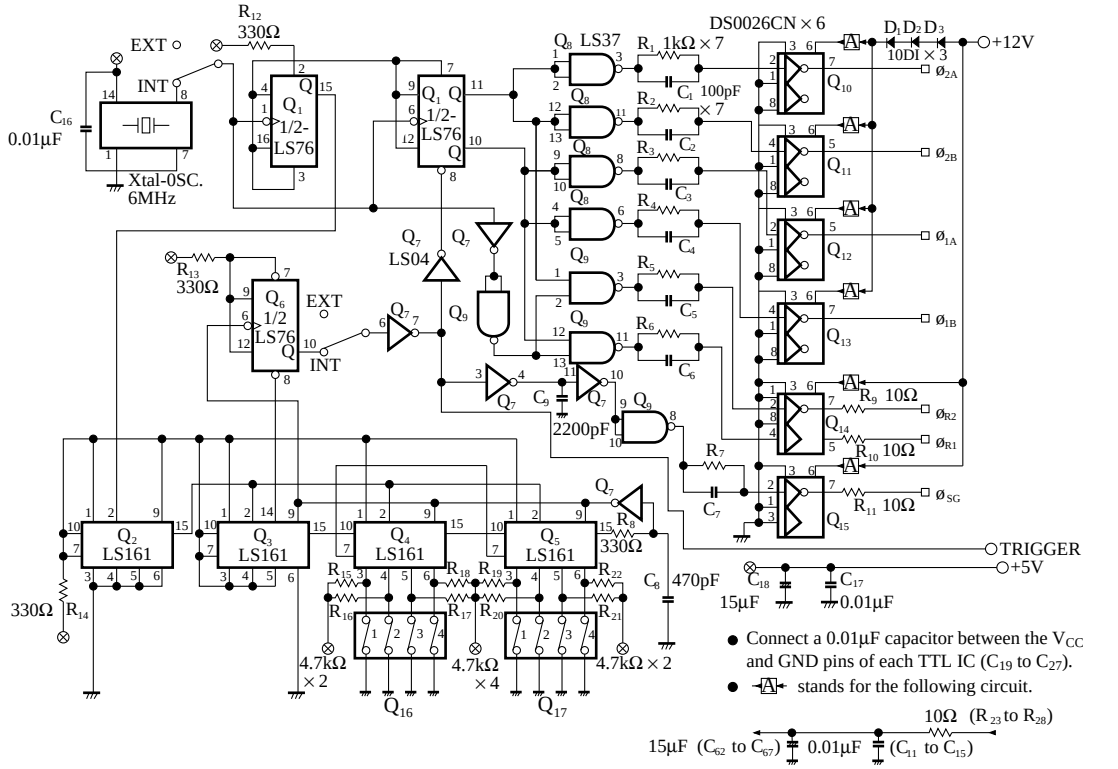
Photoelectric Conversion Characteristics



Spectral Response Characteristics



■ Drive Circuit Diagram (Digital Section)



■ Drive Circuit Diagram (Analog Section)