MN3662

3648-Bit High-Resolution CCD Linear Image Sensor

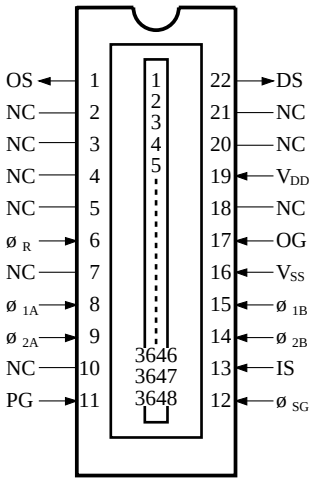
■ Overview

The MN3662 is a high responsivity CCD linear image sensor having floating photodiodes in the photodetector region, CCD analog shift registers for read out.
It provides large output at a high S/N ratio for visible light inputs over a wide range of wavelength.

■ Features

- 3648 floating photodiodes and n-channel buried type CCD shift registers for read out are integrated in a single chip.
- High blue responsivity of a maximum responsivity ratio of 40% (typ.) at 400nm, and smooth spectral response over the entire visible region.
- Large signal output of 1500mV (typ.) at saturation, and hold type combined odd/even output that makes signal processing easy.
- 24 Black dummy bits and low optical response (typ. 1%) at the areas other than the photodetector region.
- Operation with a single +12V positive power supply.

■ Pin Assignments

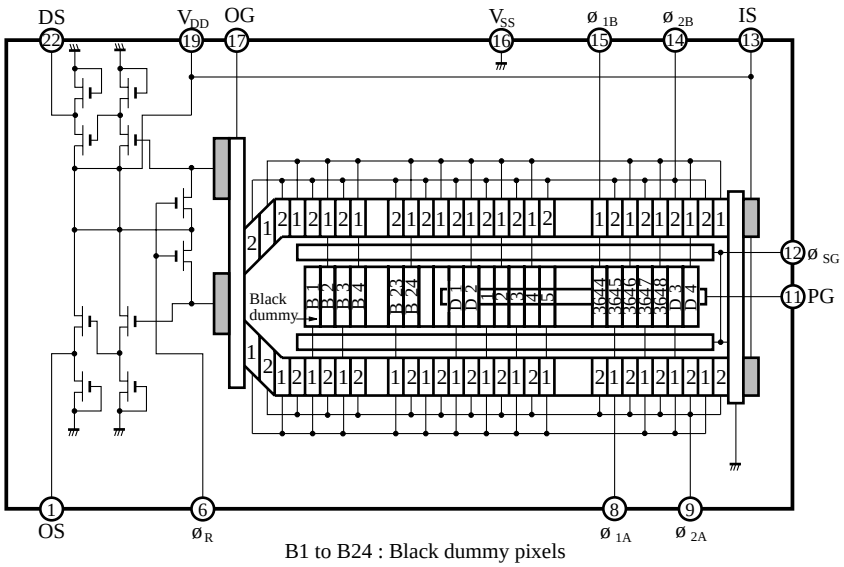


(Top View)
C21 WDIP022-G-0450

■ Application

- Reading out drawings, characters and numerals in image scanners, OCRs, etc.
- Measurement of position and dimensions of objects.

■ Block Diagram



B1 to B24 : Black dummy pixels

■ Absolute Maximum Ratings (Ta=25˚C, V_{SS}=0V)

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	– 0.3 to +17	V
Input pin voltage	V_I	– 0.3 to +17	V
Output pin voltage	V_O	– 0.3 to +17	V
Operating temperature range	T_{opr}	–20 to + 60	˚C
Storage temperature range	T_{stg}	–40 to +100	˚C

■ Operating Conditions

• Voltage conditions (Ta=–25 to + 60˚C, V_{SS}=0V)

Parameter	Symbol	Condition	min	typ	max	Unit
Power supply voltage	V_{DD}		11.2	12.0	12.8	V
IS test pin voltage	V_{IS}	V_{IS} =V_{DD}	11.2	12.0	12.8	V
Photo storage gate voltage	V_{PG}	V_{DD}=12V	4.2	4.5	4.8	V
Output gate voltage	V_{OG}	V_{DD}=12V	4.2	4.5	4.8	V
CCD shift register clock High level	$V_{øH}$		9.0	10.0	12.0	V
CCD shift register clock Low level	$V_{ø L}$		0	0.5	0.8	V
Reset gate clock High level	V_{RH}		9.0	10.0	12.0	V
Reset gate clock Low level	V_{RL}		0	0.5	0.8	V
Shift gate clock High level	V_{SH}		9.0	10.0	12.0	V
Shift gate clock Low level	V_{SL}		0	0.5	0.8	V

• Timing conditions (Ta=–25 to + 60˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock frequency	f_C	f_C =1/2T	0.1	—	1.0	MHz
Reset clock frequency	f_R	f_R =1/T	0.2	—	2.0	MHz
Shift clock rise time	t_{Sr}	See timing diagrams (1) to (3).	0	15	200	ns
Shift clock fall time	t_{Sf}		0	15	200	ns
Shift clock set up time	t_{Ss}		0	0.03	10.0	µs
Shift clock pulse width	t_{SW}		10	12	100	µs
Shift clock hold time	t_{Sh}		0	0.5	10	µs
Shift register clock rise time	t_{Cr}		0	20	200	ns
Shift register clock fall time	t_{Cf}		0	20	200	ns
Reset clock rise time	t_{Rr}		0	15	30	ns
Reset clock fall time	t_{Rf}		0	15	30	ns
Reset clock pulse width	t_{Rw}		30	60	120	ns
Reset clock set up time	t_{Rs}		200	400	—	ns
Reset clock hold time	t_{Rh}		0	5	60	ns
Output signal set up time ✻	t_{OS}		—	120	—	ns

✻ OS output level=300mV

■ Electrical Characteristics

• DC characteristics (Ta=0 to + 60˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Power supply current	I_{DD}	V_{IN} =+12V	—	10	25	mA
Photostorage gate pin leak current	I_{PG}	V_{IN} =+5V	—	—	50	µA
Output gate pin leak current	I_{OG}		—	—	50	µA

• Clock input capacitance (Ta=–20 to + 60˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock input capacitance	C_1, C_2	V_{IN} =12V f=1MHz	—	500	—	pF
Reset clock input capacitance	C_R		—	10	—	pF
Shift clock input capacitance	C_S		—	150	—	pF

■ Optical Characteristics (Ta=25˚C, Normal operating condition, f_R=1MHz, $T_{int.}$ (acccumulation time)=10ms)

Parameter	Symbol	Condition	min	typ	max	Unit
Saturation output voltage	V_{SAT}	(Note 1)	1000	1500	—	mV
Saturation exposure	SE	(Note 1)	1.30	1.95	—	lx · s
Minimum saturation exposure output voltage	$V_{SEmin.}$	(Note 2) exposure: 1.31x · s	1000	—	1400	mV
Photoresponse non-uniformity	PRNU	(Note 3) exposure: 1.31x · s	—	—	20	%
Bit non-uniformity	BNU	(Note 4) exposure: 1.31x · s	—	—	±10	%
Odd/even bit non-uniformity	O/E	(Note 5) exposure: 1.31x · s	—	1	5	%
Dark signal output voltage	V_d	(Note 6) Dark condition	—	—	10	mV
Shift register total transfer efficiency	STTE	(Note 7) exposure: 1.31x · s	92	99	—	%
Modulation transfer function	MTF_R	(Note 8)	—	76	—	%

• Optical system: Light source = G-54 green fluorescent lamp (peak wavelength=543nm), using a slit of size 40mm × 40mm. Distance between slit and sensor = 200mm (equivalent to F=5)

• Inspected by the output from a unity gain differential amplifier to which the OS and DS are input (input impedance=100kΩ or more)

• These specifications apply to the 3648 valid pixels excluding the dummy pixels D1 to D4.

Note 1) Saturation output voltage: This is the output voltage at the point beyond which it is not possible to maintain the linearity of the photoelectric conversion characteristics as the exposure is increased. (The exposure at this point is called the saturation exposure.)

Note 2) Minimum saturation exposure output voltage: This is the output voltage at the minimum specified value (1.3lx·s) of the saturation exposure. It is possible to calculate the responsivity from this parameter. That is,

Responsivity (minimum value) = 1.0V/1.3lx·s = 0.77V/lx·s

Responsivity (maximum value) = 1.4V/1.3lx·s = 1.08V/lx·s

The responsivity when a daylight type flourescent lamp is used as the light source will be about 1.5 times the responsivity when the G-54 green fluorescent lamp is used.

Note 3) Photoresponse non-uniformity (PRNU): This is defined by the following equation where the difference between the maximum and minimum values in the output of all the 3648 active pixels is denoted by Δx when the photodetector region is illuminated by a light of uniform illumination intensity distribution, and the average value of the output voltage from all the 3648 pixels is denoted by $X_{ave.}$.

$$PRNU = \frac{\triangle x}{X_{ave}} \times 100\ (\%)$$

Note 4) Bit non-uniformity: This is defined by the following equation where the output voltage of each pixel among the 3648 pixels is denoted by Xi (i = 1 to 3648) when the photodetector region is illuminated by a light of uniform illumination intensity distribution, and the average output voltage of the pixels near the ith pixel is denoted by $X_{local\text{-}ave.}$ (a total of 20 pixels with 10 pixels before and 10 pixels after that pixel). Here, the max. operation consists of comparing with the absolute value and assigning the sign of the numerator.

$$BNU = \max.\ \left(\frac{Xi - X_{local\text{-}ave.}}{X_{local\text{-}ave.}} \right) \times 100\ (\%)$$

Note 5) Odd-even bit non-uniformity: This is defined by the following equation where the average output voltage of the 1824 even numbered pixel photodiodes is denoted by $X_{even\text{-}ave.}$, the average output voltage of the 1824 odd numbered pixel photodiodes is denoted by $X_{odd\text{-}ave.}$, and the average output voltage of all the 3648 pixels is denoted by $X_{ave.}$, when the photodetector region is illuminated by a light of uniform illumination intensity distribution.

$$O/E = \frac{| X_{even\text{-}ave.} - X_{odd\text{-}ave.} |}{X_{ave.}} \times 100\ (\%)$$

Note 6) Dark signal output voltage: This is the maximum value of the outputs from the 3648 valid pixels in the dark condition with Ta=25˚C and $T_{int.}$ = 10ms. The dark signal output voltage normally gets doubled with an increase of about 8 to 10˚C in Ta, and is proportional to $T_{int.}$.

Note 7) Shift register total transfer efficiency: This is given by the following equation where the average output voltage of all the 3648 pixels is denoted by $X_{ave.}$ and the larger of the output voltages of the 2 dummy pixels following the dummy pixel D4 is denoted by X_r when the photodetector region is illuminated by a light of uniform illumination intensity distribution.

$$STTE = \frac{X_{ave.} - X_r}{X_{ave.}} \times 100\ (\%)$$

Note 8) Modulation transfer function: This is defined by the following equation where the average output voltages from the pixels with the white pattern and the pixels with the black pattern are respectively denoted by V_W and V_B when a black and white stripe pattern (in which the black and white patterns alternate at every pixel) is projected on the photodetector region in phase (equivalent to the Nyquist spatial frequency).

$$MTF_R = \frac{V_W - V_B}{V_W + V_B} \times 100\ (\%)$$

This value is a measure of resolution of the sensor.
This parameter is not a guaranteed value but is merely a reference value.

■ Pin Descriptions

Pin No.	Symbol	Pin name	Condition
1	OS	Signal output	
2	NC	Non connection	
3	NC	Non connection	
4	NC	Non connection	
5	NC	Non connection	
6	$ø_R$	Reset clock	
7	NC	Non connection	
8	$ø_{1A}$	CCD shift register clock	
9	$ø_{2A}$	CCD shift register clock	
10	NC	Non connection	
11	PG	Photo storage gate	
12	$ø_{SG}$	Shift gate clock	
13	IS	Test pin	Connect externally to V_{DD}.
14	$ø_{2B}$	CCD shift register clock	
15	$ø_{1B}$	CCD shift register clock	
16	V_{SS}	Ground	Connected to the substrate.
17	OG	Output gate	
18	NC	Non connection	
19	V_{DD}	Power supply	
20	NC	Non connection	
21	NC	Non connection	
22	DS	Compensatin output	

Note) Connect all NC pins externally to Ground.

■ Construction of the Image Sensor

The MN3662 can be made up of the three sections of—a) photo detector region, b) CCD transfer region (shift register), and c) output region.

a) Photo detector region

- The photoelectric conversion device consists of a 5µm floating photodiode and a 3µm channel stopper for each pixel, and 3648 of these devices are linearly arranged side by side at a pitch of 8µm.
- The photo detector's windows are 8µm × 8µm squares and light incident on areas other than these windows is optically shut out.
- The photo detector is provided with 24 optically shielded pixels which serve as the black reference.

b) CCD Transfer region (shift register)

- The optical output after photoelectric conversion is transferred respectively to the odd and even CCD transfer region at the timing of the shift gate electrode ($ø_{SG}$), the photoelectric converted output transferred to this analog shift register is transferred successively to the output region.
- A buried type CCD that can be driven by a 2-phase clock is used as the analog shift register.

c) Output region

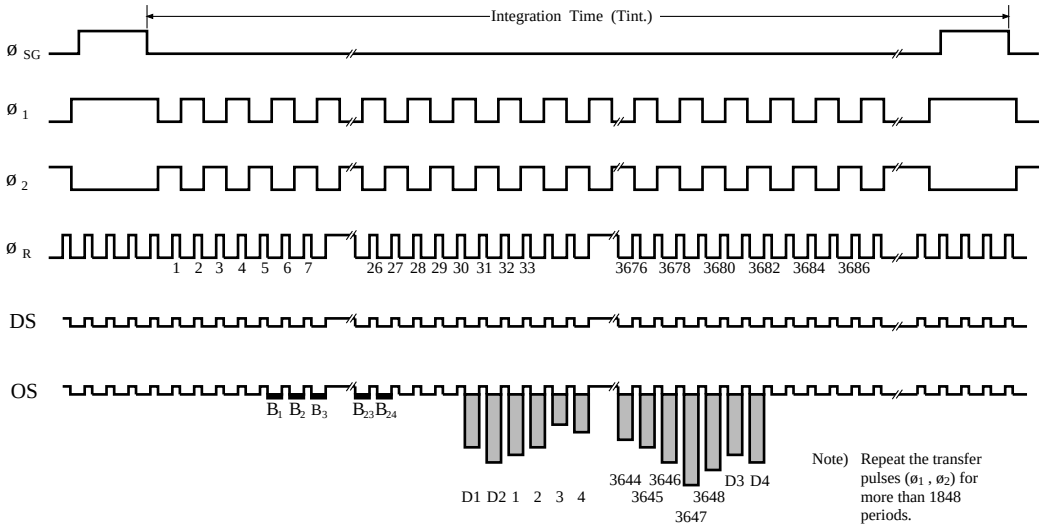
- The signal transferred to this region is sent to the detector region and is output after impedance conversion by a two stage source follower amplifier.

Evaluation board

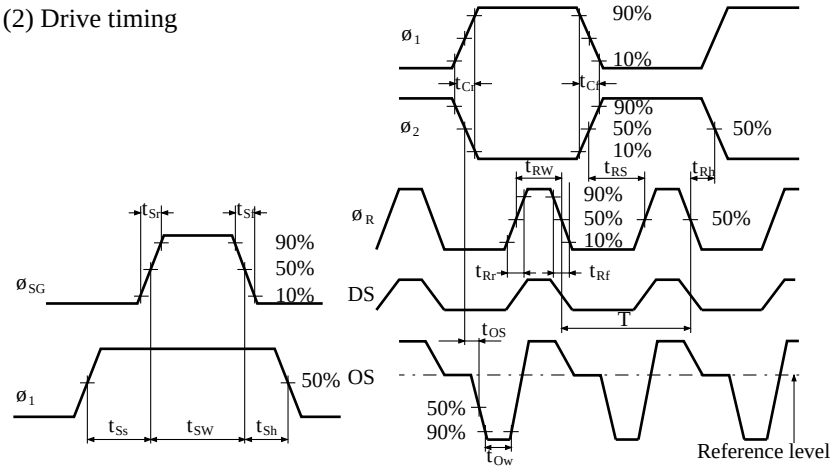
The placement of the each component is very important in order to get a good output signal. The evaluation board BS801 is available for evaluating the MN3662.

■ Timing Diagram

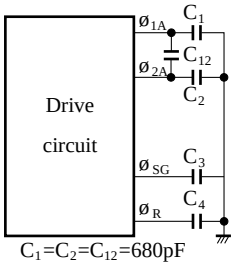
(1) I/O timing



(2) Drive timing



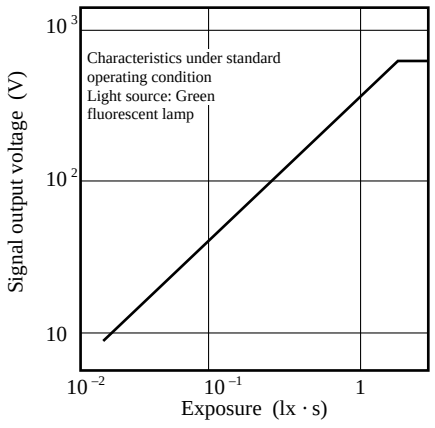
(3) Timing condition measuring circuit



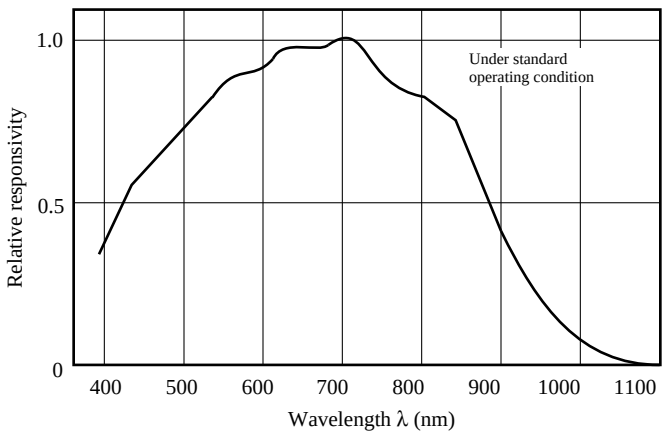
$C_1=C_2=C_{12}=680pF$
$C_3=150pF$
$C_4=10pF$

■ Graphs and Characteristics

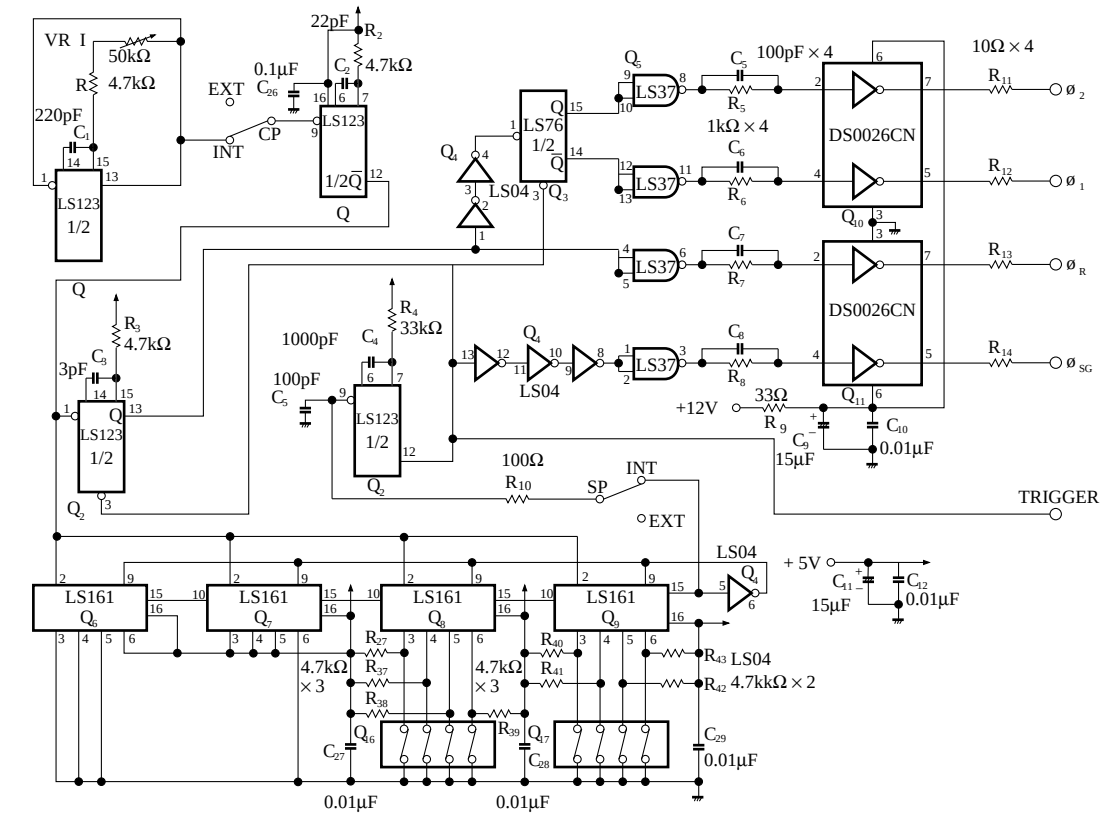
Photoelectric Conversion Characteristics



Spectral Response Characteristics



■ Drive Circuit Diagram (Digital Section)



■ Drive Circuit Diagram (Analog Section)