MN3112SA

Vertical Driver for Video-Camera CCD Area-Image-Sensor

■ Overview

The MN3112SA is a vertical driver LSI incorporating four vertical driver channels and one sub driver channel for a 2-dimensional interline CCD image sensor.

The MN3112SA enables low current dissipation and the part reductions.

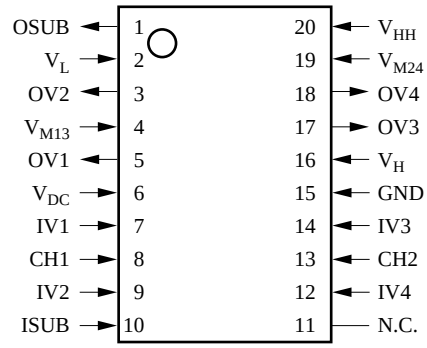
■ Features

- 3V power supply for input section

■ Applications

- Video cameras

■ Pin Assignment



(TOP VIEW)

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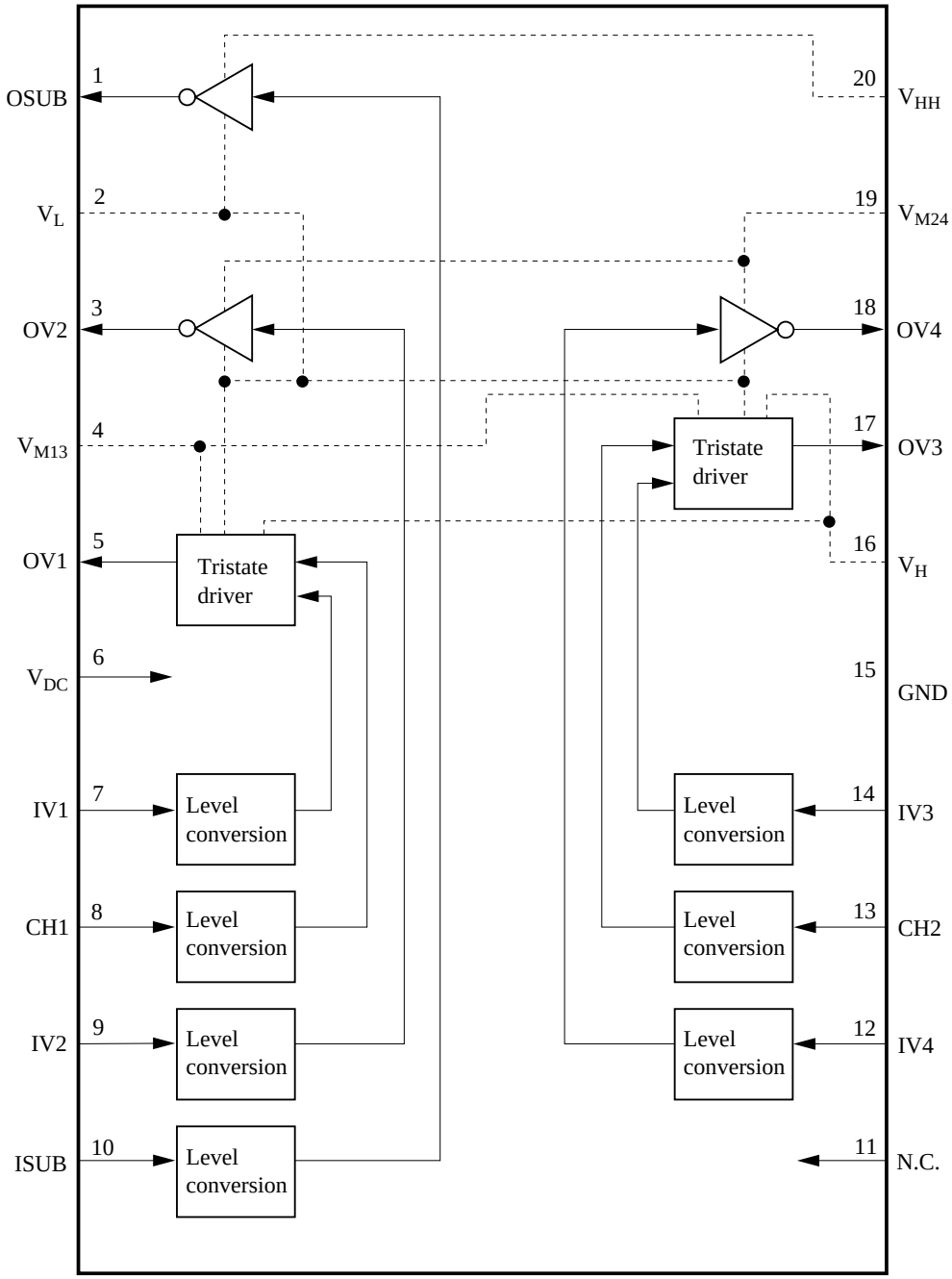
■ Block Diagram



V_{DC}, V_L, GND : Common power supply
V_{M13}, V_{M24} : Binary and tristate independent power supplies for vertical driver section
V_{HH}, V_H : Independent power supplies for sub driver section and vertical driver section

■ Pin Descriptions

Pin No.	Symbol	Pin Name	I/O	Function Description
6	V_{DC}	Input section high-level power supply	I	5V high-level input
15	GND	Input section low-level power supply	I	5V low-level input
16	V_H	Vertical driver section high-level power supply	I	High-level input at high-voltage section
20	V_{HH}	SUB driver section high-level power supply	I	High-level input at high-voltage section
4 19	V_{M13} V_{M24}	Middle-level power supply	I	Middle-level input at high-voltage section Input externally to both V_{M13} and V_{M24}.
2	V_L	Low-level power supply	I	Low-level input at high-voltage section
9	IV2	Transfer pulse input	I	Charge transfer pulse input pin
12	IV4	Transfer pulse input	I	Charge transfer pulse input pin
7	IV1	Transfer pulse input	I	Charge transfer pulse input pin
14	IV3	Transfer pulse input	I	Charge transfer pulse input pin
8	CH1	Charge pulse input	I	Charge read pulse input pin
13	CH1	Charge pulse input	I	Charge read pulse input pin
10	ISUB	SUB pulse input	I	Unwanted charge sourcing pulse input pin
18	OV4	Binary transfer pulse output	O	Binary transfer pulse output pin (V_{M24}, V_L)
3	OV2	Binary transfer pulse output	O	Binary transfer pulse output pin (V_{M24}, V_L)
17	OV3	Tristate transfer pulse output	O	Tristate transfer pulse output pin (V_H, V_{M13}, V_L)
5	OV1	Tristate transfer pulse output	O	Tristate transfer pulse output pin (V_H, V_{M13}, V_L)
1	OSUB	SUB pulse output	O	Unwanted charge sourcing pulse output pin (V_{HH}, V_L)
11	N.C.	No connection	—	

■ Functions

Binary transfer pulse (vertical driver section)

IV2 IV4	OV2 OV4
H	L
L	M

Tristate transfer pulse (vertical driver section)

CH1 CH2	IV1 IV3	OV1 OV3
H	H	L
	L	M
L	H	L
	L	H

*1 IV1, IV2, IV3, IV4, CH1, CH2

H: V_{DC}

L: GND

OV1, OV2, OV3, OV4

H: V_H

M: V_{M13} or V_{M24}

L: V_L

Unwanted charge sourcing pulse (SUB driver section)

ISUB	OSUB
H	L
L	H

*1 ISUB

H: V_{DC}

L: GND

OSUB

H: V_{HH}

L: V_L

■ Electrical Characteristics

(1) DC characteristics

V_{HH}=18.0V , V_H=13.0V , V_{M13}=V_{M24}=1.0V , V_L= –7.0V,

V_{DC}=5.00V , GND=0.0V , Ta= –10˚C to +70˚C

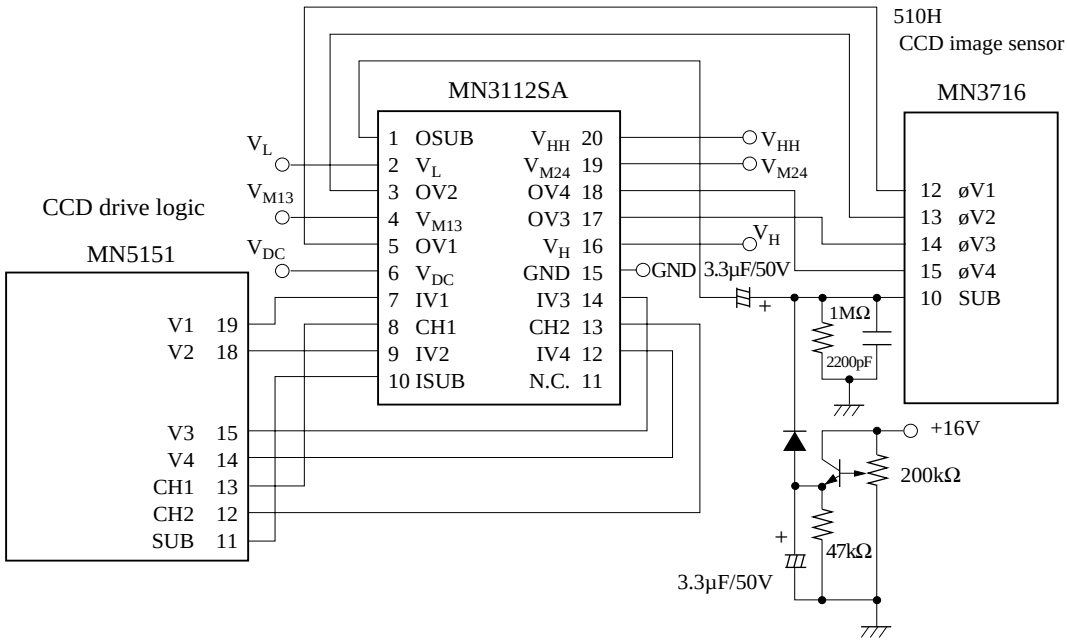
Parameter	Symbol	Test Conditions	min	typ	max	Unit
Quiescent supply current	I_{DDST}	V_I=GND , V_{DC}=3.0V			2.5	mA
		V_I=GND , V_{DC}=5.0V			4	
Operating supply current	I_{DDDYN}	V_I=GND , V_{DC}			7	mA
Input pins IV1 , IV2 , IV3 , IV4 , CH1 , CH2 , ISUB						
Voltage "H" level	V_{IH}		0.7 × V_{DC}		V_{DC}	V
Voltage "L" level	V_{IL}		GND		0.3 × V_{DC}	V
Input leakage current	I_{LI}	V_I=0 to 5V			±1	µA
Output pins 1 (binary output) OV2 , OV4						
Output voltage middle level	V_{OM1}	I_{OM1}= –1mA	0.9		V_{M24}	V
Output voltage "L" level	V_{OL1}	I_{OL1}=1mA	V_L		—	V
Output on-resistance middle level	R_{ONM1}	I_{OM1}=–50mA			40	Ω
Output on-resistance "L" level	R_{ONL1}	I_{OL1}=50mA			40	Ω
Output pins 2 (tristate output) OV1 , OV3						
Output voltage "H" level	V_{OH2}	I_{OH2}=–1mA	12.9		V_H	V
Output voltage middle level	V_{OM2}	I_{OM2}=–1mA	0.9		V_{M13}	V
Output voltage "L" level	V_{OL2}	I_{OL2}=1mA	V_L		—	V
Output on-resistance "H" level	R_{ONH2}	I_{OH2}=–50mA			50	Ω
Output on-resistance middle level	R_{ONM2}	I_{OM2}=±50mA			40	Ω
Output on-resistance "L" level	R_{ONL2}	I_{OL2}=50mA			40	Ω
Output pin 3 (SUB output) OSUB						
Output voltage "H" level	V_{OHH3}	I_{OHH3}=–1mA	17.9		V_{HH}	V
Output voltage "L" level	V_{OL3}	I_{OL3}=1mA	V_L		—	V
Output on-resistance middle level	R_{ONHH3}	I_{ONHH3}=–50mA			50	Ω
Output on-resistance "L" level	R_{ONL3}	I_{ONL3}=50mA			40	Ω

(2) AC characteristics

V_{HH}=18.0V , V_H=13.0V , V_{M13}=V_{M24}=1.0V , V_L=–7.0V,
V_{DC}=3.0V , GND=0.0V , Ta=–10˚C to +70˚C

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Output pins 1 (binary output)	OV2 , OV4					
Transmission delay time	t_{PLM} t_{PML}	No load "L" level — middle level		100	200	ns
Rise time Fall time	t_{TLM} t_{TML}			200	300	ns
Output pins 2 (tristate output)	OV1 , OV3					
Transmission delay time	t_{PLM} t_{PML}	No load "L" level — middle level		100	200	ns
Transmission delay time	t_{TMH} t_{THM}	No load middle level — "H" level		200	400	ns
Rise time Fall time	t_{TLM} t_{TML}			200	300	ns
Rise time Fall time	t_{TMH} t_{THM}			200	300	ns
Output pin 3 (SUB output)	OSUB					
Transmission delay time	t_{PLHH} t_{PHHL}	No load "L" level — "H" level		100	200	ns
Rise time Fall time	t_{TLHH} t_{THHL}			200	300	ns

■ Application Circuit Example



Note *1: Connect a bypass capacitor as close as possible to each of the MN3112SA's power supply pins (V_{HH}, V_H, V_{M13}, V_{M24}, V_L, V_{DC}).

■ Package Dimensions (Unit: mm)

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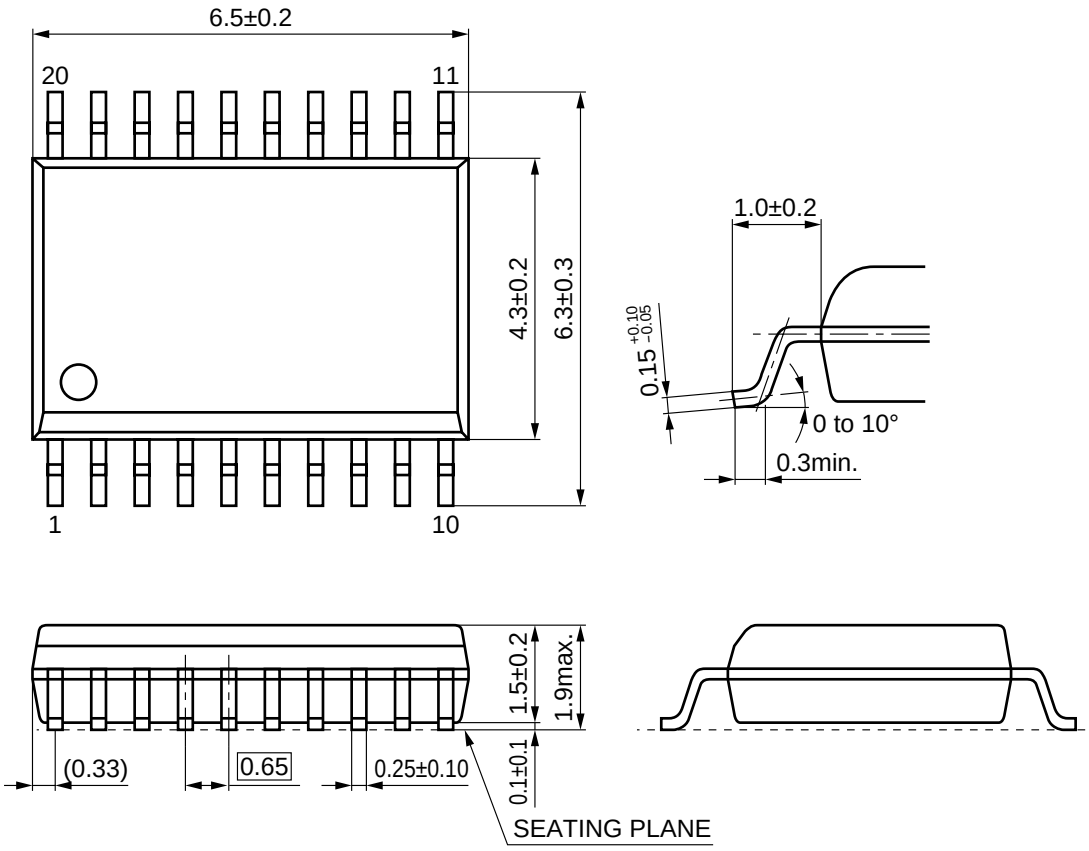

■ Usage Notes

(1) When the sub driver is not used

1. Connect V_{HH} (pin 20) to V_H (pin 16).
2. Connect ISUB (pin 10) to V_{DC} (pin 6) or GND (pin 15).
3. Make no connection for OSUB (pin 1).

(2) Connect a bypass capacitor as close as possible to MN3112SA power supply pins V_{HH} (pin 20), V_H (pin 16), V_{M13} (pin 4), V_{M24} (pin 19), V_L (pin 2), and V_{DC} (pin 6).

(3) Guarantee period after unsealing

The guarantee period after opening the dry-sealed packaging is three weeks under the environment conditions of 30˚C/70% (temperature/humidity).

(4) The recommended reflow temperature is 230˚C.