## 5.6, 6.2 15 & 20 Volt SOT-23 Dual Monolithic Common Anode Zeners

## **Transient Voltage Suppressors** for ESD Protection

These dual monolithic silicon zener diodes are designed for applications requiring transient overvoltage protection capability. They are intended for use in voltage and ESD sensitive equipment such as computers, printers, business machines, communication systems, medical equipment and other applications. Their dual junction common anode design protects two separate lines using only one package. These devices are ideal for situations where board space is at a premium.

#### **Specification Features:**

- SOT–23 Package Allows Either Two Separate Unidirectional Configurations or a Single Bidirectional Configuration
- Peak Power 24 or 40 Watts @ 1.0 ms (Unidirectional), per Figure 5 Waveform
- Maximum Clamping Voltage @ Peak Pulse Current
- Low Leakage < 5.0 μA</li>
- ESD Rating of Class N (exceeding 16 kV) per the Human Body Model

#### **Mechanical Characteristics:**

- · Void Free, Transfer-Molded, Thermosetting Plastic Case
- · Corrosion Resistant Finish, Easily Solderable
- · Package Designed for Optimal Automated Board Assembly
- Small Package Size for High Density Applications
- Available in 8 mm Tape and Reel

Use the Device Number to order the 7 inch/3,000 unit reel. Replace the "T1" with "T3" in the Device Number to order the 13 inch/10,000 unit reel.

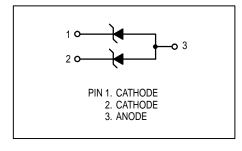
# MMBZ5V6ALT1\* MMBZ6V2ALT1 MMBZ15VALT1 MMBZ20VALT1

Motorola Preferred Devices

SOT-23 COMMON ANODE DUAL ZENER OVERVOLTAGE TRANSIENT SUPPRESSORS 24 & 40 WATTS PEAK POWER



CASE 318-08 STYLE 12 LOW PROFILE SOT-23 PLASTIC



#### THERMAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Characte	Symbol	Value	Unit	
Peak Power Dissipation @ 1.0 ms (1) @ T <sub>A</sub> ≤ 25°C	MMBZ5V6ALT1, MMBZ6V2ALT1 MMBZ15VALT1, MMBZ20VALT1	P <sub>pk</sub>	24 40	Watts
Total Power Dissipation on FR–5 Board (2) Derate above 25°C	PD	225 1.8	mW mW/°C	
Thermal Resistance Junction to Ambient	$R_{ heta JA}$	556	°C/W	
Total Power Dissipation on Alumina Substra Derate above 25°C	PD	300 2.4	mW mW/°C	
Thermal Resistance Junction to Ambient		$R_{ heta JA}$	417	°C/W
Junction and Storage Temperature Range		T <sub>J</sub> T <sub>stg</sub>	- 55 to +150	°C
Lead Solder Temperature — Maximum (10	Tı	260	°C	

- (1) Non–repetitive current pulse per Figure 5 and derate above  $T_A = 25^{\circ}C$  per Figure 6.
- (2)  $FR-5 = 1.0 \times 0.75 \times 0.62$  in.
- (3) Alumina =  $0.4 \times 0.3 \times 0.024$  in., 99.5% alumina
- \*Other voltages may be available upon request

Thermal Clad is a trademark of the Bergquist Company

Preferred devices are Motorola recommended choices for future use and best overall value.

#### Rev 1



### **ELECTRICAL CHARACTERISTICS** (T<sub>A</sub> = 25°C unless otherwise noted) **UNIDIRECTIONAL** (Circuit tied to Pins 1 and 3 or Pins 2 and 3)

 $(V_F = 0.9 \text{ V Max } @ I_F = 10 \text{ mA})$ 

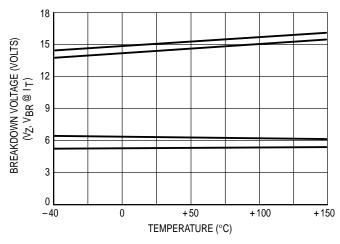
E	Breakdov	wn Volta	ge	Max Ro Leakage	everse Current	Max Zener II	mpedan	ce (5)	Max Reverse	Max Reverse Voltage @ IRSM(4)	Maximum Temperature
	V <sub>ZT</sub> (3) (V)		@ <del> </del> Т (mA)	I <sub>R</sub>	V <sub>R</sub> (V)	Z <sub>ZT</sub> @ I <sub>ZT</sub> (Ω) (mA)			Surge Current I <sub>RSM</sub> (4)	(Clamping Voltage)	Coefficient of VBR (mV/°C)
Min	Nom	Max	()	(62.1)	(-)			(A)	(V)	(11147 0)	
5.32	5.6	5.88	20	5.0	3.0	11	1600	0.25	3.0	8.0	1.26
5.89	6.2	6.51	1.0	0.5	3.0	_	_	_	2.76	8.7	2.80

 $(V_F = 1.1 \text{ V Max } @ I_F = 200 \text{ mA})$ 

Breakdown Voltage  VBR(3) (V) (mA)		Reverse Voltage	Max Reverse	Max Reverse	Max Reverse	_Maximum		
		@ <del> </del> Т (mA)	Working Peak L VRWM	Leakage Current	Surge Current IRSM(4)	Voltage @ I <sub>RSM</sub> (4) (Clamping Voltage) V <sub>RSM</sub>	Temperature Coefficient of VBR	
Min	Nom	Max	()	(V)	I <sub>R</sub> (nA)	(A)	(V)	(mV/°C)
14.25	15	15.75	1.0	12.0	50	1.9	21	12.3
19.0	20	21.0	1.0	17.0	50	1.4	28	17.2

- (3)  $V_Z/V_{BR}$  measured at pulse test current  $I_T$  at an ambient temperature of 25°C.
- (4) Surge current waveform per Figure 5 and derate per Figure 6.
- (5) Z<sub>ZT</sub> and Z<sub>ZK</sub> are measured by dividing the AC voltage drop across the device by the AC current supplied. The specfied limits are I<sub>Z</sub>(AC) = 0.1 I<sub>Z</sub>(DC), with AC frequency = 1 kHz.

#### TYPICAL CHARACTERISTICS





(Upper curve for each voltage is bidirectional mode, lower curve is unidirectional mode)

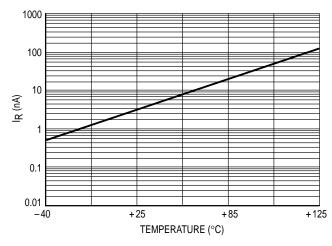


Figure 2. Typical Leakage Current versus Temperature

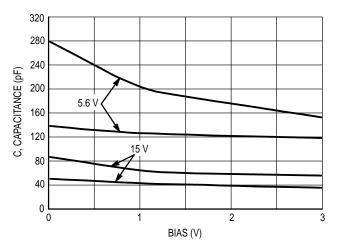


Figure 3. Typical Capacitance versus Bias Voltage
(Upper curve for each voltage is unidirectional mode,
lower curve is bidirectional mode)

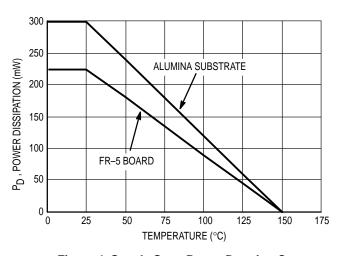


Figure 4. Steady State Power Derating Curve

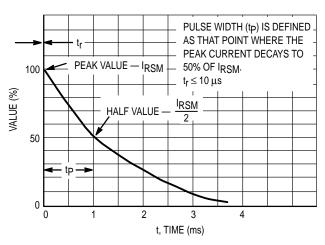


Figure 5. Pulse Waveform

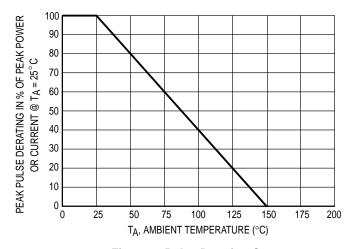


Figure 6. Pulse Derating Curve

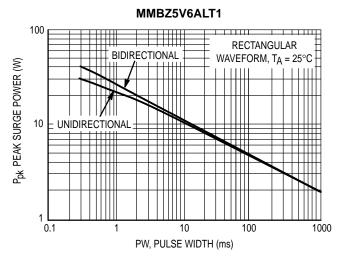


Figure 7. Maximum Non-repetitive Surge Power, Ppk versus PW

Power is defined as  $V_{RSM} \times I_Z(pk)$  where  $V_{RSM}$  is the clamping voltage at  $I_Z(pk)$ .

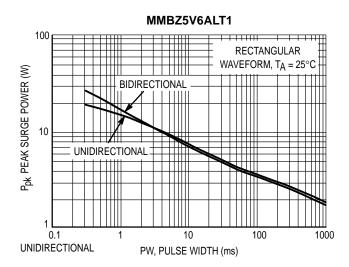


Figure 8. Maximum Non-repetitive Surge Power, Ppk(NOM) versus PW

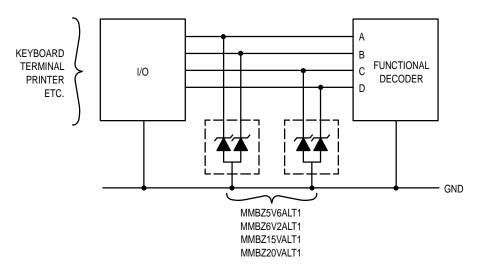
Power is defined as  $V_Z(NOM) \times I_Z(pk)$  where  $V_Z(NOM)$  is the nominal zener voltage measured at the low test current used for voltage classification.

#### **TYPICAL COMMON ANODE APPLICATIONS**

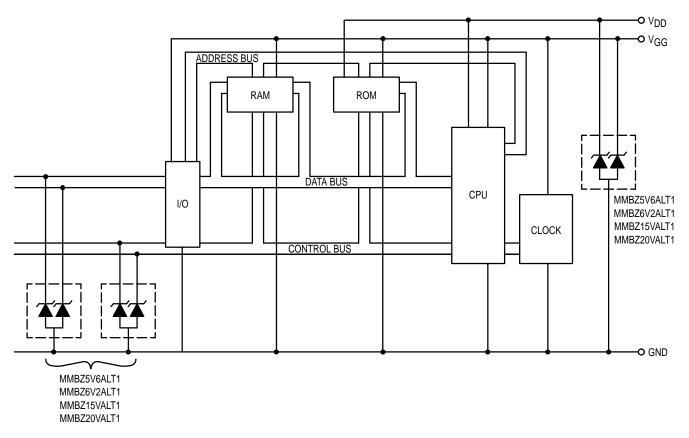
A quad junction common anode design in a SOT–23 package protects four separate lines using only one package. This adds flexibility and creativity to PCB design especially

when board space is at a premium. Two simplified examples of TVS applications are illustrated below.

#### **Computer Interface Protection**



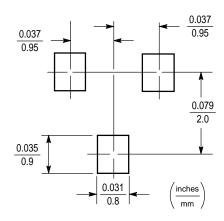
#### **Microprocessor Protection**



#### INFORMATION FOR USING THE SOT-23 SURFACE MOUNT PACKAGE

#### MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT-23

#### SOT-23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by  $T_{J(max)}$ , the maximum rated junction temperature of the die,  $R_{\theta JA}$ , the thermal resistance from the device junction to ambient, and the operating temperature,  $T_A$ . Using the values provided on the data sheet for the SOT–23 package,  $P_D$  can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature  $T_A$  of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150^{\circ}C - 25^{\circ}C}{556^{\circ}C/W} = 225 \text{ milliwatts}$$

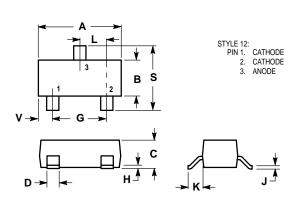
The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

#### **SOLDERING PRECAUTIONS**

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.\*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes.
   Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.
- \* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

#### **OUTLINE DIMENSIONS**



- 1. DIMENSIO Y14.5M, 1982. DIMENSIONING AND TOLERANCING PER ANSI
- CONTROLLING DIMENSION: INCH.
  MAXIUMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL

	INC	HES	MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.1102	0.1197	2.80	3.04	
В	0.0472	0.0551	1.20	1.40	
С	0.0350	0.0440	0.89	1.11	
D	0.0150	0.0200	0.37	0.50	
G	0.0701	0.0807	1.78	2.04	
Н	0.0005	0.0040	0.013	0.100	
J	0.0034	0.0070	0.085	0.177	
K	0.0140	0.0285	0.35	0.69	
L	0.0350	0.0401	0.89	1.02	
S	0.0830	0.1039	2.10	2.64	
V	0.0177	0.0236	0.45	0.60	

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