GreenLine™

MMBF0202PLT1

Motorola Preferred Device

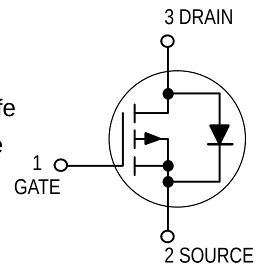
Low $r_{DS(on)}$ Small-Signal MOSFETs TMOS Single P-Channel Field Effect Transistors

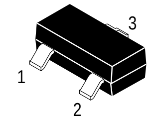
P–CHANNEL ENHANCEMENT–MODE TMOS MOSFET $r_{DS(on)}$ = 1.4 OHM

Part of the GreenLine™ Portfolio of devices with energy–conserving traits.

These miniature surface mount MOSFETs utilize Motorola's High Cell Density, HDTMOS process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in small power management circuitry. Typical applications are dc–dc converters, power management in portable and battery–powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SOT–23 Surface Mount Package Saves Board Space





CASE 318–07, Style 21
SOT–23 (TO–236AB)

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	20	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 20	Vdc
Drain Current — Continuous @ T_A = 25°C — Continuous @ T_A = 70°C — Pulsed Drain Current ($t_p \le 10\ \mu s$)	I_D I_D I_{DM}	300 240 750	mAdc
Total Power Dissipation @ T_A = 25°C(1)	P_D	225	mW
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Thermal Resistance — Junction–to–Ambient	$R_{\theta JA}$	625	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

DEVICE MARKING

P3

(1) Mounted on G10/FR4 glass epoxy board using minimum recommended footprint.

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MMBF0202PLT1	7″	12 mm embossed tape	3000
MMBF0202PLT3	13″	12 mm embossed tape	10,000

Preferred devices are Motorola recommended choices for future use and best overall value.

(Replaces MMBF0202P/D)

MOTOROLA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 10 μA)		$V_{(BR)DSS}$	20	—	—	Vdc
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 16 Vdc, V_{GS} = 0 Vdc)			—	—	1.0	
(V_{DS} = 16 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	10	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	±100	nAdc
ON CHARACTERISTICS(1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	1.0	1.7	2.4	Vdc
Static Drain–to–Source On–Resistance		$r_{DS(on)}$				Ohms
(V_{GS} = 10 Vdc, I_D = 200 mAdc)			—	0.9	1.4	
(V_{GS} = 4.5 Vdc, I_D = 50 mAdc)			—	2.0	3.5	
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 200 mAdc)		g_{FS}	—	600	—	mMhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 5.0 V)	C_{iss}	—	50	—	pF
Output Capacitance	(V_{DS} = 5.0 V)	C_{oss}	—	45	—	
Transfer Capacitance	(V_{DG} = 5.0 V)	C_{rss}	—	20	—	
SWITCHING CHARACTERISTICS(2)						
Turn–On Delay Time	(V_{DD} = –15 Vdc, R_L = 75 Ω, I_D = 200 mAdc, V_{GEN} = –10 V, R_G = 6.0 Ω)	$t_{d(on)}$	—	2.5	—	ns
Rise Time		t_r	—	1.0	—	
Turn–Off Delay Time		$t_{d(off)}$	—	16	—	
Fall Time		t_f	—	8.0	—	
Gate Charge (See Figure 5)	(V_{DS} = 16 V, V_{GS} = 10 V, I_D = 200 mA)	Q_T	—	2700	—	pC
SOURCE–DRAIN DIODE CHARACTERISTICS						
Continuous Current		I_S	—	—	0.3	A
Pulsed Current		I_{SM}	—	—	0.75	
Forward Voltage(2)		V_{SD}	—	1.5	—	V

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

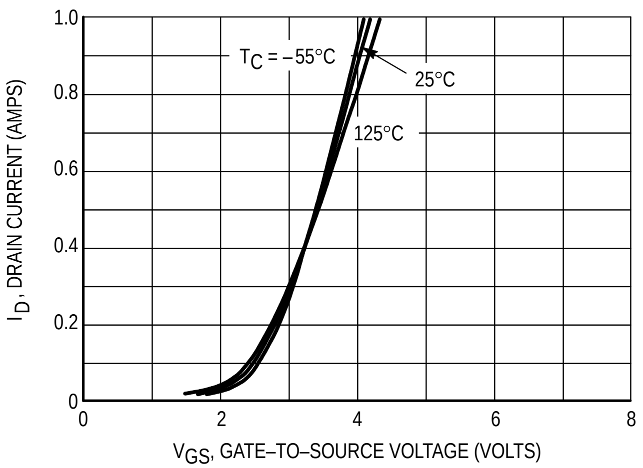


Figure 1. Transfer Characteristics

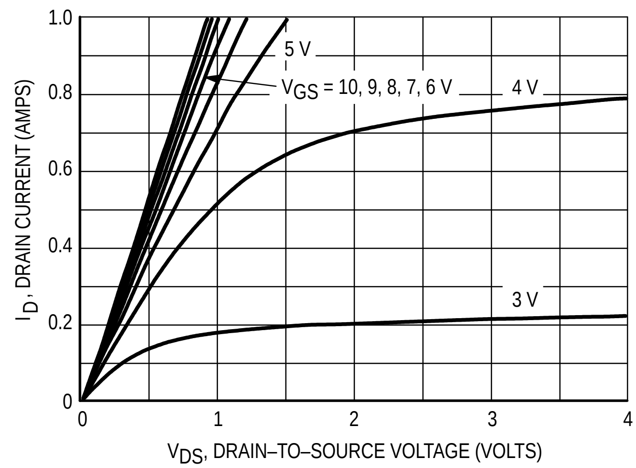


Figure 2. On–Region Characteristics

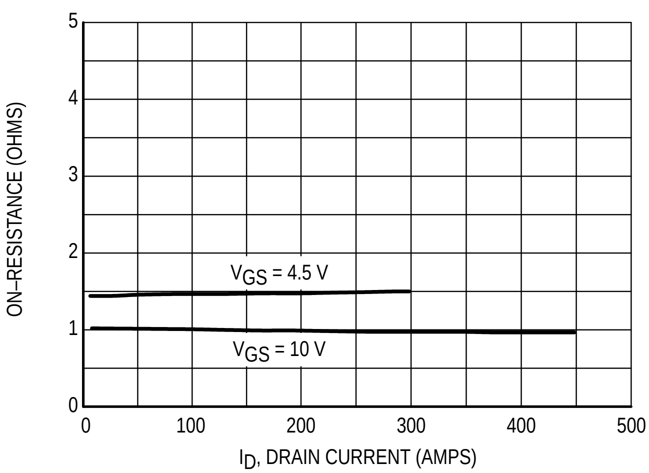


Figure 3. On–Resistance versus Drain Current

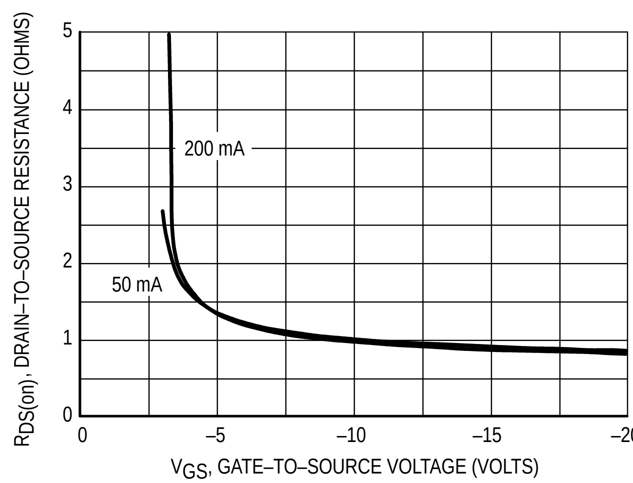


Figure 4. On–Resistance versus Gate–to–Source Voltage

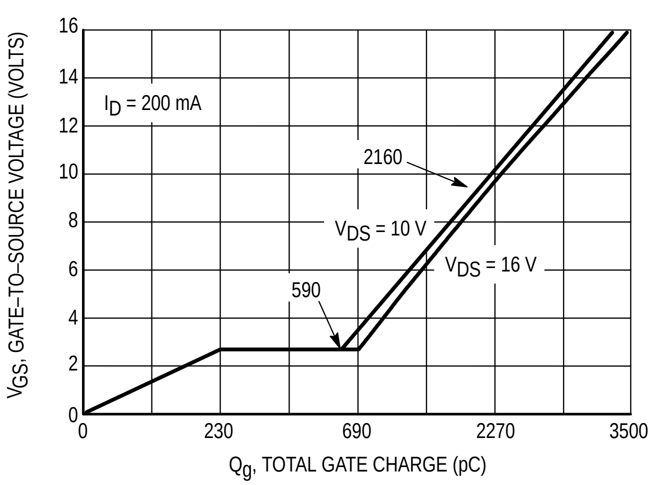


Figure 5. Gate Charge

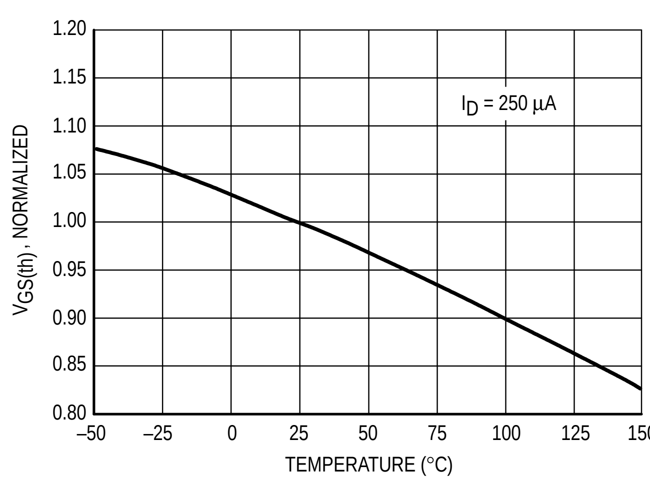


Figure 6. Threshold Voltage Variance Over Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

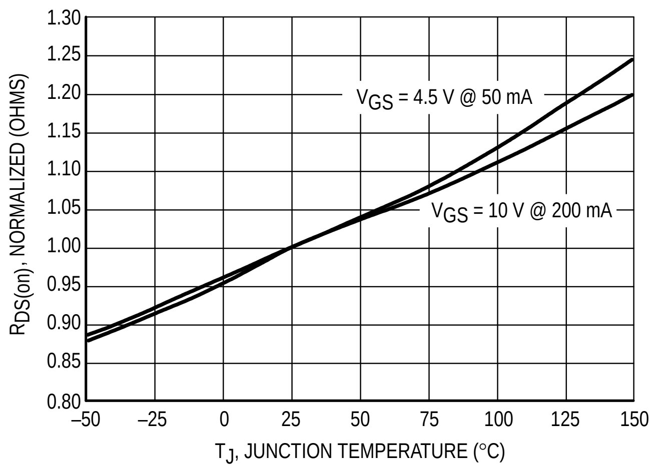


Figure 7. On–Resistance versus Junction Temperature

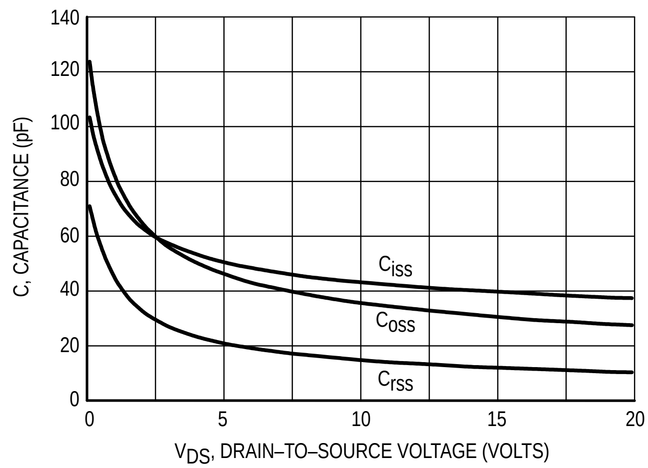


Figure 8. Capacitance

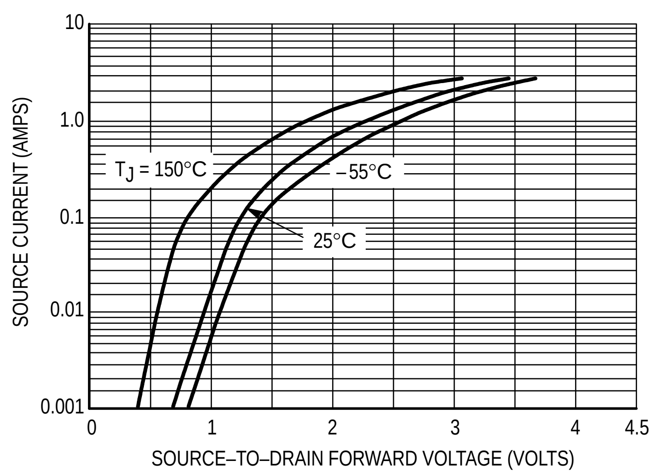
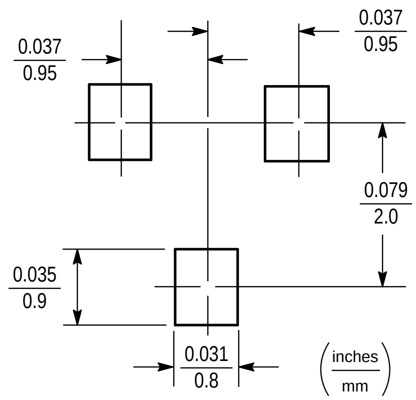


Figure 9. Source–to–Drain Forward Voltage versus Continuous Current (I_S)

INFORMATION FOR USING THE SOT–23 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT–23

SOT–23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SOT–23 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150°C - 25°C}{556°C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

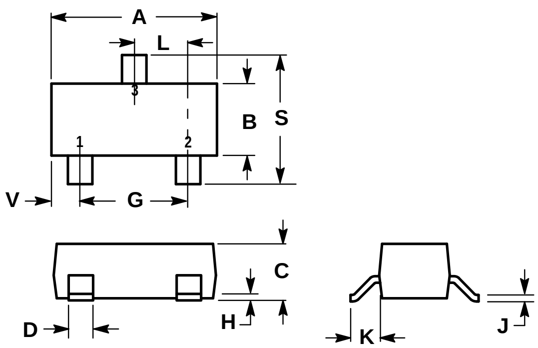
SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIUMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0180	0.0236	0.45	0.60
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.0984	2.10	2.50
V	0.0177	0.0236	0.45	0.60

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

CASE 318–07
SOT–23 (TO–236AB)
ISSUE AD

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