



# MIC706P/R/S/T, MIC708R/S/T

## $\mu$ P Supervisory Circuits

### Description

The MIC706P/R/S/T and MIC708R/S/T are inexpensive microprocessor supervisory circuits that monitor power supplies in 3.0 and 3.3 Volt microprocessor based systems. The circuit functions include a watchdog timer, microprocessor reset, power failure warning and a debounced manual reset input.

The MIC706 offers a watchdog timer function, while the MIC708 has no watchdog timer but has an active high reset output in addition to the active low reset output.

The R, S, and T versions are similar in all respects except for supply voltage reset threshold levels. The threshold levels are 2.63, 2.93, and 3.08V respectively. When the supply voltage drops below the reset threshold level,  $\overline{\text{RESET}}$  (and RESET for the MIC708) is asserted.

The MIC706P is identical to the MIC706R, except that the Reset output is asserted high.

### Typical Applications

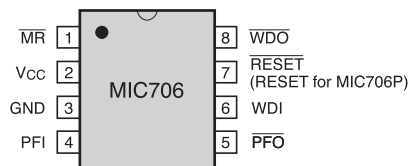
- Laptop Computers
- Intelligent Instruments
- Critical Microprocessor Power Monitoring
- Printers
- Computers
- Controllers

### Ordering Information

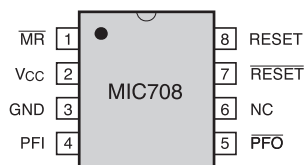
Part	Package	Temp. Range
MIC70__N	8-Lead PDIP	-40°C to +85°C
MIC70__M	8-Lead SOIC	-40°C to +85°C

### Pin Configuration

Top View



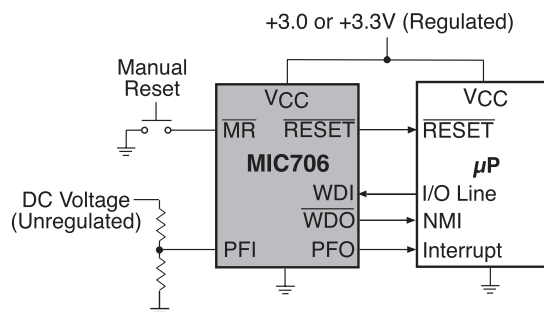
N Package - 8 Lead Plastic DIP Package  
M Package - 8 Lead Plastic SOIC Package



### Features

- 30 $\mu$ A Maximum Supply Current
- Debounced Manual Reset Input is TTL/CMOS Compatible
- Reset Pulse Width, 200ms
- Watchdog Timer, 1.6s (MIC706)
- Precision Supply Voltage Monitor
- Early Power Fail Warning or Low Battery Detect

### Typical Operating Circuit



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## Absolute Maximum Ratings

Terminal Voltage  
VCC ..... -0.3V to 6.0V  
All Other Inputs ..... -0.3V to (VCC + 0.3V)  
Input Current  
VCC, Gnd. .... 25mA  
Output Current (all outputs) ..... 20mA

Operating Temperature Range  
MIC70\_N, MIC70\_M ..... -40°C to 85°C  
Storage Temperature Range ..... -65°C to 150°C  
Lead Temperature (Soldering - 10 sec.) ..... 300°C  
Power Dissipation (PDIP) ..... 475mW  
Power Dissipation (SOIC) ..... 400mW

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability. Operating ranges define those limits between which the functionality of the device is guaranteed.

## Electrical Characteristics

VCC = 2.70V to 5.5V for MIC70\_P/R, VCC = 3.00V to 5.5V for MIC70\_S, VCC = 3.15V to 5.5V for MIC70\_T, TA = -40°C to 85°C unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage Range, VCC		1.4		5.5	V
Supply Current				30	$\mu$ A
Reset Voltage Threshold	MIC70_P/R MIC70_S MIC70_T	2.55 2.85 3.00	2.63 2.93 3.08	2.70 3.00 3.15	V
Reset Threshold Hysteresis			20		mV
Reset Pulse Width, tRS		140	200	280	ms
RESET Output Voltage (MIC70_R/S/T)	ISource = 200 $\mu$ A ISink = 1.2mA ISink = 50 $\mu$ A, VCC = 1.4V	0.8 x VCC		0.3 0.3	V
RESET Output Voltage (MIC706P)	ISource = 200 $\mu$ A ISink = 1.2mA	0.8 x VCC		0.3	V
RESET Output Voltage (MIC708R/S/T)	ISource = 200 $\mu$ A ISink = 500 $\mu$ A	0.8 x VCC		0.3	V
Watchdog Timeout Period, tWD		1.0	1.6	2.25	sec
WDI Minimum Input Pulse, tWP	VIL = 0.4V, VIH = 80% of VCC VIL = 0.4V, VIH = 80% of VCC>4.5V	100 50			ns ns
WDI Threshold Voltage	VIH VIL	0.7 x VCC		0.6	V
WDI Input Current	WDI = 0V or VCC	-1		1	$\mu$ A
WDO Output Voltage	ISource = 200 $\mu$ A ISink = 500 $\mu$ A	0.8 x VCC		0.3	V

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Parameter	Conditions	Min	Typ	Max	Units
$\overline{MR}$ Pull-Up Current	$\overline{MR}$ = 0V	20	250	600	$\mu$ A
$\overline{MR}$ Pulse Width, $t_{MR}$	$V_{CC} > 4.5V$	500 150			nS nS
$\overline{MR}$ Input Threshold	$V_{IL}$ $V_{IH}$	$0.7 \times V_{CC}$		0.6	V
$\overline{MR}$ to Reset Output Delay, $t_{MD}$				750	nS
PFI Input Threshold		1.2	1.25	1.3	V
PFI Input Current		-25	0.01	+25	nA
PFO Output Voltage	$I_{Sink} = 1.2mA$ $I_{Source} = 200\mu A$	$0.8 \times V_{CC}$		0.3	V

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## Pin Functions

Pin Name	Pin No.			
	MIC706 R/S/T	MIC706P	MIC708	
<b><math>\overline{\text{MR}}</math></b>	1	1	1	Manual Reset Input forces reset outputs to assert when pulled below 0.8V. An internal pull-up current of 250 $\mu$ A on this input forces it high when left floating. This input can also be driven from TTL or CMOS logic.
<b>VCC</b>	2	2	2	Primary supply input, +5V.
<b>GND</b>	3	3	3	IC ground pin, 0V reference.
<b>PFI</b>	4	4	4	Power fail input. Internally connected to the power fail comparator which is referenced to 1.25V. The power fail output ( $\overline{\text{PFO}}$ ) remains high if PFI is above 1.25V. PFI should be connected to GND or $\text{V}_{\text{OUT}}$ if the power fail comparator is not used.
<b><math>\overline{\text{PFO}}</math></b>	5	5	5	Power fail output. The power fail comparator is independent of all other functions on this device.
<b>WDI</b>	6	6	N/A	Watchdog input. The WDI input monitors microprocessor activity, an internal watchdog timer resets itself with each transition on the watchdog input. If the WDI pin is held high or low for longer than the watchdog timeout period, $\overline{\text{WDO}}$ is forced to active low. The watchdog function cannot be disabled.
<b>N/C</b>	N/A	N/A	6	No Connect
<b><math>\overline{\text{RESET}}</math></b>	7	N/A	7	$\overline{\text{RESET}}$ is asserted if either $\text{V}_{\text{CC}}$ goes below the reset threshold or by a low signal on the manual reset input ( $\overline{\text{MR}}$ ). $\overline{\text{RESET}}$ remains asserted for one reset timeout period (200ms) after $\text{V}_{\text{CC}}$ exceeds the reset threshold or after the manual reset pin transitions from low to high. The watchdog timer will not assert $\overline{\text{RESET}}$ unless $\overline{\text{WDO}}$ is connected to $\overline{\text{MR}}$ .
<b><math>\overline{\text{WDO}}</math></b>	8	8	N/A	Output for the watchdog timer. The watchdog timer resets itself with each transition on the watchdog input. If the WDI pin is held high or low for longer than the watchdog timeout period, $\overline{\text{WDO}}$ is forced low. $\overline{\text{WDO}}$ will also be forced low if $\text{V}_{\text{CC}}$ is below the reset threshold and will remain low until $\text{V}_{\text{CC}}$ returns to a valid level.
<b>RESET</b>	N/A	7	8	RESET is the compliment of $\overline{\text{RESET}}$ and is asserted if either $\text{V}_{\text{CC}}$ goes below the reset threshold or by a low signal on the manual reset input (MR). RESET is suitable for microprocessors systems that use an active high reset.

## Block Diagram

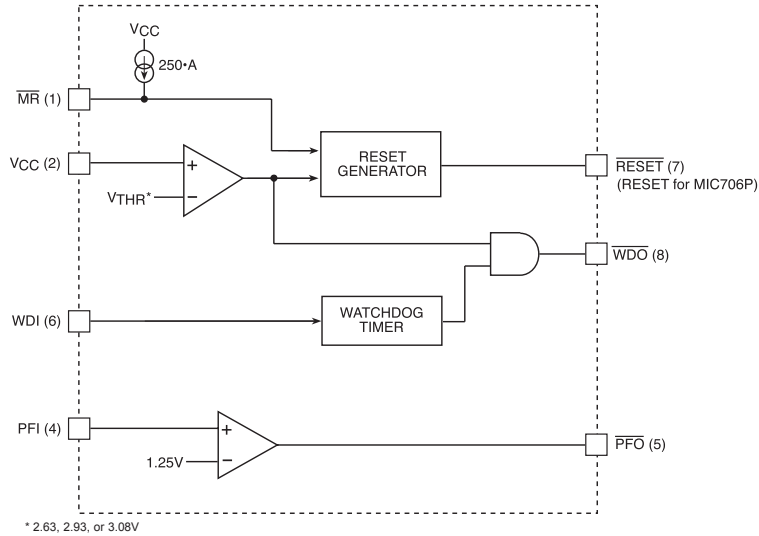


Figure 1. MIC706 Block Diagram

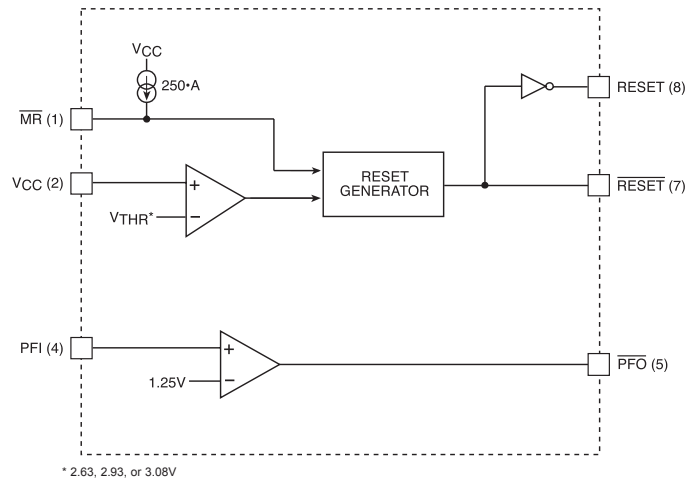
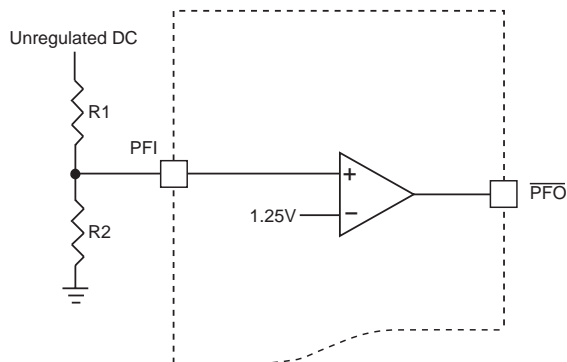


Figure 2. MIC708 Block Diagram

## Circuit Description

### Power Fail Warning

An additional comparator which is independent of other functions on the MIC706/MIC708 is provided for early warning of power failure. An external voltage divider



**Figure 3. Power Fail Comparator**

can be used to compare unregulated DC to an internal 1.25V reference. The voltage divider ratio on the input of the power fail comparator (PFI) can be chosen so as to trip the power fail comparator a few milliseconds before VCC falls below the maximum reset threshold voltage. The output of the power fail comparator ( $\overline{\text{PFO}}$ ) can be used to interrupt the microprocessor when used in this mode and execute shut-down procedures prior to power loss.

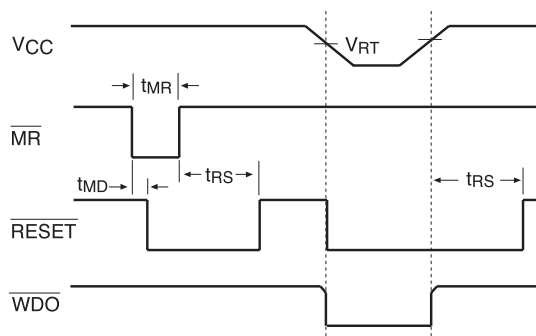
### Watchdog Timer

The microprocessor can be monitored by connecting the WDI pin (watchdog input) to a bus line or I/O line. If a transition doesn't occur on the WDI pin within the watchdog timeout period, then  $\overline{\text{WDO}}$  will go low. A minimum pulse of 50ns (4.5V supply) or 100ns (2.7V supply) or any transition low-to-high or high-to-low on

the WDI pin will reset the watchdog timer. The output of the watchdog timer ( $\overline{\text{WDO}}$ ) will remain high if WDI sees a valid transition within the watchdog timeout period. If VCC falls below the reset threshold voltage then  $\overline{\text{WDO}}$  goes low immediately regardless of WDI. Likewise,  $\overline{\text{WDO}}$  goes high immediately after VCC exceeds the reset threshold.  $\overline{\text{WDO}}$  can be connected to  $\overline{\text{MR}}$  to generate a reset pulse upon watchdog timeout.

### Microprocessor Reset

The RESET pin is asserted whenever VCC falls below the reset threshold voltage or when  $\overline{\text{MR}}$  goes low. The reset pin remains asserted for a period of 200ms after



**Figure 4. Reset Timing Diagram**

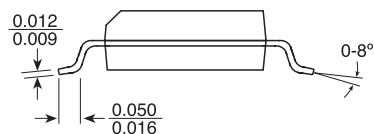
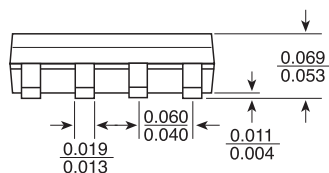
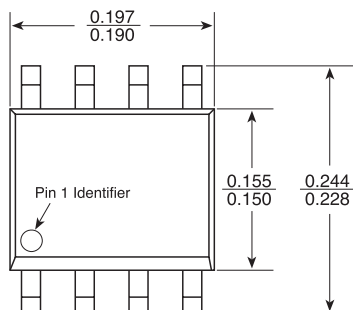
VCC has risen above the reset threshold voltage and  $\overline{\text{MR}}$  goes high. The reset function ensures the microprocessor is properly reset and powers up into a known condition after a power failure. RESET will remain valid with VCC as low as 1.4V.

## Alternate Source Cross Reference Guide

<u>Industry P/N</u>	<u>MIC Direct Replacement</u>
MAX706PCPA	MIC706PN
MAX706PCSA	MIC706PM
MAX706PEPA	MIC706PN
MAX706PESA	MIC706PM
DS706PEPA	MIC706PN
DS706PESA	MIC706PM
MAX706RCPA	MIC706RN
MAX706RCSA	MIC706RM
MAX706REPA	MIC706RN
MAX706RESA	MIC706RM
DS706REPA	MIC706RN
DS706RESA	MIC706RM
MAX706SCPA	MIC706SN
MAX706SCSA	MIC706SM
MAX706SEPA	MIC706SN
MAX706SESA	MIC706SM
DS706SEPA	MIC706SN
DS706SESA	MIC706SM
MAX706TCPA	MIC706TN
MAX706TCSA	MIC706TM
MAX706TEPA	MIC706TN
MAX706TESA	MIC706TM
DS706TEPA	MIC706TN
DS706TESA	MIC706TM
MAX708RCPA	MIC708RN
MAX708RCSA	MIC708RM
MAX708REPA	MIC708RN
MAX708RESA	MIC708RM
DS708REPA	MIC708RN
DS708RESA	MIC708RM
MAX708SCPA	MIC708SN
MAX708SCSA	MIC708SM
MAX708SEPA	MIC708SN
MAX708SESA	MIC708SM
DS708SEPA	MIC708SN
DS708SESA	MIC708SM
MAX708TCPA	MIC708TN
MAX708TCSA	MIC708TM
MAX708TEPA	MIC708TN
MAX708TESA	MIC708TM
DS708TEPA	MIC708TN
DS708TESA	MIC708TM

## Packaging Information

**M Package, 8-Pin Small Outline**



**N Package, 8-Pin Plastic Dual-In-Line**

