MIC50398/MIC50399

Six Decade Counter / Display Decoder

Not Recommended for New Designs

General Description

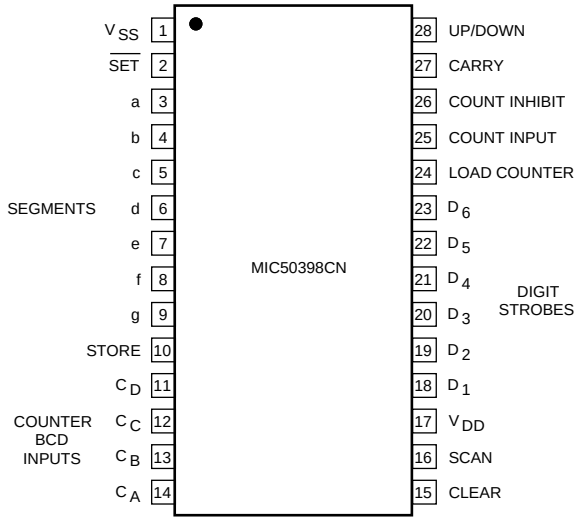
The MIC50398/9 is an ion-implanted, P-channel MOS six-decade synchronous up/down-counter/display driver with storage latches. The counter can be loaded digit-by-digit with BCD data. The counter has an asynchronous-clear function.

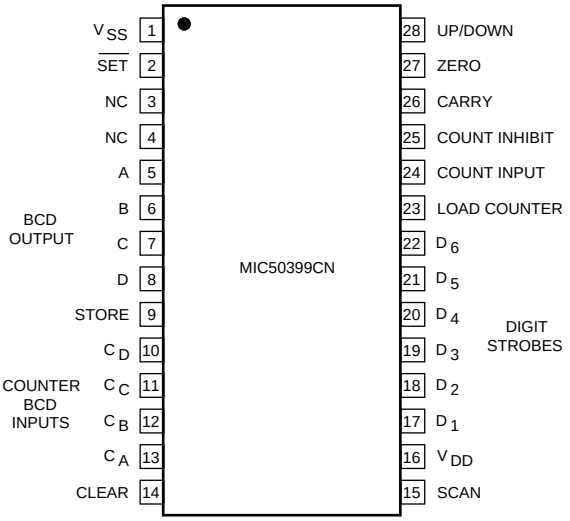
Scanning is controlled by the scan oscillator input which is self-oscillating or can be driven by an external signal. The contents of the counter can be transferred into the 6-digit latch which is then multiplexed from MSD to LSD in BCD or 7-segment format to the output. These devices are intended to interface directly with the standard CMOS logic families.

Features

- Single power supply
- Schmitt-Trigger on the count-input
- Six decades of synchronous up/down counting
- Look-ahead carry or borrow
- Loadable counter
- Multiplexed seven-segment outputs MIC50398N
- Multiplexed BCD outputs, MIC50399N
- Internal scan oscillator

Pin Connection

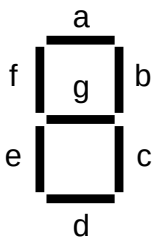




Ordering Information

Part Number	Temp. Range	Package
MIC50398CN	0°C to 70°C	28-pin Plastic DIP
MIC50399CN	0°C to 70°C	28-pin Plastic DIP

Segment Identification



Operations:

Six Decade Counter, Latch

The six decade counter is synchronously incremented or decremented on the positive edge of the count input signal. A Schmitt trigger on this input provides hysteresis for protection against both a noisy environment and double triggering due to a slow rising edge at the count input.

The count inhibit can be changed in coincidence with the positive transition of the count input. Count inhibit must remain high while the count input is high to inhibit counting.

The counter will increment when up/down input is high (V_{SS}) and will decrement when up/down input is low. The up/down input can be changed 0.75 μs prior to the positive transition of the count input.

The clear input is asynchronous and will reset all decades to zero when brought high but does not affect the six digit latch or the scan counter.

As long as store input is low, data is continuously transferred from the counter to the display. Data in the counter will be latched and displayed when store input is high. Store can be changed in coincidence with the positive transition of the count input.

The counter is loaded digit by digit corresponding to the digit strobe outputs. BCD thumb wheel switches with four diodes per decade connected between the digit strobe outputs and the BCD inputs is one method to supply BCD data for loading the counter decades.

The load counter pulse must be at V_{SS} 2 μs prior to the positive transition of the digit strobe of the digit to be loaded. The load counter pulse may be removed after the positive transition of the digit strobe since the chip internally latches this signal. The BCD data to be loaded must be valid through the negative transition of the digit strobe.

Inputs, Outputs

The seven segment outputs are open drain capable of sourcing 10mA average current per segment over one digit cycle. Segments are on when at V_{SS}. The Carry, Zero, BCD and digit strobe outputs are push pull and are on when at V_{SS}. All inputs except Counter BCD and SCAN inputs are high impedance CMOS compatible.

Two basic outputs originate from the counter: zero output, and carry output. Each output goes high on the positive (V_{SS}) going edge of the count input under the following conditions:

Zero output goes high for one count period when all decades contain zero. During a load counter operation the zero output is inhibited. Zero output is on the MIC50399 only.

The carry output goes high with the leading edge of the count input at the count of 000000 when counting up or at 999999 when counting down and goes low with the negative going edge of the same count input. During a load counter operation the carry output is inhibited.

A count frequency of 1.5 MHz can be achieved if the zero output and carry output are not used. These outputs do not respond at this frequency due to their output delay illustrated on the timing diagram.

BCD & Seven Segment Outputs

BCD or seven segment outputs are available. Digit strobes are decoded internally by a divide by six Johnson counter. This counter scans from MSD to LSD. By bringing the $\overline{SET}$ input low, this counter will be forced to the MSD decade count. During this time the segment outputs are blanked to protect against display burn out.

BCD outputs are valid for MSD when $\overline{SET}$ is low. Applying V_{SS} to $\overline{SET}$ allows normal scan to resume. Digit 6 output is active (V_{SS}) until the next scan clock pulse brings up digit 5 output.

The segment outputs and digit strobes are blanked during the interdigit blanking time. Typically the interdigit blanking time is 3 to 10 microseconds when using the internal scan oscillator.

BCD output data changes at the beginning of the interdigit blanking time. Therefore the BCD output data is valid when the positive transition of a digit output occurs. BCD outputs are on MIC50399 only.

Scan Oscillator

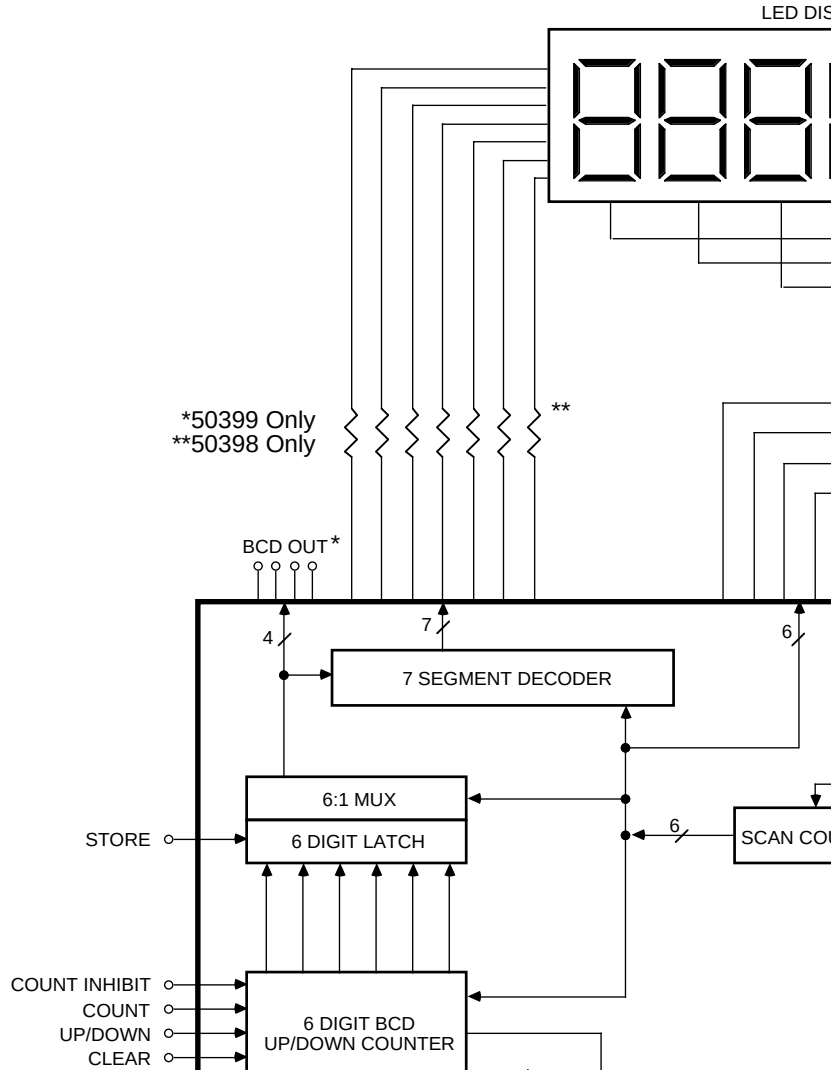
The counters have an internal scan oscillator. The frequency of the scan oscillator is determined by an external capacitor between V_{SS} or V_{DD} and scan input. The wave form present on the scan oscillator input is triangular in the self oscillate mode. An external oscillator may also be used to drive the scan input.

In the external drive mode the interdigit blanking time will be the sum of the negative dwell period of the external oscillator and the normal self oscillate blanking time. (3→10 μs). Display brightness can be controlled by the duty cycle of the external scan oscillator.

Typically, the scan oscillator will oscillate at the following frequencies with these nominal capacitor values from V_{SS} to scan input.

C_{IN}	Min	Max
820 pF	1.4 kHz	4.8 kHz
470 pF	2.0 kHz	6.8 kHz
120 pF	7.0 kHz	20 kHz

Functional Diagram



Absolute Maximum Ratings*

Voltage on Any Terminal Relative to V_{SS} +0.3V to –20V
Operating Temperature Range (Ambient) 0°C to +70°C
Storage Temperature Range (Ambient) –40°C to +100°C

*Operating above absolute maximum ratings may damage the device.

Maximum Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
T_A	Operating Temperature	0	70	°C	
V_{SS}	Supply voltage (V_{DD} = 0V)	10	15	V	
I_{SS}	Supply Current		40	mA	1
B_V	Break Down Voltage (Segment only @ 10 µA)		V_{SS} – 26	V	MIC50398 only
P_D	Power Dissipation		670	mW	2

Electrical Characteristics

(V_{DD} = 0V, V_{SS} = +10.0V to +15.0, 0°C ≤ T_A ≤ 70°C)

Static Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage, “0”	V_{DD}	0.2 V_{SS}	V	
V_{IH}	Input High Voltage, “1”	V_{SS} – 1	V_{SS}	V	3
V_{OL}	Output Voltage “0” @ 30 µA		0.2 V_{SS}	V	4
V_{OH}	Output Voltage “1” @ 1.5 mA	0.8 V_{SS}		V	4
I_{OH}	Output Current “1” Digit strobes Segment outputs	 3.0 10.0		 mA mA	 5 6
I_{SCAN}	Scan Input Pullup Current @ 0 V		5.5	mA	
I_{SCAN}	Scan Input Pulldown Current @ 15 V	2	40	µA	
$I_{\overline{SET}}$	$\overline{SET}$ Input Pullup Current @ 0V	5	60	µA	

Note 1: I_{SS} with inputs and outputs open at 0°C. 33 mA at 25°C and 28 mA at 70°C. This does not include segment current. Total power per segment must be limited not to exceed power dissipation of package. (θ_{JA} = 100°C/Watt)

Note 2: All outputs loaded.

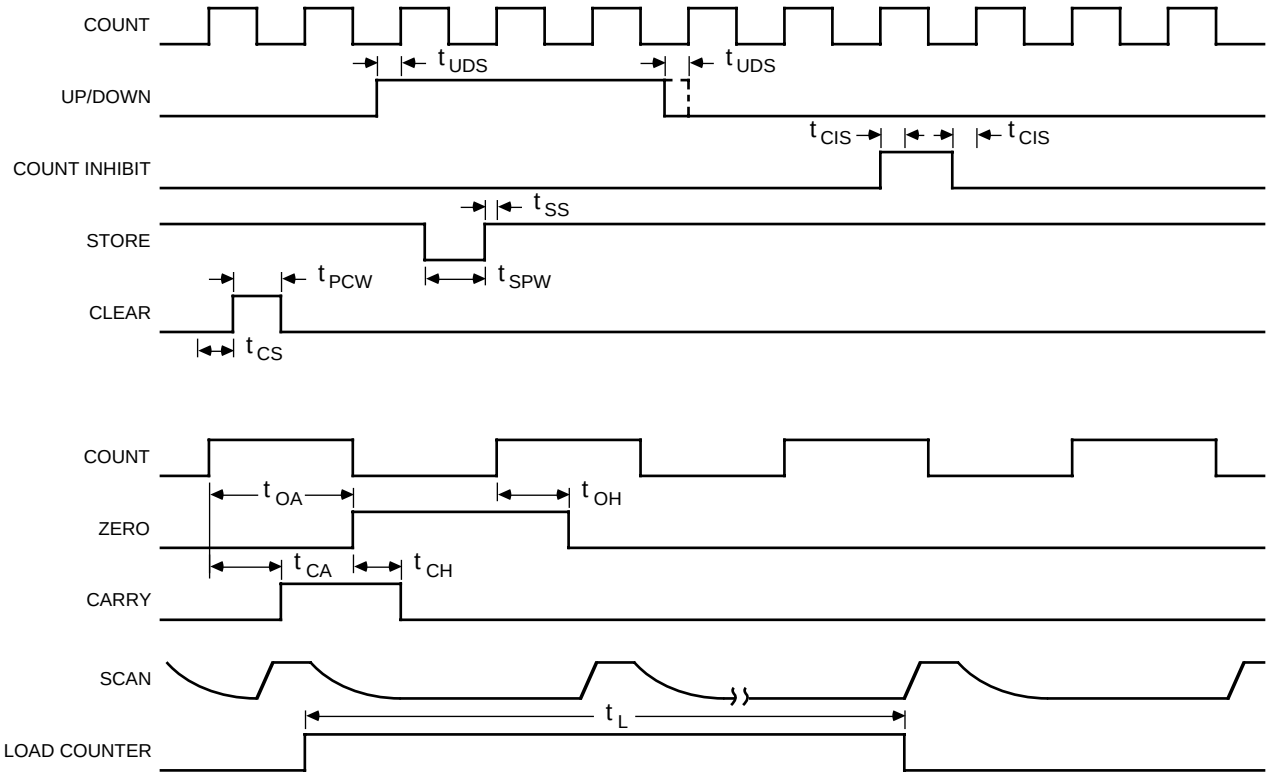
Note 3: MIN V_{IH} from C_A C_B C_C C_D inputs is V_{SS} – 3.5 V. Those inputs have internal pulldown resistors to V_{DD}.

Note 4: This applied to the push pull CMOS compatible outputs. Does not include digit strobes on segment outputs.

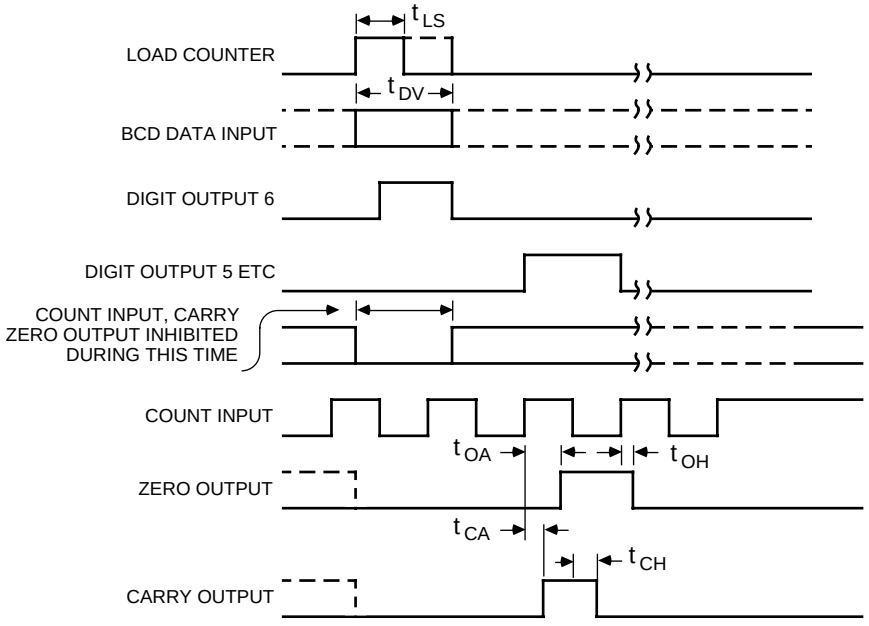
Note 5: For V_{OUT} = V_{SS} – 2.0 Volts. Average value over one digit cycle.

Note 6: For V_{OUT} = V_{SS} – 3.0 Volts. Average value over one digit cycle.

Timing



Loading Counter, Register (1 Digit)



t_{LS} 2.0 µs min NOTE: REF. TO POSITIVE TRANSITION OF DIGIT OUTPUT

t_{DV} 2.0 µS min NOTE: REF. TO NEGATIVE EDGE OF DIGIT OUTPUT

NOTE:
The inhibit function of the zero or carry outputs does not end when the Load Counter input goes to a “0” unless that transition occurs during interdigit blanking period at least 2.0 µs prior to a positive transition of a digit output.

Dynamic Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
f_{CI}	Count Input Frequency	0	1.5	MHz	7,8
f_{SI}	Scan Input Frequency	0	20	kHz	
t_{CPW}	Count Pulse Width	325		ns	9
t_{SPW}	Store Pulse Width	2.0		µs	
t_{SS}	Store Setup Time	0		µs	10
t_{CIS}	Count Inhibit Setup Time	0		µs	10
t_{UDS}	Up/Down setup Time	–0.75		µs	10
t_{CPW}	Clear Pulse Width	2.0		µs	10
t_{CS}	Clear Setup Time	–0.5		µs	10
t_{OA}	Zero Access Time		3.0	µs	10 MIC50399 only
t_{OH}	Zero Hold Time		1.5	µs	10 MIC50399 only
t_{CA}	Carry Access Time		1.5	µs	10
t_{CH}	Carry Hold Time		0.9	µs	11
t_L	Load Time	1/6 f_{SI}			12

Note 7: Measured at 50% duty cycle.

Note 8: If carry or zero outputs are used, the count frequency will be limited by their respective output times.

Note 9: The count pulse width must be greater than the carry access time when using the carry output.

Note 10: The positive edge of the count input is the t = 0 reference.

Note 11: Measured from negative edge of count input.

Note 12: Time to load one digit.