

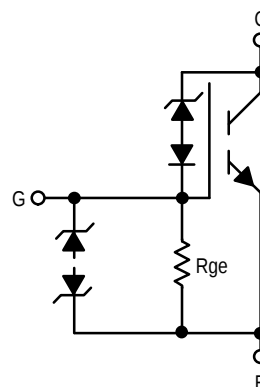
Advanced Information

SMARTDISCRETES™

Internally Clamped, N-Channel IGBT

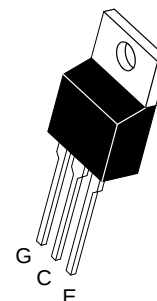
This Logic Level Insulated Gate Bipolar Transistor (IGBT) features Gate–Emitter ESD protection, Gate–Collector overvoltage protection from SMARTDISCRETES™ monolithic circuitry for usage as an **Ignition Coil Driver**.

- Temperature Compensated Gate–Drain Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessors
- Low Saturation Voltage
- High Pulsed Current Capability



MGP20N35CL

**20 AMPERES
VOLTAGE CLAMPED
N-CHANNEL IGBT
 $V_{ce(on)} = 1.8$ VOLTS
350 VOLTS (CLAMPED)**



**CASE 221A-06, Style 9
TO-220AB**

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	CLAMPED	Vdc
Collector–Gate Voltage	V_{CGR}	CLAMPED	Vdc
Gate–Emitter Voltage	V_{GE}	CLAMPED	Vdc
Collector Current — Continuous @ $T_C = 25^\circ\text{C}$	I_C	20	Adc
Reversed Collector Current – pulse width < 100 μs	I_{CR}	12	Apk
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ (TO-220)	P_D	150	Watts
Electrostatic Voltage — Gate–Emitter	ESD	3.5	kV
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case – (TO-220) — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	$^\circ\text{C}$
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

UNCLAMPED INDUCTIVE SWITCHING CHARACTERISTICS

Single Pulse Collector–Emitter Avalanche Energy @ Starting $T_J = 25^\circ\text{C}$ @ Starting $T_J = 150^\circ\text{C}$	E_{AS}	550 150	mJ
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This document contains information on a new product. Specifications and information herein are subject to change without notice.

MGP20N35CL

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-to-Emitter Breakdown Voltage ($I_{\text{Clamp}} = 10 \text{ mA}$, $T_J = -40$ to 150°C)	B_{VCEs}	320	350	380	Vdc
Zero Gate Voltage Collector Current ($V_{\text{CE}} = 250 \text{ V}$, $V_{\text{GE}} = 0 \text{ V}$, $T_J = 125^\circ\text{C}$) ($V_{\text{CE}} = 15 \text{ V}$, $V_{\text{GE}} = 0 \text{ V}$, $T_J = 125^\circ\text{C}$)	I_{CES}	— —	— —	1.0 200	mA μA
Resistance Gate-Emitter ($T_J = -40$ to 150°C)	R_{GE}	10k	16k	30k	Ω
Gate-Emitter Breakdown Voltage ($I_G = 2 \text{ mA}$)	B_{VGEs}	11	13	15	$\pm \text{ V}$
Collector-Emitter Reverse Leakage ($V_{\text{CE}} = -15 \text{ V}$, $T_J = -40$ to 150°C)	I_{CES}	—	8	100	mA
Collector-Emitter Reversed Breakdown Voltage ($I_E = 75 \text{ mA}$)	B_{VCEr}	26	40	120	V

ON CHARACTERISTICS (1)

Gate Threshold Voltage ($V_{\text{CE}} = V_{\text{GE}}$, $I_C = 1 \text{ mA}$) ($V_{\text{CE}} = V_{\text{GE}}$, $I_C = 1 \text{ mA}$, $T_J = 150^\circ\text{C}$)	$V_{\text{GE(th)}}$	1.0 0.75	1.7 —	2.4 1.8	V
Collector-Emitter On-Voltage ($V_{\text{GE}} = 5 \text{ V}$, $I_C = 5 \text{ A}$) ($V_{\text{GE}} = 5 \text{ V}$, $I_C = 10 \text{ A}$) ($V_{\text{GE}} = 5 \text{ V}$, $I_C = 10 \text{ A}$, $T_J = 150^\circ\text{C}$)	$V_{\text{CE(on)}}$	— — —	1.1 1.4 1.4	1.4 1.9 1.8	V
Forward Transconductance ($V_{\text{CE}} > 50 \text{ V}$, $I_C = 10 \text{ A}$)	g_{fs}	10	16	—	S

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{\text{CE}} = 25 \text{ Vdc}$, $V_{\text{GE}} = 0 \text{ Vdc}$, $f = 1.0 \text{ MHz}$)	C_{iss}	—	2800	—	pF
Output Capacitance		C_{oss}	—	200	—	
Transfer Capacitance		C_{rss}	—	25	—	

SWITCHING CHARACTERISTICS (1)

Total Gate Charge	$(V_{\text{CC}} = 280 \text{ V}$, $I_C = 20 \text{ A}$, $V_{\text{GE}} = 5 \text{ V})$	Q_g	—	45	80	nC
Gate-Emitter Charge		Q_{gs}	—	8.0	—	
Gate-Collector Charge		Q_{gd}	—	20	—	
Turn-Off Delay Time	$(V_{\text{CC}} = 320 \text{ V}$, $I_C = 20 \text{ A}$, $L = 200 \mu\text{H}$, $R_G = 1 \text{ K}\Omega$)	$t_{\text{d(off)}}$	—	TBD	TBD	μs
Fall Time		t_f	—	TBD	TBD	
Turn-On Delay Time	$(V_{\text{CC}} = 14 \text{ V}$, $I_C = 20 \text{ A}$, $L = 200 \mu\text{H}$, $R_G = 1 \text{ K}\Omega$)	$t_{\text{d(on)}}$	—	TBD	TBD	μs
Rise Time		t_r	—	TBD	TBD	

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL ELECTRICAL CHARACTERISTICS

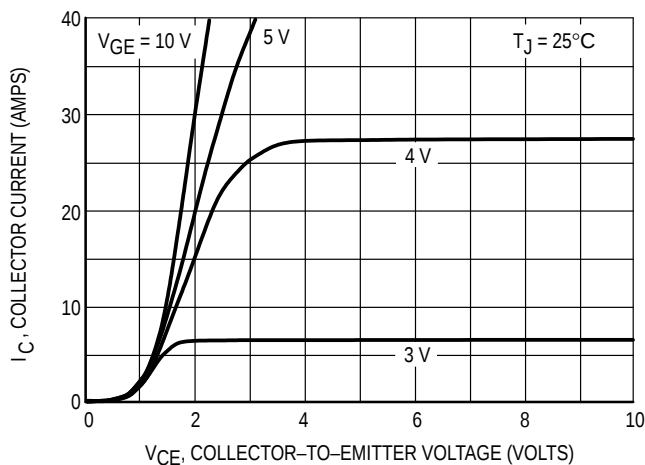
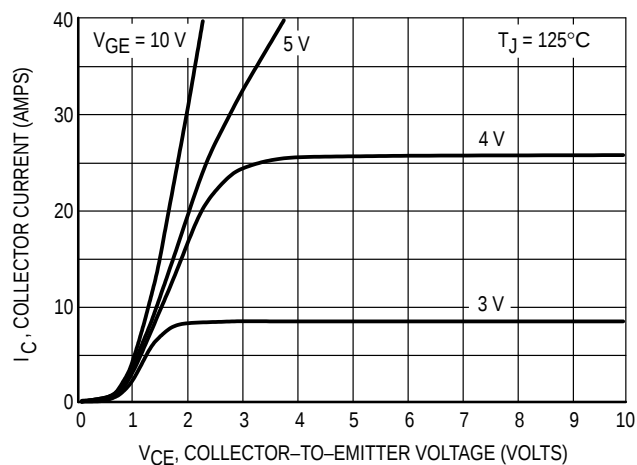
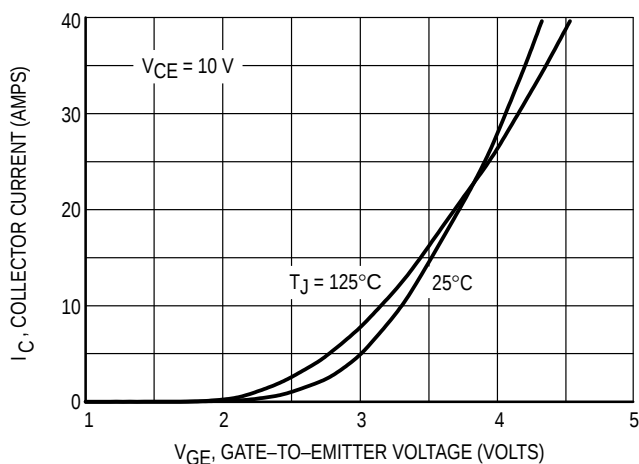
Figure 1. Output Characteristics, $T_J = 25^\circ\text{C}$ Figure 2. Output Characteristics, $T_J = 125^\circ\text{C}$ 

Figure 3. Transfer Characteristics

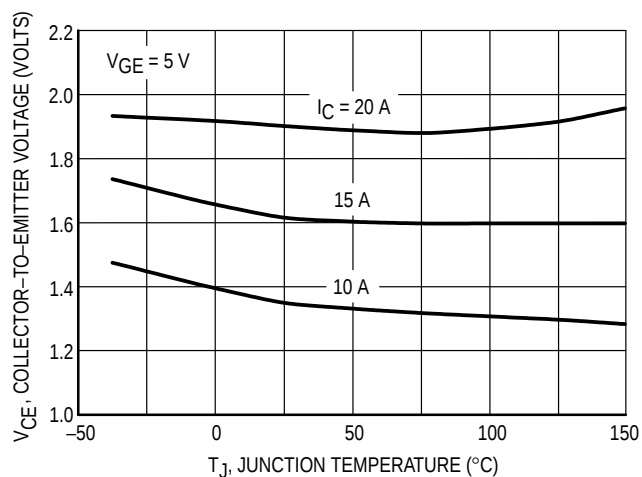


Figure 4. Collector-to-Emitter Saturation Voltage versus Junction Temperature

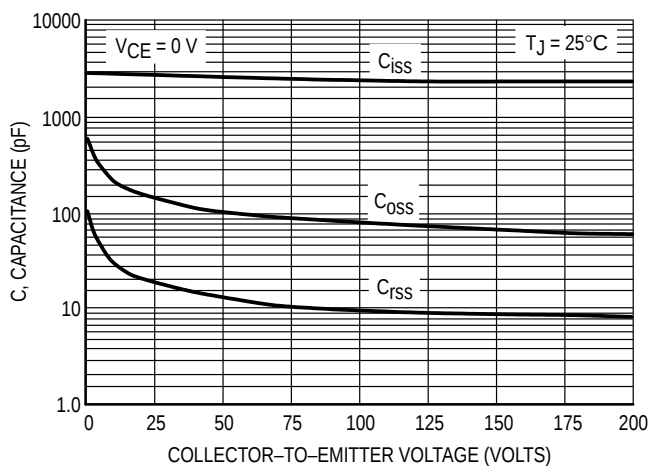


Figure 5. Capacitance Variation

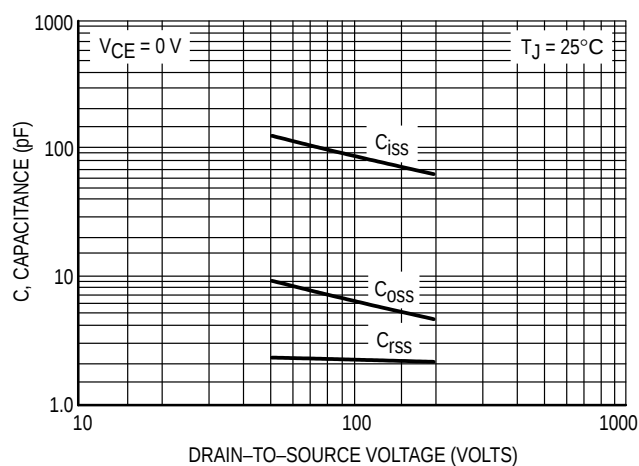


Figure 6. High Voltage Capacitance Variation

MGP20N35CL

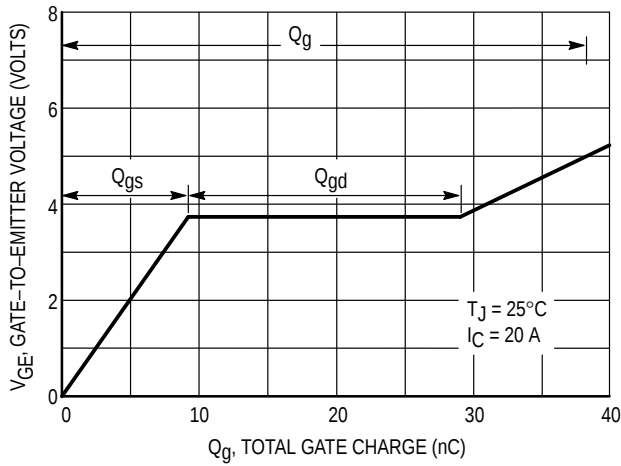


Figure 7. Gate-to-Emitter and Collector-to-Emitter Voltage vs Total Charge

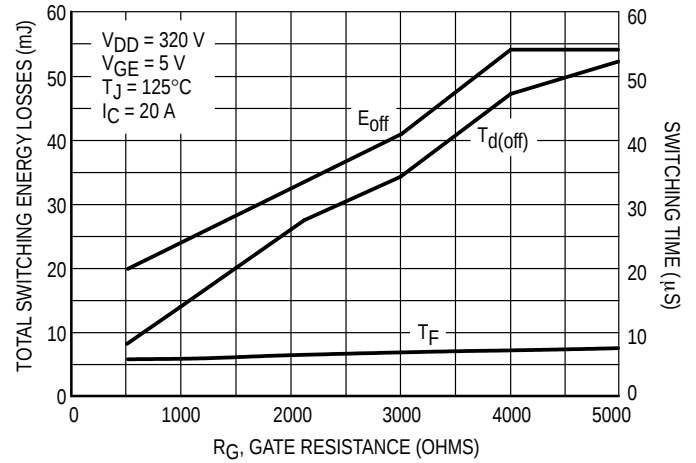


Figure 8. Total Switching Losses versus Gate Temperature

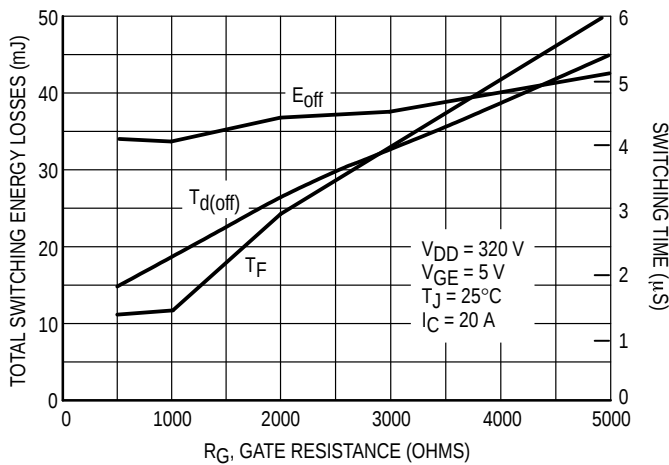


Figure 9. Total Switching Losses versus Gate Resistance

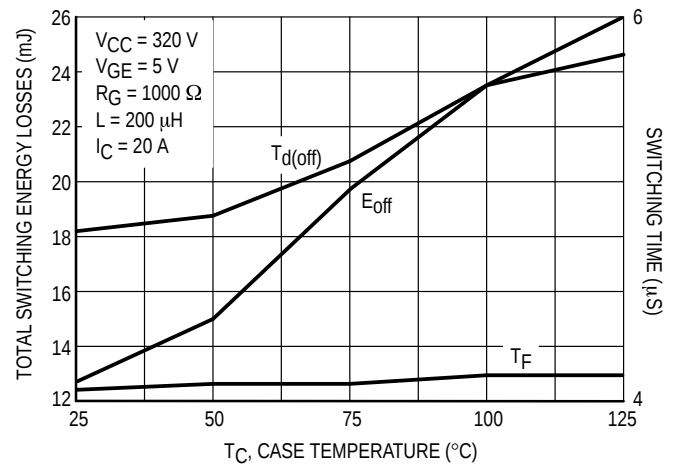


Figure 10. Total Switching Losses versus Case Temperature

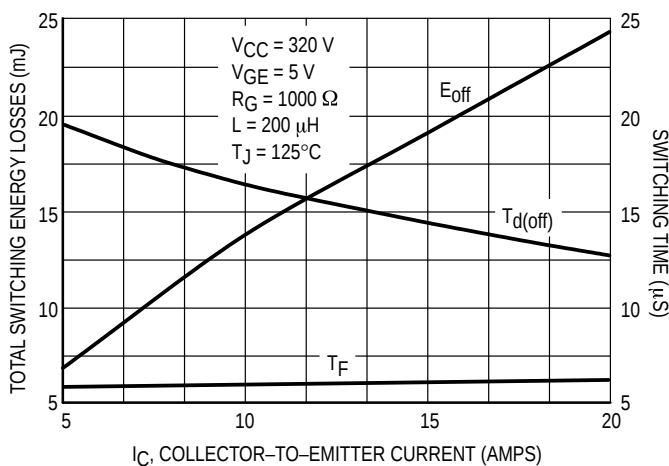


Figure 11. Total Switching Losses versus Collector Current

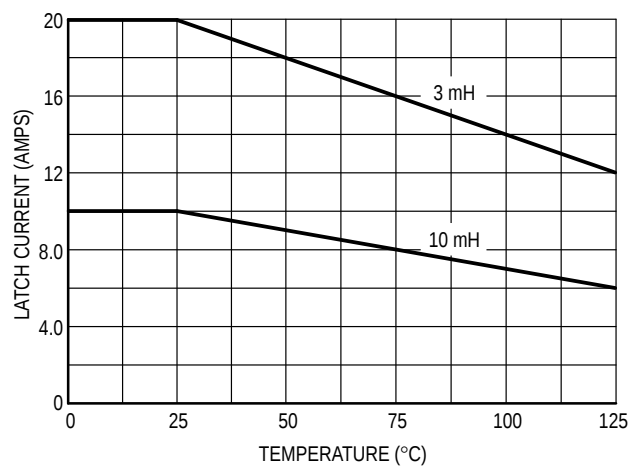


Figure 12. Latch Current versus Temperature

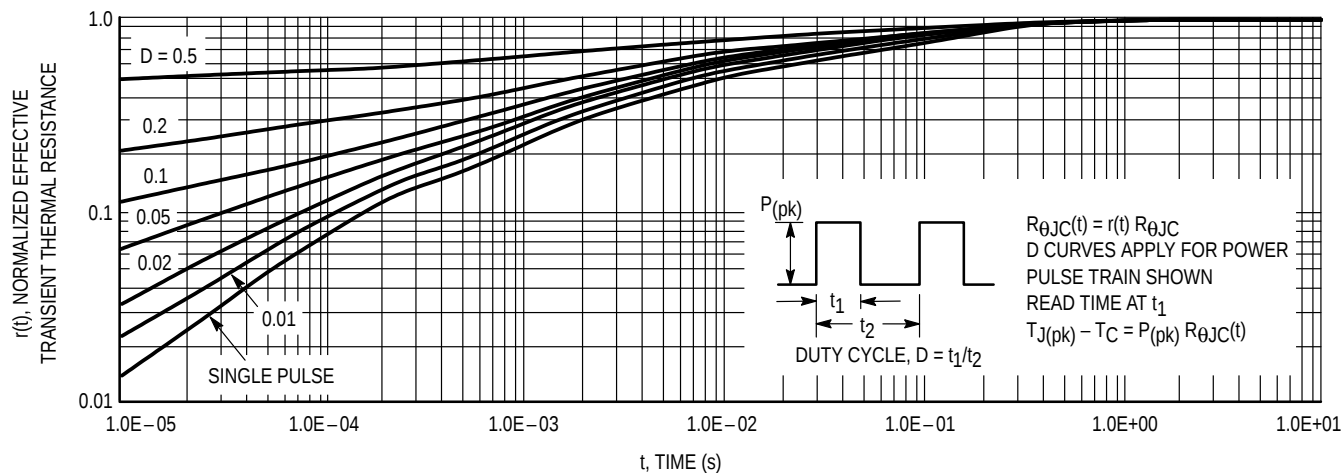
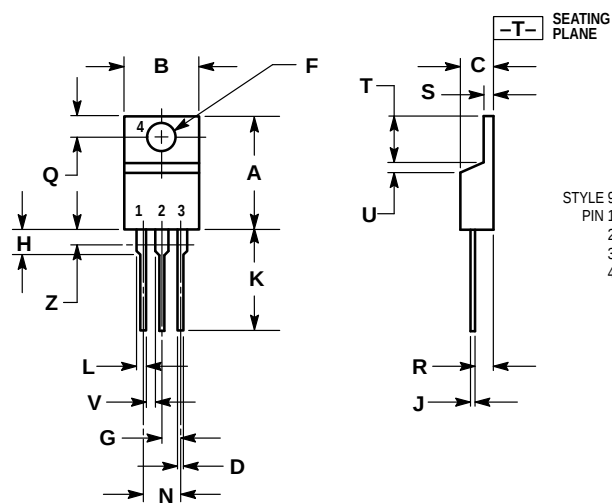


Figure 13. Thermal Response

PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

CASE 221A-06
(TO-220AB)
ISSUE Y

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