MCM2802

32x32 BIT SERIAL ELECTRICALLY ERASABLE PROM

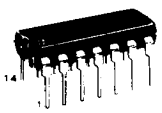
The MCM2802 is a 1K-bit serial Electrically Erasable PROM designed for applications requiring both non-volatile memory and in-system information updates. In digital tuning systems, it provides storage for up to 32 channels. It has external control of timing functions and serial format for data and address.

- Single 5V supply in Read mode
- Organised as 32 Words of 32 Bits
- 5V and 25V supply for Erase and Program
- In-System Program/Erase Capability
- 0—100 kHz clock rate
- Floating gate process
- Expandable to 16K-bit systems
- Word and Array erasable
- 100,000 Write/Erase Cycles

MOS

(N-CHANNEL, SILICON GATE)

32 × 32 BIT
ELECTRICALLY ERASABLE PROM



P SUFFIX
PLASTIC PACKAGE
CASE 646

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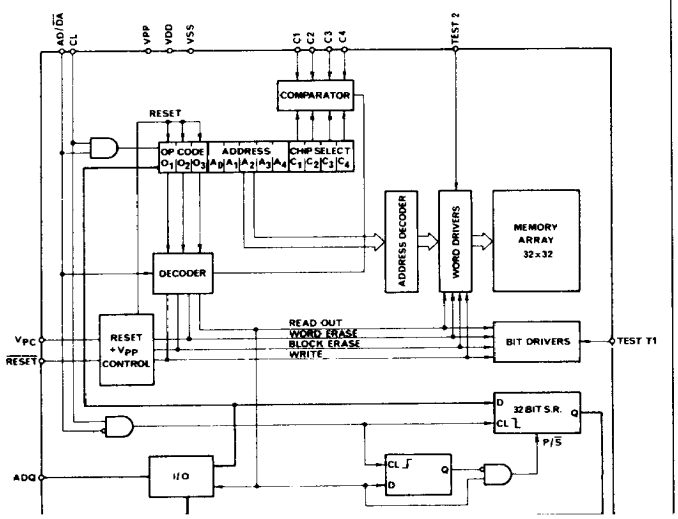
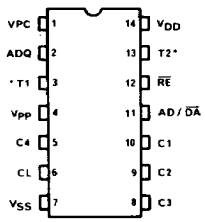
FIGURE 1 — BLOCK DIAGRAM



PIN ASSIGNMENT



*For normal operation, hardwired to VSS

PIN NAMES

VPC	Program Voltage Control
ADQ	Address Input + Data Input/Output
T1, T2	Margin Testing
C1, C2, C3, C4	Chip Address 1 to 4
CL	Clock
$\overline{RE}$	Reset
AD/$\overline{DA}$	Shift Register Select

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maxi-

ABSOLUTE MAXIMUM RATINGS (Voltages referred to V_{SS})

Rating	Symbol	Min.	Max.	Unit
DC Supply Voltage	V_{DD}	− 0.5	8	Vdc
Programming Voltage	V_{PP}	− 0.5	28	Vdc
Input Voltage	V_{IN}	− 0.5	8	Vdc
VP Control Output	V_{PC}	− 0.5	28	Vdc
Operating Temperature Range	T_A	0	70	°C
Storage Temperature Range	T_{STG}	− 55	150	°C

NOTE – Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

SWITCHING CHARACTERISTICS (T_A = 0... 70°C, V_{DD} = 5V ± 10%, V_{PP} = 25V ± 1V)

Pin	Symbol	Parameter	Fig. No.	Min.	Max.	Unit
	t_{ER}	Erase time		100		ms
	t_{WR}	Write time		10		ms
CL	F_{CL}	Clock Frequency $F_{CL} = 1/T_{CL}$	2		100	kHz
CL	t_{CLH}	Clock High Level Hold Time	2	4		µs
CL	t_{CLL}	Clock Low Level Hold Time	2	4		µs
CL	t_{CLRF}	Clock Fall Time and Rise Time	2		1	µs
AD/DA	$t_{AD/DA}$	Register Control to Clock				
		Delay Time except for t_{READ}	2	1		µs
	t_{READ}	After READ opcode only	3	2	100	µs
ADQ	t_{DSUP}	Address/Data In Set-Up	2, 3	2		µs
	t_{DH}	Address/Data In Hold	2, 3	2.0		µs
ADQ	t_{DOUTS}	Data Out Serial Delay	3		1	µs.
	t_{DOUTP}	Data Out Parallel Delay	3		3	µs
	C_{out}	Output Capacitance (V_{out} = 0 V)			12	pF
	C_{in}	Input Capacitance (V_{in} = 0 V)			12	pF

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DC CHARACTERISTICS (T_A = 0... 70°C, V_{DD} = 5V ± 10%, V_{PP} = 25V ± 1V)

Pin	Characteristic	Condition	Symbol	Min.	Max.	Unit
V_{PP}	Supply Current		I_{PP}		3	mA
V_{DD}	Supply Current		I_{DD}		20	mA
ADQ	Tristate Input/Output	V_{OH} = 2.4V	I_{OH}	− 0.1		mA
		V_{OL} = 0.5V	I_{OL}	1.6		mA
		Tristate	I_{IN}		10	µA
All Inputs Except ADQ	Input Leakage		I_{IN}		10	µA
V_{PC}	VP Control	V_{ON} = 1V	I_{ON}	0.7		mA
	Pull down device	OFF state	V_{MAX}		V_{PP}	V
		V_{OFF} = VP	I_{OFF}		10	µA
All Inputs	Input Low Voltage	V_{IL}		0.1	0.8	V
	Input High Voltage	V_{IH}		2.4	5.5	V

FIGURE 2 — GENERAL TIMINGS

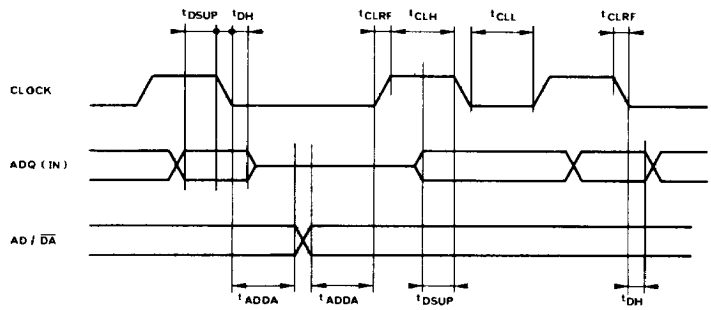


FIGURE 3 — READOUT TIMINGS

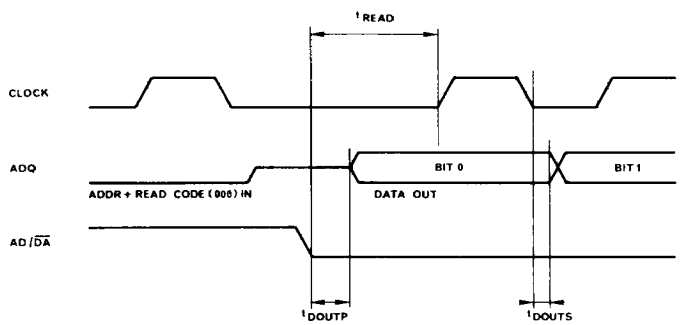


FIGURE 4 – READOUT SEQUENCE

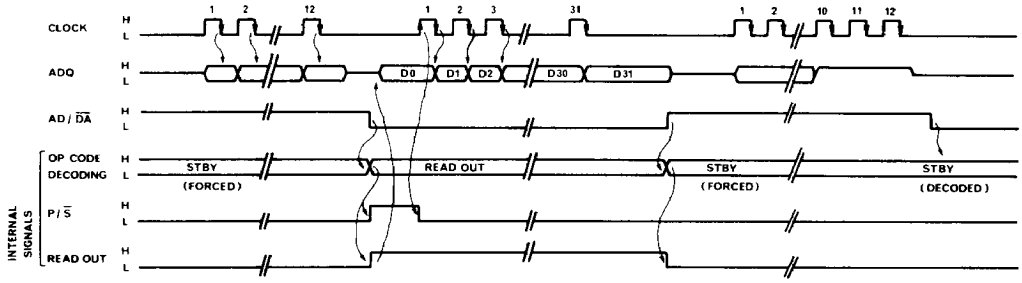


FIGURE 5 – WRITE SEQUENCE

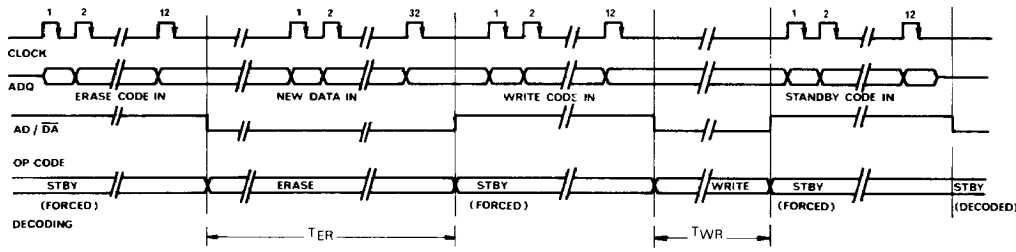
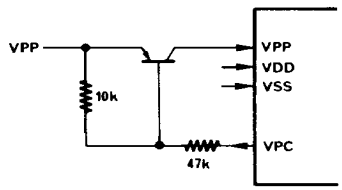
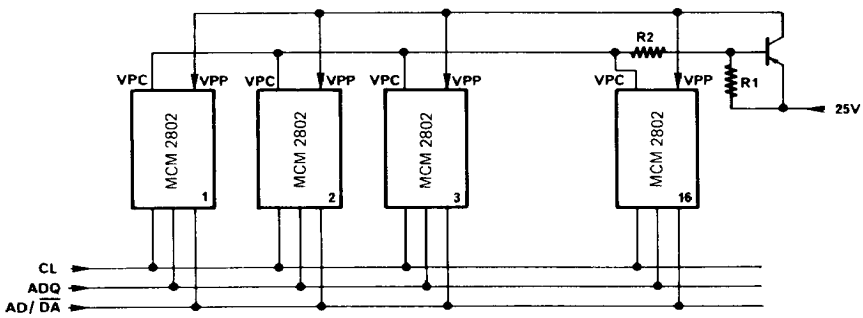


FIGURE 6 – V_{PP} CONTROL AND MULTICHIP SETUP





FUNCTIONAL DESCRIPTION

The circuit accepts 12 bits of Address/Op code in the address register and 32 bits of data in the data register (see figure 1: Block diagram).

ADDRESS/OP CODE FORMAT (figure 1)

The four shifted bits C1 to C4 are used as chip select word in multichip systems. The chip address is defined by hardwiring the C1 to C4 pins. These bits are adjacent to the address field, so that no software modification is required in a program designed for a multi-1K memory application.

The five following A1 to A5 bits select one of the word addresses. The last 3 bits 01 to 03 control the operating modes.

Function	01	02	03
Read	0	0	0
Word Erase	0	1	0
Block Erase	1	1	0
Write	1	0	0
Standby	X	X	1

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READ OPERATION (figure 4)

1) The ADDRESS/OP CODE is loaded. The address selecting the word to be read and the op code bits being the READ code.

2) The AD/$\overline{DA}$ is switched to the data mode, thus initiating the parallel transfer from the core to the shift register. First bit of data is present at the output.

3) As soon as the first of the 31 data out clock pulses is applied, the parallel transfer is stopped and data is shifted at the output. Data is recirculated in the data register.

4) The output buffer is turned on only when READ is internally decoded, AD/$\overline{DA}$ is low and chip is selected by C1 and C4. Otherwise it is in the high impedance state.
Addresses and data are clocked in and out with the falling edge of clock.
An erased bit corresponds to a low level output.

WRITING (figure 5)

1) ADDRESS/OP CODE is shifted in, the op code being either BLOCK ERASE or WORD ERASE.

2) Switching the AD/$\overline{DA}$ line low for $t = t_{ERASE}$ initiates

4) The AD/$\overline{DA}$ line is switched low again for a $t = t_{WRITE}$, during which the selected word is programmed.

5) At the end of the WRITE operation it is recommended to load op code STANDBY and to return input AD/$\overline{DA}$ to the low state.

ERASE

Both BLOCK ERASE and WORD ERASE are provided and are controlled by the op code. V_{PP} has to be applied for BLOCK ERASE, WORD ERASE and for WRITE. For all other conditions it can be switched off to high impedance or V_{DD} or V_{SS}.

STANDBY

When AD/$\overline{DA}$ is high, the instruction decoder is disabled and hence STANDBY is forced. By shifting the STANDBY op code into the address register STANDBY will be recognized independently of the state of AD/DA.

CLOCK

The active high clock is only used for shifting data and addresses. This shift occurs on the clock falling edge.

CHIP SELECTION

The ADDRESS/DATA line can be used as a chip select in a system having other serial I/O devices. DATA and CLOCK lines being shared the non-volatile memory is only activated when the AD/$\overline{DA}$ line is low. Shifting information to the data register has no effect to the core while the chip is deselected.
In a multi-memory arrangement, all the lines including ADDRESS/DATA, CLOCK and DATA, are shared, with the exception of C1 to C4 which are hardwired to V_{DD} or V_{SS}, thus defining the circuit address. All V_P control outputs of the memory circuits can be combined in a wired OR configuration.

DATA PROTECTION

When V_{PP} is turned off, data stored in the array is always protected. A V_{PP} control output is provided for switching the V_{PP} supply. It consists of a pull down device to V_{SS}. This device is turned on only when: V_{DD} is present, a WRITE or ERASE code has been loaded in the address register and AD/$\overline{DA}$ is low.
Schematics for this external V_{PP} control are proposed in figure 6.