MCM2801

Advance Information

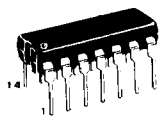
16 x 16-BIT SERIAL ELECTRICALLY ERASABLE PROM

The MCM2801 is a 256-bit serial Electrically Erasable PROM designed for handling small amounts of data in applications requiring both non-volatile memory and in-system information updates.

The MCM2801 offers in-system erase and reprogram capability. It has external control of timing functions and serial format for data and address. The MCM2801 is fabricated in floating gate technology for high reliability and producibility.

- Single +5 V power supply
- Organized as 16 words of 16 bits
- MPU Bus compatible
- Single + 25 V power supply for erase and program
- In-System program/erase capability
- Both word and whole array erasable
- 100,000 write/erase cycles

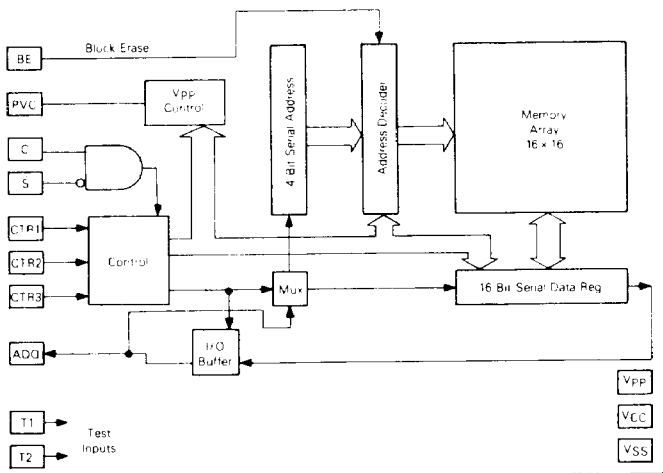
MOS
(N-CHANNEL, SILICON GATE)
16 × 16 BIT ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY



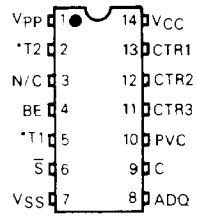
PLASTIC PACKAGE
CASE 646

6

BLOCK DIAGRAM



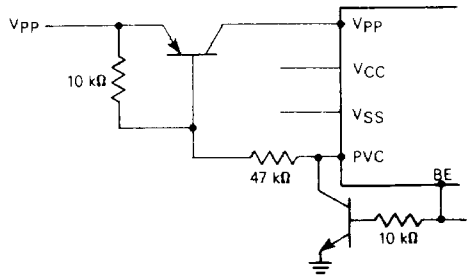
PIN ASSIGNMENT



*For normal operation, these inputs should be hardwired to V_{SS}

PIN NAMES	
ADQ	Multiplexed Address/ Data-In/Data-Out
C	Clock
PVC	Program Voltage Control
CTR1, 2, 3	Control
$\overline{BE}$	Block Erase
$\overline{S}$	Chip Select
T1, T2	Test Pins

FIGURE 1 - TYPICAL Vpp CONTROL
(See AC CONDITIONS AND CHARACTERISTICS - NOTE 2)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is advance information and specifications are subject to change without notice.

MODE SELECTION

Mode	Pin Number						
	1 V_{PP}	6 $\overline{S}$	7 V_{SS}	11 CTR3	12 CTR2	13 CTR1	14 V_{CC}
Standby	V_{SS} or V_{CC}	V_{IH}	V_{SS}	V_{IH}	V_{IH}	V_{IH}	V_{CC}
Word Erase	V_{PP}	V_{IL}	V_{SS}	V_{IH}	V_{IL}	V_{IL}	V_{CC}
Write	V_{PP}	V_{IL}	V_{SS}	V_{IL}	V_{IH}	V_{IL}	V_{CC}
Serial Data Out	V_{SS} or V_{CC}	V_{IL}	V_{SS}	V_{IH}	V_{IH}	V_{IL}	V_{CC}
Serial Address In	V_{SS} or V_{CC}	V_{IL}	V_{SS}	V_{IL}	V_{IL}	V_{IH}	V_{CC}
Serial Data In	V_{SS} or V_{CC}	V_{IL}	V_{SS}	V_{IH}	V_{IL}	V_{IH}	V_{CC}
Read	V_{SS} or V_{CC}	V_{IL}	V_{SS}	V_{IL}	V_{IH}	V_{IH}	V_{CC}
Standby	V_{SS} or V_{CC}	V_{IH}	V_{SS}	V_{IL}	V_{IL}	V_{IL}	V_{CC}

ABSOLUTE MAXIMUM RATINGS (1)

Rating	Value	Unit
Temperature Under Bias	−40 to +85	°C
Operating Temperature Range	0 to +70	°C
Storage Temperature	−55 to +150	°C
All Input or Output Voltages with Respect to V_{SS} (Except PVC)	+8 to −0.5	V
V_{PP} Supply Voltage with Respect to V_{SS}	+28 to −0.5	V
PVC Voltage with Respect to V_{SS}	+28 to −0.5	V

NOTE 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

6

RECOMMENDED DC OPERATING CONDITIONS (Full operating voltage and temperature range unless otherwise noted.)

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC} V_{PP}	4.5 24.0	5.0 25	5.5 26.0	V
Input High Voltage	V_{IH}	2.4	–	V_{CC} + 1.0	V
Input Low Voltage	V_{IL}	−0.1	–	0.8	V

OPERATING DC CHARACTERISTICS

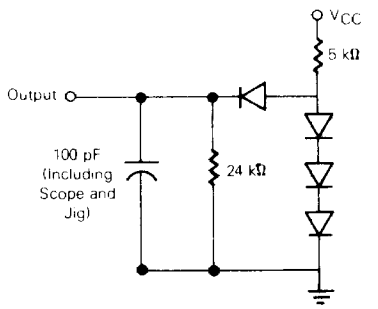
Characteristic	Condition	Symbol	Min	Typ	Max	Units
Input Sink Current	$0 < V_{in} < V_{CC}$	I_{in}	–	–	10	μA
V_{CC} Supply Current	V_{CC} = 5.5 V	I_{CC}	–	–	30	mA
V_{PP} Supply Current	V_{PP} = 26.0 V	I_{PP}	–	–	4.0	mA
Output Low Voltage	I_{OL} = 1.0 mA	V_{OL}	–	–	0.5	V
Output High Voltage	I_{OH} = −0.1 mA	V_{OH}	2.4	–	–	V
PVC Current (Write or Word Erase)	PVCL = 1 V	PVC_{ON}	200	–	–	μA
PVC Leakage	PVCH = 26 V	PVC_{OFF}	–	–	5	μA

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = +5 V, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{ID}	–	6.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	–	12	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta_t/\Delta V$.

FIGURE 2 – OUTPUT LOAD



AC OPERATING CONDITIONS AND CHARACTERISTICS

Input Pulse Levels ..... 0.65 Volts and 2.6 Volts
Input Rise and Fall Times ..... 20 ns
Input Timing Levels ..... 1.0 Volt and 3.8 Volts
Output Timing Levels ..... 1.0 Volt and 2 Volts
Output Load ..... See Figure 2

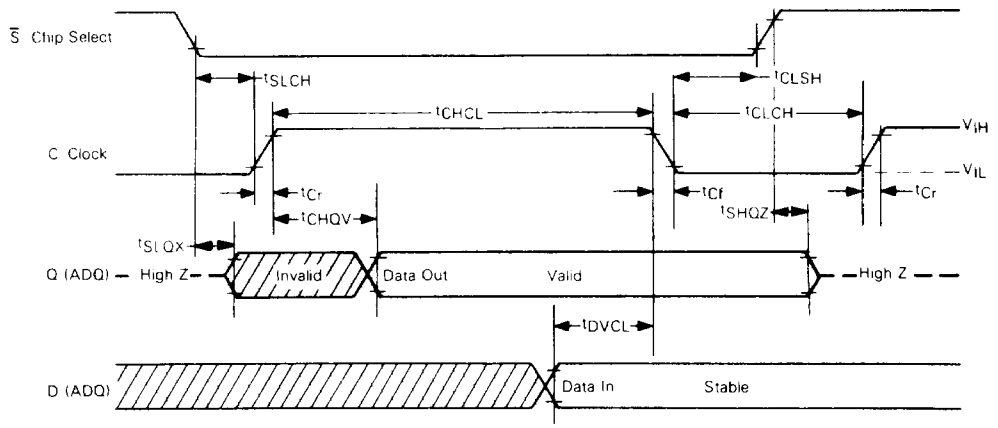
Characteristic	Symbol	Min	Max	Unit
Erase Time	t_{ERASE}	100	–	ms
Write Time	t_{WRITE}	10	–	ms
Clock High Level Hold Time	t_{CHCL}	4	10	µs
Clock Low Level Hold Time	t_{CLCH}	4	–	µs
Clock Rise Time	t_{Cr}	5	1000	ns
Clock Fall Time	t_{Cf}	5	1000	ns
Chip Select Setup	t_{SLCH}	1	–	µs
Chip Select Hold	t_{CLSH}	1	–	µs
Data Out Delay	t_{CHQV}	–	1	µs
Address In Setup	t_{AVCL}	1	–	µs
Data In Setup	t_{DVCL}	1	–	µs
Control Setup Time	t_{CtrVCH}	1	–	µs
Control Hold Time	t_{CtrX}	50	–	ns
Data-Off Time (from the Clock)	t_{CHQZ}	–	3.0	µs
Chip Select Low to Output Active Time	t_{SLQX}	–	2.0	µs
Data-Off Time (from Chip Select)	t_{SHQZ}	–	2.0	µs

NOTE 2: During application of V_{PP}, a 1 µF ceramic capacitor is recommended between V_{PP} and Ground to suppress any voltage transients which might damage the device.

6

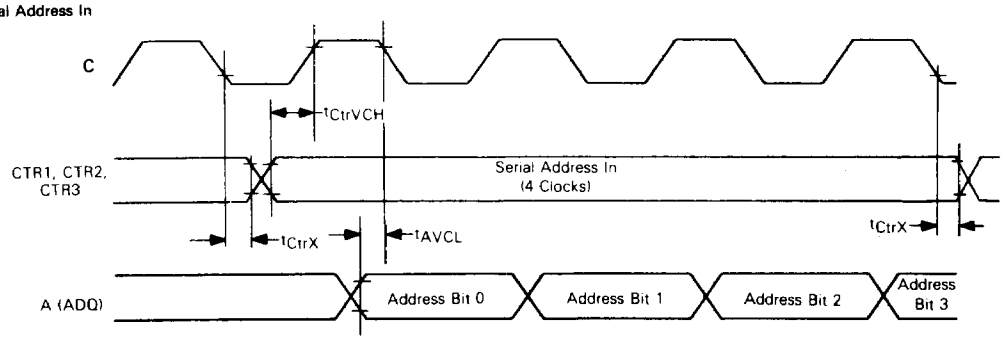
TIMING DIAGRAMS

Clock Cycle Detail



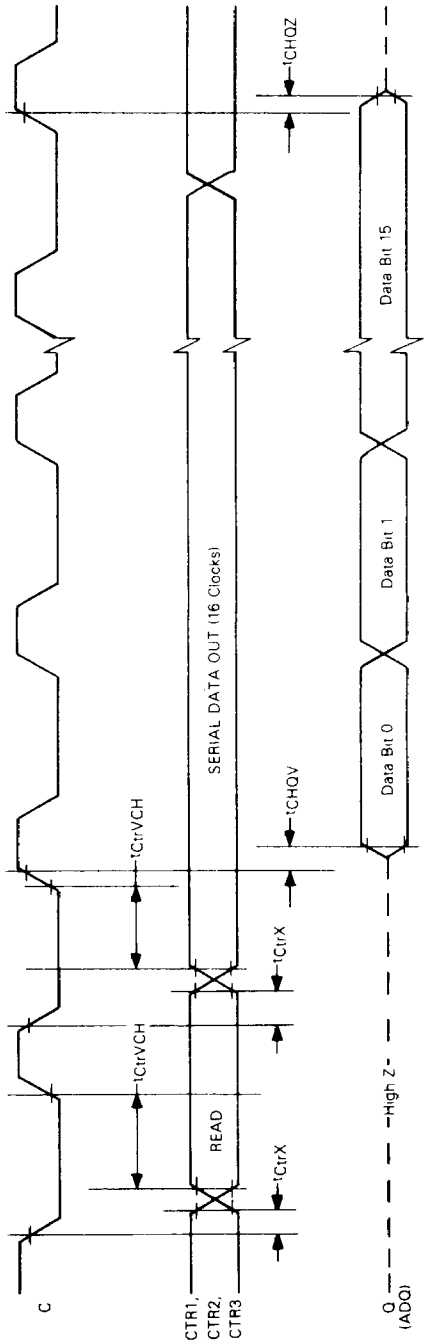
All times defined at 10% or 90% points.

Serial Address In

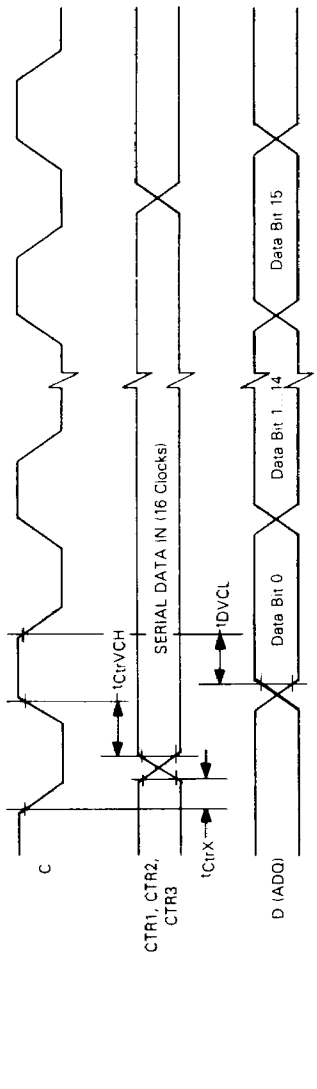


6

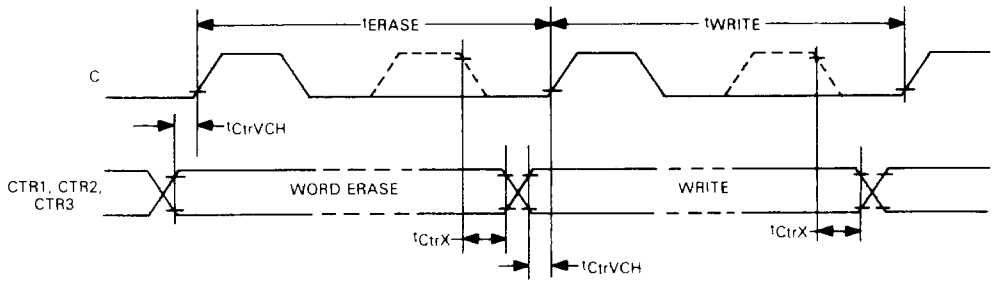
READ AND SERIAL DATA OUT



SERIAL DATA IN



ERASE-WRITE SEQUENCE



NOTE: One clock pulse is sufficient to load a new control code.

FUNCTIONAL DESCRIPTION

The memory stores sixteen words, each of sixteen bits. All functions are selected by a 3 bit parallel control code. The clock line is used to strobe these codes and to serially shift data and addresses.

Read-Out

1. The 4-bit serial address is shifted on the ADQ line while the SERIAL ADDRESS-IN code is applied on the three control pins.
2. The READ instruction is strobed with one clock pulse. This reads the word from the new address in the memory array and parallel loads it into the data register.
3. While the SERIAL DATA-OUT code is being applied, data is shifted out on the ADQ pin with 16 clock pulses. In this mode, the ADQ pin output buffer is active.

Writing

1. The address is changed, if necessary, in the same manner as in the readout.
2. While the SERIAL DATA-IN code is being applied, data is shifted in on the ADQ pin with 16 clock pulses. If the data to be written has already been shifted into the data register, it is not necessary to re-enter the 16 bits, so this step may be omitted.
3. The WORD ERASE code is strobed in with one clock pulse. After the specified ERASE time, the addressed word is erased.
4. The WRITE code is strobed in with one clock pulse. After the specified WRITE time, a STANDBY code can be strobed in to stop writing. Data will be programmed at the specified address.

   It is also possible to change the sequence by erasing a memory location before starting a write sequence.

Standby

Either of the two STANDBY codes, when strobed in with a clock pulse, puts the memory in a quiescent state. The output is then in the high-impedance state and the absence or presence of the clock will not affect the device.

Pin Description

The active high clock signal (C) is used for shifting addresses and data into or out of the chip. It is also used for strobing control codes.

The I/O pin (ADQ) is used for entering addresses and data in. It is in the output state only for shifting output data.

The active low Chip Select pin (S) is only used to block the clock and put the ADQ buffer into the high-impedance mode. It has no influence on the operating status of the device and does not force a standby condition.

The programming voltage control pin (PVC) is an open-drain output that is active when a WORD ERASE or WRITE control code is strobed in. As shown in Figure 1, it can be used to control the V_{PP} supply applied to the circuit. The BLOCK ERASE (BE) pin can be used to clear the whole array. As the PVC output is not active in this state, the programming voltage should be directly applied to the V_{PP} pin for the specified erase time.

The Test inputs (TEST1) and TEST2) are provided for testing purpose only and should be connected to V_{SS} in any application.

Data Protection

When V_{PP} is turned off, data stored in the array is protected. The programming voltage should not be applied to the V_{PP} pin if V_{CC} is not present. Therefore, use of the PVC control output, which is controlled by the V_{CC} supply is recommended. Using this feature, V_{PP} and V_{CC} can be turned on or off in any sequence without disturbing data in the array. However, to avoid spurious control codes being strobed into the device, all inputs should be stable when V_{PP} is on.

General Comments

The erased state corresponds to a logical zero at the ADQ output.

WRITE (for any address) must be preceded by an ERASE at the same address.

V_{PP} is necessary for WRITE, WORD ERASE or BLOCK ERASE. In all other cases, it can be switched to high impedance, V_{CC} or V_{SS}.

6