Preliminary Data Sheet Supplement

Subject:	LFBGA81 Package Specification
Data Sheet Concerned:	MAS 35x9F, 6251-505-1PD, Aug. 1, 2001 MAS 3587F, 6251-542-1PD, July 9, 2001
Supplement:	No. 2/ 6251-548-1PDS
Edition:	Sept. 14, 2001

LFBGA81 Package Specification for MAS 35x9F Version B4 and MAS 3587F Version B2:

1. Outline Dimensions

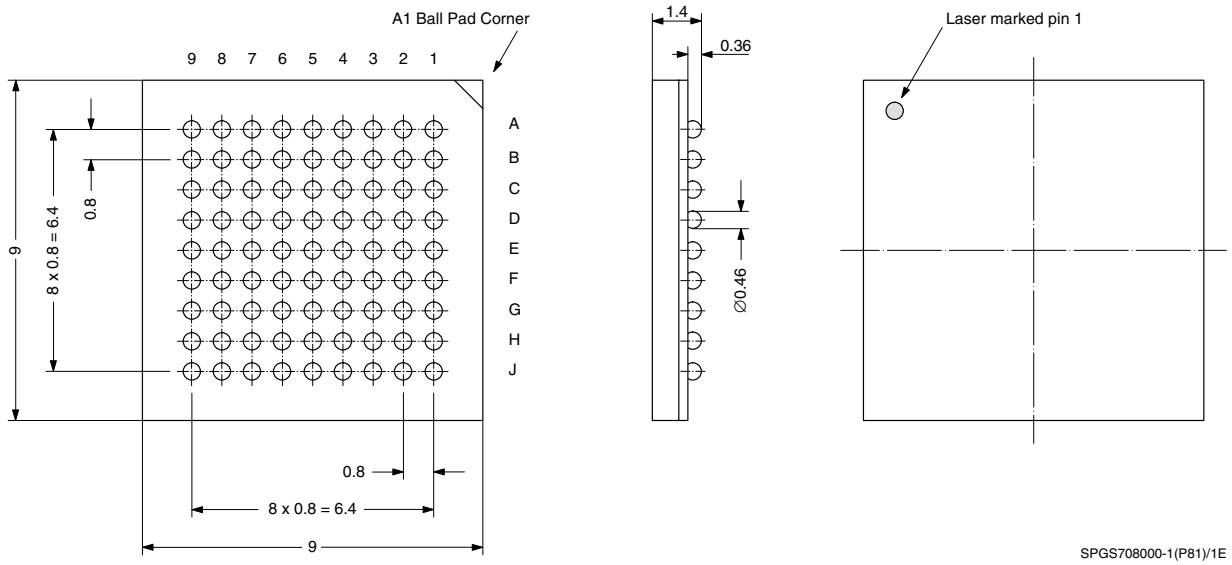

Fig. 1:
81-Ball Low Profile Fine Pitch Ball Grid Array
(LFBGA81)
Weight approximately 0.19 g
Dimensions in mm

2. Pin Connections and Short Descriptions

NC not connected, leave vacant
LV If not used, leave vacant
X obligatory, pin must be connected as described in application information
VDD connect to positive supply
VSS connect to ground

Pin No. PLQFP/ PMQFP 64-pin	Pin No. LFBGA 81-pin	Pin Name	Type	Connection (If not used)	Short Description
1	H2	AGNDC		X	Analog reference voltage
2	J2	MICIN	IN	LV	Input for internal microphone amplifier
3	J3	MICBI	IN	LV	Bias for internal microphone
4	H3	INL	IN	LV	Left A/D input
5	H4	INR	IN	LV	Right A/D input
6	G4	TE	IN	X	Test enable
7	J4	XTI	IN	X	Crystal oscillator (ext. clock) input
8	J5	XTO	OUT	LV	Crystal oscillator output
9	G5	$\overline{\text{POR}}$	IN	X	Power on reset, active low
10	H5	VSS	SUPPLY	X	DSP supply ground
11	J6	XVSS	SUPPLY	X	Digital output supply ground
12	J7	VDD	SUPPLY	X	DSP supply
13	H6	XVDD	SUPPLY	X	Digital output supply
14	H7	I2CVDD	SUPPLY	X	I^2C supply
15	G6	DVS	SUPPLY	X	I^2C device address selector
16	J8	VSENS1	IN/OUT	VDD	Sense input and power output of DC/DC 1 converter
17	J9	DCSO1	SUPPLY	LV	DC/DC 1 switch output
18	H8	DCSG1	SUPPLY	VSS	DC/DC 1 switch ground
19	H9	DCSG2	SUPPLY	VSS	DC/DC 2 switch ground
20	G8	DCSO2	SUPPLY	LV	DC/DC 2 switch output
21	G9	VSENS2	IN/OUT	VDD	Sense input and power output of DC/DC 2 converter
22	F8	DCEN	IN	VSS	DC/DC enable (both converters)
23	F9	CLKO	OUT	LV	Clock output
24	E8	I2CC	IN/OUT	X	I^2C clock

Pin No. PLQFP/ PMQFP 64-pin	Pin No. LFBGA 81-pin	Pin Name	Type	Connection (If not used)	Short Description
25	E9	I2CD	IN/OUT	X	I^2C data
26	E7	SYNC	OUT	LV	Sync output
27	D9	VBAT	IN	LV	Battery voltage monitor input
28	D8	PUP	OUT	LV	DC Converters Power-Up Signal
29	C9	$\overline{EOD}$	OUT	LV	PIO end of DMA, active low
30	C8	$\overline{PRTR}$	OUT	LV	PIO ready to read, active low
31	B9	$\overline{PRTW}$	OUT	LV	PIO ready to write, active low
32	B8	PR	IN	VDD	PIO DMA request, active high
33	A9	$\overline{PCS}$	IN	VSS	PIO chip select, active low
34	A8	PI19	IN/OUT	LV	PIO data bit 7 (MSB)
35	B7	PI18	IN/OUT	LV	PIO data bit 6
36	A7	PI17	IN/OUT	LV	PIO data bit 5
37	B6	PI16	IN/OUT	LV	PIO data bit 4
38	A6	PI15	IN/OUT	LV	PIO data bit 3
39	C6	PI14	IN/OUT	LV	PIO data bit 2
40	A5	PI13	IN/OUT	LV	PIO data bit 1
41	B5	PI12	IN/OUT	LV	PIO data bit 0 (LSB)
42	C5	SOD	OUT	LV	Serial output data
43	A4	SOI	OUT	LV	Serial output word identification
44	B4	SOC	OUT	LV	Serial output clock
45	B3	SID	IN	VSS	Serial input data, interface A
46	A3	SII	IN	VSS	Serial input word identification, interface A
47	C4	SIC	IN	VSS	Serial input clock, interface A
48	E3	SPDO	OUT	LV	S/PDIF output interface
49	A1	SIBD	IN	VSS	Serial input data, interface B
50	A2	SIBC	IN	VSS	Serial input clock, interface B
51	B2	SIBI	IN	VSS	Serial input word identification, interface B
52	B1	SPDI2	IN	LV	Active differential S/PDIF input 2
53	C2	SPDI1	IN	LV	Active differential S/PDIF input 1

Pin No. PLQFP/ PMQFP 64-pin	Pin No. LFBGA 81-pin	Pin Name	Type	Connection (If not used)	Short Description
54	D2	SPDIR	IN	LV	Reference differential S/PDIF input 1 and 2
55	C1	FILTL	IN	X	Feedback input for left amplifier
56	E2	AVDD0	SUPPLY	X	Analog supply for output amplifiers
57	D1	OUTL	OUT	LV	Left analog output
58	E1	OUTR	OUT	LV	Right analog output
59	F2	AVSS0	SUPPLY	X	Analog ground for output amplifiers
60	F1	FILTR	IN	X	Feedback for right output amplifier
61	G2	AVSS1	SUPPLY	X	Analog ground
62	G1	VREF		X	Analog reference ground
63	H1	PVDD	SUPPLY	X	Internal power supply
64	J1	AVDD1	SUPPLY	X	Analog Supply
65		SUB		VSS	Substrate connection

In the 81-pin LFBGA housing, the pins C3, C7, D3, D4, D5, D6, D7, E4, E5, E6, F3, F4, F5, F6, F7, G3 and G7 are common substrate contacts.

3. Pin Configuration

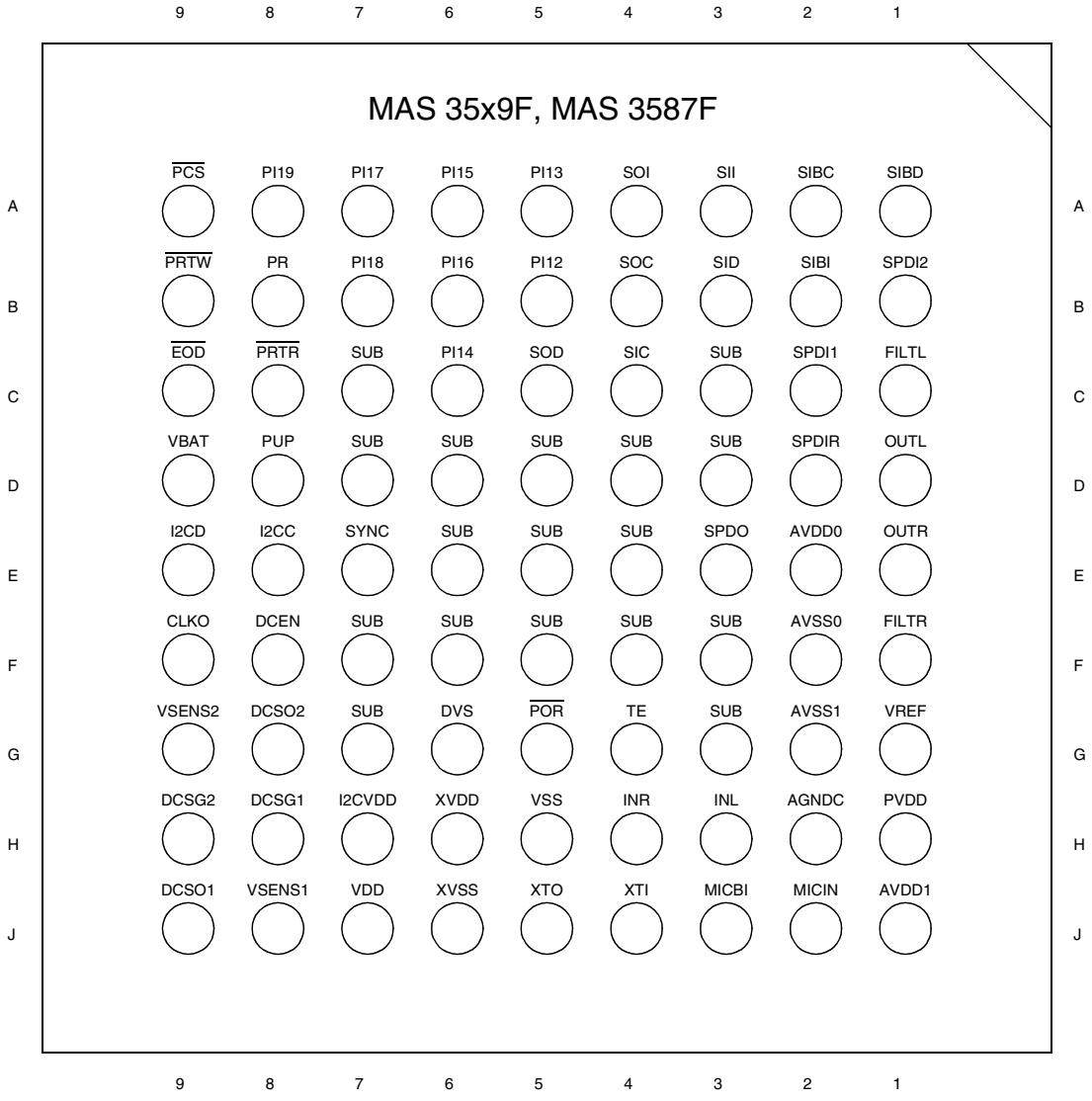

Fig. 1–1: LFBGA81 package

4. Electrical Characteristics

4.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient operating temperature – operating conditions – extended temperature range[1)]		 0 –40	 65 65	 °C °C
T_S	Storage temperature		–40	125	°C
P_{TOT}	Power dissipation	VDD, XVDD, AVDD0/1, I2CVDD		650	mW

[1)] The functionality of the device in the "extended temperature range" was checked by electrical characterization on sample base. Data sheet parameters are valid for "operating conditions" only.

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.