Preliminary Data Sheet Supplement

Subject:	Version Change from A2 to B4
Data Sheet Concerned:	MAS 35x9F 6251-505-1PD, Edition Aug. 1, 2001
Supplement:	No. 3/ 6251-505-1PDS
Edition:	Sept. 13, 2001

Changes from the MAS 35x9F Version A2 to the MAS 35x9F Version B4:

Note: All section or table numbers refer to the Preliminary Data Sheet, Edition: Aug. 1, 2001; 6251-505-1PD

1. The MAS 35x9F-B4 is not hardware or software compatible to the MAS 35x9F-A2.

2. Hardware changes:
   – optional OSC-clock pre-divider, 28 MHz external clock possible (see Table 3–3 on page 20)

3. Firmware changes:
   – IC identification (see Table 3–5 on page 23 and section 3.3.2.12. on page 27)
   – Fast program download now functions correctly (see section 3.3.2.10. on page 26).
   – SD-card: key handling (is not described in data sheet; for more information, please contact Micronas application support)

4. User interface changes:

Table 3–3: Direct configuration registers

I^2C Sub-address (hex)	Function		Name
6A	bit[7]	Enable crystal input clock divider of 1.5 (extended range up to 28 MHz)	CONTROL
	bit[6:0]	Reserved, must be set to zero	
76	bit[8]	Reserved, must be set to zero	DCCF
	bit[0]	Reserved, must be set to zero	
	Note, that the reference voltage for DC/DC converter 1 is derived from the main reference source supplied via pin AVDD1. Therefore, if the DC/DC converter is used, its output must be connected to the analog supply.		
	The DC/DC converters are up-converters only. Thus, if the battery voltage is higher than the selected nominal voltage, the output voltage will exceed the nominal voltage.		

Table 3–9: DSP register – D0 control memory cells

Address	Function change	Name
D0:347	**Interface Status Control** (reset = 05_{hex}) **MPEG** bit[0] Enable/Disable SDI[1)] 0 enable 1 (reset) disable	InterfaceControl
D0:350	**Soft Mute** **MPEG** Address changed from AA_{hex} (DSP register) to 350_{hex} (D0 control memory cell)	SoftMute
D0:351	**S/PDIF channel status bits category code setting** (reset = 8200_{hex}) **All** New D0 control memory cell: S/PDIF channel status bits category code setting (reset = 8200_{hex})	SpdOutBits
D0:34F	**Interface Status Control** (reset = 25_{hex}) **G.729** This control cell is used to enable/disable interfaces in G.729 mode. bit[6],[4] Reserved, must be set to zero bit[5] Reserved, must be set to zero bit[3] Enable/Disable serial data output SDO 0 (reset) SDO valid data 1 SDO invalid data bit[2] Output clock characteristics (SDO and S/PDIF outputs) 0 low impedance 1 (reset) high impedance bit[1] Reserved, must be set to zero bit[0] Enable/Disable SDI[1)] 0 enable 1 (reset) disable	G729_InterfaceControl
D0:FCF	**AAC bitrate in bit/s**	AACbitrate
[1)] **Note:** The pins SIC, SII, SID are switched to output mode if bit[0] = 1 (reset value)		

5. Electrical Characteristics

4.6.2. Recommended Operating Conditions

Table 4-5: Analog input and output recommendations

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
DC/DC-Converter External Circuitry (please refer to application example)						
C_1	VSENS blocking (<100 mΩ ESR)	VSENS1/2		330		µF
V_{TH}	Schottky diode threshold voltage	DCSO1/2 VSENS1/2	0.39			V
L	Ferrite core coil inductance	DCSO1/2		22		µH

4.6.3.1. I²C Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
t_W	Wait time	I2CC, I2CD	0	0.5	4	ms

4.6.3.2. Serial I²S Input Interface Characteristics

at T = T_A, V_{SUPD}, V_{SUPA} = 2.5 ... 3.6 V, $f_{CRYSTAL}$ = 18.432 MHz, Typ. values for T_A = 25 °C in P(L/M)QFP package

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
t_{SICLK}	I²S clock input clock period	SI(B)C		325		ns	f_S = 48 kHz Stereo, 32 bits per sample (for demand mode, see Table 4–6)

Table 4–6: Maximum allowed sample clock frequency in Demand Mode

f_{Sample} (kHz)	f_C (MHz)	min. t_{SICLK} (ns)
48, 32	6.144	162
44.1	5.6448	177
24, 16	3.072	325
22.05	2.8224	354
12, 8	1.536	651
11.025	1.4112	708

Table 4–7: Allowed transmission delays of external data source MPEG1/2 Layer 2/3

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
$t_{START48-320}$	Allowed delay time before start of serial data transmission after assertion of signal at $\overline{EOD}$	$\overline{EOD}$			3.1	ms	48 kHz/s, 320 kbit/s
$t_{START48-64}$					5.7	ms	48 kHz/s, 64 kbit/s
$t_{START24-320}$					4.2	ms	24 kHz/s, 320 kbit/s
$t_{START24-32}$					9.2	ms	24 kHz/s, 32 kbit/s
$t_{START12-64}$					23.1	ms	12 kHz/s, 64 kbit/s
$t_{START12-16}$					25.6	ms	12 kHz/s, 16 kbit/s
$t_{START8-64}$					34.8	ms	8 kHz/s, 64 kbit/s
$t_{START8-8}$					38.4	ms	8 kHz/s, 8 kbit/s
t_{STOP}	Allowed delay time before stop of serial data transmission after deassertion of signal at $\overline{EOD}$	$\overline{EOD}$			1.3	ms	Clock rate of input data 1 Mbit/s

4.6.4. Analog Characteristics

at T = T_A, V_{SUPDn}, V_{SUPx} = 2.5 ... 3.6 V, V_{SUPA} = 2.2 ... 3.6 V, $f_{CRYSTAL}$ = 13...20 MHz, typical values at T_A = 25 °C and $f_{CRYSTAL}$ = 18.432 MHz in P(L/M)QFP package

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Analog Audio Input							
R_{inAI}	Analog line input resistance	INL/R		97		kΩ	at minimum analog input gain, i.e. –3 dB
SNR_{AI}	Signal-to-noise ratio of line input	INL/R		74		dB(A)	BW = 20 Hz...20 kHz, analog gain = 0 dB, input 1 kHz at V_{AI}–20 dB
SNR_{MI}	Signal-to-noise ratio of microphone input	MICIN		73		dB(A)	BW = 20 Hz...20 kHz, analog gain = +21 dB, input 1 kHz at V_{MI}–20 dB
$PSRR_{AI}$	Power supply rejection ratio for analog audio inputs	AVDD0/1, INL/R MICIN		45		dB	1 kHz sine at 100 mV_{rms}
Audio Output							
SNR_{AO}	Signal-to-noise ratio of analog output	OUTL/R		94		dB(A)	R_L≥16 Ω BW = 20 Hz...20 kHz, analog gain = 0 dB input = –20 dBFS
Lev_{MuteAO}	Mute level	OUTL/R		–113		dBV	A-weighted BW = 20 Hz...22 kHz, no digital input signal, analog gain = mute
$PSRR_{AO}$	Power supply rejection ratio for analog audio outputs	AVDD0/1 OUTL/R		70		dB	1 kHz sine at 100 mV_{rms}
				35		dB	≤100 kHz sine at 100 mV_{rms}

4.6.5. DC/DC Converter Characteristics

at T = T_A, V_{in} = 1.2 V, V_{outn} = 3.0 V, f_{clk} = 18.432 MHz, f_{sw} = 384 kHz, PWM-mode, L = 22 µH, in P(L/M)QFP package (unless otherwise noted) Typ. values for T_A = 25 °C

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IN}	Minimum operating input voltage						[1]
	DC1 DC2			1.1 1.2		V	I_{LOAD} = 200 mA, DCCF = 5050_{hex} (reset)
V_{OTOL}	Output voltage tolerance	VSENSn	–4		4	%	I_{LOAD} = 20 mA T_A = 25 °C[2]
$dV_{OUT}/dV_{IN}/V_{OUT}$	Line regulation	VSENSn		0.7		%/V	I_{LOAD} = 20 mA

[1] Since the regulators are bootstrapped, once started they will operate down to 0.7 V input voltage
[2] PFM-mode regulates approx. 1% higher