Subject:	Additional Information for MAS 35x9F
Data Sheet Concerned:	MAS 35x9F 6251-505-2AI, Edition October 31, 2000
Supplement:	No. 2/ 6251-505-1AIS
Edition:	Aug. 7, 2001

Additional Information for MAS 35x9F:

3.3.3.2. Application Specific Control

Table 3-7: D0 control memory cells

Memory Address (hex)	Function	Name
D0:347	**Interface Status Control** (reset = 05_{hex}) **MPEG** This control cell allows to enable/disable the data I/O interfaces. In addition, the clock of the output data interface interfaces, S/PDIF and SDO, can be set to a low-impedance mode. bit[6] S/PDIF input selection (used for download modules) 0 (reset) select S/PDIF input 1 1 select S/PDIF input 2 bit[5] Enable/disable S/PDIF output 0 (reset) enable S/PDIF output 1 S/PDIF output (invalid) bit[4] Reserved, must be set to zero bit[3] Enable/disable serial data output SDO 0 (reset) SDO valid data 1 SDO invalid data bit[2] Output clock characteristic (SDO and S/PDIF outputs) 0 low impedance 1 (reset) high impedance bit[1] reserved, must be set to zero bit[0] Enable/disable SDI[1)] 0 enable 1 (reset) disable Both digital outputs, S/PDIF and I^2S, and the D/A converters may use the decoded audio independent of each other. Changes at this memory address must be validated by setting bit[0] of $D0:346_{hex}$.	InterfaceControl
[1)] **Note:** The pins SIC, SII, SID are switched to output mode if bit[0] = 1 (reset value).		

Table 3-7: D0 control memory cells, continued

Memory Address (hex)	Function	Name
D0:34f	**Interface Status Control** (reset = 25_{hex}) **G.729** This control cell is used to enable/disable interfaces in G.729 mode. bit[6],[4] reserved, must be set to zero bit [5] reserved, must be set to one bit[3] Enable/disable serial data output SDO 0 (reset) SDO valid data 1 SDO invalid data bit[2] Output clock characteristic (SDO and S/PDIF outputs) 0 low impedance 1 (reset) high impedance bit[1] reserved, must be set to zero bit[0] Enable/disable SDI[1)] 0 enable 1 (reset) disable	g729_InterfaceControl
[1)] **Note:** The pins SIC, SII, SID are switched to output mode if bit[0] = 1 (reset value).		

4.2. Pin Connections and Short Descriptions

NC not connected, leave vacant
LV If not used, leave vacant
X obligatory, pin must be connected as described in application information (see Fig. 4-33 on page 6)
VDD connect to positive supply
VSS connect to ground

Pin No. PLQFP/ PMQFP 64-pin	Pin Name	Type	Connection (If not used)	Short Description
1	AGNDC		X	Analog reference voltage
2	MICIN	IN	LV	Input for internal microphone amplifier
3	MICBI	IN	LV	Bias for internal microphone
4	INL	IN	LV	Left A/D input
5	INR	IN	LV	Right A/D input
6	TE	IN	X	Test enable
7	XTI	IN	X	Crystal oscillator (ext. clock) input
8	XTO	OUT	LV	Crystal oscillator output
9	$\overline{\text{POR}}$	IN	X	Power on reset, active low
10	VSS	SUPPLY	X	DSP supply ground
11	XVSS	SUPPLY	X	Digital output supply ground
12	VDD	SUPPLY	X	DSP supply
13	XVDD	SUPPLY	X	Digital output supply
14	I2CVDD	SUPPLY	X	I^2C supply
15	DVS	IN	X	I^2C device address selector
16	VSENS1	IN/OUT	VDD	Sense input and power output of DC/DC 1 converter
17	DCSO1	SUPPLY	LV	DC/DC 1 switch output
18	DCSG1	SUPPLY	VSS	DC/DC 1 switch ground
19	DCSG2	SUPPLY	VSS	DC/DC 2 switch ground
20	DCSO2	SUPPLY	LV	DC/DC 2 switch output
21	VSENS2	IN/OUT	VDD	Sense input and power output of DC/DC 2 converter
22	DCEN	IN	VSS	DC/DC enable (both converters)
23	CLKO	OUT	LV	Clock output

Pin No. PLQFP/ PMQFP 64-pin	Pin Name	Type	Connection (If not used)	Short Description
24	I2CC	IN/OUT	X	I^2C clock
25	I2CD	IN/OUT	X	I^2C data
26	SYNC	OUT	LV	Sync output
27	VBAT	IN	LV	Battery voltage monitor input
28	PUP	OUT	LV	DC Converters Power-Up Signal
29	$\overline{EOD}$	OUT	LV	PIO end of DMA, active low
30	$\overline{PRTR}$	OUT	LV	PIO ready to read, active low
31	$\overline{PRTW}$	OUT	LV	PIO ready to write, active low
32	PR	IN	VDD	PIO DMA request, active high
33	$\overline{PCS}$	IN	VSS	PIO chip select, active low
34	PI19	IN/OUT	LV	PIO data bit[7] (MSB)
35	PI18	IN/OUT	LV	PIO data bit[6]
36	PI17	IN/OUT	LV	PIO data bit[5]
37	PI16	IN/OUT	LV	PIO data bit[4]
38	PI15	IN/OUT	LV	PIO data bit[3]
39	PI14	IN/OUT	LV	PIO data bit[2]
40	PI13	IN/OUT	LV	PIO data bit[1]
41	PI12	IN/OUT	LV	PIO data bit[0] (LSB)
42	SOD	OUT	LV	Serial output data
43	SOI	OUT	LV	Serial output word identification
44	SOC	OUT	LV	Serial output clock
45	SID	IN/OUT	X	Serial input data, interface A
46	SII	IN/OUT	X	Serial input word identification, interface A
47	SIC	IN/OUT	X	Serial input clock, interface A
48	SPDO	OUT	LV	S/PDIF output interface
49	SIBD	IN	VSS	Serial input data, interface B
50	SIBC	IN	VSS	Serial input clock, interface B
51	SIBI	IN	VSS	Serial input word identification, interface B
52	SPDI2	IN	LV	Active differential S/PDIF input 2
53	SPDI1	IN	LV	Active differential S/PDIF input 1
54	SPDIR	IN	LV	Reference differential S/PDIF input 1 and 2

Pin No. PLQFP/ PMQFP 64-pin	Pin Name	Type	Connection (If not used)	Short Description
55	FILTL	IN	X	Feedback input for left amplifier
56	AVDD0	SUPPLY	X	Analog supply for output amplifiers
57	OUTL	OUT	LV	Left analog output
58	OUTR	OUT	LV	Right analog output
59	AVSS0	SUPPLY	X	Analog ground for output amplifiers
60	FILTR	IN	X	Feedback for right output amplifier
61	AVSS1	SUPPLY	X	Analog ground
62	VREF		X	Analog reference ground
63	PVDD	SUPPLY	X	Internal power supply
64	AVDD1	SUPPLY	X	Analog Supply

4.3. Pin Descriptions

4.3.3. DC/DC Converters and Battery Voltage Supervision

VSENS1/VSENS2 **IN**
Sense input and power output of DC/DC converters. If the respective DC/DC converter is not used, this pin should be connected to a supply to enable proper function of the PUP-signals.

4.3.7. Serial Input Interface (SDI)

SID **DATA** **IN/OUT**
SII **WORD STROBE** **IN/OUT**
SIC **CLOCK** **IN/OUT**
I^2S compatible serial interface A for digital audio data. In the standard firmware this interface is not used.
Note: Please refer to Interface Status Register (D0:7f2) Bit [0] (Table 3–9).

4.5. Internal Pin Circuits

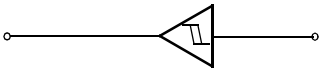

Fig. 4-9: Input pins SIBC, SIBI, SIBD

4.3.12. Analog Input Interfaces

In the standard MPEG-decoding DSP firmware the analog inputs are not used. However, they can be selected as a source for the D/A converters
(set MIX ADC scale of the D/A Converter Source Mixer, Register 00 06_{hex} in Table 3–15).

4.3.14. Miscellaneous

$\overline{\text{POR}}$ **IN**
The Power-On Reset pin completely resets the MAS 35x9F. The $\overline{\text{POR}}$ is an active-low signal (see Fig. 4-33 on page 82).

4.7. Typical Application in a Portable Player

– MMC/SDI-Card or SMC/CF2+ used as storage media
– Dashed lines show optional (external) devices

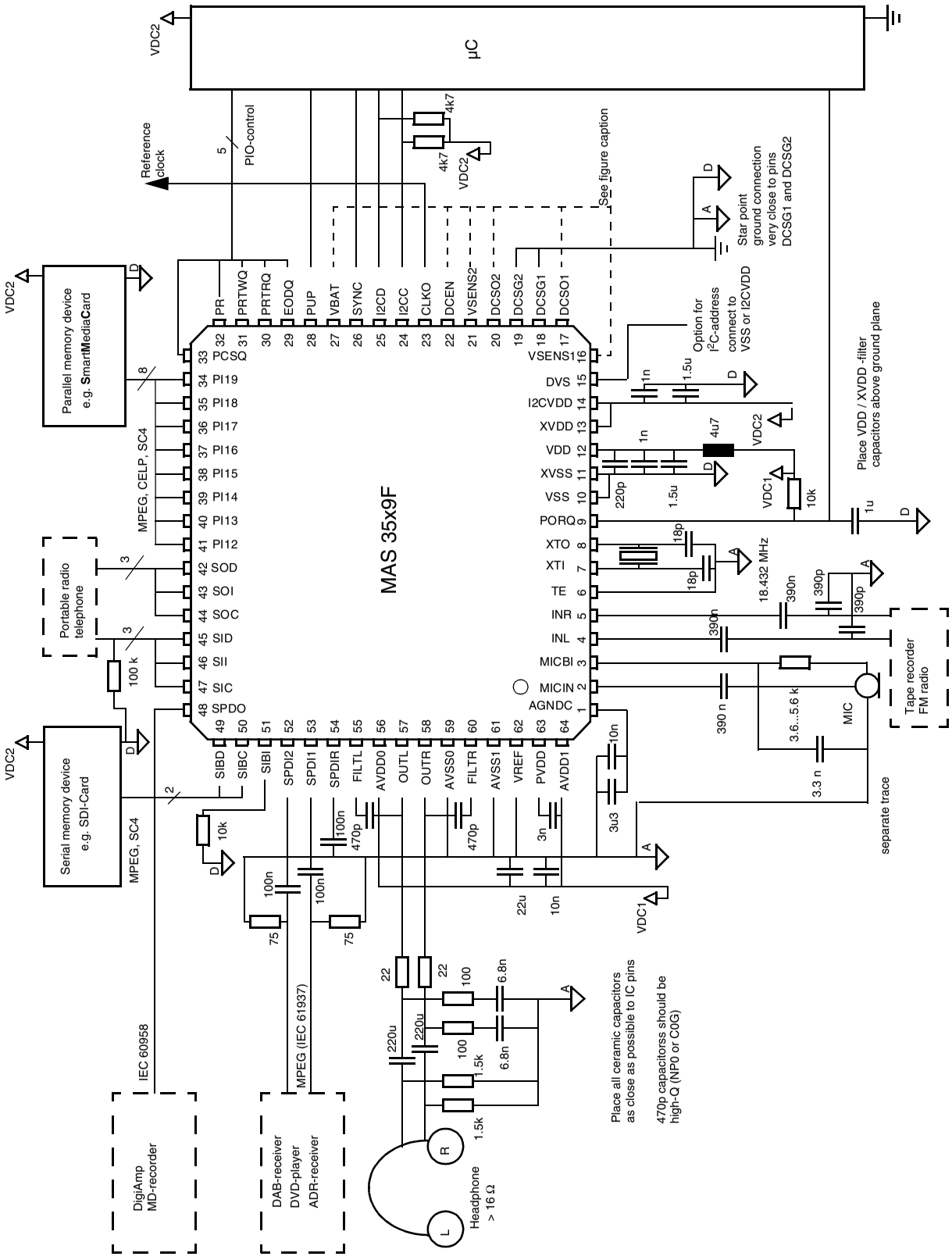

Fig. 4-33: Application circuit of the MAS 35x9F. For connections of the DC/DC converters, please refer to Fig. 4–34