Advance Information Supplement

Subject:	Description of the S/PDIF Input-Problem
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Description of the S/PDIF input interface malfunction on the MAS 3587F Version B2:

The S/PDIF input interface synchronizes itself onto the bit clock of the incoming S/PDIF signal. This synchronization is performed by an internal control circuit that locks after synchronization.

The malfunction in the S/PDIF input interface leads occasionally during synchronization to a bit shift of the received data that are passed to the internal processing.

This bit shift leads to a signal amplitude error prior to decoding that may cause bad level adjustment or even clipping prior to the encoding process. If the bit shift error occurs once, it affects all subsequent samples.

However, the bit shift can be recognized by an inherent parity checking, which is used for the following workaround:

Workaround:

– Detect the parity error by checking bit [12] of the S/PDIF status register 0x52 after synchronization and periodically (e.g. after every frame) during the encoding process.

– Bit [12] = 1 means: parity error.

– If the parity error occurs (even a single error will be remembered by the interface), restart the recording process.

– Periodic checking of the parity error is necessary if the S/PDIF signal might be distorted during the encoding process (e.g. by disconnecting the cable or cable defects)

This workaround is only reliable for stable, error-free S/PDIF transmission that are firm in normal consumer environments with cable lengths below 3 m. If due to a cable defect etc. an error prone transmission occurs, the recording result will be extremely distorted in any case.