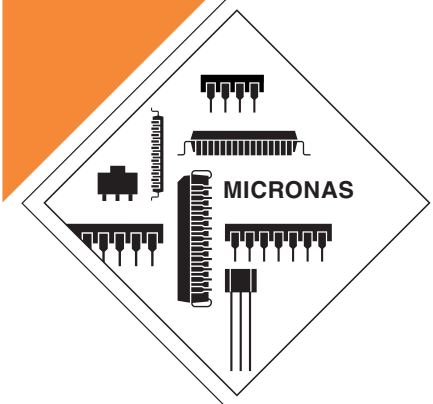

PRELIMINARY DATA SHEET

MAS 3528E
Dolby Digital and MPEG-1 Layer-2 Audio Decoder

DOLBY DIGITAL

Edition Dec. 10, 2001
6251-509-1PD

MICRONAS

Contents

Contents, continued

Contents, continued

References

1. Digital Audio Compression (AC-3), ATSC Standard, Advances Television Systems Committee, James C. McKinney, Chariman, Dr. Robert Hopkins, Executive Director (Dec. 20, 1995)

2. Dolby Licensee Information Manual: Dolby Digital Consumer Decoder, Issue 3, 1999

License Notice

Dolby Digital and MPEG-1 Layer-2 Audio Decoder

This datasheet applies to the MAS 3528E version E7 and following versions.

1. Introduction

The Micronas MAS 3528E is a single-chip Dolby Digital and MPEG-1 Layer-2 decoder. Together with the Surround Sound Processor DPL 4519G, it acts as a complete implementation of a Dolby Digital consumer decoder. In a television environment, these two integrated circuits are complemented by the Micronas Multistandard Sound Processor MSP 44x0G which performs the standard TV sound decoding.

Table 1–1: ICs used for the Dolby Digital System Solution

Type	Description
MSP 44x0G	Multistandard Sound Processor with 48 kHz processing
DPL 4519G	Sound Processor for digital and analog Surround Systems
MAS 3528E	Dolby Digital/MPEG-1 decoder

1.1. Features

- Two multiplexed S/PDIF, IEC-958, IEC 61937, AES/EBU, EIA-J CP-340 receivers
- Two freely configurable multiplexed serial inputs
- Decoders for 5.1-channel Dolby Digital (AC-3) and MPEG-1 Layer-2
- Handling of PCM input format
- S/PDIF PCM output or loop-through for all input formats (including DTS)
- Optional surround encoding (Lt, Rt) or straight downmixing to two channels (Lo, Ro)
- Multi-channel I^2S output
  (four stereo data lines or one 8-channel line)
- Dynamic range compression
- Karaoke downmixing
- Delay for center (0…5 ms)
- Delay for surround (two channels, 0…15 ms)
- Bandpass-shaped/white-noise generator
- Bass management according to Dolby specification (output configuration 0, 1, 2, 3, and DVD)
- I^2C-control

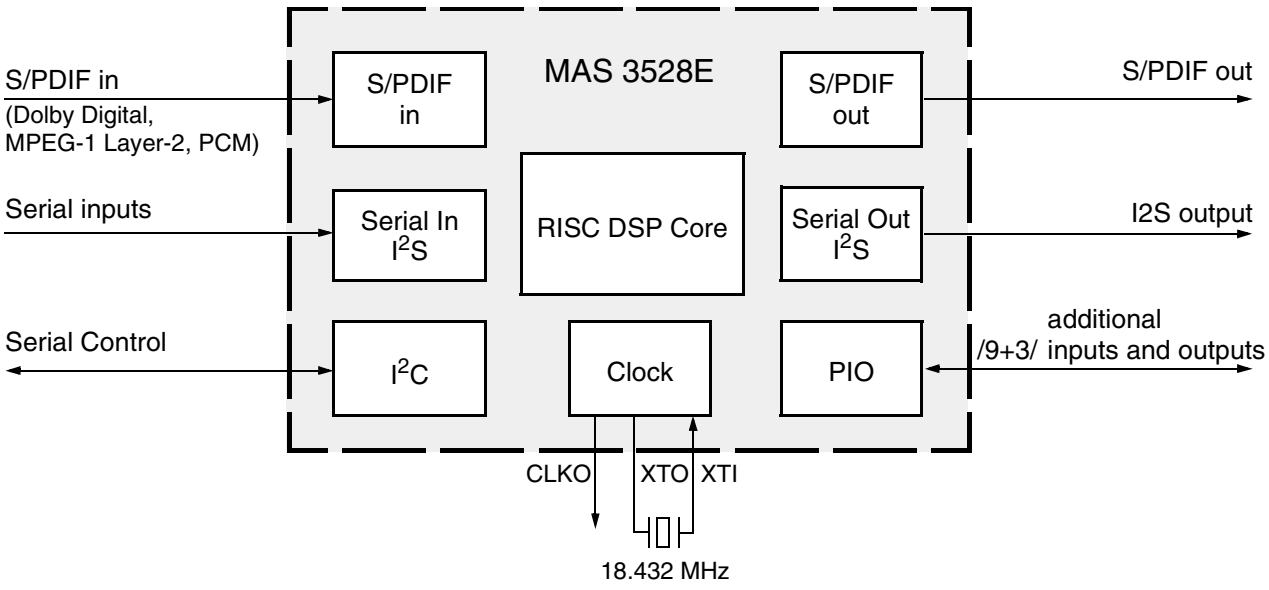

Fig. 1–1: Block diagram MAS 3528E

1.2. System Application

The Micronas Dolby Digital system solution consists of three dedicated integrated circuits:

– The MSP 44x0G is the interface for all TV-sound and analog input signals. It performs the TV-audio demodulation including analog stereo, NICAM, and Wegener Panda decompression. It has four pairs of audio D/A-converters, two of them including sound control facilities, and one additional subwoofer D/A-converter.

– The DPL 4519G adds the Dolby Surround Sound features and has three pairs of audio D/A-converters, two of them including sound control facilities, and one additional subwoofer D/A converter.

– The MAS 3528E performs the Dolby Digital or MPEG decoding and has additional functions that are necessary for the Dolby Digital system.

While the MSP 44x0G is a stand-alone TV-sound solution, the combination with a DPL 4519G results in a high-end TV with Dolby Pro Logic functionality.

With the addition of the MAS 3528E, the TV provides full Dolby Digital/MPEG-1 capabilities.

A combination of the DPL 4519G with the MAS 3528E is a fully functional Dolby Digital integration for multimedia applications with a total of seven high-quality audio D/A-converters.

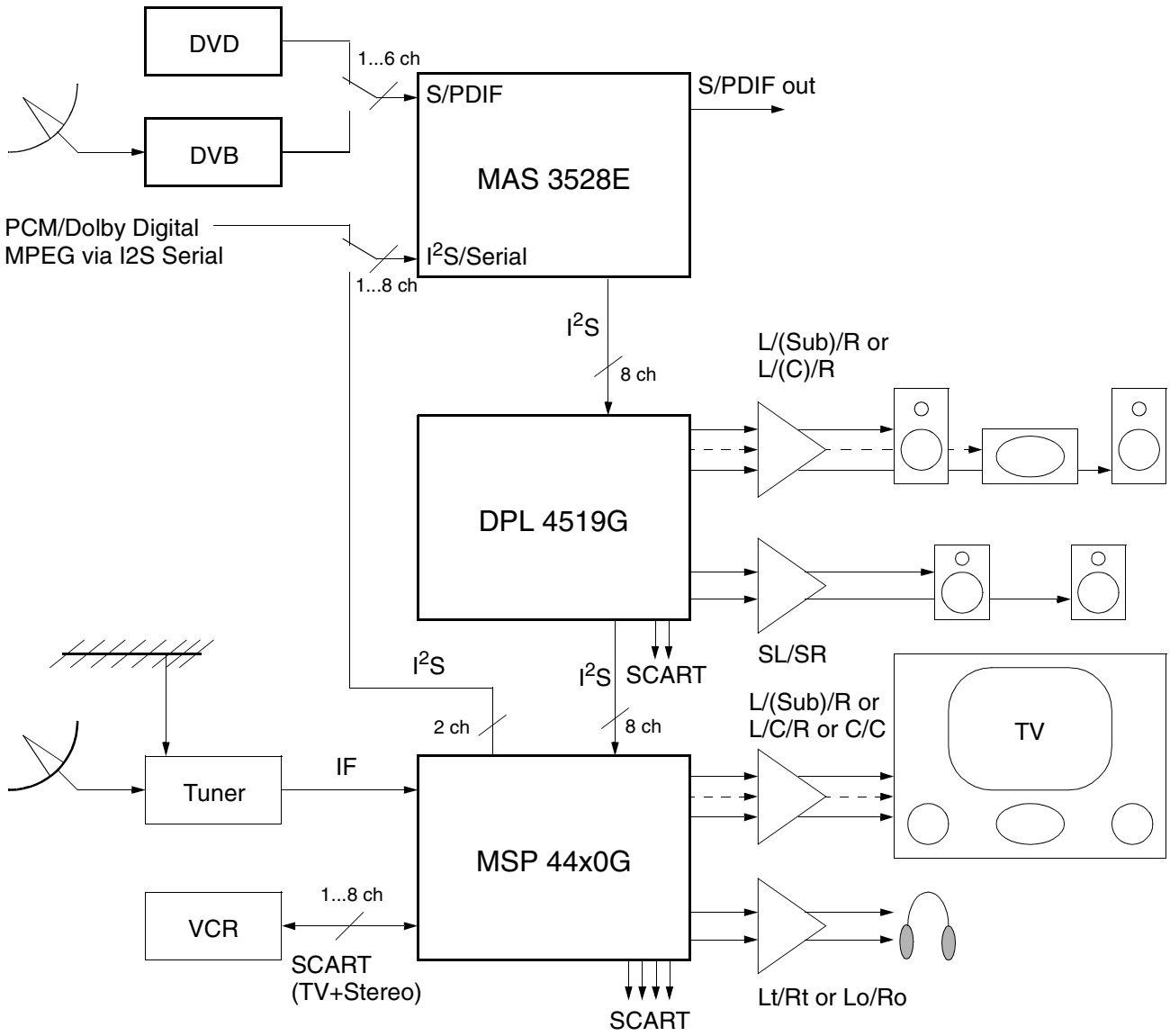

Fig. 1–2: Configuration of the Micronas Dolby Digital TV system solution.

1.3. Application Details

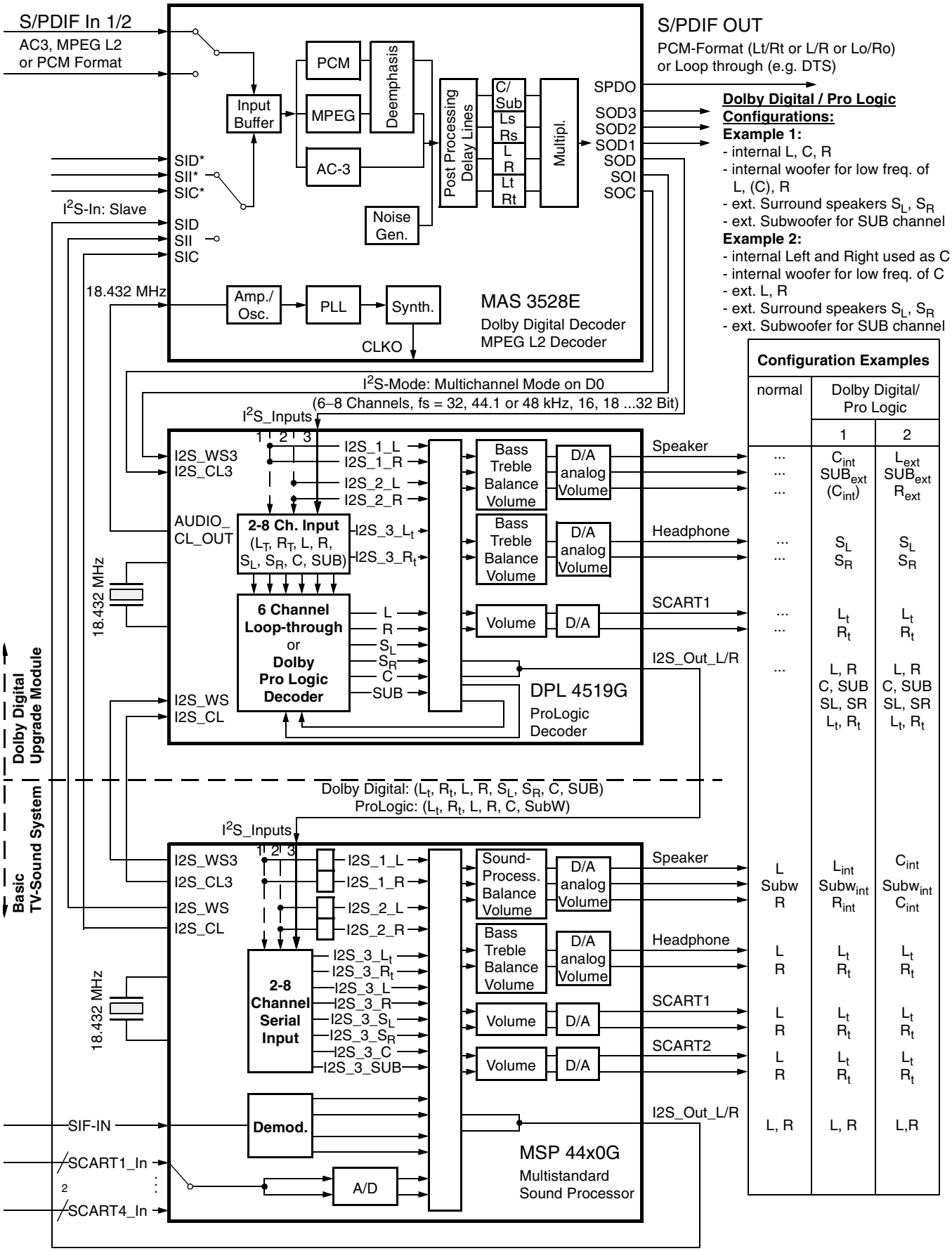

Fig. 1–3: Block diagram of a MAS 3528E in a television environment with all D/A-converters shown.

2. Functional Description

2.1. Overview

The MAS 3528E is intended for use in high-end consumer audio applications. It receives S/PDIF or serial data streams and decodes the Dolby Digital (AC-3), MPEG or PCM-encoded audio formats.

Due to the automatic format detection, no controller interaction is needed for the standard operation. On the other hand, the controller has full access to all vital information contained in the Dolby Digital bit stream. The choice of different output formats, as defined by Dolby, guarantees good adaption to various listening environments.

2.2. Architecture

The hardware of the MAS 3528E consists of a high performance RISC Digital Signal Processor (DSP) and appropriate interfaces. Fig. 2–1 shows a hardware overview of the IC; Fig. 2–2 on page 11 shows the functional aspects.

2.3. DSP Core

The internal processor is a dedicated audio DSP. All data input and output actions are based on a ‘non cycle stealing’ background DMA that does not cause any computational overhead.

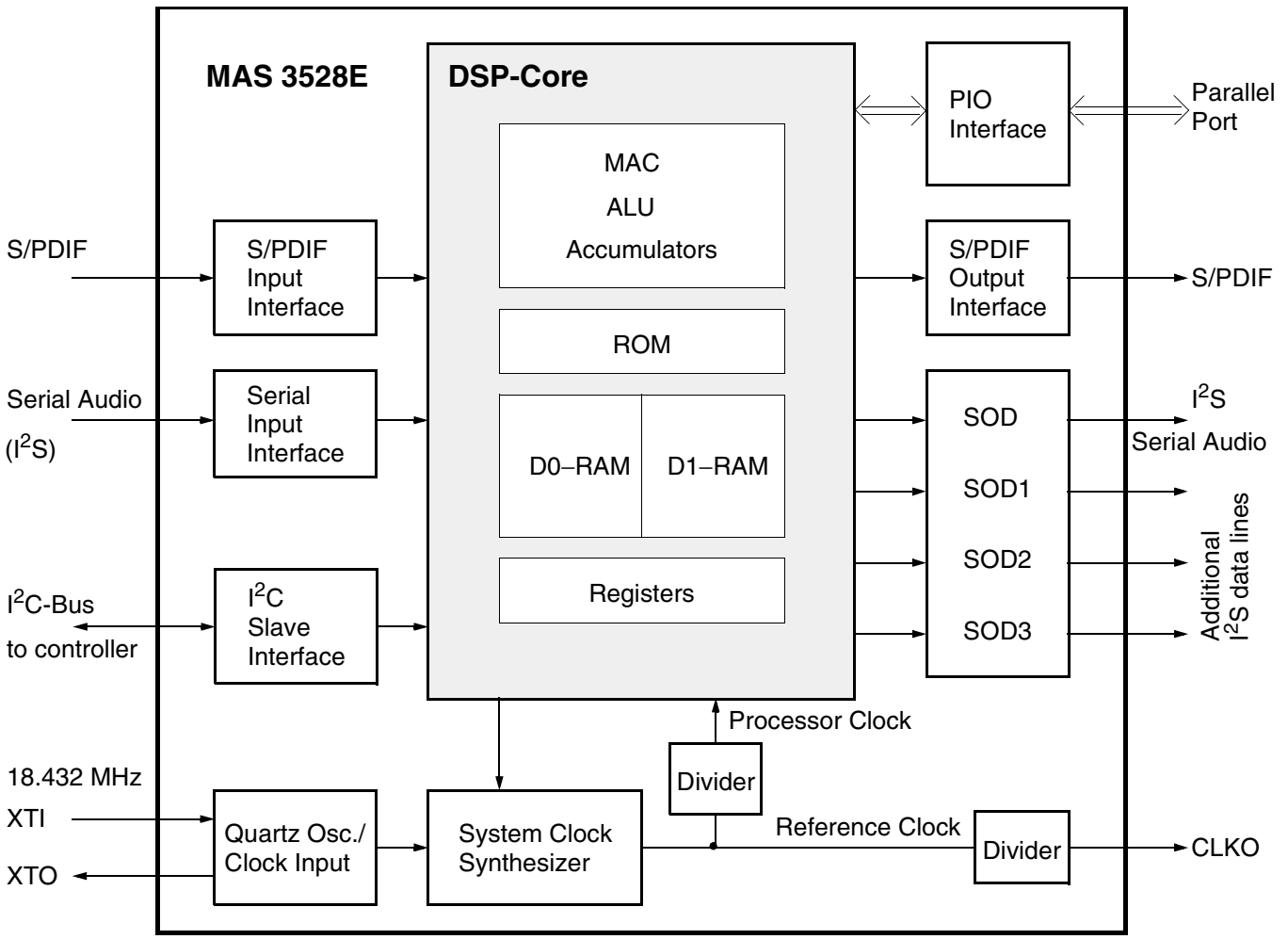

Fig. 2–1: The MAS 3528E architecture

2.4. Internal Program ROM and Firmware

The firmware implemented in the program ROM of the MAS 3528E provides Dolby Digital decoding including the required downmixing, output configurations and delay lines (part of an Implementation of Dolby Digital), MPEG-1 Layer-2 audio data decompression, handling of PCM-encoded audio, and loop-through of DTS-formats received via the S/PDIF-input.

For PCM and MPEG-signals, a deemphasis can be applied to achieve a flat frequency response as required by Dolby Pro Logic decoders.

On power-on, the DSP starts the firmware in an automatic standard detection mode with the S/PDIF-input selected. Therefore, only minimal controlling is necessary. In addition, the I^2C-interface provides a set of I^2C instructions that give access to internal DSP-registers and memory areas.

2.5. RAM and Registers

The DSP-core has access to two RAM-banks denoted D0 and D1. All RAM-addresses can be accessed in a 20-bit or a 16-bit mode via I^2C-bus. For more details, please refer to Section 3.4.on page 18.

For fast access of internal DSP-states, the processor core has an address space of 256 data registers (see Section 3.5. on page 22) which can be accessed via I^2C-bus.

2.6. Clock Management

The MAS 3528E is driven by a single clock at a frequency of 18.432 MHz. The clock may either be provided from an external source to pin XTI or generated with a crystal. At pin XTO, the clock signal is available for other applications.

The internal reference clock and processor clock are derived from the 18.432 MHz and synchronized to the audio sample frequency of the decompressed bit stream by a PLL. In case of Dolby Digital decoding, the clock frequency may be selected between a high and a low value by bit[16] in configuration memory cell UIC_Out_Clk_Scale (D0:13DF) – (see Table 3–7 on page 31). It is highly recommended to use the high system clock. The resulting processor clocks are given in Table 2–1.

At pin CLKO, a clock output can be provided e.g. for additional D/A-converters. The output frequency at CLKO is the reference clock divided by a factor as selected by bits[18:17] in D0:13DF. By default, CLKO is disabled.

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Table 2–2: Reference clock frequencies in dependence of bit[16] of UIC_Out_Clk_Scale (D0:13DF).

Format	f_s/kHz	Reference Clock/MHz	
		bit[16] = 0	bit[16] = 1
Dolby Digital	48	61.44	73.728
	44.1	56.448	67.7376
	32	40.96	49.152
MPEG, PCM	48	73.728	
	44.1	67.7376	
	32	49.152	

Table 2–1: Processor clock frequencies in dependence of bit[16] of UIC_Out_Clk_Scale (D0:13DF).

Format	f_s/kHz	Processor Clock/MHz	
		bit[16] = 0	bit[16] = 1
Dolby Digital	48	61.44	73.728
	44.1	56.448	67.7376
	32	40.96	49.152
MPEG, PCM	48	36.864	
	44.1	33.8688	
	32	24.576	

2.7. Interfaces

2.7.1. I²C Control Interface

For controlling, a standard I²C-interface is implemented. A detailed description of all functions can be found in Section 3. on page 17.

2.7.2. S/PDIF-Input Interfaces

Two multiplexed S/PDIF-input interfaces are installed which are capable of PCM, Dolby Digital, MPEG, or (without decoding) DTS auto-detection. In addition to the signal input pins SPDI/SPDI2, a reference pin SPREF is provided to support balanced signal sources or twisted pair transmission lines. The following features are supported:

– Fast synchronization on input signal (<50 ms)

– Burst-Mode support for Dolby Digital and MPEG-bitstreams

– Locking on 32, 44.1, 48 kHz sample frequencies

– Incoming first 20 channel status bits are mirrored in Register 56_{hex} (see Table 3–5 on page 22)

2.7.3. S/PDIF-Output

At pin SPDIFOUT, the baseband audio is provided as an S/PDIF-signal.

Channel status bits in S/PDIF output (especially copyright, category code, and generation status) can be configured in D0:13EA (see Table 3–7 on page 31).

Alternatively, this output can mirror the unprocessed signal of the S/PDIF-input (Output_Conf: Register $2E_{hex}$). This loop-through is necessary for DTS (Digital Theater System) signals where no internal decoding action is performed.

2.7.4. Serial Input Interface

If the serial input interface carries Dolby Digital, MPEG Layer-2, or PCM, the MAS 3528E processes the data. The interface consists of the three pins: SIC, SII, and SID. For MPEG and Dolby Digital decoding operation, the SII pin must always be connected to V_{SS}, while for PCM-data, the interface acts as an I²S-type and SII is used as a word strobe. An example of an input signal format is shown in Fig. 4–16 on page 52. The data values are latched with the falling edge of the SIC signal. It is possible to use a word length of 16 or 32 bits. For controlling details, please refer to memory address D0:13D0 (I/O Control) and D0:13DF (Auxiliary Interface Control) in Table 3–7 on page 31.

If the MPEG or Dolby Digital signal was formatted (e.g. to 8-bit or 16-bit words) by the storing or transportation medium (PC, memory), the serial data must be sent “MSB first” as produced by the encoder.

2.7.4.1. Multiline Serial Output

The serial audio output interface of the MAS 3528E is a standard I²S-like interface consisting of four data lines SODx, the word strobe SOI, and the clock signal SOC. The output bitstream can either carry eight channels on one line (SOD) or two channels on each of four lines (SOD, SOD1, SOD2, SOD3). Furthermore, it is possible to choose between different interface configurations (with word strobe time offset and/or with inverted SOI-signal). The serial output generates 32 bits per audio sample, but only the first 20 bits will carry valid audio data. The 12 trailing bits are set to zero by default (see Fig. 4–18 on page 53).

The configuration of the output interface is done in D0:13D0 and D0:13DF (see Table 3–7 on page 31).

2.7.5. Frame Synchronization

For microprocessor interrupts, a frame synchronization output pin (SYNC) is provided.

After decoding a valid header, the SYNC pin level changes to High. Most of the status information (UIS cells in Table 3–6 on page 23) is updated now. To generate an edge for the controller, the level changes to Low during processing the next header. After having completed this, the SYNC pin level changes to High again. If the level is Low for more than 1 ms, no decoding is performed. Memory cell UIH_LAST_MESSAGE (D0:13FF) provides background information thereof.

Notes for Dolby Digital:

After first CRC is done, the SYNC pin level changes to High, all information for a frame is valid, and decoding is performed. The SYNC pin level changes to Low before new status information is written. Please take into account that UIS_DYNRNG (D0:13B4), UIS_DYNRNG2 (D0:13B5), and UIS_KARAOKEFLAG (D0:13B6) are valid for the audio block only; the SYNC pin does not signalize their validity.

Notes for MPEG:

After processing CRC, the SYNC pin level changes to High, all information for a frame is valid, and decoding is performed. The SYNC pin level changes to Low before evaluating new header information.

2.8. Power-Supply Regions

The MAS 3528E has three power supply regions. The VDD/VSS-pin pair supplies all digital parts including the DSP-core.The XVDD/XVSS-pin pair is connected to the signal pin output buffers.The AVDD/AVSS-supply is for the clock oscillator, PLL-circuits, and system clock synthesizer.

2.9. Functional Blocks and Operation

A block diagram of the MAS 3528E functionality is shown in Fig. 2–2.

2.9.1. Power-Up Sequence and Default Operation

After applying the appropriate voltages to the three supply pins and releasing the reset signal, the circuit starts normal operation with the S/PDIF as the expected input and automatic standard recognition (Dolby Digital, MPEG, PCM). No further action is necessary for default operation or DTS loop-through.

A power-on reset can be issued at any time via pin $\overline{\text{POR}}$.

When the input format is changed (e.g. from Dolby Digital to MPEG), the synchronization is lost and the audio output is muted. The automatic standard recognition then checks the new input format and, after successful recognition, resumes normal operation.

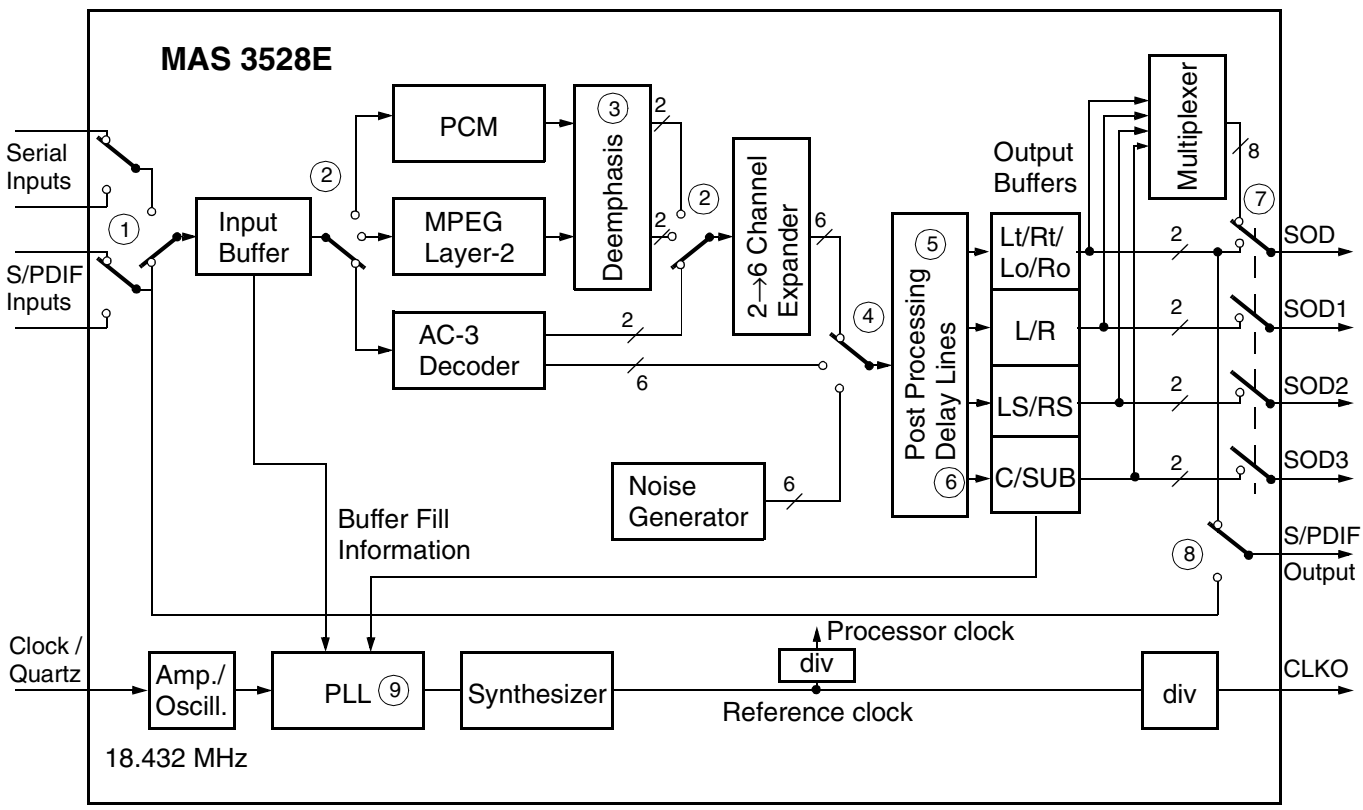

Fig. 2–2: Functionality of the MAS 3528E

2.9.2. Input Switching

Both input interfaces, the S/PDIF (default ① in Fig. 2–2) or the serial input interface, may carry any of the three data formats: Dolby Digital (AC-3), MPEG Layer-2, or PCM. The filling status of the input buffer represents the data rate and therefore controls the system clock. The input interface can be selected in the UIC_IO control D0:13D0.

The DTS-format can only be received via the S/PDIF-interface for loop-through.

2.9.3. Standard Selection and Decoding

In the default mode, an automatic standard recognition (auto-detection) selects the decoding algorithm according to the data format at the S/PDIF-input. The detected standard is shown in the Global Operating Status (D0:13BB). The standard selection for the I^2S inputs can be selected manually in the I/O control D0:13D0 ②.

2.9.4. Dolby Digital Data Stream

The digital input signal can either be an S/PDIF or an I^2S-source. In the Dolby Digital mode, the IC performs the following tasks:

– Data input with clock synchronization
– S/PDIF-channel selection (one of eight possible)
– Decoding of AC-3 bitstream elements
– Compression control for Dolby Digital signals (D0:13D7...13D9)
– Output mode control
– Dolby Bass Management
– Center and surround delays
– Level adaption

If the signal source is the S/PDIF-input, the controller may select one of eight content channels depending on availability (D0:13BC). The respective service information is displayed in cell Bit Stream Mode (D0:13A2).

The bit stream elements contain all necessary information required to correctly handle the audio. All elements important for controller actions are displayed in the status memory (see Table 3–6 on page 23).

The MAS 3528E decodes all Dolby Digital formats from 1 to 5.1 audio channels. Accordingly, one to six of the output channels are used for the decoded audio. The output mode is selected in D0:13D6. An additional downmix pair can either be Dolby Surround encoded (Lt, Rt) or plain stereo (Lo, Ro; D0:13DE).

If the Dolby Digital input only contains a stereo pair, the controller must recognize this (Dolby Surround Mode; D0:13A6) and should activate an external Pro Logic decoder (e.g. in the DPL 4519G).

2.9.5. MPEG Layer-2 Data Stream

In the MPEG mode a valid MPEG-1 Layer-2 data signal is expected. The steps for decoding are

– Clock synchronization to data input
– S/PDIF-channel selection (one of eight possible)
– Side information extraction
– Audio data decompression
– Optional deemphasis
– Digital volume

If the signal source is the S/PDIF-input, the controller may select one of eight content channels depending on availability (D0:13BC).

2.9.6. PCM Audio Data

PCM-data are received via S/PDIF or I^2S. Sampling frequency will be detected automatically and mirrored in D0:13A0 (UIS_FS_CODE).

If the PCM-data are received via I^2S-bus, the MAS 3528E expects a valid wordstrobe, and I/O-control (D0:13D0) has to be set as described in Table 3–7. In this case the deemphasis must be activated by the controller if necessary.

2.9.7. Deemphasis

For the PCM- and MPEG-formats a deemphasis can be applied to the signal ③ (D0:13E0). This is necessary because the possibly following Dolby Pro Logic encoding requires a flat audio frequency response. For MPEG-encoded audio and via S/PDIF transmitted PCM, this block is activated automatically. For proper operation of PCM signals via I^2S, the controller has to determine whether the PCM signals have been pre-emphasized or not.

2.9.8. Channel Expander

The outputs of the PCM/MPEG-decoders consist of two channels each; the output of the Dolby Digital decoder may have any number between one and six (5.1) channels. To unify the output format between different modes the audio is always mapped to six channels ④.

2.9.9. Noise Generator

A bandpass-shaped or white noise signal can be routed to any combination of the six main output channels ④. The required channel sequence must be done by the controller in D0:13D1.

There is no noise signal available at the Extra Stereo Output.

2.9.10. Post Processing / Bass Management

The implemented post processing functions ⑤ can be applied to the following audio formats. They are

– Downmixing to Lo/Ro or surround sound encoding to Lt/Rt (D0:13DE) for Dolby Digital multichannel signals
– Mixing and digital filtering for the different Output and Bass configurations according to the Dolby Digital Licensee Information Manual (D0:13D5, D0:13D6, D0:13DA)
– Digital volume control (D0:13E1...13E8) for all audio formats
– Appropriate delay lines for center and surround channels (D0:13D2...13D4) for Dolby Digital multichannel signals

2.9.10.1. Extra Stereo Output

For headphone and VCR-recordings, a downmixed output is provided that may be switched from Lt/Rt (surround encoded, default) to Lo/Ro (headphone encoded) ⑥.

Both, the 6-channel output and the Extra Stereo Output ± are routed to the serial data output interface ð.

Note: In order to prevent clipping due to the downmixing in the Custom and Line Modes, the High-Level Cut Compression Scale Factor (D0:13D8) must always be left at $7FFFF_{hex}$ when the Extra Stereo Output is used in conjunction with non-downmixed channels (D0:13D6).

2.9.10.2. Digital Volume

The digital volume control provided is mainly intended for balancing purposes and initially set to 0 dB. Volume control, output configuration, and delays should be set by the controller according to the actual listening situation.

2.9.10.3. Bass Management

Generally, not all of the five loudspeakers in a Dolby Digital system can reproduce the full audio bandwidth. Bass Management allows redirecting low frequencies to loudspeakers which are capable of reproducing this frequency range.

The MAS 3528E supports the following Bass Management modes:

Bass Management mode 0 (D0:13DA = 8)

Attenuation of −15 dB in the SUB channel should be compensated by a 15 dB gain in the D/A-converter.

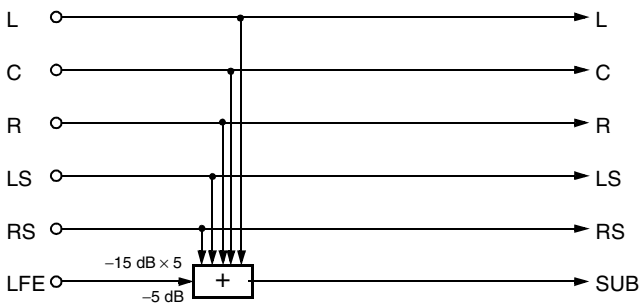

Fig. 2–3: Bass Management configuration 0

Bass Management mode 1 (D0:13DA = 9)

Attenuation of −15 dB in the SUB channel should be compensated by a 15 dB gain in the D/A-converter.

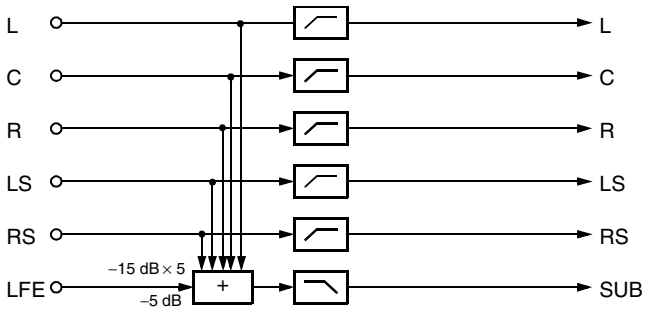

Fig. 2–4: Bass Management configuration 1

Bass Management mode 2 (D0:13DA = A_{hex})

Level adjustment is implemented with −12 db.

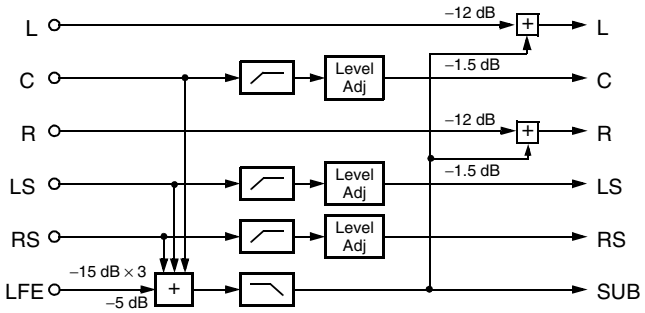

Fig. 2–5: Implementation of configuration 2

Bass Management mode 3 (D0:13DA = B_{hex})

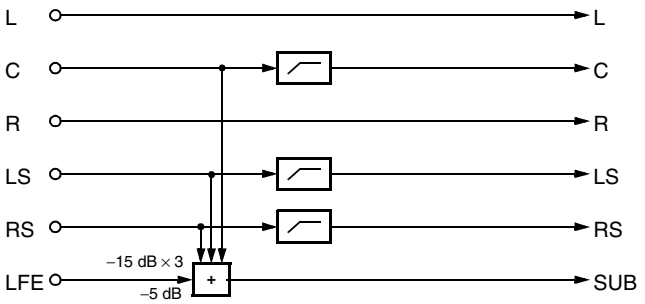

Fig. 2–6: Alternative implementation of configuration 2

Bass Management mode 4 (D0:13DA = C_{hex})

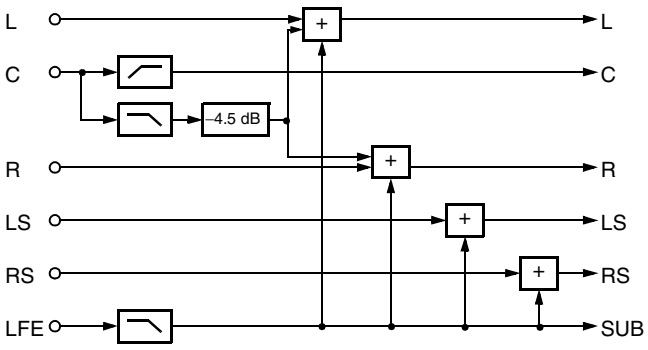

Fig. 2–7: Implementation of configuration 3

Bass Management mode 5 (D0:13DA = D_{hex})

The analog part of SUB should add a +10 db gain

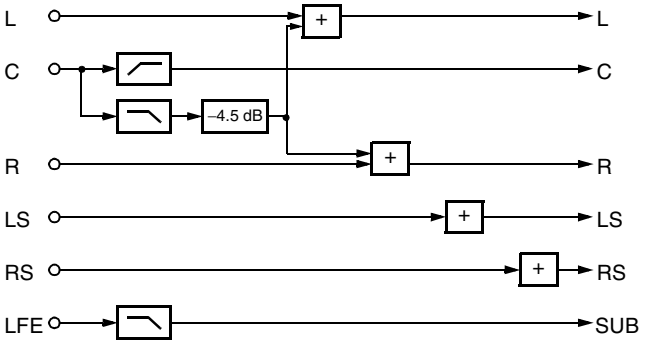

Fig. 2–8: Implementation of configuration three with subwoofer

Bass Management mode 6 (D0:13DA = E_{hex})

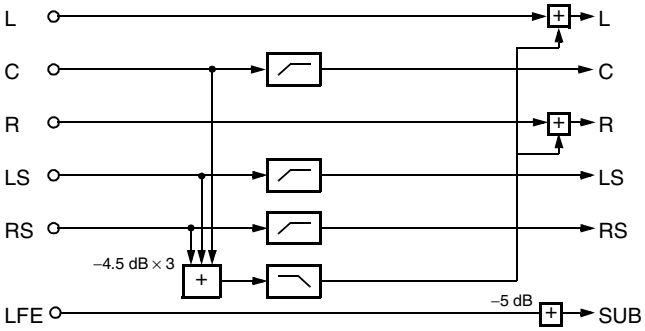

Fig. 2–9: Simplified Bass Management for Multichannel Source Products (I)

Bass Management mode 7 (D0:13DA = F_{hex})

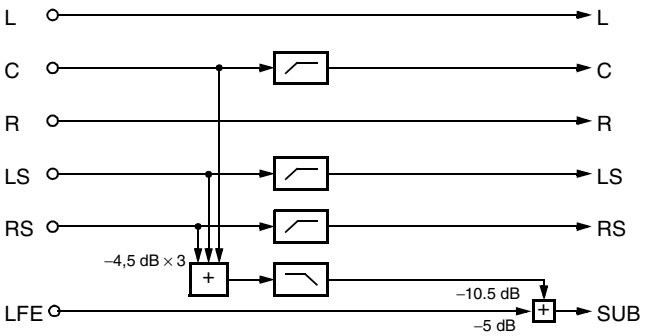

Fig. 2–10: Simplified Bass Management for Multichannel Source Products (II)

2.9.11. Output Format Selection

The output is an I^2S-bus format with either eight audio channels on one line (default) or two audio channels on each of four lines (⑦, D0:13D0). If the 4x2-configuration is selected, the clock and word strobe lines SOC and SOI apply to all four data lines SOD...SOD3. Clock and word strobe signals can be configured to different standards (polarity, delay). The data word length is always 32 bits.

In the 1x8 format, the output data are in the following order:
L, LS, C, Lt/Lo, R, RS, Sub, Rt/Ro.

2.9.12. DTS / S/PDIF Loop-Through

An incoming DTS signal (via S/PDIF) will be reflected in UIS_GOS (D0:13BB).

By default, a recognized DTS signal is looped-through. This means that the signal at S/PDIF input is routed to S/PDIF output without processing – regardless of bit 1 in register $2E_{hex}$.

This automatism can be disabled by setting bit 12 in register $2E_{hex}$ to “1”. Now, the controller is to choose via bit 1 whether a PCM audio signal is output (in case of a DTS signal the output is muted) or whether the input data is looped-through.

2.9.13. Output Sampling Rate

The internally generated system clock is derived from the filling status of the input data buffer by a PLL ⑨. This clock is synchronous to the original sampling rate and is used throughout the complete data processing. Except in the ambiguous case of PCM-data at the serial audio input where the original sampling rate must be defined (D0:13DB), no controller interaction is needed for clock operation.

The output sampling rate is 32 kHz, 44.1 kHz, or 48 kHz, depending on the source.

Since in the Micronas Dolby Digital TV sound solution all further signal processing is on a rate of 48 kHz, the input stage of the DPL 4519G performs the sample rate conversion if necessary.

2.10. System Interaction

2.10.1. Minimum Required Interconnections

The MAS 3528E requires the following connections for normal operation:

– Power supply with adequate blocking capacitors (VDD, VSS, AVDD, AVSS, XVDD, XVSS)

– Crystal with capacitors or clock input (XTI, XTO)

– I^2C-bus and reset-line (I2CC, I2CD) and reset line ($\overline{POR}$) for controlling

– S/PDIF-input (SPDI/SPDI2, SPREF) or serial/I^2S-input (SID, SIC, SII or SID*, SIC*, SII*). In the standard Micronas-solution, the I^2S-signal comes from the MSP 44x0G

– I^2S-output (SOD, SOC, SOI). In the standard configuration, this signal is fed to the DPL 4519G.

Please refer to Fig. 4–20 on page 55 or to the application kit for details.

2.10.2. Required Special Modes in the System

The MAS 3528E interfaces require no configuration. The I^2S outputs and inputs of the Dolby Pro Logic IC DPL 4519G and the MSP 44x0G, however, must be configured to send/accept the 8-channel multiplexed digital PCM-data stream.

The DPL 4519G may generate up to seven analog signals (three pairs plus subwoofer). Further audio signals can be forwarded to the MSP 44x0G for D/A-conversion.

Dolby Pro Logic encoded audio originating from the MSP 44x0G (TV-sound) must be routed through the MAS 3528E to the DPL 4519G for further processing.

2.10.3. Minimum System Set-Up

The following I^2C-command sequence is necessary for the DPL 4519G:

– I^2C-controlled reset

– Write MODUS Register (set I^2S-input to slave mode)

– Write I2S_CONFIG (multi sample mode, 32 bits, clock to 8*32 bits)

– Set I2S3 Resorting Matrix to “left/right eight MAS 3528E”. The signal pairs are now in the following order: Lt/Rt, L/R, SL/SR, C/Sub

– Select first I^2S3-input pair as source for I^2S Output (because of 8*32-bit mode all 4*2 channels will be looped through to the MSP 44x0G) and set to transparent stereo

– Select one input pair as source for Loudspeaker Output (numbers 7...10 mean first...fourth pair)

– Select one input pair as source for Aux Output (numbers 7...10 mean first...fourth pair)

– Set volume control for Loudspeaker Output

– Set volume control for Aux Output

If a Multistandard Sound Processor is present in the system, similar set-up commands are required. For further details, please refer to the DPL 4519G or the MSP 44x0G data sheets.

If both devices are used on the same I^2C-bus, the device addresses must be set to different values by hardware means.

The D/A-conversion of audio signals may be freely appointed between the DPL 4519G and the MSP 44x0G. For an example, please refer to Table 2–4.

Table 2–3: Output configuration matrix. All registers are at I^2C-subaddress 12_{hex} of the respective device. Note that only one code per register applies.

Device	**DPL 4519G**			**MSP 44x0G**			
Register → Signal Pair ↓	**Loudsp. 00 08_{hex}**	**Aux 00 09_{hex}**	**SCART1 00 $0A_{hex}$**	**Loudsp. 00 08_{hex}**	**Aux 00 09_{hex}**	**SCART1 00 $0A_{hex}$**	**SCART2 00 41_{hex}**
Lt/Rt (Lo/Ro)	07 20_{hex}	07 20_{hex}	07 20_{hex}	07 20_{hex}	07 20_{hex}	07 20_{hex}	07 20_{hex}
L/R	08 20_{hex}	08 20_{hex}	08 20_{hex}	08 20_{hex}	08 20_{hex}	08 20_{hex}	08 20_{hex}
SL/SR	09 20_{hex}	09 20_{hex}	09 20_{hex}	09 20_{hex}	09 20_{hex}	09 20_{hex}	09 20_{hex}
C/Sub	0A 20_{hex} [1)]	0A 20_{hex} [1)]	0A 20_{hex} [1)]	0A 20_{hex} [1)]	0A 20_{hex} [1)]	0A 20_{hex} [1)]	0A 20_{hex} [1)]
[1)] Use 0A 20_{hex} for C/Sub output, 0A 00_{hex} for Center signal on both outputs, 0A 10_{hex} for Sub signal on both outputs							

Table 2–4: Example: In the DPL 4519G use both loudspeaker output channels for center, the auxiliary output for surround, the SCART1 output for Lt/Rt. In the MSP 44x0G use the loudspeaker output for L/R, both auxiliary output channels for Sub and the SCART1 output for an additional Lt/Rt-signal.

Device	**DPL 4519G**			**MSP 44x0G**			
Register → Signal Pair ↓	**Loudsp. 00 08_{hex}**	**Aux 00 09_{hex}**	**SCART1 00 $0Aa_{hex}$**	**Loudsp. 00 08_{hex}**	**Aux 00 09_{hex}**	**SCART1 00 $0A_{hex}$**	**SCART2 00 41_{hex}**
Lt/Rt (Lo/Ro)			07 20_{hex}			07 20_{hex}	
L/R				08 20_{hex}			
SL/SR		09 20_{hex}					
C/Sub	0A 00_{hex}				0A 10_{hex}		

3. Control Interface

3.1. Start-Up Sequence

After power-up and a reset (see Section 3.3. on page 18), the IC is in its default state (see Table 3–7 on page 31). The controller has to initialize all memory cells for which a non-default setting is necessary.

3.2. I²C Interface Access

3.2.1. General

Control communication with the MAS 3528E is done via an I²C slave interface. The device addresses are $3A_{hex}$ (write) and $3B_{hex}$ (read) as shown in Table 3–1.

I²C clock synchronization is used to slow down the interface if required.

Table 3–1: I²C device address

A7	A6	A5	A4	A3	A2	A1	W/R
0	0	1	1	1	0	1	0/1

3.2.2. I²C Registers and Subaddresses

The interface uses one level of subaddresses. The MAS 3528E interface has 3 subaddresses allocated for the corresponding I²C-registers.

The address $6A_{hex}$ is used for basic control, i.e. reset and task select. The other addresses are used for data transfer from/to the MAS 3528E.

The I²C-control and data registers of the MAS 3528E are 16 bits wide, the MSB is denoted as bit [15]. Transmissions via I²C-bus have to take place in 16-bit words (two byte transfers, MSB sent first); thus for each register access two 8-bit data words must be sent/received via I²C-bus.

Table 3–2: Subaddresses

Sub-address	I²C-Register	Function
68_{hex}	data	Controller writes to MAS 3528E data register
69_{hex}	data	Controller reads from MAS 3528E data register
$6A_{hex}$	control	Controller writes to MAS 3528E control register

3.2.3. Conventions for the Command Description

The description of the various controller commands uses the following formalism:

– **Abbreviations** used in the following descriptions:
  a address
  d data value
  n count value
  o offset value
  r register number
  x don't care

– A data value is split into 4-bit nibbles which are numbered zero-bound.

– Data values in nibbles are always shown in hexadecimal notation.

– A hexadecimal 20-bit number **d** is written, e.g. as **d** = $17C63_{hex}$, its five nibbles are d0 = 3_{hex}, d1 = 6_{hex}, d2 = C_{hex}, d3 = 7_{hex}, and d4 = 1_{hex}.

– **Variables** used in the following descriptions:

dev_write	$3A_{hex}$	device write
dev_read	$3B_{hex}$	device read
data_write	68_{hex}	data register write
data_read	69_{hex}	data register read
control	$6A_{hex}$	control register write

– **Bus signals**

S	Start		
P	Stop		
A	ACK	=	Acknowledge
N	NAK	=	Not acknowledge
W	Wait	=	I²C clock line is held low while the MAS 3528E is processing the current I²C command

– **Symbols** in the telegram examples

<	Start Condition
>	Stop Condition
dd	data byte
xx	ignore

All telegram numbers are hexadecimal, data originating from the MAS 3528E are shown in gray.
Example:

<3A 68 dd dd>	write data to DSP
<3A 69 <3B dd dd>	read data from DSP

Fig. 3–1 shows I²C bus protocols for read and write operations of the interface; the read operation requires an extra start condition and repetition of the chip address with the read command ($3B_{hex}$). Fields with signals/data originating from the MAS 3528E are marked by a gray background. Note that in some cases, the data reading process must be concluded by a NAK condition.

Example: I2C write access

S	dev_write ($3A_{hex}$)	W	A	data_write (68_{hex})	A	high data word	A	low data word	A	P

Example: I^2C read access

S	dev_write ($3A_{hex}$)	W	A	data_read (69_{hex})	A	S	dev_read ($3B_{hex}$)	W	A	high data word	A	
										low data word	N	P

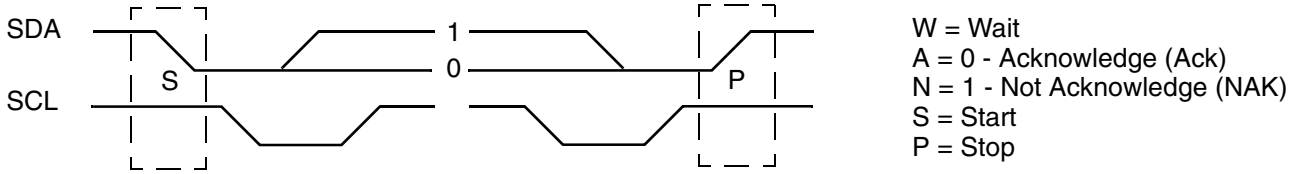

Fig. 3–1: I^2C bus protocol for the MAS 3528E (MSB first; data must be stable while clock is high)

3.2.4. The Internal Fixed Point Number Format

In the following sections, two number representations are used: The fixed point notation ‘v’ and the 2’s complement number notation ‘r’.

The conversion between the two forms of notation is easily done (see the following equations).

$r = v*524288.0+0.5; (-1.0 \leq v < 1.0)$ (EQ 1)

$v = r/524288.0; (-524288 < r < 524287)$ (EQ 2)

3.3. I^2C Control Register (Code $6A_{hex}$)

S	dev_write	W	A	control	A	d3,d2	A	d1,d0	A	P

The I^2C control register is a write-only register. Its main purpose is the software reset of the MAS 3528E. The software reset is done by writing a 16-bit word to the MAS 3528E with bit 8 set. The four least significant bits are reserved for task selection. In standard Dolby Digital/MPEG-decoding, these bits must always be set to 0.

Table 3–3: Control register bit assignment1)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
x	x	x	x	x	x	x	R	0	0	0	0	T3	T2	T1	T0

1) x = don’t care, R = reset, T3...T0 0 task selection

3.4. I^2C Data Register (Codes 68_{hex} and 69_{hex}) and the MAS 3528E DSP-Command Syntax

The DSP-core of the MAS 3528E has two RAM-banks denoted D0 and D1. The word size is 20 bits. All RAM-addresses can be accessed in a 20-bit or a 16-bit mode via I^2C-bus. For fast access of internal DSP-states, the processor core also has an address space of 256 data registers. All register and RAM-addresses are given in hexadecimal notation.

The control of the DSP in the MAS 3528E is done via the I^2C data register by using a special command syntax. These commands allow the controller to access the DSP-registers and RAM-cells and thus monitor internal states, set the parameters for the DSP-firmware, control the hardware, and even provide a download of alternative software modules.

The DSP-commands consist of a “Code” which is sent to I^2C-data register together with additional parameters.

S	dev_write	W	A	data_write	A	**Code**,...	A	...,...	A	...

The MAS 3528E firmware scans the I^2C interface periodically and checks for pending or new commands. The commands are then executed by the DSP during its normal operation without any loss or interruption of the incoming data or outgoing audio data stream. However, due to some time critical firmware parts, a certain latency time for the response has to be expected. The theoretical worst case response time does not exceed 4 ms. However, the typical response time is less than 0.5 ms. Table 3–4 on page 19 shows the basic controller commands that are available by the MAS 3528E.

Table 3–4: Basic controller command codes

Code (hex)	Command	Function
A	Read from register	Controller reads an internal register of the MAS 3528E.
B	Write to register	Controller writes an internal register of the MAS 3528E.
C	Read D0 memory	Controller reads a block of the DSP memory.
D	Read D1 memory	Controller reads a block of the DSP memory.
E	Write D0 memory	Controller writes a block of the DSP memory.
F	Write D1 memory	Controller writes a block of the DSP memory.

Table 3–4 gives an overview of the different commands which the DSP-core may receive. The “Code” is always the first data nibble transmitted after the “data_write” byte. A second auxiliary code nibble is used for the short memory access commands.

Because of the 16-bit width of the I^2C-data register, all actions always transmit telegrams with multiples of 16 data bits.

3.4.1. Read Register (Code A_{hex})

1) send command

S	dev_write	W	A	data_write	A	**A**,r1	A	r0,0	W	A	P

2) get register value

S	dev_write	W	A	data_read	A	S	dev_read	W	A		
	x,x	A	x,d4	W	A	d3,d2	A	d1,d0	W	N	P

The MAS 3528E has an address space of 256 DSP-registers. Some of the registers (**r** = r1,r0 in the figure above) are direct control inputs for various hardware blocks, others control the internal program flow. In Section 3.5. on page 22, the registers of interest with respect to the Dolby Digital/MPEG-decoding firmware are described in detail. In contrast to memory cells, registers cannot be accessed as a block but must always be addressed individually.

Example:
Read the content of register ($2E_{hex}$):

```
<3A 68 A2 E0>                    define register
<3A 69 <3B xx xd dd dd>          and read
```

3.4.2. Write Register (Code B_{hex})

S	dev_write	W	A	data_write	A	**B**,r1	A	r0,d4	W	A	
						d3,d2	A	d1,d0	W	A	P

The controller writes the 20-bit value (**d** = d4,d3,d2,d1,d0) into the MAS 3528E register (**r** = r1,r0). A list of registers is given in Section 3.5. on page 22

Example: Disable automatic S/PDIF loop-through for DTS by writing the value 1000_{hex} into the register with the number $2E_{hex}$:

```
<3A 68 B2 E0 10 00>
```

3.4.3. Read Memory (Codes C_{hex} and D_{hex})

The MAS 3528E has 2 memory areas called D0 and D1. Both areas have different read and write commands. The memory areas D0 can be read by using the codes C_{hex}.

1) send command (e.g. Read D0)

S	dev_write	W	A	data_write	A	**C**,0	A	0,0	W	A	
						n3,n2	A	n1,n0	W	A	
						a3,a2	A	a1,a0	W	A	P

2) get memory value

S	dev_write	W	A	data_read	A	S	dev_read	W	A		
	x,x	A	x,d4	W	A	d3,d2	A	d1,d0	W	A	
	....repeat for n data values....										
	x,x	A	x,d4	W	A	d3,d2	A	d1,d0	W	N	P

The *Read D0 Memory* command gives the controller access to all 20 bits of D0-memory cells of the MAS 3528E. The telegram to read three words starting at location D0:100 is

```
<3A 68 C0 00 00 03 01 00>
<3A 69 <3B xx xd dd dd
           xx xd dd dd xx xd dd dd>
```

The *Read D1 Memory* command (D_{hex})is provided to get information from D1 memory cells of the MAS 3528E.

3.4.4. Short Read Memory (Codes $C4_{hex}$ and $D4_{hex}$)

Because most cells in the Dolby Digital user interface are only 16 bits wide, it is faster and more convenient to access the memory locations with a special 16-bit mode for reading:

1) send command (e.g. Short Read D0)

S	dev_write	W	A	data_write	A	**C,4**	A	0,0	W	A	
						n3,n2	A	n1,n0	W	A	
						a3,a2	A	a1,a0	W	A	P

2) get memory value

S	dev_write	W	A	data_read	A	S	dev_read	W	A		
						d3,d2	A	d1,d0	W	A	
	....repeat for n data values....										
						d3,d2	A	d1,d0	W	N	P

This command is similar to the normal 20-bit read command and uses the same command codes C_{hex} and D_{hex} for D0 and D1-memory, respectively, however, it is followed by a 4_{hex} rather than a 0_{hex}.

The *Short Read D1 Memory* command works similarly to the *Read D1 Memory* command but with the code D_{hex} followed by a 4_{hex}.

Example: Read 16 bits of D1:123 has the following I^2C protocol:

```
<3A 68 D4 00          read 16 bits from D1
       00 01          one word to be read
       01 23>         start address
<3A 69 <3B dd dd>     start reading
```

3.4.5. Write Memory (Codes E_{hex} and F_{hex})

The memory areas D0 and D1 can be written by using the codes E_{hex} and F_{hex}, respectively.

e.g. Write D0

S	dev_write	W	A	data_write	A	**E**,0	A	0,0	W	A
						n3,n2	A	n1,n0	W	A
						a3,a2	A	a1,a0	W	A
						0,0	A	0,d4	W	A
						d3,d2	A	d1,d0	W	A

....repeat for n data values....

0,0	A	0,d4	W	A	
d3,d2	A	d1,d0	W	A	P

With the *Write D0/D1 Memory* command n 20-bit memory cells in D0*/D1* can be initialized with new data.

Example: Write 80234_{hex} to D0:FFB has the following I^2C protocol:

```
<3A 68 E0 00          write D0 memory
       00 01          1 word to write
       0F Fb          start address FFB_hex
       00 08          value = 80234_hex
       02 34>
```

3.4.6. Short Write Memory (Codes $E4_{hex}$ and $F4_{hex}$)

e.g. Short Write D0

S	dev_write	W	A	data_write	A	**E,4**	A	0,0	W	A
					A	n3,n2	A	n1,n0	W	A
					A	a3,a2	A	a1,a0	W	A
					A	d3,d2	A	d1,d0	W	A

....repeat for n data values....

A	d3,d2	A	d1,d0	W	A	P

For faster access, only the lower 16 bits of each memory cell are accessed. The four MSBs of the cell are cleared. The command uses the same codes E_{hex} and F_{hex} for D0/D1 as for the 20-bit command but followed by a 4 rather than a 0.

3.4.7. Default Read

The *Default Read* command is the fastest way to get information from the MAS 3528E. Executing the *Default Read* in a polling loop can be used to detect a special state during decoding.

S	DW	W	A	data_read	A	S	dev_read	W	A			
							d3,d2	A	d1,d0	W	N	P

The *Default Read* command immediately returns the lower 16 bit content of a specific RAM location as defined by the pointer D0:FFB. The pointer must be loaded before the first *Default Read* action occurs. If the MSB of the pointer is set, it points to a memory location in D1 rather than to one in D0.

Example: For watching D1:123, the pointer D0:FFB must be loaded with 8123_{hex}:

```
<3A 68 E0 00          write to D0 memory
     00 01            one word to write
     0F Fb            start address FFB
     00 08            value = 8_hex...
     01 23>                ...0123_hex
```

Now the *Default Read* commands can be issued as often as desired:

```
<3A 69 <3B            Default Read command
  dd dd>              16 bit content of the
                      address as defined by the
                      pointer
<3A 69 <3B dd dd>     ... and do it again
```

3.5. Registers

In Table 3–5, the internal registers that are useful for controlling the MAS 3528E are listed. They are accessible by Read/Write Register I^2C commands (see Section 3.4.1. and Section 3.4.2. on page 20).
Note: Registers not given in this table must not be written.

Table 3–5: Command Register Table

Register Address (hex)	R/W	Function	Default (hex)	Name
2E	R/W	**Loop-through and Sync Pin Controlling** bit[12] 0: automatic active loop-through if DTS is recognized or the input format at S/PDIF_in cannot be determined (default) 1: bit[1] controls loop-through bit[11:2] reserved: do not change! bit[1] 0: normal operation 1: connect SPDI_in to SPDIF OUT (loop-through) bit[0] sync bit (will be automatically detected and set by internal software)	00000	Output_Conf
4B	W	**PIO Configuration** Configuration of pins must be zero.	00000	PIO_Config
48	R	**PIO Data Input** The input level of every PI pin in the input mode can be read out of this register; the bit number corresponds to the PI number. bit[n] 0: input is low bit[n] 1: input is high		PIO_Data_In
49	W	**PIO Data Output** The output level of every PI pin in the output mode can be defined by this register; the bit number corresponds to the PI number. bit[n] 0: output is low bit[n] 1: output is high		PIO_Data_Out
CC	R/W	**PIO Direction** Every bit switches the PI pin with the corresponding number from input to output. bit[n] 0: input mode bit[n] 1: output mode bit[14:16] must be zero if PI14, PI15, and PI16 are used as alternative inputs SID*, SII*, and SIC*.	00000	PIO_Direction
56	R	**Incoming S/PDIF Channel Status Bits** bit[19:0] mirrors first 20 channel status bits		SPI0CS

3.6. Special Memory Locations and User Interface

Operation of the DSP and the interfaces can be observed and controlled via the memory locations of the user interface. These memory cells are located at the high end of the D0-RAM.

Status cells are written by the DSP and read by the controller, configuration cells are written by the controller and read by the DSP, hybrid cells can be written and read by either side.

Note: Memory addresses not given in this table must not be accessed.

3.6.1. Status Interface for Decoding

The following table contains the memory locations of the firmware status information. Addresses are hexadecimal, memory cell content is binary when written without indicator and hexadecimal when written with a hex-suffix.

Table 3–6: Status memory cells

Memory Address (hex)	Function	Mode	Name
D0:13A0	**Sample Rate of Input Bitstream** (Table 5.1 of ATSC Spec. A/52) bit[1:0] 00 48 kHz 01 44.1 kHz 10 32 kHz 11 not detected (default)	**Dolby Digital** **MPEG** **PCM**	UIS_FSCOD
D0:13A1	**Bit Stream Identification (bsid)** (Section 5.4.2.1 of ATSC Spec. A/52) bit[4:0] 00_{hex}...$1f_{hex}$ current bsid value Bit streams that have a bsid higher than the decoder's version number may be incompatible. In this case, the decoding is inhibited. The version number for the implemented firmware is 8.	**Dolby Digital**	UIS_BSID
D0:13A2	**Bit Stream Mode (bsmod)** (Table 5.2 of ATSC Spec. A/52) bit[2:0] 000 main audio service: complete main (CM) 001 main audio service: music and effects (ME) 010 associated service: visually impaired (VI) 011 associated service: hearing impaired (HI) 100 associated service: dialogue (D) 101 associated service: commentary (C) 110 associated service: emergency (E) 111 acmod = 001, associated service: voice over (VO) 111 acmod = 010-111, main audio service: karaoke This information is valid after selecting (D0:13D0) an available (D0:13BC) channel (data stream) from the S/PDIF-input. Prior to this, the bsmod can be directly derived from the Pc-preambles of the S/PDIF-data (D0:13BD...13C4).	**Dolby Digital**	UIS_BSMOD

Table 3–6: Status memory cells, continued

Memory Address (hex)	Function	Mode	Name
D0:13A3	**Audio Coding Mode (acmod)** (Table 5.3 of ATSC Spec. A/52) bit[2:0] 000 1+1 Ch1, Ch2 — bsmod != '111'; Voice Over (VO) — bsmod = '111' (Karaoke) 001 1/0 C 010 2/0 L, R — L, R 011 3/0 L, C, R — L, M, R 100 2/1 L, R, S — L, R, V1 101 3/1 L, C, R, S — L, M, R, V1 110 2/2 L, R, SL, SR — L, R, V1, V2 111 3/2 L, C, R, SL, SR — L, M, R, V1, V2 For user information: indicates the applied main channel.	**Dolby Digital**	UIS_ACMOD
D0:13A4	**Center Mix Level (cmixlev)** (Table 5.4 of ATSC Spec. A/52) bit[1:0] 00 0.707 (–3.0 dB) 01 0.595 (–4.5 dB) 10 0.500 (–6.0 dB) 11 reserved (–6.0 dB), nominal downmix level of center with respect to left and right channels Used in the internal algorithm.	**Dolby Digital**	UIS_CLEV
D0:13A5	**Surround Mix Level (surmixlev)** (Table 5.5 of ATSC Spec. A/52**)** bit[1:0] 00 0.707 (–3.0 dB) 01 0.500 (–6.0 dB) 10 0 11 reserved (–6.0 dB), nominal downmix level of surround channels Used in the internal algorithm.	**Dolby Digital**	UIS_SLEV
D0:13A6	**Dolby Surround Mode (dsurmod)** (Table 5.6 of ATSC Spec. A/52) bit[1:0] 00 not indicated 01 not Dolby Surround encoded 10 Dolby Surround encoded 11 reserved (not indicated) As soon as the audio is Dolby Surround encoded, the controller must activate the Dolby Pro Logic decoder (e.g. in the DPL 4519G) without any user interaction.	**Dolby Digital**	UIS_DSURMOD
D0:13A7	**Low Frequency Effects Channel (lfeon)** (Section 5.4.2.7 of ATSC Spec. A/52) bit[0] 0 LFE off 1 LFE on The user may want to choose a different output configuration depending on the availability of the LFE.	**Dolby Digital**	UIS_LFEON

Table 3–6: Status memory cells, continued

Memory Address (hex)	Function	Mode	Name
D0:13A8	**Dialogue Nomalization (dialnorm)** (Section 5.4.2.8 of ATSC Spec. A/52) bit[4:0] 01_{hex}... average dialog level –1 dB...–31 dB below $1F_{hex}$ 100% digital 00_{hex} reserved Used in the internal algorithm.	**Dolby Digital**	UIS_DIALNORM
D0:13AA	**Language Code (langcode, langcod)** (Sections 5.4.2.11 and 5.4.2.12 of ATSC Spec. A/52) bit[15:0] $FFFF_{hex}$ langcode = 0 (langcod nonexistent in stream) bit[7:0] langcod The controller may check all S/PDIF-data streams (channels) for the desired language.	**Dolby Digital**	UIS_LANGCOD
D0:13AB	**Mixing Level and Room Type (audprodie, mixlevel, roomtyp)** (Sections 5.4.2.13, 5.4.2.14 and 5.4.2.15 of ATSC Spec. A/52) bit[15:0] $FFFF_{hex}$ audprodie = 0 (mixlevel, roomtyp nonexistent in data stream) bit[6:2] mixlevel bit[1:0] roomtyp For user information.	**Dolby Digital**	UIS_MIXLEVEL_ ROOMTYP
D0:13AC	**Dialogue Nomalization 2 for Dual Mono Mode 1+1 (dialnorm2)** (Section 5.4.2.16 of ATSC Spec. A/52) bit[4:0] 01_{hex}...$1F_{hex}$ average dialog level –1dB...–31dB below 100% digital 00_{hex} reserved Used in the internal algorithm.	**Dolby Digital**	UIS_DIALNORM2
D0:13AE	**Language Code 2 for Ch2 in Dual Mono Mode 1+1 (langcod2e, langcod2)** (Section 5.4.2.19 and 20 of ATSC Spec. A/52) bit[15:0] $FFFF_{hex}$ langcod2e = 0 (langcod2 nonexistent in stream) bit[7:0] langcod2 Used in the internal algorithm.	**Dolby Digital**	UIS_LANGCOD2
D0:13AF	**Mixing Level and Room Type for Ch2 in Dual Mono Mode 1+1 (audprodi2e, mixlevel2, roomtyp2)** (Section 5.4.2.21, 22 and 23 of ATSC Spec. A/52) bit[15:0] $FFFF_{hex}$ audprodi2e = 0 (mixlevel2, roomtyp2 nonexistent in stream) bit[6:2] mixlevel2 bit[1:0] roomtyp2 For user information.	**Dolby Digital**	UIS_MIXLEVEL2_ ROOMTYP2

Table 3–6: Status memory cells, continued

Memory Address (hex)	Function	Mode	Name
D0:13B0	**Copyright Bit (copyrightb)** (Section 5.4.2.24of ATSC Spec. A/52) bit[0] 0 not protected 1 protected by copyright	**Dolby Digital**	UIS_COPYRIGHTB
D0:13B1	**Original Bit Stream (origbs)** (Section 5.4.2.25 of ATSC Spec. A/52) bit[0] 0 copy of a bit stream 1 original bit stream	**Dolby Digital**	UIS_ORIGBS
D0:13B2	**Time Code 1** (Section 5.4.2.27of ATSC Spec. A/52) bit[15:0] $FFFF_{hex}$ timecod1e = 0 (time code 1 nonexistent) bit[13:0] time code 1(first half) bit[13:9] time in hours (0...23 valid) bit[8:3] time in minutes (0...59 valid) bit[2:0] time in 8-second increments (0 = 0 seconds) (1 = 8 seconds) : (7 = 56 seconds) For external synchronization purposes.	**Dolby Digital**	UIS_TIMECOD1
D0:13B3	**Time Code 2** (Section 5.4.2.28of ATSC Spec. A/52) bit[15:0] $FFFF_{hex}$ timecod2e = 0 (time code 2 nonexistent) bit[13:0] time code 2 (second half) bit[13:11] time in 8-second increments, see time code 1 bit[10:6] time in frames (0...29 valid) bit[5:0] time in 1/6 frames For external synchronization purposes.	**Dolby Digital**	UIS_TIMECOD2
D0:13B4	**Dynamic Range Gain Word (dynrnge, dynrng)** (Section 5.4.3.3 and 5.4.3.4 of ATSC Spec. A/52) bit[15:0] $FFFF_{hex}$ dynrnge = 0 (dynrng nonexistent in stream) bit[7:0] current dynrng value Used in the internal algorithm.	**Dolby Digital**	UIS_DYNRNG
D0:13B5	**Dynamic Range Gain Word 2 for Ch2 in dual mono mode (dynrng2e, dynrng2)** (Section 5.4.3.5 and 5.4.3.6 of ATSC Spec. A/52) bit[15:0] $FFFF_{hex}$ dynrng2e = 0 (dynrng2 nonexistent in stream) bit[7:0] current dynrng value Used in the internal algorithm.	**Dolby Digital**	UIS_DYNRNG2

Table 3–6: Status memory cells, continued

Memory Address (hex)	Function		Mode	Name
D0:13B6	**Karaoke Flag**		**Dolby Digital**	UIS_ KARAOKEFLAG
	bit[0]	0	no Karaoke info in bit stream	
		1	Karaoke info in bit stream	
D0:13B7	**Frame Count**		**Dolby Digital, MPEG**	UIS_FRAME_ COUNTER
	bit[19:0]		counts 0, 1, 2, 3, 4, ..., 1048575 (= $FFFFF_{hex}$), 1, ...	
D0:13B8	**MPEG Header Bits 12...31**		**MPEG**	UIS_MPEG_ HEADER
	bit[19]		ID (must be 1 for MPEG-1)	
	bit[18:17]		Layer	
		00	reserved	
		01	Layer 3	
		10	Layer 2	
		11	Layer 1	
	bit[16]		Protection	
		0	CRC	
		1	no CRC	
	bit[15:12]		bit rate (see table in IEC 11172-3, Layer 2)	
		0_{hex}	free	
		1	32	
		2	48	
		3	56	
		4	64	
		5	80	
		6	96	
		7	112	
		8	128	
		9	160	
		a	192	
		b	224	
		c	256	
		d	320	
		e	384	
		f	forbidden	
	bit[11:10]		sampling frequency (MPEG-1 Layer-2)	
		00	44.1 kHz	
		01	48 kHz	
		10	32 kHz	
		11	reserved	
	...			

Table 3–6: Status memory cells, continued

Memory Address (hex)	Function		Mode	Name
D0:13B8 (continued)	bit[9]		padding bit	
	bit[8]		private bit	
	bit[7:6]		Mode	
		00	stereo	
		01	joint stereo	
		10	dual channel	
		11	reserved	
	bit[5]		Joint Stereo Mode Extension ms_stereo	
		0	off	
		1	on	
	bit[4]		Joint Stereo Mode Extension Intensity Stereo	
		0	off	
		1	on	
	bit[3]		Copyright	
		0	not protected	
		1	protected	
	bit[2]		Original/Copy	
		0	copy	
		1	original	
	bit[1:0]		Emphasis	
		00	none	
		01	50/15 µs	
		10	reserved	
		11	CCITT J.17	
D0:13B9	**MPEG Status**		**MPEG**	UIS_MPEG_ STATUS
	bit[5]	0	mono	
		1	stereo	
	bit[4]	1	CRC error	
	bit[3:2]	>0	other decoding error (not enough data)	
	bit[1:0]	>0	header error	

Table 3–6: Status memory cells, continued

Memory Address (hex)	Function	Mode	Name
D0:13BB	**Global Operation Status (GOS)**	**S/PDIF-Input**	UIS_GOS
	bit[7:5] GOS_Type 0 GOS_NODEC, not decodable 1 GOS_PCM_WARN, channel status not plausible 2 GOS_DATA, data type 3 GOS_PCM 4...6 reserved 7 GOS_I2S		
	bit[4:1] Appl_Type 0 AC-3 1 MPEG Layer-2 2 PCM 3 time code 4 noise generator 5 DTS 15 unknown		
	bit[0] 0 unsynchronized (default) 1 valid bit stream detected		
	This status cell reflects the result of the decoding with the parameters given. If an incorrect input data type (D0:13D0) is selected, the input data stream will not be decodable. The GOS_PCM_WARN-flag is set when the S/PDIF-channel status indicates PCM-encoded audio, but valid synchronization headers (Dolby Digital or MPEG) are found.		
D0:13BC	**Bit Stream Information**	**S/PDIF-Input**	UIS_DSI
	each bit: 1 channel available 0 channel not available bit[7] bit stream number 7 ... bit[0] bit stream number 0 Available bit streams (channels) in the S/PDIF-data.		

Table 3–6: Status memory cells, continued

Memory Address (hex)	Function	Mode	Name
D0:13BD ... D0:13C4	**Pc Information of Selected Data Stream (burst_info)** (Section 4.4.3 of Annex B of ATSC Spec. A/52)	**S/PDIF-Input**	UIS_PC<i>, i = 0...7
	bit[15:13] $0_{hex}...7_{hex}$ channel number (data_stream_number) bit[12:8] data_type_dependent, see below bit[7] error flag (error_flag) 0 data may be valid 1 data burst may contain errors bit[6:5] reserved bit[4:0] 00_{hex} reserved 01_{hex} AC-3 data 02_{hex} reserved 03_{hex} pause 04_{hex} MPEG Layer-1 05_{hex} MPEG-1 Layer-2, 3, or MPEG-2 without extension 06_{hex} MPEG-2 data with extension 07_{hex} reserved 08_{hex} MPEG-2 Layer-1 low fs 09_{hex} MPEG-1 Layer-2, 3 low fs $0A_{hex}$ reserved $0B_{hex}...D_{hex}$ DTS $0E_{hex}...1F_{hex}$ reserved This memory cell mirrors the Pc-word of the S/PDIF-preamble (burst_info) of the selected of eight possible data streams (channels) if available.		
	Meaning of Field data_type_dependent AC-3: (Section 4.7 of Annex B of ATSC Spec. A/52) bit[12,11] 00 reserved, shall be '00' bit[10:8] value of bsmod as described in D0:13A2	**Dolby Digital**	
D0:13C7	**S/PDIF Status** bit[3:2] 0 no error >0 parity error bit[1] Data Mode 0 PCM 1 compressed audio data bit[0] S/PDIF Copy Active 0 inactive 1 active	**S/PDIF**	UIS_SP_STATUS
D0:1FFF	**Version Number** Returns the version number of the ROM-code as ASCII	**All**	UIS_VERSION

3.6.2. Control Interface for Decoding Operation

The following table gives the writable memory addresses of the control interface for the decoding firmware.

Table 3–7: Configuration memory cells

Memory Address (hex)	Function	Mode	Reset Value (hex)	Name
D0:13D0	**I/O Control**		00000	UIC_IO_CONTROL
	Soft Mute bit[15] Soft Mute 0 Soft mute off 1 Soft mute on This switch is provided for user-controlled fast audio mute.	**All**		
	CRC Check bit[14] CRC1 0 CRC1 on 1 CRC1 off bit[13] CRC2 0 CRC2 on 1 CRC2 off **Dolby Digital:** CRC1 protects the header and 3/5 of the data, CRC2 protects the remaining 2/5 of the data. It is recommended that both AC-3 CRC-checks are enabled which yields to an automatic mute upon detection of an error. However, under special operating conditions (noisy channel), it may be advantageous to turn one (preferably CRC2) or both CRC-checks off. In this case, it is important to decrease the listening volume to prevent hearing injuries and damages to the equipment. **MPEG:** For MPEG, only CRC1 is applied. It is recommended to enable CRC1 to avoid strong digital noise in case of deranged or unreliable signals.	**Dolby Digital** **MPEG**		
	S/PDIF Channel Select bit[12:10] S/PDIF channel select 000 Channel 0 ... 111 Channel 7 The S/PDIF may carry up to eight channels of compressed audio. Their content is shown in the S/PDIF-Pc-preambles (D0:13B8...13BF).	**S/PDIF**		

Table 3–7: Configuration memory cells, continued

Memory Address (hex)	Function		Mode	Reset Value (hex)	Name
D0:13D0 (continued)	**Input and Mode Selection**		**All**	00000	UIC_IO_CONTROL
	bit[9]		S/PDIF or I^2S Input Select		
		0	S/PDIF input		
		1	I^2S input		
	bit[8]		I^2S input select		
		0	I^2S input at SID (word mode)		
		1	Continuos data stream at SID (SII connected to ground)		
	bit[7:6]		Input data type		
		00	Auto-detection		
		01	AC-3 (Dolby Digital)		
		10	MPEG Layer-2		
		11	PCM		
	Output Interface Mode		**All**		
	bit[5]	0	default		
		1	I^2S output mode: invert wordstrobe		
	bit[1]		I^2S output channels		
		0	8×1 channel		
		1	4×2 channels The clock and wordstrobe outputs SOC and SOI apply to all 4 data outputs SOD...SOD3		
	bit[0]		I^2S output mode		
		0	no delay (as used in Sony Mode)		
		1	delay of data related to wordstrobe slope (as used in Philips Mode)		
	Input Interface Mode		**All**		
	bit[4]	0	default		
		1	delay of data related to wordstrobe		
	bit[3]	0	default		
		1	invert wordstrobe		
	bit[2]	0	default		
		1	invert clock		

Table 3–7: Configuration memory cells, continued

Memory Address (hex)	Function	Mode	Reset Value (hex)	Name
D0:13D1	**Noise Generator** (Sec. 4.10.2 of Dolby Digital Licensee Information Manual Issue 3) bit[7] 0 Noise generator off 1 Noise generator on bit[6] Noise type 0 White noise 1 Band-pass shaped noise bit[5:0] 000001 L 000010 C 000100 R 001000 LS 010000 RS 100000 LFE 000000 No channel selected By combining the appropriate bits, more than one channel can output noise. The noise type can be selected between white and band-pass filtered with a maximum between 500 and 1000 Hz. The required stepping actions have to be initiated by the controller.	**All**	00000	UIC_NOISE
D0:13D2	**Center Channel Delay** (Sec. 4.10.1 of Dolby Digital Licensee Information Manual Issue 3) bit [2:0] 000 0 ms ... 101 5 ms	**Dolby Digital**	00000	UIC_C_DELAY
D0:13D3	**Left Surround Channel Delay** (Sec. 4.10.1 of Dolby Digital Licensee Information Manual Issue 3) bit[3:0] 0000 0 ms ... 1111 15 ms The surround delay for Dolby Pro Logic decoded signals must be set in the DPL 4519G.	**Dolby Digital**	00001	UIC_SL_DELAY
D0:13D4	**Right Surround Channel Delay** (Sec. 4.10.1 of Dolby Digital Licensee Information Manual Issue 3) bit[3:0] 0000 0 ms ... 1111 15 ms The surround delay for Dolby Pro Logic decoded signals must be set in the DPL 4519G.	**Dolby Digital**	00000	UIC_SR_DELAY
D0:13D5	**LFE Channel Enable** bit[0] Route LFE Channel to subwoofer output (if it exists in stream) 1 enable LFE 0 disable LFE The subwoofer output is assembled from the LFE and the other channels depending on the Output Configuration. This switch disables only content coming from the LFE.	**Dolby Digital**	00001	UIC_OUT_LFE

Table 3–7: Configuration memory cells, continued

Memory Address (hex)	Function	Mode	Reset Value (hex)	Name
D0:13D6	**Output Mode Control (Dolby Downmix)** (Section7.8 of ATSC Spec. A/52)	**Dolby Digital**	00007	UIC_OUT_MODE_CONTROL
	bit[4:3] Dual mono setting of Dolby C decoder, applicable only if Audio Coding Mode is dual mono (acmod = 0). The actual mixing depends on the number of available output channels (speakers). 00 Stereo (straight output of both channels) 01 Left Mono (channel 1) 10 Right Mono (channel 2) 11 Mixed Mono (sum of both channels)			
	bit[2:0] Listening Mode Selector Defines the number of available (desired) output channels (loudspeakers). 000 2/0 L, R Dolby Surround compatible 001 1/0 C 010 2/0 L, R 011 3/0 L, C, R 100 2/1 L, R, S 101 3/1 L, C, R, S 110 2/2 L, R, SL, SR 111 3/2 L, C, R, SL, SR			
	These downmixing options are independent of the setting of the Extra Stereo Output (D0:13DE). Undesired channels can be muted by setting the volume to zero or by muting the outputs in the DPL 4519G or MSP 44x0G, respectively. Only listening modes 1/0, and 2/0 should be used if dual mono is transmitted.			
D0:13D7	**Compression Control (Operational Modes, Dialog Normalization)** (Sec. 3.7 of Dolby Digital Licensee Information Manual Issue 3)	**Dolby Digital**	00001	UIC_COMPRESSION_CONTROL
	bit[1:0] Setting of Dolby C decoder 00 Custom Mode 0 (analog dialog normalization) 01 Custom Mode 1 (internal digital dialog normalization) 10 Line Mode 11 Compression RF out			
	The implemented dynamic range compression uses the transmitted variables dynrng, compr, and dialnorm. In Line Mode and in the Custom Modes, the dynamic compression may be scaled down by using the user-controlled high-level cut and low-level boost factors. Note that in Custom Mode 0, the effect of dynrng must be implemented in the analog part of the audio equipment. Note that in the Custom Mode downmix, an internal digital attenuation of 11 dB is applied that must be compensated externally.			

Table 3–7: Configuration memory cells, continued

Memory Address (hex)	Function Mode	Reset Value (hex)	Name
D0:13D8	**High-Level Cut Compression Scale Factor** **Dolby Digital** (Sec. 3.7 and Sec. 4.11.9 of Dolby Digital Licensee Information Manual Issue 3) bit[19:0] 00000_{hex} (full dynamic)...$7FFFF_{hex}$ (full compression) This factor scales down potential attenuation (i.e. dynamic compression) of loud portions of the audio as defined by dynrng. High-Level Cut is only used in Line Mode (except in downmix) and in the Custom Modes. **Note:** In order to prevent clipping due to the downmixing in the Custom and Line Modes, the High-Level Cut Compression Scale Factor must always be left at $7FFFF_{hex}$ when the Extra Stereo Output (D0:13DE) is used in conjunction with non-downmixed channels (D0:13D6). Please refer to section 4.5.8. of Dolby Digital Licensee Information Manual Issue 3.	7FFFF	UIC_CUT_X
D0:13D9	**Low-Level Boost Compression Boost Factor** **Dolby Digital** (Sec. 3.7 and Sec. 4.11.9 of Dolby Digital Licensee Information Manual Issue 3) bit[19:0] 00000_{hex} (full dynamic)...$7FFFF_{hex}$ (full compression) This factor scales down potential amplification (i.e. dynamic compression) of weak portions of the audio as defined by dynrng. Low-Level Boost is only used in Line Mode and in the Custom Modes.	7FFFF	UIC_BOOST_Y
D0:13DA	**Bass Management** **All** (see chapter 2.9.10.3.;Sec. 4.7 of Dolby Digital Licensee Information Manual Issue 3) bit[4:0] 0000 Direct loop-through of all six channels without channel mixing 1000 Dolby Configuration 0 1001 Dolby Configuration 1 1010 Dolby Configuration 2 1011 Dolby Alternative Configuration 2 1100 Dolby Configuration 3 (No Subwoofer Out) 1101 Dolby Configuration 3 (Subwoofer Out) 1110 DVD Configuration (Bass to L/R) 1111 DVD Configuration (Bass to Subwoofer) **Note:** If Bass Management is enabled, high processor clock must be selected (D0:13DF; bit16 = 1) The LFE-content can be disabled in D0:13D5. The output configurations can be used for all input formats. However, for MPEG and PCM-dat, only the L and R input channels will carry information.	00000	UIC_POST_ PROCESSING
D0:13DB	**no longer required: do not write to this memory address**		

Table 3–7: Configuration memory cells, continued

Memory Address (hex)	Function	Mode	Reset Value (hex)	Name
D0:13DD	**Karaoke Mode** bit[1:0] 00 no vocals 01 vocal 1 10 vocal 2 11 vocal 1 (left) + vocal 2 (right)	**Dolby Digital**	00003	UIC_KARAOKE_MODE
D0:13DE	**Extra Stereo Output (Lt/Rt or Lo/Ro)** bit[0] 0 Lt/Rt stereo output 1 Lo/Ro stereo output For headphone operation, the 2-channel output can be switched to the Lo/Ro-mode. **Note:** In order to prevent clipping due to the downmixing in the Custom and Line Modes, the High-Level Cut Compression Scale Factor (D0:13D8) must always be left at $7FFFF_{hex}$ when the Extra Stereo Output is used in conjunction with non-downmixed channels (D0:13D6).	**Dolby Digital** (surround encoded)	00000	UIC_DOWNMIX_MODE

Table 3–7: Configuration memory cells, continued

Memory Address (hex)	Function	Mode	Reset Value (hex)	Name
D0:13DF	**Output Clock Scaling** bit[19] 0 CLKO off 1 enable CLKO disable CLKO bit[18:17] Division factor applied to the internal reference clock (see Table 2–2 on page 9) for the CLKO-output 0 divide reference clock by 1 1 divide by 2 2 divide by 4 3 divide by 8 bit[16] Low/high system clock for Dolby Digital (please refer to Table 2–1 on page 9) 0 61/56/40 MHz for 48/44.1/32 kHz 1 73/67/49 MHz for 48/44.1/32 kHz Sets the processor clock and the output clock at pin CLKO. The clock frequencies are coupled to the audio data sampling rate of the input signal by a PLL. The high clock frequencies have to be used if the internal Dolby Digital Bass Management is used.	**All**	80004	UIC_OUT_CLK_SCALE
	Auxiliary Interface Control bit[6] 0 S/PDIF input select 1 select SPDI input select SPDI2 input bit[5:3] 0 reserved (set to 0) bit[2] SOC Impedance 0 low impedance 1 high impedance bit[1] Serial input select 0 select SID, SII, SIC 1 select SID*, SII*, SIC* bit[0] 0 reserved Input/output interface selections.	**All**		

Table 3–7: Configuration memory cells, continued

Memory Address (hex)	Function	Mode	Reset Value (hex)	Name
D0:13E0	**PCM/MPEG Deemphasis Control** bit[1:0] Deemphasis 00 automatic detection (only for PCM via S/PDIF and all MPEG-inputs, no deemphasis if PCM via I^2S-input is selected) 01 50/15 µs deemphasis 10 no deemphasis 11 J17 deemphasis PCM-signals coming via the serial interface do not contain embedded deemphasis information. The correct deemphasis must therefore be initiated by the controller. PCM-signals coming via the S/PDIF-interface and MPEG-data streams contain such information. In this case, the automatic detection should be enabled to achieve the correct deemphasis.	**MPEG/PCM**	00000	UIC_DEEMPHASE_CONTROL
D0:13E1 D0:13E2 D0:13E3 D0:13E4 D0:13E5 D0:13E6 D0:13E7 D0:13E8	**Volume Control** Volume left channel Volume center channel Volume right channel Volume surround left channel Volume surround right channel Volume subwoofer channel Volume stereo left channel Volume stereo right channel bit[15:8] $7F_{hex}$ +12 dB ... 73_{hex} 0 dB ... 01_{hex} –114 dB 00_{hex} mute The resolution is 1 dB/step.	**All**	07300 (all)	UIC_L_VOLUME UIC_C_VOLUME UIC_R_VOLUME UIC_SL_VOLUME UIC_SR_VOLUME UIC_LFE_VOLUME UIC_L_ST_VOLUME UIC_R_ST_VOLUME
D0:13EA	**S/PDIF Channel Status Bits Control** bit[15] L-bit (generation status) bit[14:8] category code bit[7:6] should be “0” bit[5:3] should be “0” bit[2] cp-bit (copyright protection) bit[1] should be “0” for PCM output bit[0] should be “0” for consumer use These bits control the status word in the S/PDIF output. This control is inactive if S/PDIF loop-through is selected. **Note:** It must be made sure that bits 2, 8, .., 15 are set correctly. Incorrect settings may affect the ability to make digital copies.	**All**	01904	UIC_CHANNEL_STATUS

3.6.3. Hybrid User Interface Cells

Table 3–8: Hybrid User Interface Cells

Memory Address (hex)	Function	Reset Value (hex)	Name
D0:13FF	**Message Constants** **All** **Messages** bit[19:0] 0 no error 8 all errors with an error number higher or equal to this error number cause a restart 9 S/PDIF:sync lost during look for Pa, Pb, Pc, Pd 10 S/PDIF: sync lost during operation 11 Data Stream Error (Pa not correct) 12 Data Stream Error (Pb not correct) 13 Data Stream Error (Pc not correct) 14 Data Stream Error (Pd to big) 15 I^2S timeout error 16 no input data type selected in I^2S input mode (i.e. auto-detection is ON) 17 input type over S/PDIF changed from pcm to data 18 AC-3: initial waiting time out 19 AC-3: sync waiting time out 20 AC-3: sync lost 21 AC-3: header corrupted 22 AC-3: CRC1 wait timeout 23 AC-3: CRC1 fail 24 AC-3: CRC2 wait timeout 25 AC-3: CRC2 fail 26 selected bit-stream-number not available 27 PCM recognition inconsistent, restart 28 DATA TYPE in BurstInfo not AC-3, PCM, MPEG, or DTS. 29 AC-3 - Sampling frequency changed 30 invalid exponents detected 31 S/PDIF: Input type chosen manually (not autodetected) 32 AC3: Input buffer overrun - the input pointer overwrites the actual frame 33 S/PDIF input parity error 40 MPEG: sampling frequency changed 41 MPEG no header found 42 MPEG: no Layer 2 header found 43 MPEG: restart forced 44 MPEG: not enough data to decode 45 MPEG: S/PDIF error 46 MPEG: decoding error 47 MPEG: input timeout 48 MPEG: sync error 49 MPEG: data rate too high (probably PCM input) ...	00000	UIH_LAST_ MESSAGE

Table 3–8: Hybrid User Interface Cells, continued

Memory Address (hex)	Function	Reset Value (hex)	Name
D0:13FF (continued)	[50:66] User interface messages 50 LM_USER_CHANGE 51 LM_IO_CONTROL 52 LM_NOISE 53 LM_C_DELAY 54 LM_SL_DELAY 55 LM_RL_DELAY 56 LM_OUT_LFE 57 LM_OUT_MODE_CONTROL 58 LM_COMPRESSION_CONTROL 59 LM_CUT_X 60 LM_BOOST_Y 61 LM_POST_PROCESSING 62 LM_SAMP_FREQ 63 LM_OUTN_CHANNELS 64 LM_KARAOKE_MODE 65 LM_DOWNMIX_MODE 66 LM_OUT_CLK_SCALE 70 PCM: Sampling frequency changed in PCM Mode The latest message that occurred is displayed in this cell. The controller should frequently (e.g. once per frame) check and clear this memory location. After reading the message it is recommended to clear this cell (by writing a “0”) to see whether this message occurs again.	00000	UIH_LAST_ MESSAGE

4. Specifications

4.1. Outline Dimensions

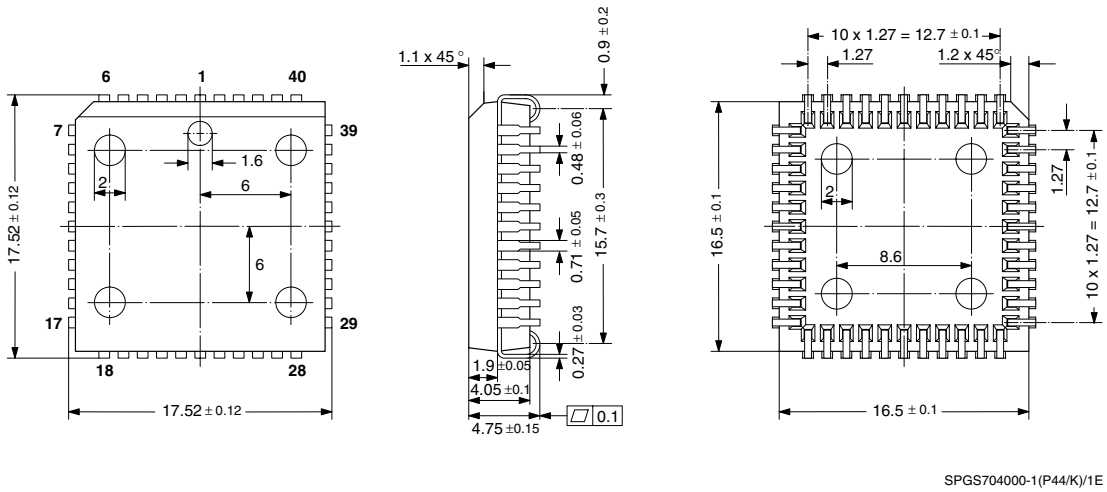

Fig. 4–1:
44-Pin Plastic Leaded Chip Carrier Package
(PLCC44K)
Weight approximately 2.5 g
Dimensions in mm

4.2. Pin Connections and Short Descriptions

NC not connected, leave vacant
LV If not used, leave vacant
X obligatory, pin must be connected as described in application information

VDD connect to positive supply
VSS connect to ground

Pin No. PLCC 44-pin	Pin Name	Type	Connection (if not used)	Short Description
1	VSS	SUPPLY	X	Ground supply for digital parts
2	VDD	SUPPLY	X	Positive supply for digital parts
3	I2CD	IN/OUT	VDD	I^2C data line
4	I2CC	IN/OUT	VDD	I^2C clock line
5	$\overline{\text{POR}}$	IN	X	Reset, active low
6	TE	IN	VSS	Test enable
7	AVSS	SUPPLY	X	Ground supply for analog circuits
8	AVDD	SUPPLY	X	Supply for analog circuits
9	XTI	IN	X	Clock input/quartz oscillator pin 1
10	XTO	OUT	LV	Quartz oscillator pin 2
11	NC		LV	
12	NC		LV	

Pin No. PLCC 44-pin	Pin Name	Type	Connection (if not used)	Short Description
13	CLKO	OUT	LV	DSP clock output for the D/A-converter
14	SOD1	OUT	LV	Serial output data 1
15	SOD2	OUT	LV	Serial output data 2
16	SOD3	OUT	LV	Serial output data 3
17	SPDIFOUT	OUT	LV	S/PDIF output
18	PI4	IN (OUT)[1)]	VSS	PIO data [4]
19	SIC	IN	VSS	Serial input clock
20	SII	IN	VSS	Serial input frame identification
21	SID	IN	VSS	Serial input data
22	XVSS	SUPPLY	X	Ground for output buffers
23	XVDD	SUPPLY	X	Positive supply for output buffers
24	PI8	IN (OUT)[1)]	VSS	PIO data [8]
25	SOC	OUT	X	Serial output clock
26	SOI	OUT	X	Serial output frame identification
27	SOD	OUT	X	Serial output data
28	PI12	IN (OUT)[1)]	VSS	PIO data [12]
29	PI13	IN (OUT)[1)]	VSS	PIO data [13]
30	SID* (PI14)	IN (OUT)[1)]	VSS	PIO data [14], SID* = alternative input for SID
31	SII* (PI15)	IN (OUT)[1)]	VSS	PIO data [15], SII* = alternative input for SII
32	SIC* (PI16)	IN (OUT)[1)]	VSS	PIO data[16], SIC* = alternative input for SIC
33	PI17	IN (OUT)[1)]	VSS	PIO data [17]
34	PI18	IN (OUT)[1)]	VSS	PIO data [18]
35	PI19	IN (OUT)[1)]	VSS	PIO data [19]
36	TP	IN	VDD	Test pin
37	TP	IN	VDD	Test pin
38	SPDI	IN	VSS	S/PDIF input 1
39	SPREF	IN	LV	S/PDIF input (reference)
40	SPDI2	IN	VSS	S/PDIF input 2
41	TP	OUT	LV	Test pin
42	TP	OUT	LV	Test pin

[1)] Pins are configured as input after reset.

Pin No. PLCC 44-pin	Pin Name	Type	Connection (if not used)	Short Description
43	TP	OUT	LV	Test pin
44	SYNC	OUT	LV	Reserved for frame synchronization

4.3. Pin Descriptions

4.3.1. Power Supply Pins

Connection of all power supply pins is mandatory for the functioning of the MAS 3528E.

VDD **SUPPLY**
VSS **SUPPLY**
The VDD/VSS pair is internally connected with all digital modules of the MAS 3528E.

XVDD **SUPPLY**
XVSS **SUPPLY**
The XVDD/XVSS pins are internally connected with the pin output buffers.

AVDD **SUPPLY**
AVSS **SUPPLY**
The AVDD/AVSS pair is connected internally with the analog blocks of the MAS 3528E, i.e. clock synthesizer and supply voltage supervision circuits.

4.3.2. Control Lines

I2CC SCL IN/OUT
I2CD SDA IN/OUT
Standard I^2C control lines.

4.3.3. General Purpose Input/Output

PI4, PI8, PI12...PI19 **IN/OUT**
General purpose input/output pins. PI14 to PI16 can be used as alternative I^2S bus inputs. Function is controlled by the registers PIO_Config, PIO_Direction, PIO_Data_Out, PIO_Data_In.

4.3.4. Clocking

XTI **IN**
This is the clock input of the MAS 3528E. The nominal clock frequency is 18.432 MHz.

XTO **IN**
This connection is needed for the quartz oscillator.

CLKO **OUT**
The CLKO is an oversupplying clock that is synchronized to the digital audio data (SOD) and the frame identification (SOI).

4.3.5. Serial Input Interface

SID **IN**
SII **IN**
SIC **IN**
Data, frame indication, and clock line of the standard I^2S (word mode) serial input interface.

PI16 SIC* **IN**
PI15 SII* **IN**
PI14 SID* **IN**
The SIC*, SID*, and SII* are alternative serial input lines. This interface can be selected in memory cell D0:13D0.

4.3.6. S/PDIF Input Interface

SPDI **IN**
SPDI2 **IN**
SPREF **IN**
Input lines (SPDI/SPDI2) and ground reference line (SPREF) of the S/PDIF-input interfaces. One of the two alternate input lines is selected by in D0:13DF.

4.3.7. S/PDIF Output Interface

SPDIFOUT **OUT**
S/PDIF-output line.

4.3.8. Serial Output Interface

SOD **OUT**
SOD1 **OUT**
SOD2 **OUT**
SOD3 **OUT**
SOI **OUT**
SOC **OUT**
Data, frame indication, and clock line of the serial output interface. The SOI indicates whether the left or the right audio sample is transmitted. Besides the two modes, it is possible to reconfigure the interface.

4.3.9. Miscellaneous

$\overline{\text{POR}}$ **IN**
The $\overline{\text{POR}}$ pin is used to reset the digital parts of the MAS 3528E. $\overline{\text{POR}}$ is a low active signal.

TE **IN**
The TE pin is for production test only and must be connected with VSS in all applications.

SYNC
The SYNC pin is set while decoding Dolby Digital or MPEG. Only during header processing, there is a short Low period (20...300 µs depending on the audio format)

4.4. Pin Configuration

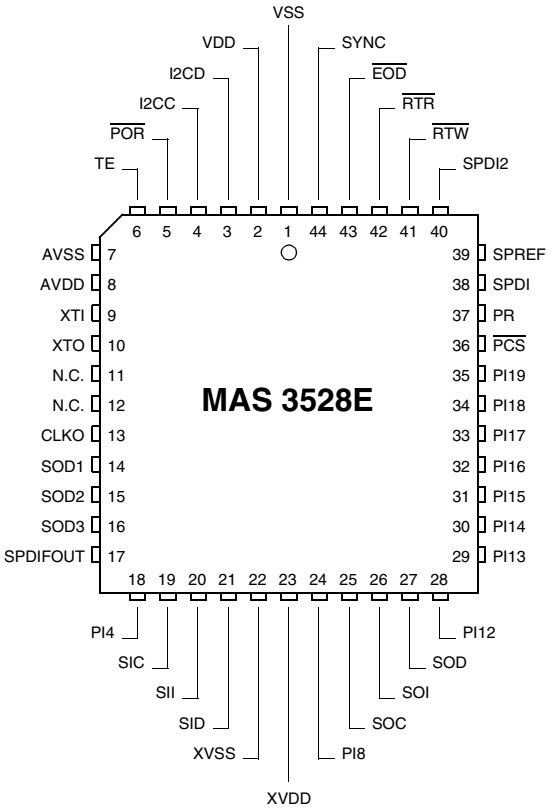

Fig. 4–2: PLCC44 package

4.5. Internal Pin Circuits

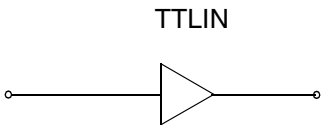

Fig. 4–3: Input pins $\overline{PCS}$, PR

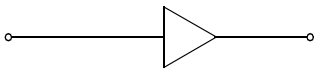

Fig. 4–4: Input pin TE

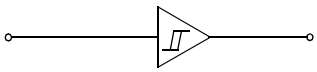

Fig. 4–5: Input pin $\overline{POR}$

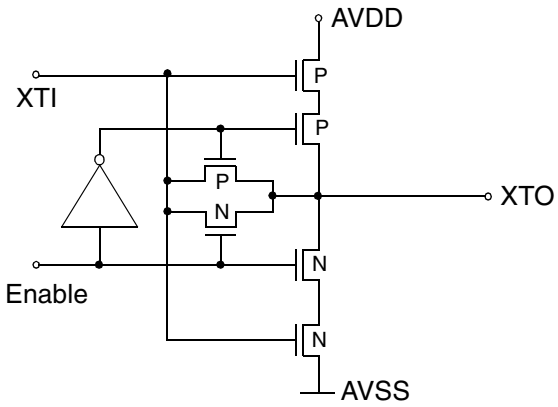

Fig. 4–6: Clock oscillator XTI, XTO

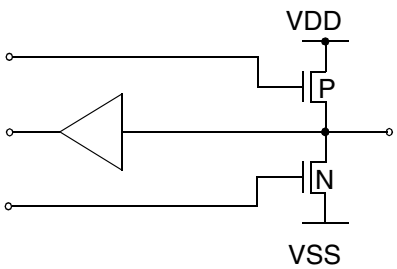

Fig. 4–7: Input/Output pins SOD1, SOD2, SOD3, SPDIFOUT, PI4, PI8, SOC, SOI, SOD, PI12...PI19

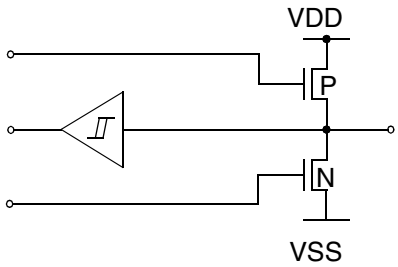

Fig. 4–8: Input/Output pins SIC, SII, SID

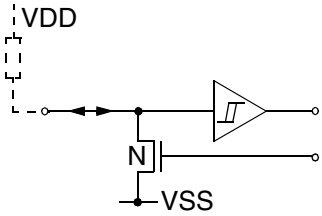

Fig. 4–9: Input/Output pins I2CC, I2CD

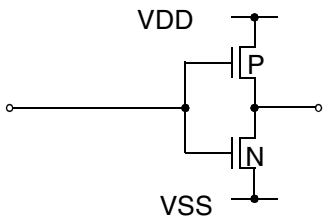

Fig. 4–10: Output pins $\overline{RTW}$, $\overline{EOD}$, $\overline{RTR}$, CLKO, SYNC

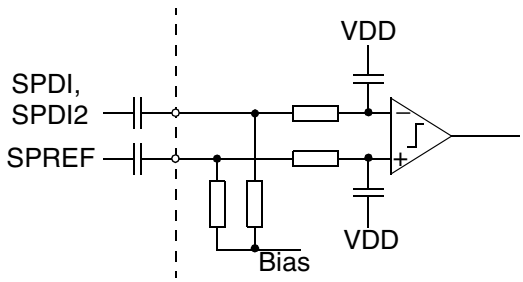

Fig. 4–11: S/PDIF Input

4.6. Electrical Characteristics

4.6.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient Operating Temperature		0	65	°C
T_C	Case Operating Temperature		0	115	°C
T_S	Storage Temperature		–40	125	°C
P_{TOT}	Power Dissipation	VDD, XVDD, AVDD		1250	mW
V_{SUPD}	Digital Supply Voltage	VDD, XVDD	–0.3	6.0	V
V_{SUPA}	Analog Supply Voltage	AVDD	–0.3	6.0	V
ΔV_{SUP}	Voltage differences between any supply region	VDD, AVDD, XVDD	–0.5	0.5	V
V_{GD}	Voltage differences between different Grounds	VSS, AVSS, XVSS	–0.5	0.5	
V_{Idig}	Input Voltage, all Digital Inputs		–0.3	V_{SUP} +0.3	V
I_{Idig}	Input Current, all Digital Inputs		–20	20	mA
Out	Current, all Digital Outputs			250	mA
	Output Load			300	pF

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

4.6.2. Recommended Operating Conditions (T_A = 0 to +65 °C)

4.6.2.1. General Recommended Operating Conditions

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
T_A	Ambient Operating Temperature		0	65	°C	
V_{SUPD}	Digital supply voltage	VDD, XVDD	4.75	5.0	5.25	V
V_{SUPA}	Analog supply voltage	AVDD	4.75	5.0	5.25	V

4.6.2.2. Reference Frequency Generation and Crystal Recommendations

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
External Clock Input Recommendations						
CLK_F	Clock frequency	XTI		18.432		MHz
CLK_{Amp}	Clock amplitude		0.7		3.5	V_{pp}
Crystal Recommendations						
T_{AC}	Ambient temperature range	XTI, XTO	–20		80	°C
f_P	Load resonance frequency at C_l = 12 pF			18.432		MHz
$\Delta f/f_S$	Accuracy of frequency adjustment		–50		50	ppm
$\Delta f/f_S$	Frequency variation vs. temperature		–50		50	ppm
R_{EQ}	Equivalent series resistance			12	30	Ω
C_0	Shunt (parallel) capacitance			3	7	pF

4.6.2.3. Input Levels at V_{DD} = 4.5 V...5.5 V

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage	POR I2CC, I2CD			0.5	V
V_{IH}	Input high voltage		2.6			V
V_{ILD}	Input low voltage	PI<i>, SII, SIC, SID, PR, TE,			0.5	V
V_{IHD}	Input high voltage		V_{SUP}× 0.5			

4.6.3. Characteristics at T_A = 0 to 65 °C, V_{DD} = 5.0 V, $f_{Crystal}$ = 18.432 MHz

4.6.3.1. General Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Supply Current							
I_{SUP}	Current consumption	all supply pins		210		mA	5.0 V, audio sampling frequency 48 kHz Dolby Digital, 61 MHz fproc
Digital Outputs and Inputs							
O_{DigL}	Output low voltage	PI<i>, SOI, SOC, SOD, SOD1, SOD2, SOD3, EOD, RTR, RTW, CLKO SPDIF-OUT			0.5	V	at I_{load} = 1 mA
O_{DigH}	Output high voltage		V_{SUP} –0.5			V	at I_{load} = 1 mA
C_{DigI}	Input capacitance	all digital Inputs			7	pF	
I_{DLeak}	Input leakage current		–1		1	µA	0 V < V_{pin} < V_{SUP}

4.6.3.2. I²C Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
R_{ON}	Output resistance	I2CC, I2CD			60	Ω	I_{load} = 5 mA, V_{DD} = 4.5 V
f_{I2C}	I²C bus frequency	I2CC			400	kHz	
t_{I2C1}	I²C START condition setup time	I2CC, I2CD	300			ns	
t_{I2C2}	I²C STOP condition setup time	I2CC, I2CD	300			ns	
t_{I2C3}	I²C clock low pulse time	I2CC	1250			ns	
t_{I2C4}	I²C clock high pulse time	I2CC	1250			ns	
t_{I2C5}	I²C data hold time before rising edge of clock	I2CC	80			ns	
t_{I2C6}	I²C data hold time after falling edge of clock	I2CC	80			ns	
V_{I2COL}	I²C output low voltage	I2CC, I2CD			0.3	V	I_{LOAD} = 5 mA
I_{I2COH}	I²C output high leakage current	I2CC, I2CD			1	µA	V_{I2CH} = 5.5 V
t_{I2COL1}	I²C data output hold time after falling edge of clock	I2CC, I2CD	20			ns	
t_{I2COL2}	I²C data output setup time before rising edge of clock	I2CC, I2CD	250			ns	f_{I2C} = 400kHz

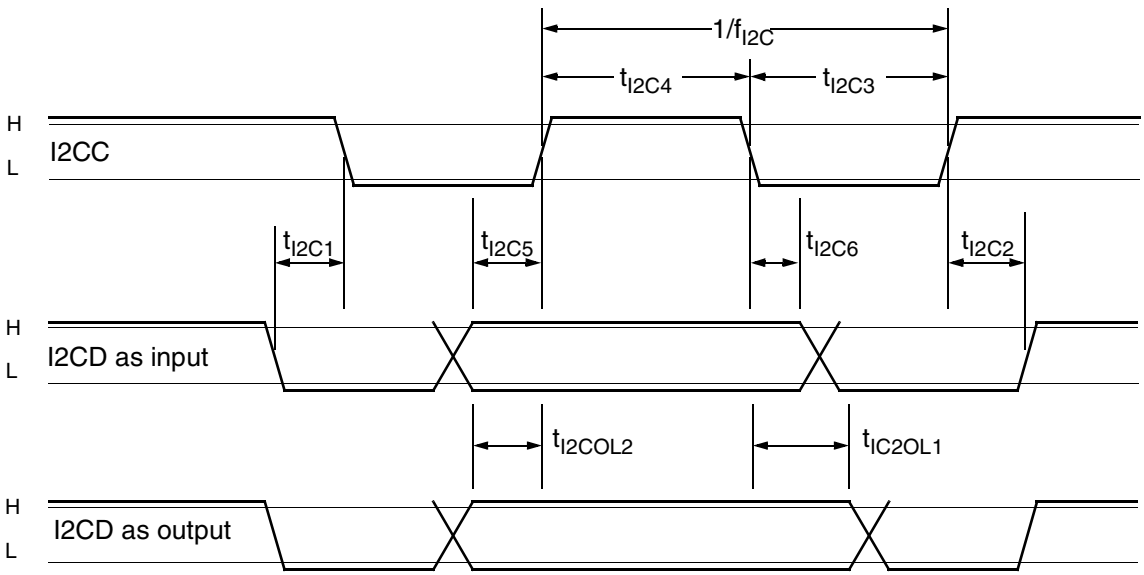

Fig. 4–12: I²C timing diagram

4.6.3.3. S/PDIF-Bus Input Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_S	Signal amplitude	SPDI, SPDI2,	200	500	1000	mV_{pp}	
f_{s1}	Biphase frequency	SPDI, SPDI2		3.072		MHz	±1000 ppm, f_s = 48 kHz
f_{s2}	Biphase frequency	SPDI, SPDI2		2.822		MHz	±1000 ppm, f_s = 44.1 kHz
f_{s3}	Biphase frequency	SPDI, SPDI2		2.048		MHz	±1000 ppm, f_s = 32 kHz
t_p	Biphase period	SPDI, SPDI2		326		ns	at f_s = 48 kHz, (highest sampling rate)
t_r	Rise time	SPDI, SPDI2	0		65	ns	at f_s = 48 kHz, (highest sampling rate)
t_f	Fall time	SPDI, SPDI2	0		65	ns	at f_s = 48 kHz, (highest sampling rate)
	Duty-cycle	SPDI, SPDI2	40	50	60	%	at “1” and f_s = 48 kHz

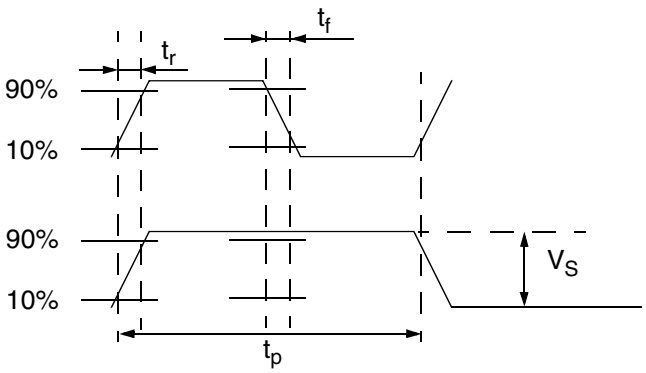

Fig. 4–13: Timing of the S/PDIF-input

4.6.3.4. S/PDIF-Bus Output Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
f_{s1}	Biphase frequency	SPDIFOUT		3.072		MHz	f_s = 48 kHz
f_{s2}	Biphase frequency	SPDIFOUT		2.822		MHz	f_s = 44.1 kHz
f_{s3}	Biphase frequency	SPDIFOUT		2.048		MHz	f_s = 32 kHz
t_p	Biphase period	SPDIFOUT		326		ns	at f_s = 48 kHz, (highest sampling rate)
t_r	Rise time	SPDIFOUT	0		2	ns	C_{load} = 10 pF
t_f	Fall time	SPDIFOUT	0		2	ns	C_{load} = 10 pF
	Duty-cycle	SPDIFOUT		50		%	at “1” and f_s = 48 kHz

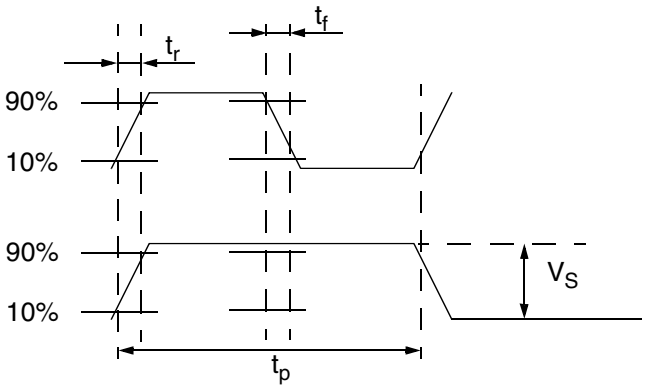

Fig. 4–14: Timing of the S/PDIF-output

4.6.3.5. I²S Bus Characteristics – Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
t_{SICLK}	I²S clock input clock period	SIC	960			ns	Burst mode, mean data rate < 150 kbit/s
t_{SIDDS}	I²S data setup time before falling edge of clock	SIC, SID	50		t_{SICLK} −100	ns	
t_{SIDDH}	I²S data hold time	SIC, SID	50			ns	
t_{SIIDS}	I²S word strobe setup time before falling(/rising) edge of clock	SIC, SII	50		t_{SICLK} −100	ns	
t_{SIIDH}	I²S word strobe hold time	SIC, SII	50			ns	
t_{bw}	Burst wait time	SIC, SID	480			ns	

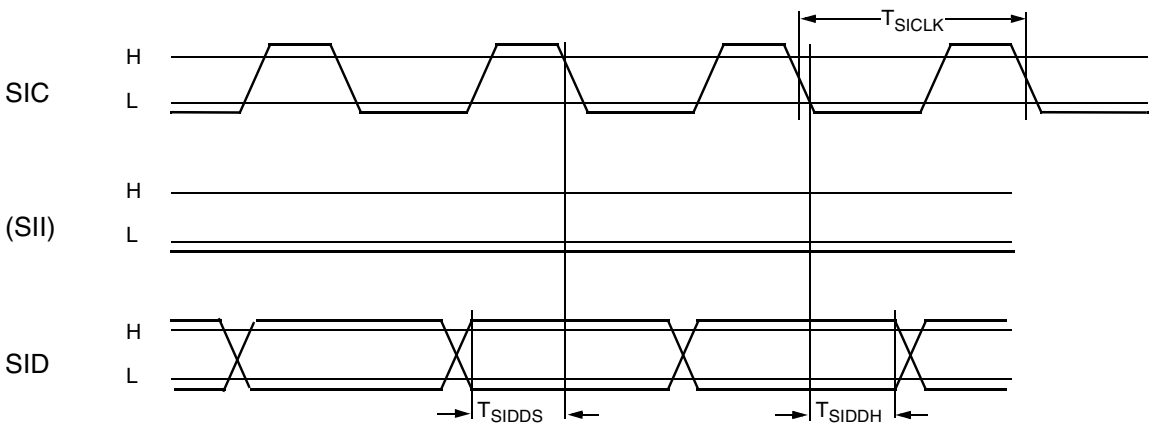

Fig. 4–15: Serial input of continuous data stream (SII must be held down). Data values are latched with falling clock per default.

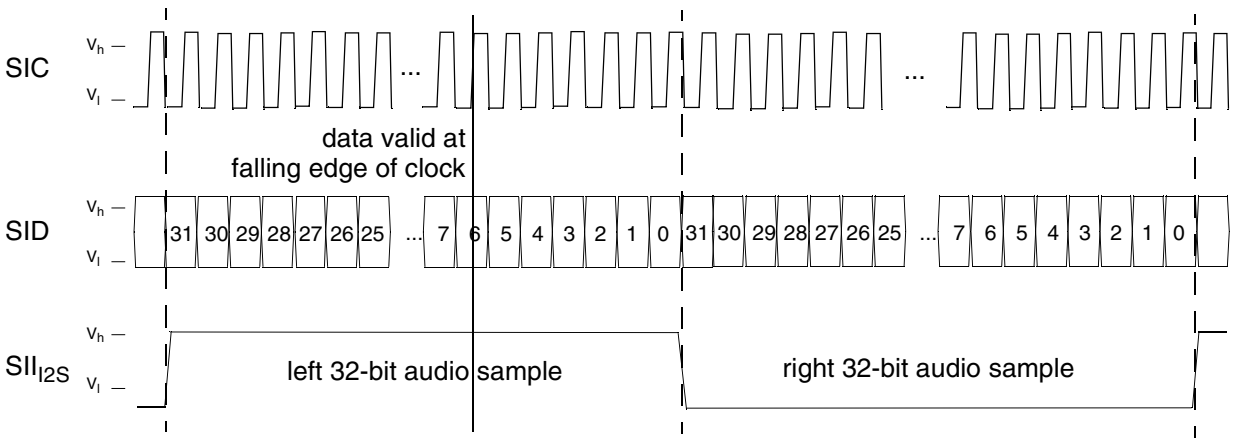

Fig. 4–16: Serial input of I²S signal (PCM). Data values are latched with rising clock per default.

4.6.3.6. I^2S Characteristics – Output

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
t_{SCLKO}	I^2S clock output frequency	SOC		325		ns	48 kHz sample rate 2×32 bits/sample
t_{SOISS}	I^2S word strobe hold time after falling edge of clock	SOC, SOI	10		t_{SCLKO} /2	ns	
t_{SOODC}	I^2S data hold time after falling edge of clock	SOC, SOD	10		t_{SCLKO} /2	ns	

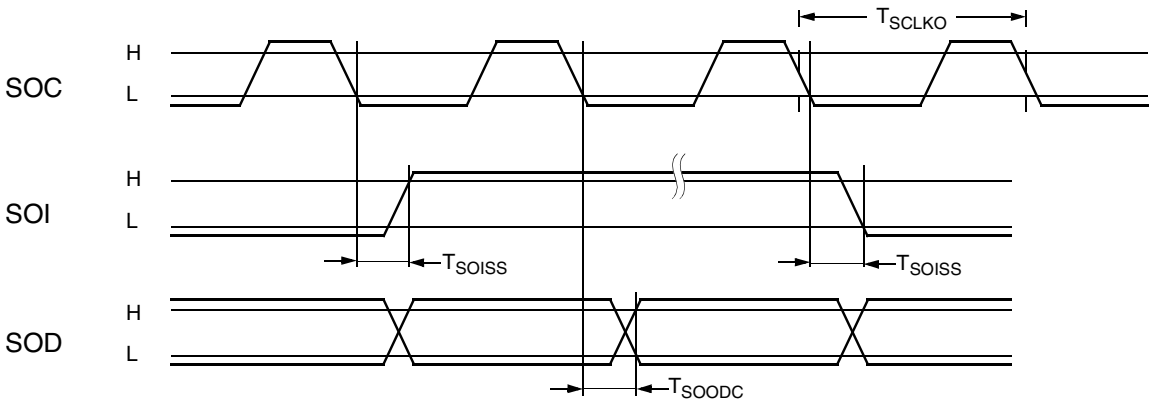

Fig. 4–17: I^2S-output. Data values are valid with rising clock per default.

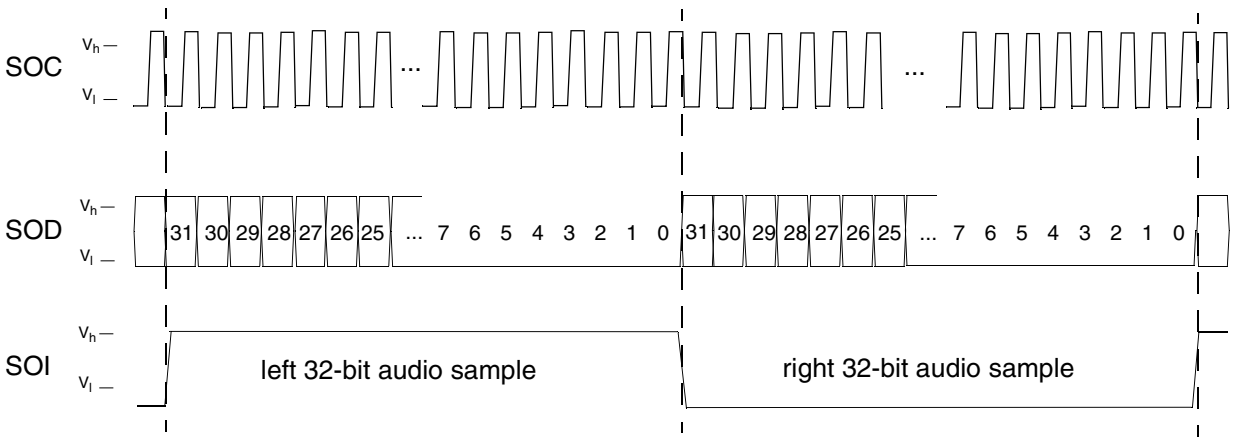

Fig. 4–18: Schematic timing of the SDO interface in 32 bit/sample mode

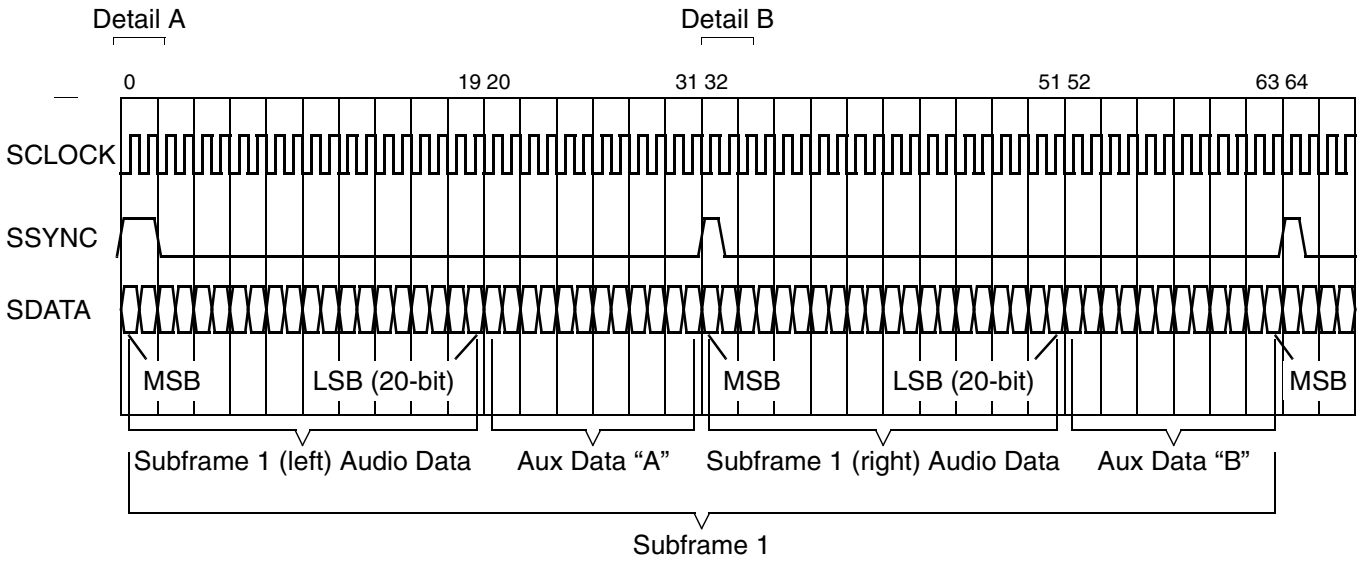

Fig. 4–19: Serial interface format for multichannel mode.

4.6.4. Firmware Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Synchronization Times for Dolby Digital Mode							
t_{DDsync}	Synchronization on Dolby Digital Bit Streams			140		ms	f_s = 48 kHz, AC-3
Synchronization Times for MPEG-Mode							
$t_{mpgsync}$	Synchronization on MPEG Bit Streams			120	48	ms	f_s = 48 kHz, MPEG
Ranges							
PLLRange	Tracking range of sampling clock recovery PLL		–200		200	ppm	

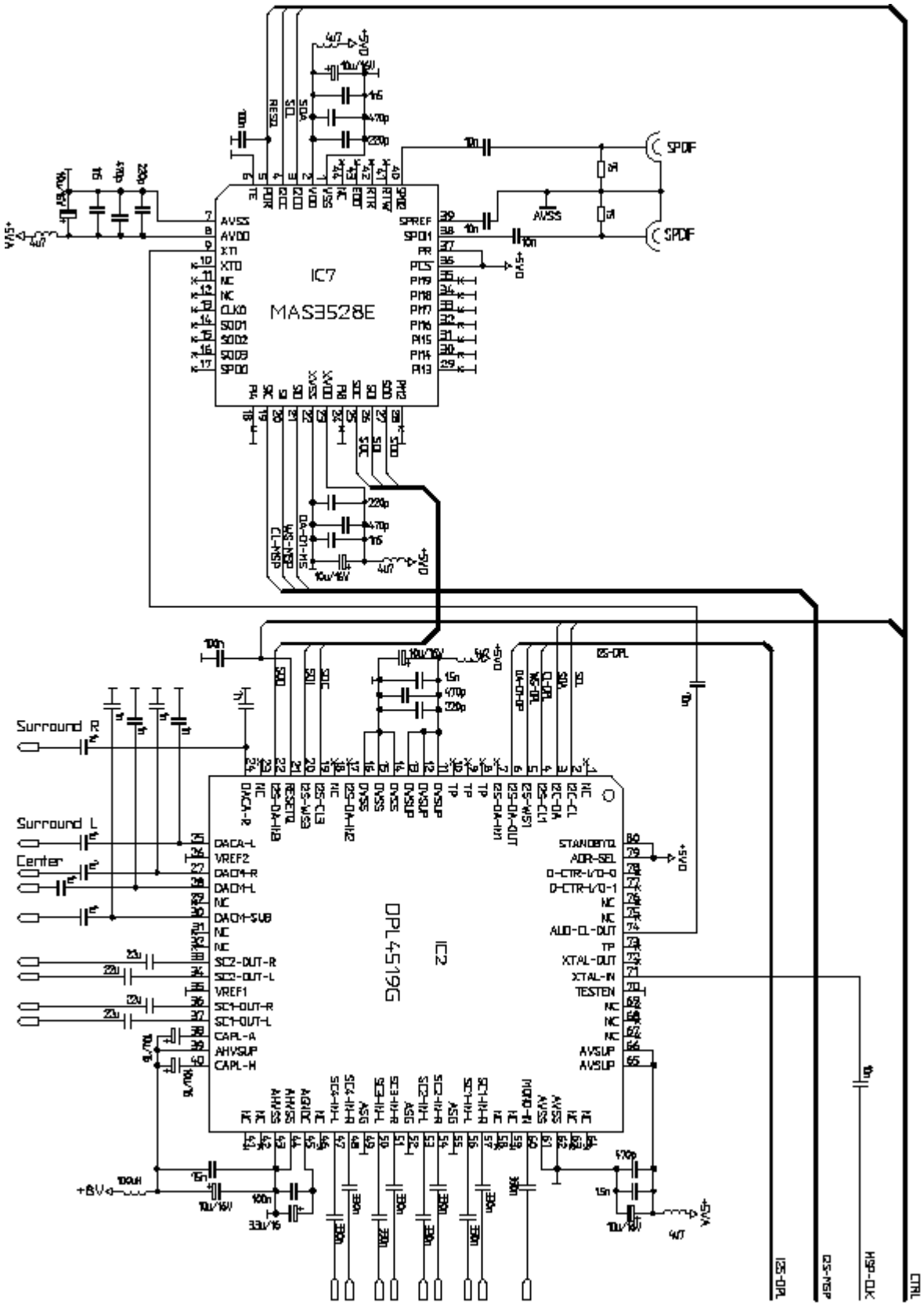

Fig. 4–20: Part 1 of the application circuit diagram. For details, please refer to the Multichannel Audio application kit.

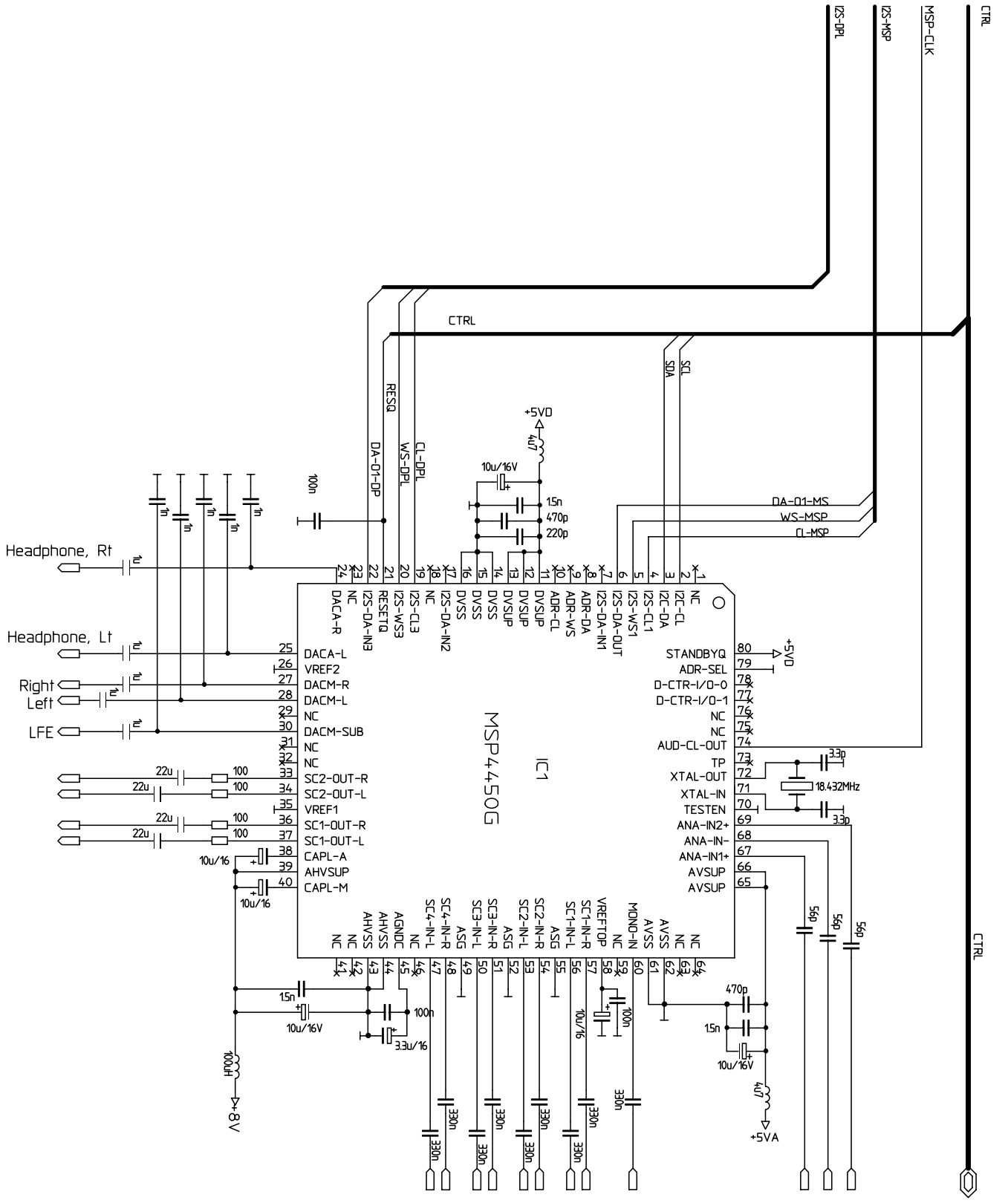

Fig. 4–21: Part 2 of the application circuit diagram. For details, please refer to the Multichannel Audio application kit.

5. Data Sheet History

1. Preliminary data sheet: “MAS 3528E Dolby Digital and MPEG-1 Layer-2 Audio Decoder”, Dec. 10, 2001, 6251-509-1PD. First release of the preliminary data sheet.

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