Preliminary Data Sheet Supplement

Subject:	Version Change
Data Sheet Concerned:	MAS 3507D 6251-459-2PD, Edition 21.10.98 MAS 3507D 6251-459-3PD, Edition 16.03.00
Supplement:	No. 6/ 6251-459-6PDS
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Description of new features and differences between version F10 and version G10 of the MAS 3507D.

Attachment:

MAS 3507D: New features and differences between version F10 and G10.

1. Introduction

This document describes new features and differences between version F10 and version G10 of the MAS 3507D, MPEG 1/2 layer 2/3 audio decoder.

1.1. New Features of Version G10

– SOC can be inverted by I^2S command

– Improved protocol for PIO-DMA

– DC converter output range extended from 2.0 V to 3.5 V

– Supply voltage range reduced to 2.5 V for low-power applications

1.1.1. SOC Output Configuration

Address	R/W	Name	Function	Default
D0:$36f	r/w	OutputConfig	Configuration of the I^2S audio output interface validate by ‘run $475’ command	

The content of this memory cell depends on the start-up configuration and will be set by the firmware. Nevertheless, the audio output interface is configurable by the software to work in different 16 bit/sample modes and 32 bit/sample modes. For adjusting to this, the following procedure has to be done:

– Choose the output mode.

– Write this value to the memory (D0:$36f).

– Send a ‘run $475’ command. With the jump to this address, the settings in the memory will become valid for the internal processing. This overrides all start-up settings

1.1.2. G10 DMA Handshake Protocol

For detailed DMA handshake protocol see preliminary data sheet MAS 3507D-3PD.

1.1.3. Extended DC/DC Converter Range

Address	R/W	Name	Function	Default
$8e	w	DCCF	Controls DC/DC operation	$08000

The DCCF register controls both the internal voltage monitor and DC/DC converter. Between the output voltage of the DC/DC converter and the internal voltage monitor threshold, an offset exists which is shown in the following table. Please pay attention to the fact, that I^2C protocol is working only if the processor works (WSEN=1). However, the setting for the DCCF register will remain active if the DCEN and WSEN lines are reset.

Table 1–1: DC Converter Output Voltages
(Bits 16...14, Bit 9 of DCCF Register)

DCCF Value (hex)[1)]	DC/DC Converter Output	Internal Voltage Monitor[2)]
1C000	3.5 V	3.3 V
18000	3.4 V	3.2 V
14000	3.3 V	3.1 V
10000	3.2 V	3.0 V
0C000	3.1 V	2.9 V
08000	3.0 V	2,8 V
04000	2.9 V	2.7 V
00000	2,8 V	2.6 V
1C200	2.7 V	2.5 V
18200	2.6 V	2.4 V
14200	2.5 V	2.3 V
10200	2.4 V	2.2 V
0C200	2.3 V	2.1 V
08200	2.2 V	2.0 V
04200	2.1 V	1.9 V
00200	2.0 V	1.8 V

1) All other bits are set to zero (f = 230 kHz)
2) PUP signal becomes inactive when output below

2. Other Technical Limitations and Changes Compared to MAS 3507D-F10

2.1. MPEG Bit Stream Interface (SDI)

The serial interface has to be initialized before the first use. Otherwise no output signal is produced. After power-up or a rising slope on pin $\overline{\text{POR}}$, write the following I^2C-command, while SIC is hold low:

W $3A 68 93 B0 00 02

(write $0020 into register $3B)

W $3A 68 00 01

(execute “RUN 1” command).

2.2. PIO-Data-Register

Changed from register address $C8 to $ED.

2.3. Memory Addresses are Shifted by $40

Changed from D0:$32D to D0:$36D (PLL Offset 48).

Changed from D0:$32E to D0:$36E (PLL Offset 44).

Changed from D0:$32F to D0:$36F (Output Config).

3. Recommended Operating Conditions

at T_A = –30 to 85 °C

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
V_{SUP}	Supply Voltage	VDD, XVDD, AVDD	2.5	2.7	3.6	V

4. Characteristics

at T_A = –30 to 85 °C

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
P_{total}	Power Consumption	VDD, XVDD, AVDD		86		mW	2.7 V, fs > 32 kHz
				46		mW	2.7 V, fs ≤ 24 kHz
				30		mW	2.7 V, fs ≤ 12 kHz