Preliminary Data Sheet Supplement

Subject:	Software Library for MAS 3507D
Documentation Concerned:	MAS 3507D 6251-459-2PD, Edition 21.10.98 MAS 3507D 6251-459-3PDS, Edition 21.07.99
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Application tips on SC4-voice codec, G723 (audible)-decoder, and PCM loop-through software modules for the MAS 3507D-D8, -F10, -G10, and -G12.

Attachment:

MAS 3507D Software Library

Contents

1. Introduction

This document provides application tips on the SC4-voice-codec, G723-(Audible)-decoder, and PCM loop-through software modules for the MAS 3507D-D8 and MAS 3507D-F10. For a quick overview, please go directly to Section 5. at the end of this document

1.1. Features for SC4

– flexibility in OFS clock

– encoder stereo-to-mono mixer

– encoder output selection compatible to PIO-DMA input pins of MAS 3507D-F10

– decoder input via PIO-DMA pins

– setting of PLL-offset possible

2. SC4 Version 247_1

2.1. Encoder: c_sc4_247_1.mob

Table 2–1: I/O-Pins

Pin[1)]	Function	Pin
SIC	I^2S-Input Clock	
SII	I^2S-Input Strobe	
SID	I^2S-Input Data	
PI0..PI3	Parallel Output Bits 0..4	PI12..PI15
PI12,PI13	Parallel Output Bits 5,6	PI16, PI17
PI17,PI18	Parallel Output Bits 7,8	PI18, PI19
PCSQ	Handshake: PIO-Chip Select, active low	
RTWQ	Handshake: PIO-Ready to Write, active low	
CLKO	OFS-Clock for A/D- or D/A-Converter[2)]	

[1)] Output pins are selectable via register 0x7B (see Table 2–2)

[2)] **Note:** The frequency at pin CLKO is either constant or scalable. This depends on the setting of the start-up configuration pin PI8 and setting of register 0x60 (see Table 2–3 and Table 2–4) (see also [1]).

Table 2–2: Selection of PIO Output Pins and Encoder Operating Mode [1)]

Value in Reg. 0x7B (Output to PI0..PI3, PI12, PI13, PI17, PI18)	Encoder Operating Mode	Value in Reg. 0x7B (Output to PI12..PI19)
0	8 kHz Stereo (default)	16
1	8 kHz Mono	17
2	11.025 kHz Stereo	18
3	11.025 kHz Mono	19
4	16 kHz Stereo	20
5	16 kHz Mono	21
6	32 kHz Mono	22

[1)] The register has to be set before start of program (RUN 0x100A) is sent to avoid click noise due to synchronization!

Table 2–3: CLKO Frequencies (Reg. 0x60 = $00000)[1)]

fs / kHz	CLKO[2)] / MHz	CLKO[3)] / MHz
32	24.576	24.576
16	12.288	24.576
11.025	5.6448	22.5792
8	6.144	24.576

[1)] CLKO is scaled with sampling rate as in version 244, but Reg. 0x60 has to be set before start of program (RUN 0x100A) is sent to avoid click noise due to synchronization!

[2)] PI8 = “0”

[3)] PI8 = “1”

Table 2–4: CLKO Frequencies[1)]

Value in Reg. 0x60	CLKO / MHz for 32, 16, 8 kHz	CLKO / MHz for 11.025 kHz
$10000	24.576	22.5792
$20000	12.288	11.2896
$40000	6.144	5.6448

1) CLKO is fixed and can be set by controller. It has to be set before start of program (RUN 0x100A) is sent to avoid click noise due to synchronization!

Table 2–5: Stereo to Mono Mapping (Reg. 0x61 write)

Value[1)]	Function
00	Stereo remains Stereo
40	L,R -> (L+R) , (L+R)
41	L,R -> (L+R)/2 , (L+R)/2
42	L,R -> (L+R)/4 , (L+R)/4

1) The register has to be set before start of program (RUN 0x100A) is sent to avoid click noise due to synchronization!

Table 2–6: I^2C-Register 0x74 (write)

Value	Function
0	32-Bit Monitor Output Mode (default)
1	16-Bit Monitor Output Mode

Note: It is strongly recommended NOT to change the above registers during recording! It will always cause click noise due to synchronization effects!

They should be set before encoding starts (send I^2C command RUN 0x100A)!

2.1.1. Input Timing

Please refer to [1]: Page 10, Fig. 2–5, Fig. 2–6, and see Figure 2–1 below.

Please note that in case of 16-bit Output Mode, no delay is activated. The time period of SII has to be the same as of SOI. Wordlengths of 8, 16, and 32 bits are supported at input.

2.1.2. Output Timing

The PIO Output Mode is used to transfer data from the MAS to an external device (microcontroller or flash) via the 8-bit parallel interface. This mode is presently used only for SC4 encoding.

Handshaking for PIO Output Mode is accomplished through the $\overline{RTW}$, $\overline{PCS}$, and PI[0:3], PI[12:13], PI[17:18] signal lines (see Fig. 2–2). The PR line has to be set to “high” level.

Please do not mix up the PIO Output Mode with the PIO-DMA Input Mode (see Section 3.)

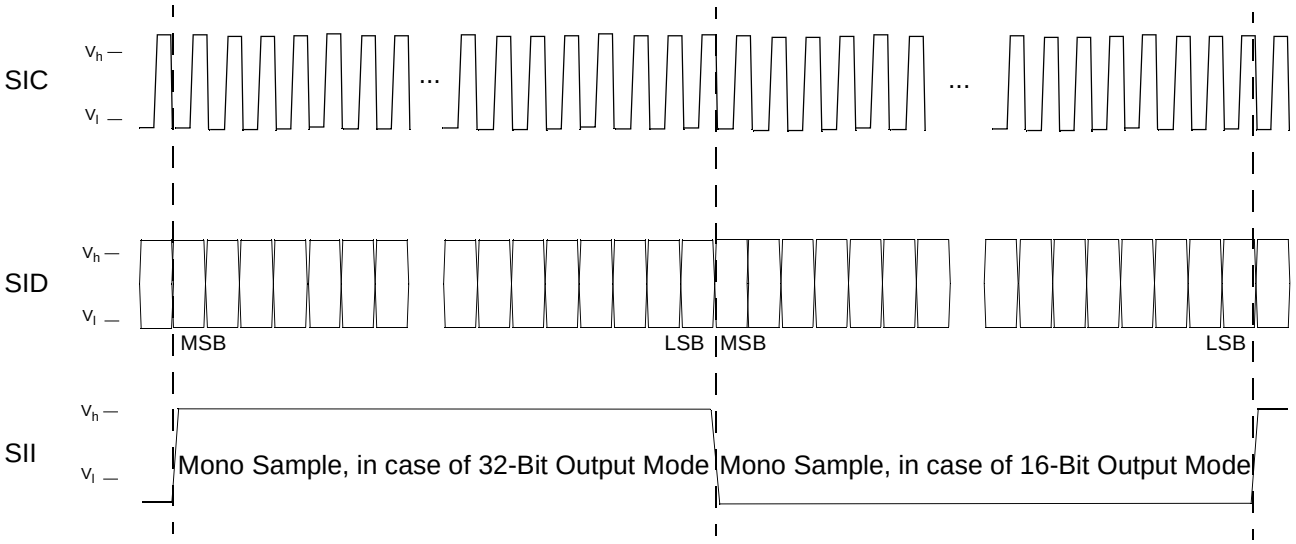

Fig. 2–1: Input timing

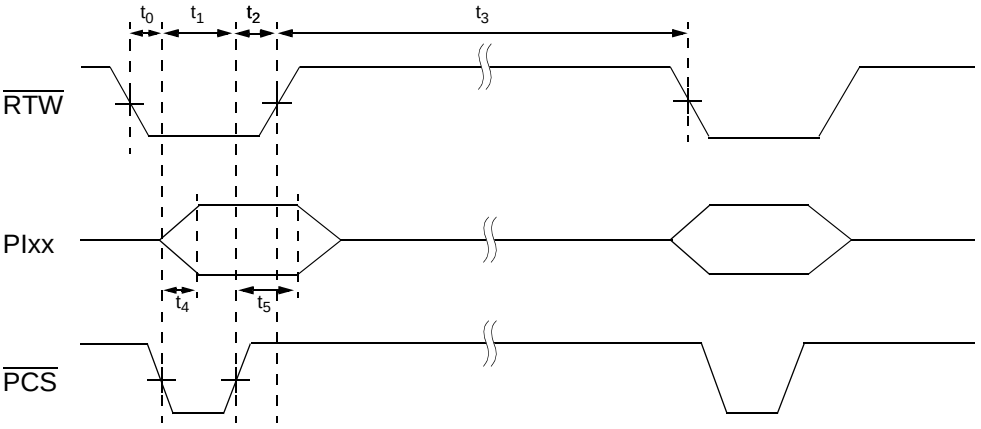

Fig. 2–2: Output timing

2.2. Pin Descriptions

$\overline{\text{RTW}}$ – Ready to Write,
is driven from MAS to indicate that data is available for output to the bus. (Output FIFO buffer is 30-35 bytes depending on header information). $\overline{\text{RTW}}$ frequency is effectively equal to the sample rate with the exception of after every 3000 bytes, 5 header bytes will be sent out during one sample period. This means that the microcontroller must be able to receive data at a rate of 5× the sample rate ($\overline{\text{PCS}} = 5 \times \overline{\text{RTW}}_{nom}$, where $\overline{\text{RTW}}_{nom}$ = sample frequency.

$\overline{\text{PCS}}$ – PIO Chip Select,
driven from microcontroller to activate data output from MAS to the bus. Data is output to the bus on the falling edge of $\overline{\text{PCS}}$ and is removed on the rising edge of $\overline{\text{PCS}}$.

PI[0:3], PI[12:13], PI[17:18] – Bidirectional Data Bus.

Table 2–7: PIO Output Mode Timing[1)]

Symbol	Pin	Min.	Max.	Unit
t_0	$\overline{\text{RTW}}$, $\overline{\text{PCS}}$	0.010	1800	µs
t_1	$\overline{\text{PCS}}$	0.330		µs
t_2	$\overline{\text{PCS}}$, $\overline{\text{RTW}}$	0.010		µs
t_3	$\overline{\text{RTW}}$	0.330	250	µs
t_4	PI	0.330		µs
t_5	PI	0.081		µs

[1)] see Figure 2–2

2.3. Handshake Description

The MAS uses a 30-byte output buffer that is filled at a rate proportional to the encoder sample rate. The fill time can be calculated by taking the number of bytes per sample (4 for stereo, 2 for mono – using 16-bit A/D), divided by the compression ratio (4:1 for SC4), multiplied by the buffer size, and divided by the sample rate.

Fill Time (16k Stereo) = 4*(1/4)*30*(1/16k) = 1.875 ms

The output buffer is increased to 35 bytes after every 3000 byte boundary to include 5 bytes of header information. $\overline{\text{RTW}}$ will go low as soon as a byte is available in the output buffer and will stay low until a byte has been read. Reading of a byte is performed with a $\overline{\text{PCS}}$ pulse. Data is latched out from the MAS on the falling edge of $\overline{\text{PCS}}$ and removed from the bus on the rising edge of $\overline{\text{PCS}}$.

2.4. A/D Interface (SDI)

The A/D interface (SDI) is a standard I^2S interface (8/16/32 bit, stereo/mono). This input is used for SC4 recording mode and must be slaved to the D/A output clock and word-strobe signals. The MAS serial input port clock sends data directly to the internal DMA data bus, so it must be disabled when recording has been completed or when the MAS is switched to playback mode. Mono inputs to the MAS must use the left input channel of the ADC. The SC4 algorithm uses the left input only and ignores any information on the right channel. Since SC4 version 247_1, it is possible to mix to L+R, (L+R)/2 or (L+R)/4.

2.5. D/A Interface

The D/A interface is a standard I^2S interface and has the option of 16 or 32-bit data words. This output is configured as an I^2S master.

2.6. Decoder: d_sc4_247_1.mob

Table 2–8: CLKO Frequencies (Register 0x60 = $00000)[1)]

fs / kHz	CLKO[2)] / MHz	CLKO[3)] / MHz
32	24.576	24.576
16	12.288	24.576
11.025	5.6448	22.5792
8	6.144	24.576

1) CLKO is scaled with sampling rate as in version 244, but register 0x60 has to be set before start of program (RUN 0x100A) is sent to avoid click noise due to synchronization! See also [1].

2) PI8 = “0”

3) PI8 = “1”

Table 2–9: CLKO Frequencies[1)]

value in Reg. 0x60	CLKO / MHz for 32, 16, 8 kHz	CLKO / MHz for 11.025 kHz
$10000	24.576	22.5792
$20000	12.288	11.2896
$40000	6.144	5.6448

1) CLKO is fixed and can be set by the controller. It has to be set before start of program (RUN 0x100A) is sent to avoid click noise due to synchronization!

Table 2–10: I²C-Register 0x74 (write)

Value	Function
0	32 Bit Output Mode (default)
1	16 Bit Output Mode

Note: It is strongly recommended NOT to change the above registers during recording! It will always cause click noise due to synchronization effects!

They should be set before encoding starts (send I²C command RUN 0x100A)!

2.6.1. Input Timing

Please refer to page 41, Section 4.6.3.2, Fig. 4–15 and Section 4.6.4.1, Fig. 4–17 in [1].

2.6.2. Output Timing

Please refer to page 10, Fig. 2–4, 2–5, 2–6 and page 42, Section 4.6.3.3, Fig. 4–16 in [1].

2.7. Decoder: dpio_sc4_247_1.mob

Table 2–11: I/O Pins[1)]

Pin	Function
PI12..PI19	Decoder Data Input
$\overline{EOD}$	PIO END of DMA, active low
PR	PIO-DMA Request
$\overline{RTR}$	PIO Ready to Read, active low
CLKO	OFS-Clock for A/D- or D/A-Converter[2)]

1) Input timing is almost the same as in PIO-DMA mode for MP3 firmware (see [2])

2) **Note:** The frequency at pin CLKO is either constant or scalable. This depends on the setting of the startup configuration pin PI8 and setting of register 0x60 (see Table 2–3 and Table 2–4).

2.7.1. Input Timing

see Section 3.

2.7.2. Output Timing

see Section 2.6.2.

3. PIO DMA Input Mode (since MAS 3507D-F10)

By setting the PIO pin PI4 or the corresponding bit of the startup configuration register during reset, the PIO DMA input mode of the MAS is activated.

The following table shows the necessary change in Table 2–3, Start-up Configuration, of [1].

Table 3–1: New PI4 Start-up configuration

PIO Pin	"0"	"1"
PI4	SDI mode	PIO DMA input mode

Please note that the meaning of PI4 during reset has completely changed. Therefore, it is no longer possible to switch the input clock to other frequencies than 14.725 MHz via the PIO-pin PI4. However, it is possible to use other clock frequencies than 14.725 MHz by setting the configuration memory as described in Section 3. Due to this, the definition during start-up of PI4 in Section 4.2, Pin Connections and Short Descriptions, has also changed as described above. Furthermore, Table 3–15 and its describing text are obsolete.

Normally, the input mode should not be altered in a customer's application. Should this nonetheless be desired, the necessary changes are described in Table 3–2 and Table 3–3.

Table 3–2: Switching from SDI- to PIO-DMA-Input

Address [1)]	Value
$e6, Bit 4	1
[1)] Startup Configuration Register	

Table 3–3: Switching from PIO-DMA- to SDI-Input

Step	Address [1)]	Value
1	$e6, Bit 4	0
2	$4b	$82
[1)] PIO Configuration Register **Note: These 2 steps must be done in above order!**		

3.1. Writing SC4 Data to the PIO-DMA

The PIO-DMA mode enables the writing of 8-bit parallel SC4[1)] data to the MAS. In this mode, PIO lines PI19...PI12 are switched to the MAS data input which hence will be an 8-bit parallel input port with MSB first (at position PI19) for the SC4 bit stream data. In order to successfully write data to this parallel port, a special handshake protocol has to be used by the controller.

Note: Either SII has to be set to "1" or SIC clock input has to be stopped ("0") in this mode.

3.2. DMA Handshake Protocol

For detailed DMA handshake protocol see:

– Preliminary data sheet supplement MAS 3507D-3PDS for version F10.

– Preliminary data sheet MAS 3507D-3PD for versions G10 and G12.

[1)] **Note:** This also applies to G723 (Audible) in all following sections!

4. Adjustment of PLLOffset

1. This version adjusts processor clock according to PLLOffset values [1]. This enables use of crystal with a non-standard frequency other than 14.725 MHz. According to [1], there are two different values that have to be set to ensure proper work of internal software. These values are PLLOffset48 (for sampling frequences which use 48 kHz as a base frequency) and PLLOffset44 (for sampling frequences which use 44 kHz as a base frequency). Formulas and description can be found in [1].

4.1. Encoder: c_sc4_247_1.mob

PLLOffset48 should be written to memory location D0:$32d, and PLLOffset44 should be written to memory location D0:$32e. Writing into these memory cells has to be done after setting bit 5 in Startup Config register (for MAS3507D-F10, [2]) and prior to downloading the code.

Procedure should look like following:

- set bit 5 in Startup Config
- write PLLOffset48 to D0:$32d
- write PLLOffset44 to D0:$32e
- download the code
- run $100a

4.2. Decoder: d_sc4_247_1.mob & dpio_sc4_247_1.mob

PLLOffset48 should be written to register $fa, and PLLOffset44 should be written to register $fb. Writing into these registers has to be done prior to downloading the code.

Procedure should look like following:

- set bit 5 in Startup Config
- write PLLOffset48 to register $fa
- write PLLOffset44 to register $fb
- download the code
- run $100a

4.3. Example of I²C command listing of Micronas MAS3507D Win95 Application Program

1. Read the PLLOffset44 (Address : D0:0x32e):

W $3A 68 E0 00 00 01 03 2E

R $3B 69 23 19 0F FA

2. Read the PLLOffset48 (Address : D0:0x32d):

W $3A 68 E0 00 00 01 03 2D

R $3B 69 D0 DE 00 02

3. Read Startup-Config Register (Address : 0xE6):

W $3A 68 DE 60

R $3B 69 00 00 00 00

4. Set the BIT 5 in Startup-Config Register and write it back

W $3A 68 9E 60 00 02

5. Write back PLLOffset44:

W $3A 68 A0 00 00 01 03 2E 23 19 00 0A

6. Write back PLLOffset48:

W $3A 68 A0 00 00 01 03 2D D0 DE 00 02

7. Write PLLOffset44 direct to register (Address 0xfb):

W $3A 68 9F B9 A2 31

8. Write PLLOffset48 direct to register (Address 0xfa):

W $3A 68 9F AE 2D 0D

9. Mute MASD (register 0xAA = 0x01):

W $3A 68 9A A1 00 00

10. Freeze MASD (Run 0):

W $3A 68 00 00

11. Stop DMA's:

Register 0x3B = 0x318:

W $3A 68 93 B8 00 31

Register 0xC3 = 0x300:

W $3A 68 9C 30 00 30

Register 0xBB = 0x318:

W $3A 68 9B B8 00 31

Register 0x43 = 0x300:

W $3A 68 94 30 00 30

Register 0x4B = 0:

W $3A 68 94 B0 00 00

Download *.MOB file

After download of encoder, the following commands are sent:

12. Set the default values for:

Sample Rate, Register 0x7b = value:

W $3A 68 97 B0 00 00

Output Bit Length, Register 0x74 = value:

W $3A 68 97 40 00 00

Stereo/Mono Mapping, Register 0x61 = value:

W $3A 68 96 10 00 04

OCLK Frequency, Register 0x60 = value:

W $3A 68 96 00 00 00

13. Run $0x100A:

W $3A 68 10 0A

5. Summary of Software Libraries

Table 5–1: MAS 3507D: Data input/output pins, acc. to IC-version / SW-module

SW-module & I/O	MAS-D8	MAS-F10, -G10, -G12[1)]	Condition/Remark for MAS-F10, -G10[2)], -G12
(MP3 Firmware) decoder input	SDI – –	SDI SDI* PInew[3)]	PI4 = 0(start up) PI4 = 0(start up), Reg$4f = 1 PI4 = 1(start up), SCL = low
(MP3 Firmware) PCM output	SDO	SDO	Reg$C5, $C6=0
(c/d_sc4_247_1) en/decoder input	SDI	SDI	PI4 = 0(start up)
(dpio_sc4_247_1) decoder input	–	PInew	PI4 = 1(start up)
(c_sc4_247_1) encoder output[4)]	PIold PInew	PIold PInew	Reg$7B = 0~6 ($01~06) Reg$7B = 16~22 ($11~16)
(d_g723_101) decoder input	–	PInew	PI4 = 1(start up)
(wav_io) PCM loop-through input	SDI	SDI	PI4 = 0(start up)
(wav_io) PCM loop-through output	SDO	SDO	Reg$C5, $C6=0

[1)] To be compatible between D8 and F10, please set register $E6, bit 5 = 1 by I^2C before downloading!

[2)] I^2S init = write $0020 to register $3B, execute ”RUN1”

[3)] PInew = PI12~PI19

[4)] PIO Output Mode used

6. References

[1]

Micronas GmbH,
MAS 3507D MPEG 1/2 Layer 2/3 Audio Decoder,
Preliminary Data Sheet, 625-459-2PD, Oct. 21, 1998

[2]

Micronas GmbH,
MAS 3507D MPEG 1/2 Layer 2/3 Audio Decoder: “New Version F10”, Preliminary Data Sheet Supplement: 625-459-3PDS, July 21, 1999

7. Version History

Version 1.2
Version 247 completed, Version 244 to be phased out

Version 1.3
Version 247_1 introduced, Version 244 deleted

Version 1.4
Version 247_1 completed