Preliminary Data Sheet Supplement

Subject:	New Version F10
Data Sheet Concerned:	MAS 3507D 6251-459-2PD, Edition Oct. 21, 1998
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Description of new features, bugfixes, and incompatibilities between version D8 and version F10 of the MAS 3507D.

Attachment:

MAS 3507D: New Version F10

Contents

1. Introduction

This document describes new features, bugfixes, and some incompatibilities between version D8 and version F10 of the MAS 3507D, MPEG 1/2 layer 2/3 audio decoder. References to the MAS 3507D Preliminary Data Sheet are indicated with “[1]”.

2. New Features

– 8-bit parallel input in PIO-DMA mode (see Section 2.1.)

– ability to use the alternative serial input (SDI*) in the SDI mode without an additional multiplexer (see Section 2.2.)

– reduced input start-up voltage (0.9 V) of the DC/DC converter (see Section 2.3.).

2.1. PIO-DMA Input Mode

By setting the PIO pin PI4 to “1”, the PIO-DMA input mode of the MAS is activated after reset.

The following table shows the necessary change in [1]: Table 2–3, Start-up Configuration. Please refer also to Section 8. in this document.

Table 2–1: New PI4 Start-up Configuration

PIO Pin	“**0**”	“**1**”
PI4	SDI mode	PIO-DMA input mode

Please note that the function of PI4 for start-up configuration has completely changed. It is no longer possible to switch the input clock to other frequencies than 14.725 MHz via the PIO-pin. However, it is possible to use other clock frequencies by applying settings to the Configuration Memory as described in Section 5.2.
Due to this, the definition during start-up of PI4 in [1]: Section 4.2. and 4.3., has also changed as described above. Furthermore, [1]: Table 3–15 is now obsolete.

Normally, the input mode should not be altered in a customer’s application. Should this nonetheless be desired, the necessary changes are described in Table 2–2 and Table 2–3.

2.1.1. Writing MPEG Data to the PIO-DMA

The PIO-DMA mode enables the writing of 8-bit parallel MPEG data to the MAS. In this mode, PIO lines PI19...PI12 are switched to the MAS data input which hence will be an 8-bit parallel input port with MSB first (at position PI19) for the MPEG bit stream data. In order to write data to this parallel port successfully, a special handshake protocol has to be used by the controller (see Fig. 2–1).

Note: Either SII has to be set to “1”, or SIC clock input has to be stopped (“0”) in this mode.

2.1.2. DMA Handshake Protocol

The data transfer can be started after the **$\overline{\text{EOD}}$** pin of the MAS is set to “high”. After verifying this, the controller indicates the transmission of data by activating the **PR** line. The MAS responds by setting the **$\overline{\text{RTR}}$** line to the “low” level. The MAS reads the data **PI[19:12]** t_{pd} ns after rising edge of the **PR**. The next data word write operation will again be initialized by setting the **PR** line via the controller. Please refer to Figure 2–1 and Table 2–4 for the exact timing.

Table 2–2: Switching from SDI- to PIO-DMA-Input

Address [1)]	Value
$e6, Bit 4	1
[1)] Startup Configuration Register	

Table 2–3: Switching from PIO-DMA- to SDI-Input

Step	Address [1)]	Value
1	$e6, Bit 4	0
2	$4b	$82
[1)] PIO Configuration Register **Note: These 2 steps must be done in above order!**		

2.1.3. End of DMA Transfer

The aforementioned procedure will be repeated until the MAS sets the **EOD** signal to “0”, which indicates that the transfer of one data block has been executed. Subsequently, the controller should set **PR** to “0”, wait until **EOD** rises again, and then repeat the procedure (see Section 2.1.2.) to send the next block of data. In the current version of the MAS 3507D, the DMA buffer is 15 bytes long. The last data byte of the DMA transfer (byte 16) will not be read in by the MAS 3507D (no **RTR** pulse). In that case, the controller should again send byte 16 in the next DMA transfer.

2.1.4. Known Difficulties of the DMA Transfer

If the controller writes the data to the MAS slowly, it is possible that the MAS 3507D reads Byte 15 and restarts the new DMA transfer before the controller generates the 16th rising edge on the **PR** line. In this case, the **EOD** line will not switch to the “low” level at all; the 16th **PR** pulse and byte 16 will become a byte 1 of the new DMA transfer. This situation could produce glitches on the **EOD** and **RTR** lines which could be impossible for the controller to detect. This may result in losing one byte or receiving the same byte twice. To avoid this situation, it is necessary to ensure that t_{p16} is shorter than 3.5 µs. This problem will be fixed in the next version of the MAS 3507D.

If the timing condition t_{p16} cannot be met, an appropriate hardware solution is described in the following section.

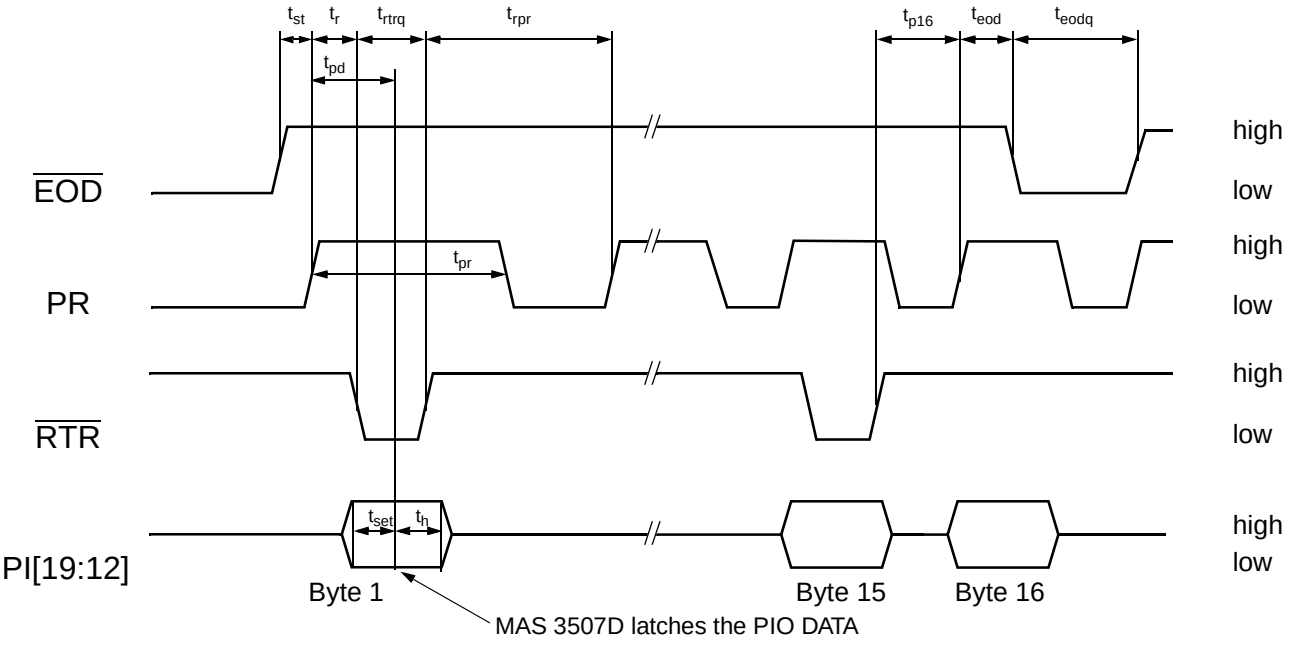


Fig. 2–1: Handshake protocol for writing MPEG data to the PIO-DMA

2.1.5. Hardware Workaround for the DMA Transfer

To generate the fast 15th and 16th **PR** pulse, external hardware can be used (see Fig. 2–2). The MUX is a multiplexer with 2 inputs (A1, B1), output control signal (PR15), and the output signal (Y1). The **PR**c input signal is the **PR** signal generated by the controller. **$\overline{\text{RTR}}$** is the MAS 3507D signal. The output of the multiplexer Y1 should be connected to the **PR** input of the MAS 3507D. During the first 14 **PR** pulses, the **PR**c signal will be sent to the MAS 3507D **PR** input. To generate the 15th and 16th **PR** pulse, the controller should switch the input from A1 to B1 using the PR15 signal. This will connect the MAS 3507D **$\overline{\text{RTR}}$** pin to the **PR** pin. The **PR** pin will go to the "high" level. The MAS 3507D will latch the PIO data and it will respond by pulling the **$\overline{\text{RTR}}$** pin down. The rising edge of the **$\overline{\text{RTR}}$** signal will generate the 16th **PR** rising edge and the MAS 3507D will finish the DMA transfer by setting the **$\overline{\text{EOD}}$** pin to the "low" level. The controller can now switch the MUX back to the **PR**c input.

The recommended PIO-DMA conditions and the characteristics of the PIO timing are given in Table 2–4.

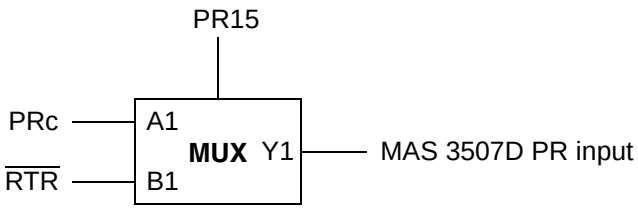


Fig. 2–2: Hardware workaround for the PIO-DMA input mode

Table 2–4: PIO-DMA Timing

Symbol	PIO Pin	Min.	Max.	Unit
t_{st}	PR, $\overline{\text{EOD}}$	0.010	2000	µs
t_r	PR, $\overline{\text{RTR}}$	40	160	ns
t_{pd}	PR, PI[19:12]	120	480	ns
t_{set}	PI[19:12]	160	no limit	ns
t_h	PI[19:12]	160	no limit	ns
t_{rtrq}	$\overline{\text{RTR}}$	200	30000	ns
t_{pr}	PR	120	no limit	ns
t_{rpr}	PR, $\overline{\text{RTR}}$	40	no limit	ns
t_{p16}	PR, $\overline{\text{RTR}}$	40	3500	ns
t_{eod}	PR, $\overline{\text{EOD}}$	40	160	ns
t_{eodq}	$\overline{\text{EOD}}$	0[1)]	500	µs
[1)] see Section 2.1.4.				

2.2. SDI* Selection

If selected, the alternative serial input (SDI*) now also behaves like an input without the necessity to apply an additional multiplexer. The alternative serial input can be selected by setting register SI1M0 at address $4f (see Table 2–5).

For further information, please refer to in [1]: Section 4.3.4.2., PIO data lines.

Table 2–5: SDI* Selection via Register SI1M0, $4f (write)

Value	Function
0	use SDI lines
2	use PI14...PI16 lines for serial input (named SDI*)

2.3. DC/DC Converter

The DC/DC converter operates at a minimum input voltage of 0.9 V. In case WSEN is active, the MAS is in the DSP operation mode. The start-up script should be as follows:

1. set DCEN to > 0.9 V
2. hold until controller operates, detects if PUP is high, and sets WSEN to “high”.

Please also refer to Figure 2–3 and Figure 2–4 where the latter is the replacement of Figure 4-18 in [1].

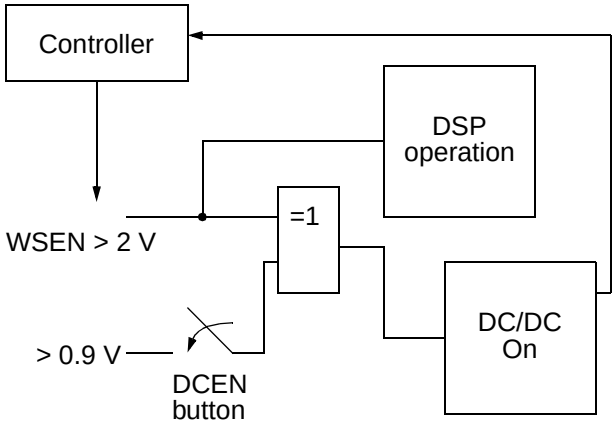


Fig. 2–3: DC/DC operation

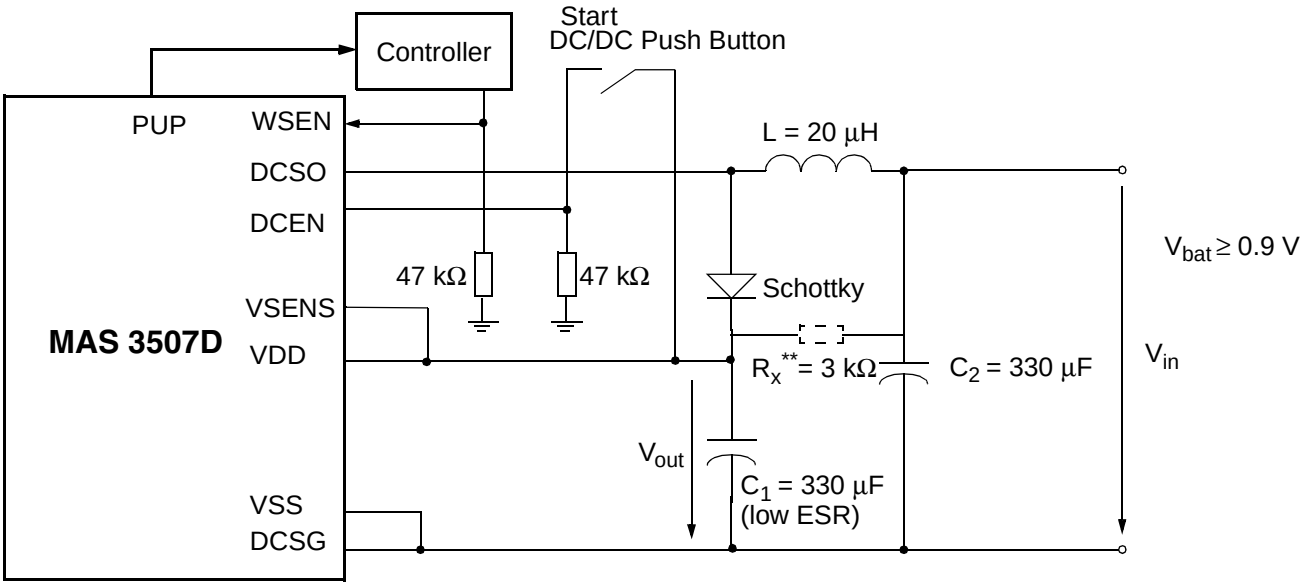


Fig. 2–4: External circuitry for the DC/DC converter**

* *R_x is proposed, if fast ON/OFF cycles of the DC/DC converter are needed. It discharges C1 in OFF-mode and has small impact on the efficiency in ON-mode.

3. Bugfixes

3.1. 8-kbps MPEG2 Synchronization Bugfix

The bug, which occurred during synchronization on an 8-kbps MPEG2 data bit stream, has now been fixed. Please note that the MPEG2 8-kbps case is a combination which is not really useful in terms of music quality.

3.2. Bass/Treble and Mute

The mute function works properly together with the bass/treble function switched on.

4. Documentation Change and Update

4.1. Command Register

In [1]: Table 3–6 on page 18, the address of the PIO data register (i.e. $c8) is not correct. Instead, in order to get the right information of the PIO pin levels (except for PI19, Demand Pin), register $ed should be read and evaluated. However, the Demand Pin PI19 is shadowed in bit 19 of register $c8.

4.2. Layer 1 Not Supported

This change applies to [1]: Table 3-10, MPEG Status 1, on page 23. Layer 1 is not supported.

4.3. Version Number

Table 4–1 shows where the MAS hardware version, its software and additional information is located.

Table 4–1: MAS Version

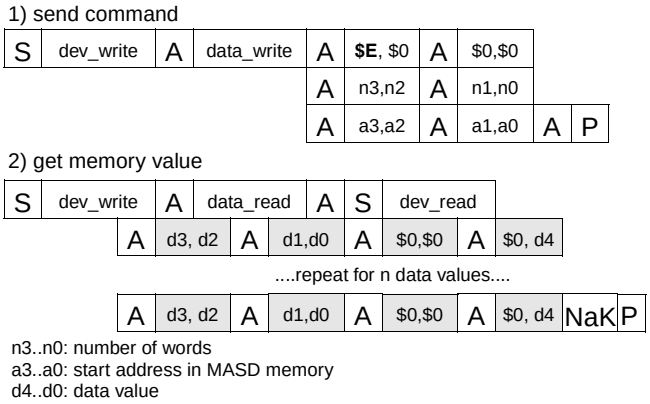
Addr.	Content	Example Value	
D1:$ff6	name of MAS version	0x03507	3507
D1:$ff7	hardware/software design code	0x00601 (increases for new versions)	0601
D1:$ff8	date of tape	0x17029	17.02 .99
D1:$ff9	description: “MPEG 1/2.5 L23”	0x04d50	MP
D1:$ffa		0x04547	EG
D1:$ffb		0x02031	1
D1:$ffc		0x02f32	/2
D1:$ffd		0x02e35	.5
D1:$ffe		0x0204C	L
D1:$fff		0x03233	23

4.4. Reference to Start-up Configuration Table

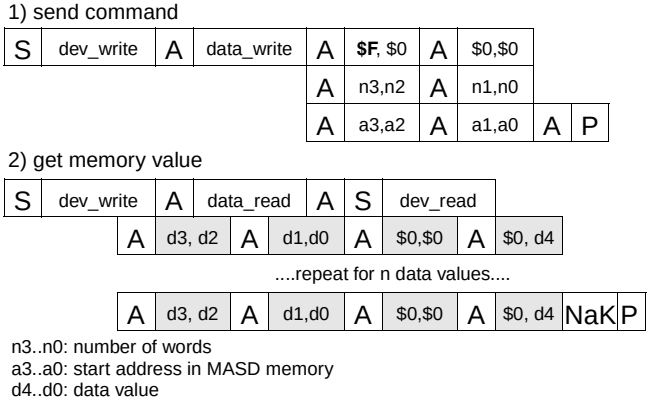
In [1]: Section 4.3.4.2. on page 35 the Start-up configuration table is referenced by [1]: Section 3.4 which is not correct. The correct reference is [1]: Section 2.7.4. on page 11.

4.5. I²C Register

4.5.1. Read D0 Memory



4.5.2. Read D1 Memory



5. Incompatibilities Versus Version D8

5.1. Software Download

Before downloading application software to the MAS, bit 5 of the start-up configuration register (StartupConfig) has to be set to “1” in order to enable the proper operation of the MAS download feature (see Table 5–1). This is due to a change in the internal memory access routine which was necessary to keep the memory access compatible to previous versions. Before resetting to MP3 mode again, bit 5 of StartupConfig has to be cleared in order to allow proper access to the MAS memory via I^2C.

Table 5–1: New Bit 5 in StartupConfig

Bit	“**0**”	“**1**”
5	Software Download disabled	Software Download enabled

5.2. Configuration Memory

The following applies to the Configuration Memory cells:

D0:$32d PLLOffset48
D0:$32e PLLOffset44
D0:$32f OutputConfig

run $475 instead of **run $fcb**.

Note! This applies only to MAS 3507D–F10.

5.3. Access for Trailing Bits at SDO Data Lines in 32-Bit Mode

The 12 trailing bits for left and right channel of the SDO interface can now be accessed by writing to registers.

Table 5–2: Access for Trailing Bits

Register	**Bit 0 ... 11**
$c5	Left Channel
$c6	Right Channel

It is highly recommended to set these bits to “0”, once after power-on reset, in order to avoid clicking during synchronization and desynchronization to an MPEG bit stream.

5.4. MPEG Status Information

Please note that the MPEG status information at pins PI0...PI8 is not available in PIO-DMA mode.

6. Recommended Operating Conditions

Table 6–1: Recommended Operating Conditions (at T_A = 0 to 70 °C)

Symbol	Parameter	Pin	Min.	Typ.	Max.	Unit
V_{SUP}	Supply Voltage	VDD, XVDD	2.6	3.0	3.3	V
V_{SUP}	Supply Voltage	AVDD	2.85	3.0	3.3	V
D_{VSUP}	Supply Voltage Difference	VDD, XVDD, AVDD	–	–	0.5	V

7. Characteristics

Table 7–1: Characteristics (at T_A = 0 to 70 °C)

Symbol	Parameter	Pin	Min.	Typ.	Max.	Unit
P_{total}	Power Consumption	VDD, XVDD AVDD		86 (2.7 V, fs=44.1 kHz) (2.85 V)		mW

8. Pin Connections and Short Descriptions

NC not connected, leave vacant
LV If not used, leave vacant
X obligatory, pin must be connected as described in application information

VDD connect to positive supply
VSS connect to ground

Pin No. PMQFP 44-pin	Pin No. PLCC 44-pin	Pin Name Test Alias in ()	Type	Connection (If not used)	Short Description
1	6	TE	IN	VSS	Test Enable
2	5	$\overline{\text{POR}}$	IN	VDD	Reset, Active Low
3	4	I2CC	IN/OUT	X	I^2C Clock Line
4	3	I2CD	IN/OUT	X	I^2C Data Line
5	2	VDD	SUPPLY	X	Positive Supply for Digital Parts
6	1	VSS	SUPPLY	X	Ground Supply for Digital Parts
7	44	DCEN	IN	VSS	Enable DC/DC Converter
8	43	$\overline{\text{EOD}}$	OUT	LV	PIO End of DMA, Active Low
9	42	$\overline{\text{RTR}}$	OUT	LV	PIO Ready to Read, Active Low
10	41	$\overline{\text{RTW}}$	OUT	LV	PIO Ready to Write, Active Low
11	40	DCSG	SUPPLY	VSS	DC Converter Transistor Ground
12	39	DCSO	OUT	VSS	DC Converter Transistor Open Drain
13	38	VSENS	IN	VDD	DC Converter Voltage Sense
14	37	PR	IN	X	PIO-DMA Request or Read/$\overline{\text{Write}}$
15	36	$\overline{\text{PCS}}$	IN	X	PIO Chip Select, Active Low
16	35	PI19	IN/OUT	LV	PIO Data [19] 1. Demand Pin in SDI mode 2. data bit [7], MSB (PIO-DMA input mode)
17	34	PI18	IN/OUT	LV	PIO Data [18] 1. MPEG header bit11 – MPEG ID (SDI mode) 2. data bit [6] (PIO-DMA input mode)
18	33	PI17	IN/OUT	LV	PIO Data [17] 1. MPEG header bit 12 – MPEG ID (SDI mode) 2. data bit [5] (PIO-DMA input mode)
19	32	PI16	IN/OUT	LV	PIO Data [16] 1. SIC*, alternative input for SIC (SDI mode) 2. data bit [4] (PIO-DMA input mode)
20	31	PI15	IN/OUT	LV	PIO Data [15] 1. SII*, alternative input for SII (SDI mode) 2. data bit [3] (PIO-DMA input mode)
21	30	PI14	IN/OUT	LV	PIO Data [14] 1. SID*, alternative input for SID (SDI mode) 2. data bit [2] (PIO-DMA input mode)

Pin No. PMQFP 44-pin	Pin No. PLCC 44-pin	Pin Name Test Alias in ()	Type	Connection (If not used)	Short Description
22	29	PI13	IN/OUT	LV	PIO Data [13] 1. MPEG header bit 13 – Layer ID (SDI mode) 2. data bit [1] (PIO-DMA input mode)
23	28	PI12	IN/OUT	LV	PIO Data [12] 1. MPEG header bit 14 – Layer ID (SDI mode) 2. data bit [0] (PIO-DMA input mode)
24	27	SOD (PI11)	OUT	LV	Serial Output Data
25	26	SOI (PI10)	OUT	LV	Serial Output Frame Identification
26	25	SOC (PI9)	OUT	LV	Serial Output Clock
27	24	PI8	IN	X	Start-up[1)]: Clock output scaler on / off
			OUT		Operation[2)]: MPEG CRC error
28	23	XVDD	SUPPLY	X	Positive Supply of Output Buffers
29	22	XVSS	SUPPLY	X	Ground of Output Buffers
30	21	SID (PI7)	IN	X	Serial Input Data
31	20	SII (PI6)	IN	VSS	Serial Input Frame Identification
32	19	SIC (PI5)	IN	X	Serial Input Clock
33	18	PI4	IN	X	Start-up[1)]: Select SDI / PIO-DMA input mode
			OUT		Operation[2)]: MPEG-Frame Sync
34	17	PI3	IN	X	Start-up[1)]: Enable Layer 3 / Disable Layer 3 decoding
			OUT		Operation[2)]: MPEG header bit 20 (Sampling frequency)
35	16	PI2	IN	X	Start-up[1)]: Enable Layer 2 / Disable Layer 2 decoding
			OUT		Operation[2)]: MPEG header bit 21 (Sampling frequency)
36	15	PI1	IN	X	Start-up[1)]: SDO: Select 32 bit mode / 16 bit I^2S mode
			OUT		Operation[2)]: MPEG header bit 30 (Emphasis)
37	14	PI0	IN	X	Start-up[1)]: Select Multimedia mode / Broadcast mode
			OUT		Operation[2)]: MPEG header bit 31 (Emphasis)
38	13	CLKO	OUT	LV	Clock Output for the D/A converter
39	12	PUP	OUT	LV	Power Up, i.e. status of voltage supervision
40	11	WSEN	IN	X	Enable DSP and Start DC/DC Converter

Pin No. PMQFP 44-pin	Pin No. PLCC 44-pin	Pin Name Test Alias in ()	Type	Connection (If not used)	Short Description
41	10	WRDY	OUT	LV	If WSEN = 0: valid clock input at CLKI If WSEN = 1: clock synthesizer PLL locked
42	9	AVDD	SUPPLY	VDD	Supply for analog circuits
43	8	CLKI	IN	X	Clock input
44	7	AVSS	SUPPLY	VSS	Ground supply for analog circuits

[1)] Start-up configuration see Section 2.7.3. in [1]
[2)] Not available in PIO-DMA mode, see Section 5.4.

9. Reference

[1]

MICRONAS INTERMETALL,
MAS 3507D MPEG 1/2 Layer 2/3 Audio Decoder,
Preliminary Data Sheet,
Edition Oct. 21, 1998
Order No. 6251-459-2PD