Preliminary Data Sheet Supplement

Subject:	Ball Grid Array Package for MAS 3507D
Data Sheet Concerned:	MAS 3507D, 6251-459-2PD, Edition 21.10.98 and Supplement No. 3, 6251-459-3PDS
Supplement:	No. 2/ 6251-459-2PDS
Edition:	July 16, 1999

New Package for MAS 3507D: 49-Ball Plastic Ball Grid Array (PBGA49)

The following information applies to MAS 3507D-F10.
This supplement replaces the previous version (Supplement No. 1, 6251-459-1PDS, Edition May 18, 1999).

1. Outline Dimensions

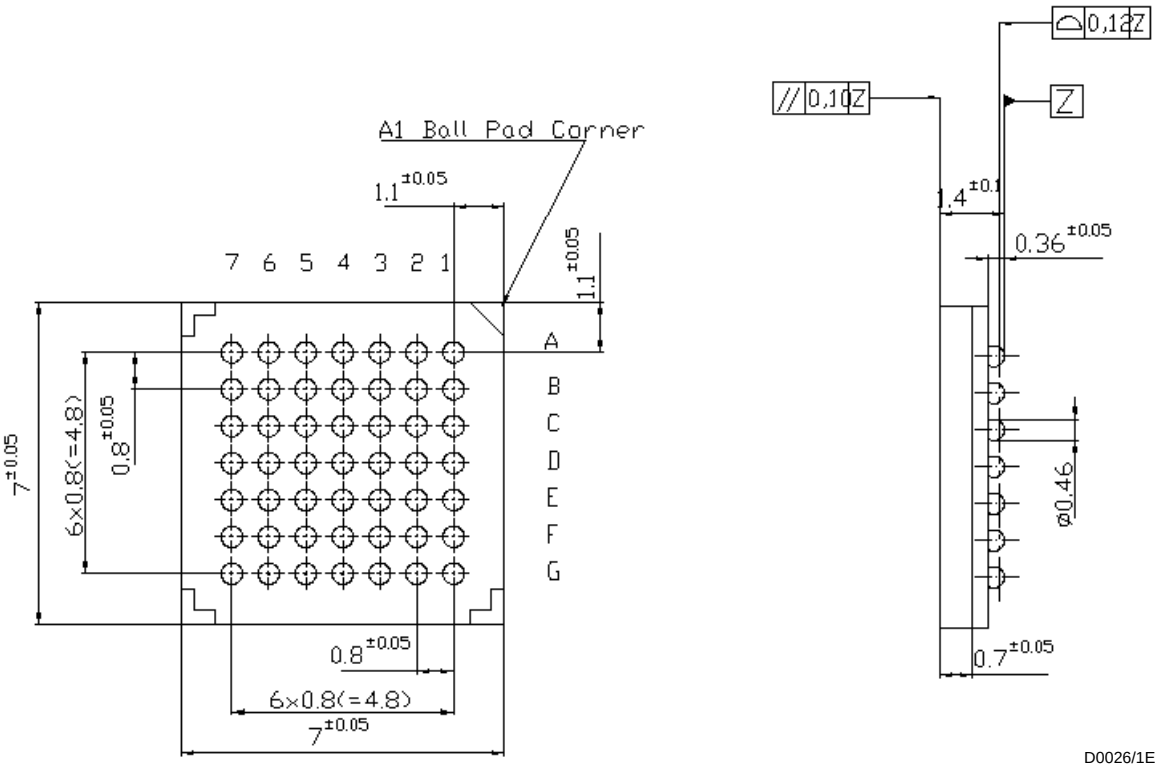

Fig. 1:
49-Ball Plastic Ball Grid Array
(PBGA49)
Dimensions in mm

2. Pin Connections and Short Descriptions

NC = not connected, leave vacant
X = obligatory; connect as described in application circuit diagram
LV = if not used, leave vacant
VSS = connect to ground
VDD = connect to positive supply

Unassigned pins must be left vacant.

Pin No.		Pin ID	Pin Name	Type	Connection	Short Description
PMQFP 44-pin	PLCC 44-pin	PBGA 49-ball	Test Alias in ()		(If not used)	
1	6	C3	TE	IN	VSS	Test Enable
2	5	C2	$\overline{\text{POR}}$	IN	VDD	Reset, Active Low
3	4	B1	I2CC	IN	VDD	I^2C Clock Line
4	3	D2	I2CD	IN/OUT	VDD	I^2C Data Line
5	2	C1	VDD	SUPPLY	X	Positive Supply for Digital Parts
6	1	D1	VSS	SUPPLY	X	Ground Supply for Digital Parts
7	44	E2	DCEN	IN	X	Enable DC/DC Converter
8	43	E1	$\overline{\text{EOD}}$	OUT	LV	PIO End of DMA, Active Low
9	42	F2	$\overline{\text{RTR}}$	OUT	LV	PIO Ready to Read, Active Low
10	41	F1	$\overline{\text{RTW}}$	OUT	LV	PIO Ready to Write, Active Low
11	40	G1	DCSG	SUPPLY	VSS	DC Converter Transistor Ground
12	39	E3	DCSO	OUT	VSS	DC Converter Transistor Open Drain
13	38	F3	VSENS	IN	VDD	DC/DC Converter Voltage Sense Input
14	37	G2	PR	IN	X	PIO DMA Request or Read/$\overline{\text{Write}}$
15	36	F4	$\overline{\text{PCS}}$	IN	X	PIO Chip Select, Active Low
16	35	G3	PI19	IN/OUT	LV	PIO Data [19] 1. Demand Pin (SDI mode) 2. data bit [7], MSB (PIO DMA input mode)
17	34	E4	PI18	IN/OUT	LV	PIO Data [18] 1. MPEG header bit 11 – MPEG ID (SDI mode) 2. data bit [6] (PIO DMA input mode)
18	33	G4	PI17	IN/OUT	LV	PIO Data [17] 1. MPEG header bit 12 – MPEG ID (SDI mode) 2. data bit [5] (PIO DMA input mode)
19	32	F5	PI16	IN/OUT	LV	PIO Data [16] 1. SIC*, alternative input for SIC (SDI mode) 2. data bit [4] (PIO DMA input mode)
20	31	G5	PI15	IN/OUT	LV	PIO Data [15] 1. SII*, alternative input for SII (SDI mode) 2. data bit [3] (PIO DMA input mode)
21	30	F6	PI14	IN/OUT	LV	PIO Data [14] 1. SID*, alternative input for SID (SDI mode) 2. data bit [2] (PIO DMA input mode)
22	29	G6	PI13	IN/OUT	LV	PIO Data [13] 1. MPEG header bit 13 – Layer ID (SDI mode) 2. data bit [1] (PIO DMA input mode)

Pin No. PMQFP 44-pin	Pin No. PLCC 44-pin	Pin ID PBGA 49-ball	Pin Name Test Alias in ()	Type	Connection (If not used)	Short Description
23	28	E5	PI12	IN/OUT	LV	PIO Data [12] 1. MPEG header bit 14 – Layer ID (SDI mode) 2. data bit [0] (PIO DMA input mode)
24	27	E6	SOD (PI11)	OUT	X	Serial Output Data
25	26	F7	SOI (PI10)	OUT	X	Serial Output Frame Identification
26	25	D6	SOC (PI9)	IN/OUT	X	Serial Output Clock
27	24	E7	PI8	IN	X	Start-up[1)]: Clock output scaler on / off
				OUT		Operation: MPEG CRC error
28	23	D7	XVDD	SUPPLY	X	Positive Supply of Output Buffers
29	22	C6	XVSS	SUPPLY	X	Ground of Output Buffers
30	21	C7	SID (PI7)	IN	X	Serial Input Data
31	20	B6	SII (PI6)	IN	X	Serial Input Frame Identification
32	19	B7	SIC (PI5)	IN	X	Serial Input Clock
33	18	A7	PI4	IN	X	Start-up[1)]: Select SDI / PIO DMA input mode
				OUT		Operation: MPEG-Frame Sync
34	17	B5	PI3	IN	X	Start-up[1)]: Enable Layer 3 / Disable Layer 3 decoding
				OUT		Operation: MPEG header bit 20 (Sampling frequency)
35	16	A6	PI2	IN	X	Start-up[1)]: Enable Layer 2 / Disable Layer 2 decoding
				OUT		Operation: MPEG header bit 21 (Sampling frequency)
36	15	B4	PI1	IN	X	Start-up[1)]: SDO: Select 32 bit mode / 16 bit I^2S mode
				OUT		Operation: MPEG header bit 30 (Emphasis)
37	14	A5	PI0	IN	X	Start-up[1)]: Select Multimedia mode / Broadcast mode
				OUT		Operation: MPEG header bit 31 (Emphasis)
38	13	C4	CLKO	OUT	LV	Clock output for the DA Converter
39	12	A4	PUP	OUT	LV	Power-up, i.e. status of voltage supervision
40	11	B3	WSEN	IN	X	WS Enable: Enable DSP and DC/DC Converter
41	10	A3	WRDY	OUT	LV	If WSEN = 0: valid clock input at CLKI If WSEN = 1: clock synthesizer PLL-locked
42	9	B2	AVDD	SUPPLY	VDD	Supply for analog circuits
43	8	A2	CLKI	IN	X	Clock input
44	7	A1	AVSS	SUPPLY	VSS	Ground supply for analog circuits

[1)] Start-up configuration see Section 2.7.3. of the MAS 3507D, 6251-459-2PD