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IN THIS ISSUE...

COVER ARTICLE
C-Load™ Op Amps Tame Instabilities 1
William Jett and George Feliz

Editor's Page 2
Richard Markell

DESIGN FEATURES
New 500ksps ADC Solves High-Speed Design Problems 3
William C. Rempfer and Ringo Lee

Triple-Output 3.3V, 5V, and 12V High-Efficiency Notebook Power Supply ... 6
Randy G. Flatness

The LT1203: 150MHz Video Multiplexer Features 25ns Switching Time and Better Than –90dB Crosstalk..... 8
John Wright and Frank Cox

LTC1065, Clock-Tunable, DC-Accurate, Fifth-Order Bessel Lowpass Filter 11
Nello Sevastopoulos

The World's First Low-Cost Micropower, 12-Bit ADCs in SO-8 Packages..... 13
William C. Rempfer and Marco Pan

DESIGN IDEAS 17–32
(complete listing on page 17)

DESIGN INFORMATION
Reconfigurable CMOS EIA562/RS232 and RS485 Transceivers..... 33
Dave Dwelley

New Device Cameos 34

LTC in the News 35

C-Load™ Op Amps Tame Instabilities

by William Jett and George Feliz

Introduction

Traditionally, operational amplifiers have been tricky to use with capacitive loads. Driving capacitive loads can bring out the worst behavior in most operational amplifiers. How often has discussion around the coffee pot centered on how to successfully decouple the op amp's output from the load so that oscillations do not run rampant?

Now the problem has become moot. Advances in process technology and innovative circuit design have made it possible for Linear Technology Corporation to develop a series of C-Load™ op amps that are tolerant of capacitive loading, including the ultimate: amplifiers that are stable with any capacitive load. These amplifiers span a range of bandwidths from 1MHz to 140MHz. The designer no longer has to worry; the amplifiers drive C_{LOAD} without problems.

The Problem

The cause of the capacitive load stability problems in most amplifiers is the pole formed by the load capacitance and the open-loop output impedance of the amplifier. This output pole increases the phase lag around the loop, reducing the phase margin of the amplifier. If the phase lag is large enough, the amplifier will oscillate.

External networks can be used to improve the amplifier's stability with a capacitive load (Figure 1). The networks cause the load impedance to appear more resistive to the output. The series resistor R_S isolates the capacitive load from the output, whereas the RC network (snubber) R_AC_A, added in parallel with the load, swamps out the load capacitance with the real impedance R_A. These networks work best when the load capacitance is well defined and constant, so the values can be optimized. Disadvantages include reduced output swing and drive current, and increased component count.

An Example

Existing op amps vary greatly in regard to stability with capacitive loads. Some older amplifiers are quite stable with resistive loads but

continued on page 15

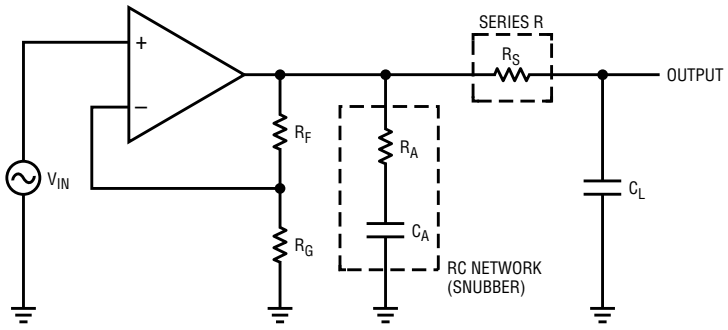


Figure 1. Conventional approaches to driving capacitive loads

New Isolator Device, LTC1145/1146, Wins Innovation of the Year Award

by Richard Markell

Innovation is the name of the game in today's fiercely competitive product environment. *EDN Magazine* recently awarded Bob Dobkin and Bob Reay of Linear Technology Corp. the Innovation of the Year award for semiconductors.

How does one innovate? How can a company cultivate an innovative environment? These are the keys to the success of LTC and of other trail blazing companies:

- Provide an environment where smart thinking and innovative ideas are rewarded.
- Give the potential innovator room to bounce ideas around a room full of critics.

Out of the swirling mists will come ideas. Some will be poor ideas. But some will be novel and produce creative products.

The LTC1145 and LTC1146 emerged from the mind of Bob Dobkin several years ago. The goal was isolation similar to that provided by opto-isolator circuits, without the hybrid LED/photodiode type of isolation barrier. Innovation came when Dobkin saw, "in a flash," that the capacitors required to provide isolation could be part of the lead frame. This "leadframe as capacitor" concept provides excellent isolation (UL approved to 4000 Volts DC) and also allows the product to be competitively priced.

The LTC1145 and LTC1146 are the first members of our isolator product line. These products include an on-chip digital filter to guarantee signal integrity, rather than speed.

Our lead article in this issue describes new operational amplifiers that drive any load capacitance. Designers no longer experience the nightmare of driving changing C_{LOAD} when they use these new LTC op amps. New analog-to-digital converters continue to come off the LTC product line; the LTC1298 and LTC1286 are new 12-bit converters in SO8 packages that convert to 12.5ksps. We also introduce the LTC1278, a 12-bit parallel ADC that samples at 500ksps.

In this issue we introduce the LT1203/LT1205 family of 150MHz, two- and four-channel multiplexers. Both feature an incredible isolation of better than –90dB at 10MHz. The LTC line of DC-accurate filters has another member: the LTC1065 fifth-order Bessel filter. The LTC1065 features less than 1 millivolt typical DC offset with 13 bits or more of dynamic range. Its cutoff frequency can be programmed by either an internal or an external clock.

Also highlighted in these pages is the LTC1142, a 5V and 3.3V synchronous, step-down switching regulator controller IC with two independent regulator sections. The LTC1142 is featured in a triple notebook power supply with outputs of 3.3V, 5V, and 12V.

Also in this issue we have information on new products from LTC for RS562 serial links. These are reconfigurable RS232/RS562/RS422/RS485 products that operate in many modes.

As is becoming our habit, in this issue we feature a good sampling of Design Ideas, as well as the famous underground LTC barometer circuit from the last LTC seminar.

FAE Cameo: Georg Dumsky

LTC now has twenty-one Field Application Engineers (FAEs) worldwide to assist our customers in the design and selection of circuits available from LTC.

Georg Dumsky is one of Linear Technology's three German Field Application Engineers. He was born in Franken, Germany and studied electronics in Munich. Georg has been with LTC for nearly six years. During most of this time, his territory has included Switzerland, Austria, and all or part of Germany.

Georg and his wife and their daughter Barbara live in Neufahrn, a small town north of Munich, near the LTC office in Eching.

Georg's hobbies include gardening, but he says he "prefers to play squash." (Do you think the pun is intended?) In the summer he is a windsurfer and in the winter he skis with his family and friends.

Georg tells a story of how he spent a long time convincing a customer that he could use an LTC reference in his system, eliminating trims while maintaining stability. A new designer who took over the project later told Georg that they did not need the LTC parts, because they "had something in there that gives 5.000 volts without adjustment." Needless to say, Georg and the new designer were talking about the same thing: the LT1029.

New 500ksps ADC Solves High-Speed Design Problems

by William C. Rempfer
and Ringo Lee

Introduction

The newest member in Linear Technology's high-speed ADC family has arrived. It is the LTC1278. This 500 kilo-samples-per-second (ksps), 12-bit device solves the major problems faced by designers of today's high speed systems: performance, power dissipation, board space, complexity, and cost. This device offers the following radical improvements to designers of telecommunications, digital signal processing, and high-speed and multiplexed data-acquisition systems:

- Single 5V or ±5V supply operation
- Low power dissipation and power shutdown
- Complete: requires no external components, crystals or clocks
- Excellent AC and DC performance
- Small 24-pin SO or 24-pin narrow DIP package

These features of the LTC1278 can simplify, improve, and lower the cost of high-speed designs. This article describes the LTC1278 and discusses its benefits and how they can solve the system designer's problems.

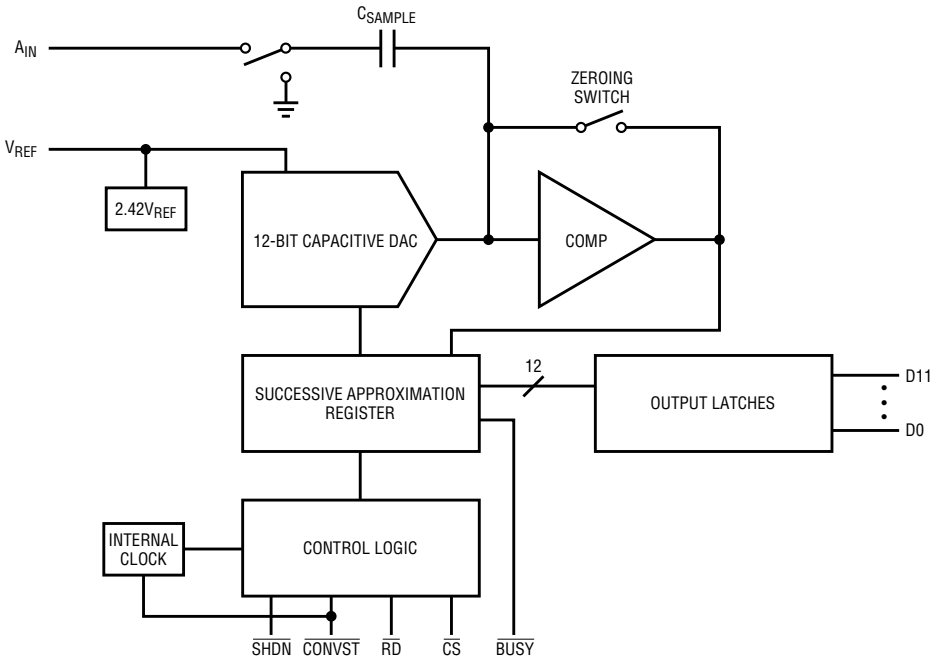


Figure 1. The LTC1278 ADC is complete, with sample-and-hold, internal reference, internally synchronized conversion clock, and power-down circuitry

Welcome the Newest ADC Family Member

The LTC1278 is a high-speed, low-power, 12-bit sampling ADC. It is complete and requires no external components. It runs at 500ksps and typically draws only 75mW from single 5V or ±5V supplies. It offers a 5mW power-down mode with instant wake up.

As shown in Table 1, the LTC1278 is the fastest member of LTC's high-speed ADC family. The family also includes 300ksps/5V members and a 140ksps/3V device. Like other family members, the LTC1278 uses a capacitively-based successive-approximation (SAR) algorithm. However, this device takes the SAR architecture to new levels of speed. By using the SAR approach, it can provide very high performance at low power and low cost.

The block diagram of Figure 1 shows the components contained within the chip: a fast SAR ADC with sample-and-hold, an internal reference, and internally synchronized conversion clock and power-down circuitry. This architecture is very similar to that of the previous family members. Process and design improvements have allowed the speed to be increased. A power-down function has been added to provide

Table 1. LTC's high-speed ADC family includes 5V and 3V devices. The 500ksps LTC1278 is the fastest member

Device Type	Sampling Frequency	S/(N + D) @Nyquist	Input Range	Power Supply	Power Dissipation
LTC1272	250kHz	65dB	0V–5V	5V	75mW
LTC1273	300kHz	70dB	0V–5V	5V	75mW
LTC1275	300kHz	70dB	±2.5V	±5V	75mW
LTC1276	300kHz	70dB	±5V	±5V	75mW
LTC1278	**500kHz**	**70dB**	**0V–5V or ±2.5V**	**5V or ±5V**	**75mW 5mW***
LTC1282	140kHz	68dB	0V–2.5V or ±1.25V	3V or ±3V	12mW

*5mW power shutdown with instant wake-up

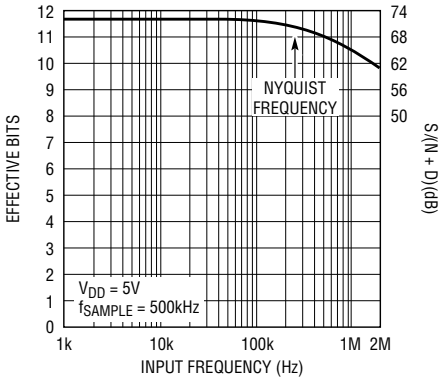


Figure 2. The LTC1278 can accurately digitize input signals up to the Nyquist frequency and beyond, making it useful even in undersampling applications

reduced power consumption during inactive periods. A separate conversion-start input and some new digital interface modes allow more flexibility and an easier interface to latches, FIFOs, and DSPs.

Benefits

The LTC1278 offers benefits in performance, power dissipation, configuration simplicity, and board space. It will operate on a single power supply.

Outstanding DC and AC Performance Beyond Nyquist

The DC performance of the new ADC includes ±1LSB INL and DNL. No missing codes performance is guaranteed over temperature. Maximum full-scale drift of the internal reference is 25ppm/°C.

On the AC front, the LTC1278 can digitize input signals up to the Nyquist rate (250kHz) with nearly perfect linearity. Even more significant is its ability to digitize beyond the Nyquist frequency. This makes it useful in "undersampling" applications such as synchronous demodulation of high frequency IF signals. Figure 2 shows how the effective bits and signal-to-noise plus distortion ratio of the converter perform as input frequency is increased.

Lowest Power Dissipation and Shutdown

The 150mW maximum power dissipation (75mW typical) is at least two times lower than any other ADC in this speed range. It is even further enhanced by a power shutdown feature (5mW typical) that can be invoked with an external pin ($\overline{SHDN}$). The ADC wakes up "instantly" (300ns) from shutdown, so power-down can be invoked even during brief inactive periods with no penalty or delay when conversions must start again.

Fewer Power Supplies

The new ADC runs at full speed on either a single 5V supply or ±5V supplies. This makes it extremely attractive in new high-speed designs, which are abandoning the ±15V supplies of the past. Many new designs use 5V supplies for reduced power dissipation and higher op amp performance. Many new high speed op amps are being developed on advanced, high-speed processes that can stand only ±5V rails. In addition to its ±5V supplies, the LTC1278's ±2.5V input span nicely matches output swings of this new generation of op amps.

Simple Configuration: No External Components

The LTC1278 is complete. No external components are required except for the normal supply and reference bypass capacitors used by all high speed ADCs. Figure 3 shows the extremely simple configuration provided by this new device.

Unbeatable Board Space

The simple configuration of Figure 3 also allows a very small board layout. All components are available in surface-mount packages, including the ADC. The actual board space, including an input op amp and bypass capacitors is one-half square inch.

Applications Abound

At least four major application areas can benefit from the LTC1278: telecommunications, digital signal processing, portable-computer data-acquisition boards, and high-speed or multiplexed data acquisition.

Telecom and DSP

In telecom applications such as HDSL (High-bit-rate Digital Subscriber Line interface), low ADC power dissipation is a must because the systems are usually powered by the phone line itself. Excellent dynamic performance is required of the ADC's sample-and-hold. Noise cancellation and echo cancellation are examples of DSP problems that also require excellent dynamic performance. The LTC1278 excels in these applications, even beating the performance of many 14- and 16-bit converters. How can

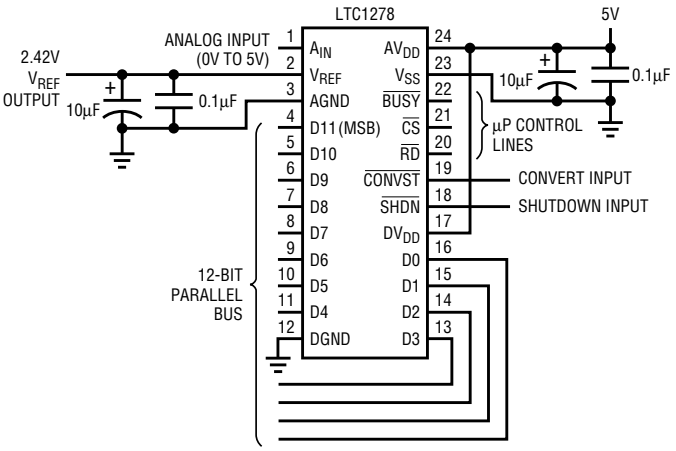


Figure 3. The complete 500ksps ADC requires only bypass capacitors and one power supply. Surface-mount packaging means the complete solution occupies well under one-half square inch of valuable real estate

this be? How can a 12-bit converter outperform higher resolution devices? The answer is in the sample-and-hold.

At low input frequencies (e.g., below 10kHz), most 14- and 16-bit ADCs will outperform 12-bit ADCs. This is because the quantization noise caused by the discrete ADC steps is smaller due to the smaller step size. However, as the input frequency is increased, the sample-and-hold can dominate and degrade the ADC performance in two ways. First, the aperture-time jitter in the sample-and-hold will translate into input-referred voltage noise via the dv/dt of the input signal. The higher the dv/dt, the higher the jitter-induced noise. This can degrade the noise floor of the higher resolution ADC to below the 12-bit level. Second, the distortion of the sample-and-hold will distort the input signal and add unwanted harmonics to the output spectrum of the ADC. This will degrade the distortion (THD) and signal-to-noise plus distortion (S/(N+D)) of the ADC. These two effects combine and can make a poorly designed 14- or 16-bit converter worse than a 12-bit device at high input frequencies.

The LTC1278 is a winner in these types of systems because of the performance of its sample-and-hold. Figure 2 shows how well the effective bits and signal-to-noise plus distortion ratio of the converter hold up as the input frequency is increased. For input signals up to the Nyquist rate (250kHz), jitter and distortion remain low enough so as not to degrade the overall ADC performance. Beyond the Nyquist frequency, the sample-and-hold still performs better than many 14- and 16-bit devices. The LTC1278 can achieve 70dB of S/(N + D) when synchronously demodulating a 455kHz IF signal.

PC Data Acquisition Cards

Another common application is PC data acquisition cards. The high sample rate, the simple, complete configuration, and the low cost of these converters make them ideal choices here. Another subtle feature, the synchronized internal conversion clock, is also useful in this application.

Other sampling ADCs require an external clock to run the conversion, in addition to the normal sample signal. Aside from the extra hardware and circuitry needed to generate the clock, a synchronizing problem occurs between the conversion clock and the sample signal. If the two signals are not synchronized, noise from the conversion clock couples into the ADC as the sample is taken, generating errors. Hence, with these converters, the two clocks must be synchronized. In constant-sample-rate systems, this is possible, although bothersome; however, in PC data-acquisition systems the sample command often comes from the outside, and its exact timing cannot be known. In this case, the system designer must design conversion-clock circuitry that senses when the sample command occurs and automatically synchronizes to it. This is difficult to do with the fast and precise clocks required by these ADCs. This is one of the big benefits of the LTC1278 and its brothers in Table 1. They have been designed with internal conversion clocks that automatically synchronize to the incoming sample command. The devices are factory trimmed with adequate precision to meet the 1.6µs conversion time of the ADC. This feature makes this new converter a clear winner for PC data acquisition cards.

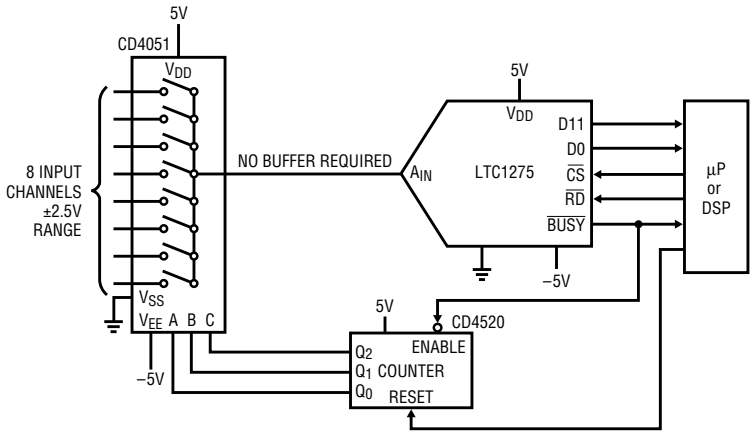


Figure 4. The high input impedance of the ADC family allows multiplexing without a buffer amplifier. The 300ksps LTC1275 is shown here with the low cost CD4051 multiplexer

Multiplexed and High-Speed Data Acquisition

Both single-channel and multiplexed high-speed data acquisition systems can benefit from the LTC1278's performance. The 1.6µs conversion time and 300nsec acquisition time allow a high 500ksps throughput on a very low power and cost budget. In addition, the high-impedance inputs of the ADCs make them very easy to multiplex. Figure 4 shows the 300ksps LTC1275 multiplexed with a low cost MUX and counter. (The LTC1278 can be used for higher speeds). The system scans through the eight channels, converting at full speed. The high input impedance of the ADC eliminates the need for a buffer between the MUX and the ADC. The combined price of the MUX and counter is less than $0.50, making an extremely low-cost configuration.

Conclusion

The ADC's new features can simplify, improve and lower the cost of high speed designs. This will make it the converter of choice for designers of telecom, DSP, and high-speed and multiplexed data-acquisition systems.

Triple-Output 3.3V, 5V, and 12V High-Efficiency Notebook Power Supply

by Randy G. Flatness

Introduction

The new LTC1142 is a dual, 5V and 3.3V synchronous, step-down switching-regulator controller, featuring automatic Burst Mode™ operation for high efficiencies at low output currents. Two independent regulator sections, each driving a pair of complementary MOSFETs, can be separately shut down to less than 20µA per output. This feature is absolutely necessary for maximizing battery life in portable applications. Additionally, the input voltage to each regulator section can be individually connected to different potentials (20V maximum), allowing a wide range of novel applications.

The operating current levels for both regulator sections can be programmed, via external current-sense resistors, to set current limits. A wide input-voltage range for the LTC1142 allows operation from 4V to 16V. The LTC1142HV extends this voltage range to 20V, permitting operation with up to 12-cell battery packs.

LTC1142 Circuit Operation

Both regulator blocks in the LTC1142 and LTC1142HV use a constant off-time current-mode architecture with Burst Mode™ operation identical to that of the LTC1148. This results in a power supply that has very high efficiency over a wide load-current range, fast transient response, and very low dropout. The LTC1142 is ideal for applications requiring 5V and 3.3V outputs with high conversion efficiencies over a wide load-current range, in a small amount of board space. The LTC1142 and LTC1142HV are available in 28-pin SSOP packages.

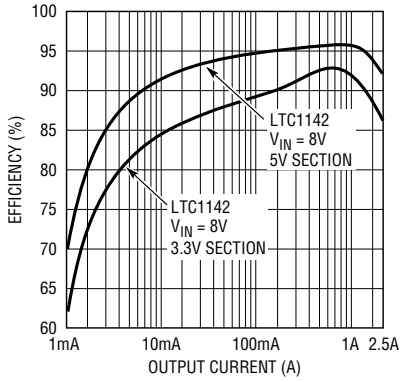


Figure 1. LTC1142 efficiency

The LTC1142 is ideal for applications requiring 5V and 3.3V outputs with high conversion efficiencies over a wide load current range, in a small amount of board space.

The application circuit in Figure 2 is configured to provide output voltages of 3.3V, 5V, and 12V. The current capability of both the 3.3V and 5V outputs is 2A (2.5A peak). The logic-controlled 12V output can provide 150mA (200mA peak), which is ideal for flash-memory applications. The operating efficiency, shown in Figure 1, exceeds 90% for both the 3.3V and 5V sections.

The 3.3V section of the circuit in Figure 2 comprises the main switch Q4, synchronous switch Q5, inductor L1, and current shunt R_{SENSE3}. The current sense resistor R_{SENSE} monitors the inductor current and is used to set the output current according to the formula $I_{OUT} = 100mV/R_{SENSE}$. Advantages of current control include excellent line and load transient rejection, inherent short-circuit protection, and controlled startup currents. Peak inductor currents for L1 and T1 of the circuit in Figure 2 are limited to $150mV/R_{SENSE}$, or 3.0A and 3.75A respectively.

When the output current for either regulator section drops below approximately $15mV/R_{SENSE}$, that section automatically enters Burst Mode™ operation to reduce switching losses. In this mode the LTC1142 holds both MOSFETs off and "sleeps" at 160µA supply current, while the output capacitor supports the load. When the output capacitor falls 50mV below its specified voltage (3.3V or 5V), the LTC1142 briefly turns this section back on, or "bursts," to recharge the output capacitor. The timing capacitor pins, which go to 0V during the sleep interval, can be monitored with an oscilloscope to observe burst action. As the load current is decreased, the circuit will burst less and less frequently.

The timing capacitors C_{T3} and C_{T5} set the off-time according to the formula $t_{OFF} = 1.3 \times 10^4 \times C_T$. The constant off-time architecture maintains a constant ripple current, while the operating frequency varies only with input voltage. The 3.3V section has an off-time of approximately 5 microseconds, resulting in a operating frequency of 120kHz with an 8V input. The 5V section has an off-time of 2.6 microseconds and a switching frequency of 140kHz with an 8V input.

Auxiliary 12V Output

The operation of the 5V section is identical to the 3.3V section, with inductor L1 replaced by transformer T1. The 12V output is derived from an auxiliary winding on the 5V inductor T1. The output from this additional winding is rectified by diode D3 and applied to the input of an LT1121 regulator. The output voltage is set by resistors R3 and R4. A turns ratio of

Burst Mode™ is a trademark of Linear Technology Corporation

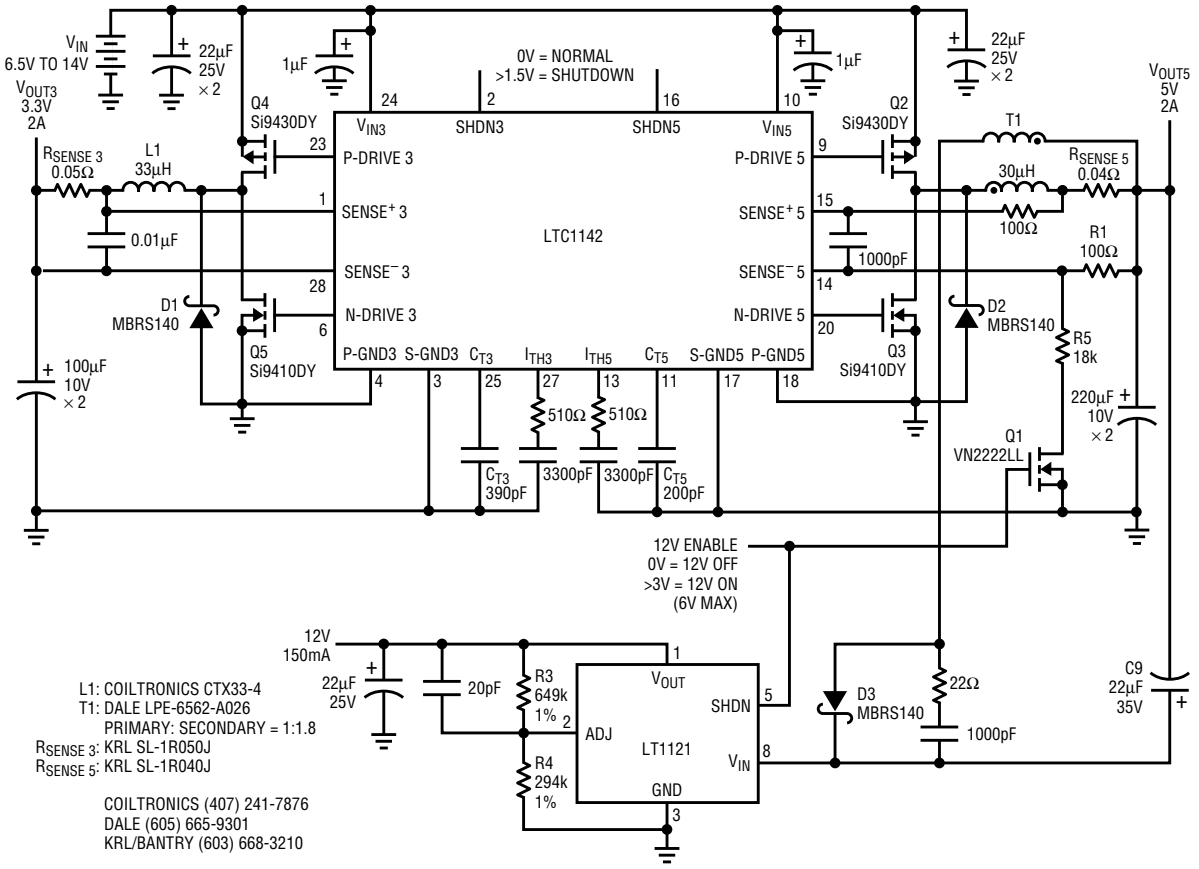


Figure 2. Schematic diagram, LTC1142 high-efficiency power supply

1:1.8 is used for T1 to ensure that the input voltage to the LT1121 is high enough to keep the regulator out of dropout mode while maximizing efficiency.

The LTC1142 synchronous switch removes the normal limitation that power must be drawn from the primary 5V inductor winding in order to extract power from the auxiliary winding. With synchronous switching, the auxiliary 12V output may be loaded without regard to the 5V primary output load, provided that the loop remains in continuous-mode operation.

When the 12V output is activated by a TTL high (6V maximum) on the 12V enable line, the 5V section of the LTC1142 is forced into continuous mode. A resistor divider composed of R1, R5, and switch Q1 forces an offset, subtracting from the internal offset at pin 14. When this external offset cancels the built-in 25mV offset, Burst Mode™ operation is inhibited.

Auxiliary 12V Output Options

The circuit of Figure 2 can be modified for operation in low-battery-count (6-cell) applications. For applications where heavy 12V-load currents exist in conjunction with low input voltages (<6.5V), the auxiliary winding should be derived from the 3.3V instead of the 5V section. As the input voltage falls, the 5V duty cycle increases to the point when there is simply not enough time to transfer energy from the 5V primary winding to the 12V secondary winding. For operation from the 3.3V section, a transformer with a turns ratio of 1:3.25 should be used in place of the 33µH inductor L1. Likewise, a 30µH inductor would replace T1 in the 5V section. With these component changes, the duty cycle of the 3.3V section is more than adequate for full 12V load currents. The minimum input voltage in this case will be determined only by the dropout voltage of the 5V output. The 100% duty cycle inherent in the LTC1142 provides low dropout operation limited only by the load current multiplied by the sum of the resistances of the 5V inductor, Q2 $R_{DS(ON)}$ and current sense resistor R_{SENSE5}.

Extending the Maximum Input Voltage

The circuit in Figure 2 is designed for a 14V maximum input voltage. The operation of the circuit can be extended to over 18V if a few key components are changed. The parts

continued on page 31

The LT1203: 150MHz Video Multiplexer Features 25ns Switching Time and Better Than –90dB Crosstalk

by John Wright
and Frank Cox

Introduction

The LT1203 is a wide-band, two-input video multiplexer designed for pixel switching and broadcast-quality routing. The LT1205 is a dual version that is configured as a four-input, two-output multiplexer. These multiplexers act as SPDT video switches with 10ns transition times at toggle rates up to 30MHz. Both devices are fast enough for SVGA or workstation applications, and are ideal for multimedia applications where signals are routed on PCBs prior to cable driving.

As picture processing and special video effects become popular, there is increased demand for higher performance switching.

The 150MHz –3dB bandwidth ensures 0.1dB flatness to 30MHz for HDTV systems, and the insertion loss at 1MHz is only 0.03dB. Easy input expansion, low switching transients, and outstanding crosstalk make the LT1203 and LT1205 ideal for quality video distribution. The LT1203 is available in 8-lead P DIP and 8-lead SO packages, whereas the LT1205 is packaged in the 16-lead narrow SO.

Advantages of Complementary Bipolar Processing

As picture processing and special video effects become popular, there is increased demand for higher performance switching. For many years video multiplexers have been fabricated on a variety of CMOS processes because of the ease of implementation and low cost; but along with low cost comes low performance. CMOS multiplexers are inherently bidirectional because they are just a switch between input and output. This results in poor output-to-input isolation during switching unless a dead-time is introduced. CMOS MUX's have been built with break-before-make switching to eliminate the talking between channels, but these parts suffer from output glitches large enough to interfere with sync circuitry and input glitches that couple to other equipment. This is shown in Figure 1. The input and output switching transients of a CMOS multiplexer are shown in Figure 2.

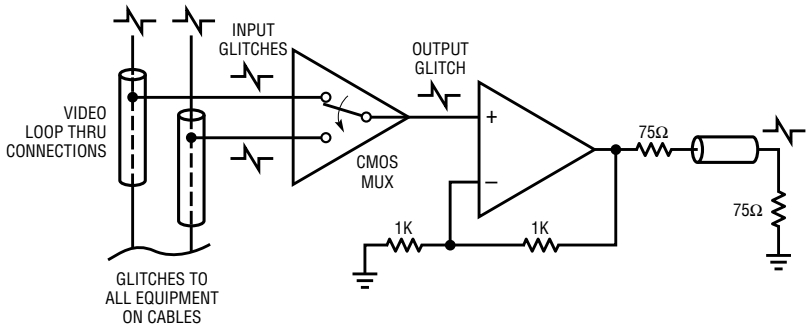


Figure 1. CMOS MUXs cause glitches on inputs and outputs

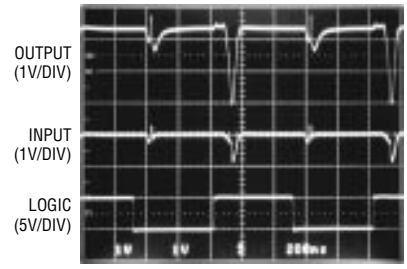


Figure 2. CMOS MUX switching glitch (R_S = 50Ω) Note: Output 1V/Div.

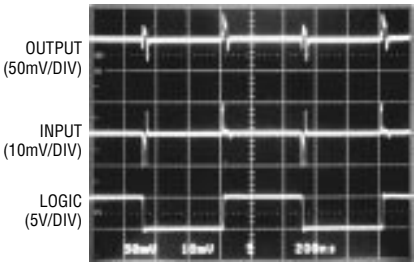


Figure 3. LT1203 switching glitch (R_S = 50Ω) Note: Output 50mV/Div.

Figure 3 is a photo of the LT1203 switching transients. The input and output transients of the LT1203 are 50 times lower than those of the CMOS multiplexer. To prevent input transients from reaching other circuitry, CMOS MUXs require buffers on each input; this raises total system complexity and cost. Outputs must also be buffered because the high on-resistance of the switch ($R_{DS(ON)}$) causes large insertion loss. CMOS multiplexers suffer other problems as well, including low operating supply voltage, varying $R_{DS(ON)}$ with supply or input voltage, part-to-part variations, and poor channel separation, even when configured as tee switches.

The LT1203 and LT1205, by contrast, are fabricated on LTC's

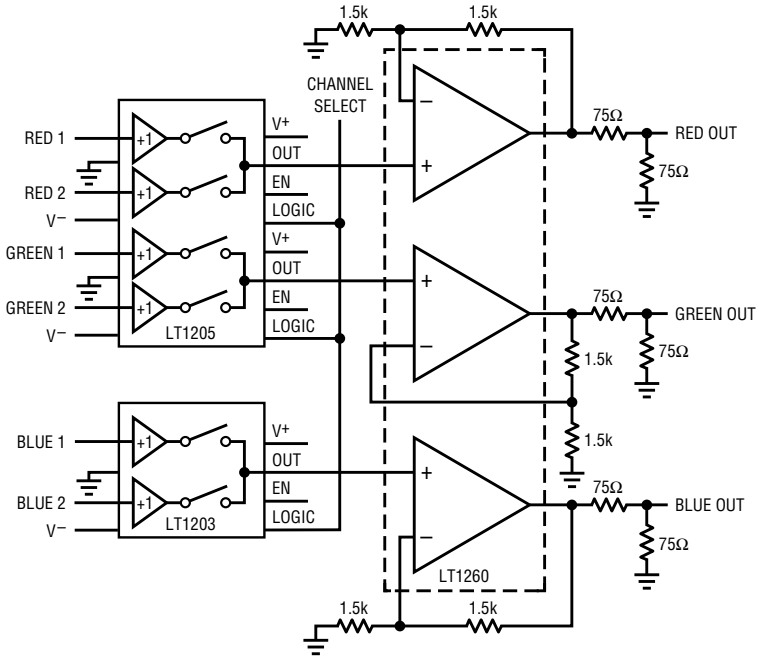


Figure 4. Fast RGB MUX

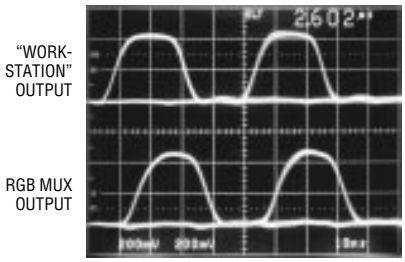


Figure 5a. Workstation and RGB MUX output

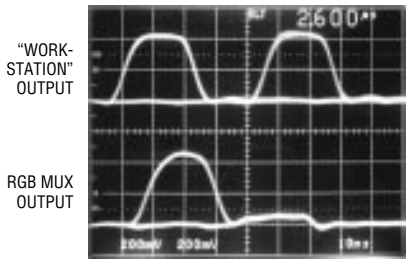


Figure 5b. RGB MUX output switched to ground after one pixel

complementary bipolar process to attain fast switching speed, high bandwidth, and a wide supply-voltage range compatible with traditional video systems. The AC characteristics change very little as the supply voltage changes from ±5V to ±15V. Channel-to-channel switching time and chip-enable time are both 25ns; hence, the delay is the same when switching between channels or between ICs.

To demonstrate the switching speed of the LT1203/LT1205, the RGB MUX of Figure 4 is used to switch the inputs of an RGB workstation with a 22ns pixel width. Figure 5a is a photo showing the workstation output and RGB MUX output. The slight rise-time degradation at the RGB MUX output is due to the bandwidth of the LT1260 current-feedback amplifier used to drive the 75 ohm cable. In Figure 5b, the LT1203 switches at the end of the first pixel to an input at zero and removes the following pixels.

Circuit Topology

The LT1203 and LT1205 use a tee switch configuration to attain excellent crosstalk and disable isolation. In addition, these multiplexers have internal input buffers to prevent switching transients from reaching their inputs. Figure 6 is the internal schematic of the LT1203. When the logic selects channel 1, Q7 and Q9 each steer 3I to the complementary Darlington configuration made up of Q1–Q4. Current sources I1 and I2 remain biased at all times and subtract 1/3 of the collector current from Q7 and Q9. This results in Q1–Q4 having a bias current of 2I, or about 1mA each. Transistors Q5 and Q6 are held off in this condition. DC offset

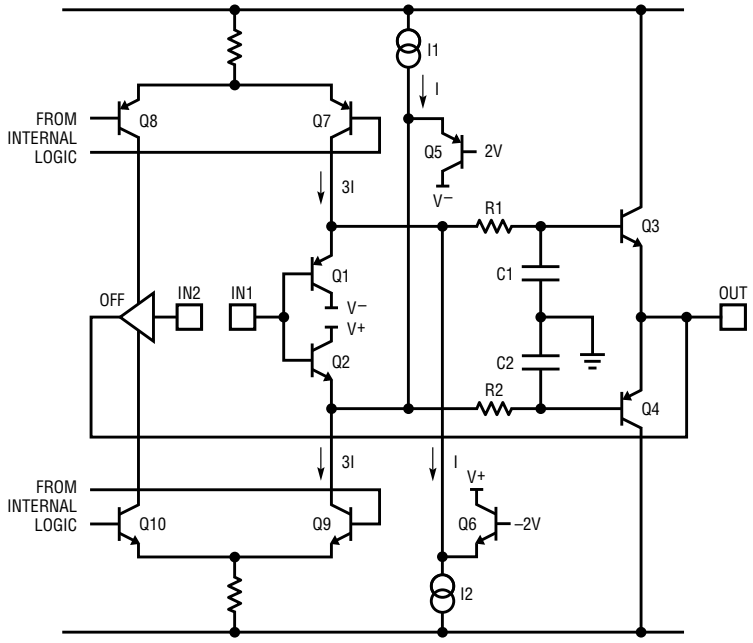


Figure 6. LT1203 internal schematic

matching between channels is more important to the video engineer than the actual value of the input offset. A DC mismatch as small as 3mV between channels is just visible on a quality video monitor. The typical V_{OS} mismatch between channels on the LT1203 is about 300µV. Components R1, C1, R2, and C2 compensate the complementary Darlington connection for capacitive loads. Maximum peaking occurs with a 50pF capacitive load, and is less than 3dB.

To change inputs, logic circuitry switches the current steering differential pairs and 3I is routed to channel 2. This current steering technique is very fast and accounts for the rapid switching of the multiplexer. Tee switches are formed when current sources I1 and I2 turn on Q5 and Q6. Q1–Q4 become reverse biased and isolate the input and output, providing over 90dB off-channel rejection at 10MHz. The complementary Darlington is protected from emitter-base breakdown by ESD clamps on the inputs that activate at ±3V.

Multiplexer Expansion with Better Than –90dB Crosstalk at 10MHz

The output impedance of the LT1203 is typically 20Ω when enabled, and 10MΩ when disabled or not selected. This high disabled output impedance allows the output of several LT1205s to be shorted together to form large cross-point arrays. Four LT1205s can be used to form a 16-to-1 cross-point switch. In this application, 15 switches are turned off and only one is active. An attenuator is formed by the 15 de-selected amplifiers and the output of the one active device. Because of the wide bandwidth in the LT1203, the output impedance is constant at 20Ω up to 10MHz and then rises. Figure 7 is the all hostile crosstalk response for this 16-to-1 MUX.

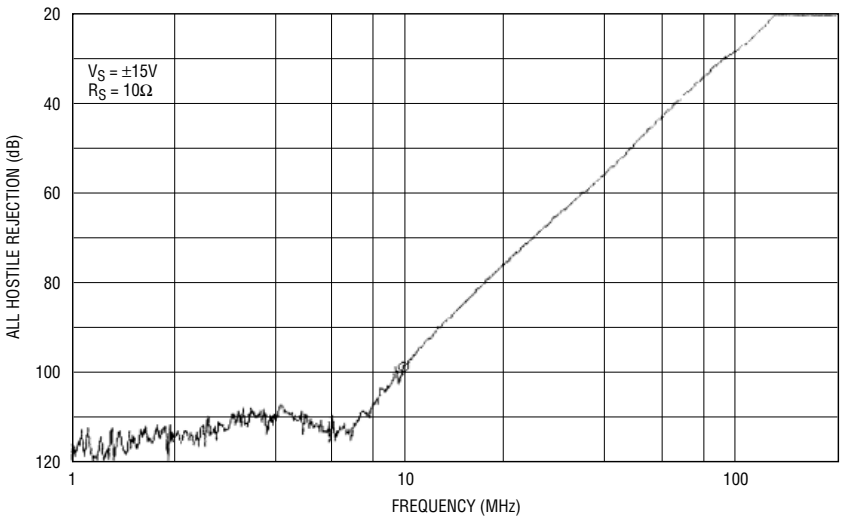


Figure 7. "All hostile" crosstalk of 16-to-1 MUX

Performance

Table 1 summarizes the major performance specifications of the LT1203.

Conclusion

By taking full advantage of LTC's complementary bipolar process, the LT1203/LT1205 can route high-speed video signals without the switching transients common in CMOS multiplexers. Switching speed is fast enough for use in SVGA or workstation environments, while all hostile crosstalk is low enough for the multiplexer to be used in very large cross-point configurations. Expansion is simple, with an enable feature that raises the output impedance to 10MΩ. These high-performance multiplexers complement the large number of video products offered by LTC. LT

Table 1. LT1203/LT1205 performance

Parameter	Conditions	Typical Value
Bandwidth	R_L = 1k	150MHz
0.1dB gain flatness	R_L = 1k	30MHz
Slew rate	R_L = 1k	300V/µs
Differential gain	R_L = 10k	0.01%
Differential phase	R_L = 10k	0.01 deg
Channel-select time	R_L = 1k, V_{IN} = 1V	25ns
Enable time	R_L = 1k	25ns
Output voltage swing	R_L = 1k	±3V
Gain error	R_L = 1k, V_{IN} = ±2V	2%
Input voltage range		±3V
Output offset voltage		10mV
Supply current		10mA
Supply current disabled		5.8mA

LTC1065, Clock-Tunable, DC-Accurate, Fifth-Order Bessel Lowpass Filter

by Nello Sevastopoulos

Introduction

The LTC1065 is a monolithic fifth-order lowpass filter with a frequency response that closely approximates a linear-phase Bessel filter. (Our hero and the frequency response of the LTC1065 are shown in Figures 1 and 2, respectively.) The LTC1065's proprietary architecture, like that of the LTC1063, gives outstanding DC and AC performance.

The LTC1065 features 1mV typical output DC offset, 13 bits or more of dynamic range, and excellent device-to-device matching. The LTC1065's cutoff frequency is programmed by either an internal or an external clock.

DC Performance

The output DC offset of the LTC1065 filter depends on the offset of a single internal op amp and on the charge injection of the input switches. The LTC1065 output DC offset is trimmed to less than 1mV and is optimized for ±5V supply operation. The output offset of the LTC1065 is low enough to allow it to compete with discrete RC active filters using low-offset op amps.

Calling the LTC1065 "DC accurate" implies that it can pass DC signals without significantly altering their values. The LTC1065's DC output offset is measured (to 13 bits of accuracy) with the input terminal grounded.

Figure 1. Our hero

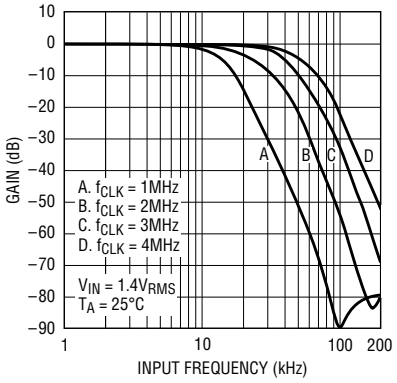


Figure 2. LTC1065 passband and gain vs. frequency response

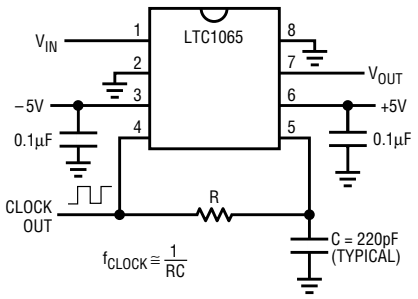


Figure 3. Setting the LTC1065 internal clock with an external RC

The common-mode rejection of the filter (in dB) is defined as the ratio of the allowed input-voltage range to the DC output offset change:

$$CMR = 20 \log(V_{IN(DC)}/V_{OS(OUT)}) \text{ (dB)}$$

Table 1 shows the measured CMR of several devices over the industrial temperature range.

For example, an LTC1065 is placed in front of an A/D converter with ±2.5V input range, V_S = ±5V. The filter output DC offset will not change by more than 0.7mV over the entire ±2.5V DC input range and over –40 to 85 degrees C. If a 12-bit A/D is used, the filter will contribute slightly more than 1/2 LSB DC error.

DC accuracy is obtained if the output DC offset does not change with varying input DC signals. Power supply decoupling and PC board layout are extremely critical in achieving a constant output offset over a wide range of cutoff frequencies. Note that the DC performance of the LTC1065 will degrade somewhat when the filter cutoff frequency exceeds 15kHz.

AC Performance

Clock Requirements

An external or internal clock programs the filter's cutoff frequency with a clock-to-cutoff-frequency ratio of 100:1. If no external clock is available, the internal oscillator can be used. The clock frequency of the internal oscillator is set by a simple RC network, as shown in Figure 3. Note that the ±3% typical tolerance of the internal oscillator frequency does not affect the flatness of the filter passband. Figure 4 shows how to select the exact values of the external RC network: for a given power supply choose the value of parameter K, set C = 220pF + 4pF (parasitic capacitance) and solve for R.

Example:

f_{CUTOFF} = 2kHz, f_{CLK} = 200kHz, V_S = ±5V, K = 1, C = 220pF, R = 22.6K (1% value)

For clock frequencies above 500kHz and for more information on temperature behavior, please consult the LTC1065 final data sheet or the LTC1063 data sheet.

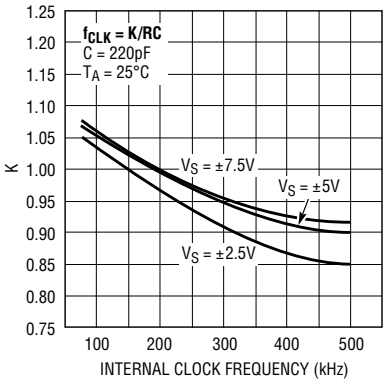


Figure 4. Selecting the external RC components for a given clock frequency

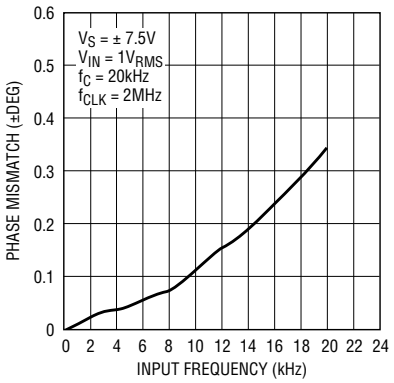


Figure 5. LTC1065 typical phase matching (device-to-device)

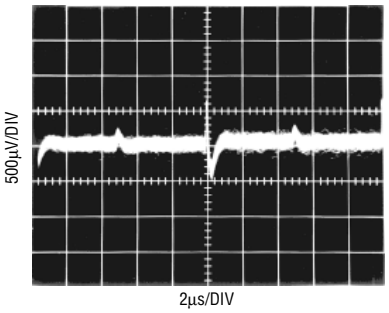


Figure 6. LTC1065 output clock feedthrough + noise; filter input grounded

Device-to-Device Matching

The unique filter architecture of the LTC1065 and LTC1063 allows outstanding device-to-device phase and amplitude matching. Channel-to-channel matching is a common requirement of multichannel systems. Figure 5 shows the phase matching of a group of fifty randomly selected devices. The filters were set up for a 20kHz cutoff frequency and phase versus frequency was measured. The worst phase mismatch between two devices was a total 0.7 degrees at 20kHz. Amplitude matching in the devices is also excellent. Amplitude mismatch ranges from an infinitesimal 0.01dB to 25% of the filter passband to a mere 0.05dB at 50% of the filter passband.

Noise, Clock Feedthrough, and Dynamic Range

The LTC1065 design approach is based on optimum S/N ratio plus THD rather than just low noise. The total noise of the LTC1065, however, is quite low (80µV_{RMS}) and is independent of the value of the cutoff frequency. The noise peak distribution is gaussian. Using a crest factor of 5.5, the amplitude of a noise peak is 220µV. Note that 1/2LSB of a 14-bit system is 305µV (10V full scale). This means that when noise is the critical factor, the LTC1065 can be placed in front of a 14-bit A/D. Signal-to-noise ratio is 93dB (measured RMS) with a 10Vp-p output swing. The device's maximum S/N ratio is 95dB.

Internal layout techniques minimize clock feedthrough. Clock feedthrough is defined as the sum of the RMS amplitudes of the clock and its harmonics measured at the output of the filter. In the past, clock feedthrough was orders of magnitude greater in amplitude and it could, at best, cause system errors and, at worst, render the filter unusable in other than telephone-type applications.

Figure 6 shows an oscilloscope photo of the filter output when its input is grounded. The clock feedthrough is embedded in the peak-to-peak wideband noise. The switching transients shown in Figure 6 have frequency contents well above the clock frequency and, if they are bothersome, they can be removed either with a simple RC network, or by bandwidth limiting the circuits following the filter.

Figure 7 shows the typical configuration for dynamic range measurement. An inverting buffer is preferred over a unity-gain follower. Large input common-mode signals can severely degrade the distortion performance of a noninverting buffer. Figure 8 shows the THD-plus-noise performance of the LTC1065 measured with a 1kHz pure sine wave input. Curve A shows the dynamic range for $V_{IN} \leq 2V_{RMS}$ (5.6Vp-p) being limited by wideband noise. Harmonic distortion dominates over noise for input voltages ranging from $2V_{RMS}$ up to $4.2V_{RMS}$. The outstanding

continued on page 31

Table 1. CMR data, f_{CLK} = 100kHz

Power Supply	ΔV_{IN}	–40°C	25°C	85°C	25°C (V_{OS} Nulled)
±2.5V	±1.8V	84dB	83dB	80dB	83dB
±5V	±4V	82dB	78dB	77dB	78dB
±7.5V	±6V	80dB	77dB	76dB	80dB

The above data is valid for clock frequencies up to 800kHz, 900kHz, 1MHz for V_S = ±2.5V, ±5V, and ±7.5V respectively

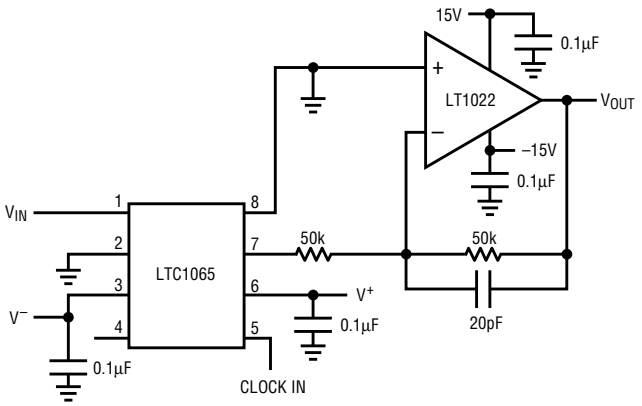


Figure 7. Typical connection for dynamic range measurement

The World's First Low-Cost Micropower, 12-Bit ADCs in SO-8 Packages

by William C. Rempfer and Marco Pan

Introduction

Small, low-cost, battery-powered electronic instruments are appearing everywhere. Examples include cellular phones, hand-held scanners, pen-based computers, and a host of others. Designers of these new systems face unbelievable challenges as they struggle to provide ever increasing performance and battery life in smaller and lighter packages at ever lower costs.

Many of these systems require internal A/D conversion. Some applications, such as digitizing the pen-screen input in pen-based computers, have A/D converters at their very cores. Others use ADCs more peripherally, to monitor voltages or other parameters inside the instrument. Regardless of the use of the ADC, it has been difficult to obtain small ADCs at low enough power levels and prices.

Fortunately, relief is here in the form of the world's first 12-bit, micropower ADCs in SO-8 packages: the LTC1286 and LTC1298. These two converters provide the micropower, small-size, low-cost conversion sought after by system designers. This article discusses these two new converters and some of their benefits.

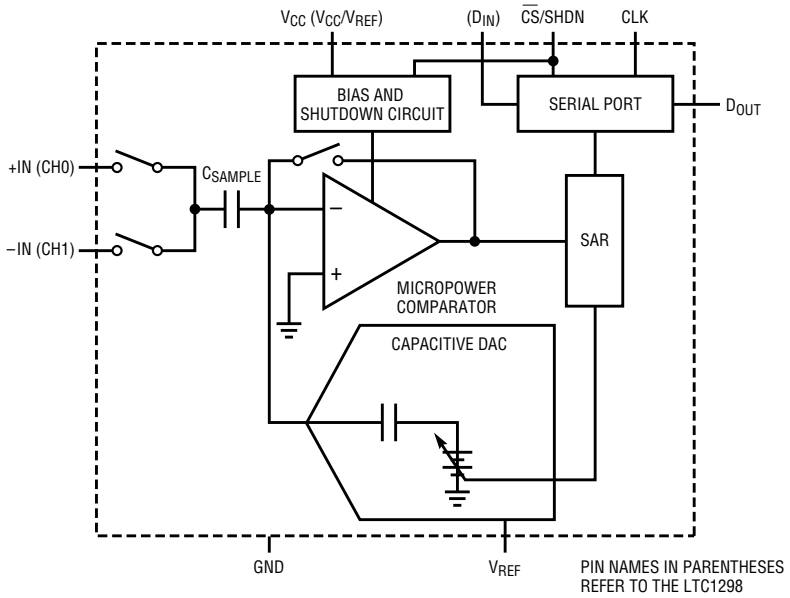


Figure 1. Micropower design of the ADC's comparator achieves a supply current of only 250 microamps for the LTC1286 (340 microamps for the LTC1298). Auto-shutdown between conversions saves even more power as sample rate is reduced

Micropower and 12-Bits in an SO-8 Package

The LTC1286 and LTC1298 add to LTC's SO-8 family of ADCs (see Table 1). They are 12-bit upgrades of the popular 8-bit, micropower LTC1096/LTC1098, which were also the first of their kind in SO-8 packages. The block diagram of Figure 1 shows the successive approximation (SAR) architecture. The pinouts of the LTC1286 and LTC1298 are similar, as shown in Figure 2. Both converters contain sample-and-holds and have serial inputs and outputs. The LTC1286 is a single-channel device with differential inputs. The LTC1298 is a two-channel device. The channel selection is made with the digital input pin (D_{IN}). The LTC1286 draws only 250 microamperes from a single 5V supply when running at full speed. Both devices also feature automatic shutdown, which reduces the current to 1 nanoamp (typical) whenever the ADC is not converting. This reduces power consumption as the sample rate is reduced (see Figure 3). The LTC1286 samples at a maximum of 12.5ksps, whereas the LTC1298 samples at a maximum rate of 11.1ksps. At an average sample rate

Table 1. The 12-bit LTC1286/LTC1298 add to LTC's growing family of SO-8 packaged ADCs

	Resolution	Sample Rate	Supply Current at f_s max	Auto Shutdown	SO-8 Package
LTC1096	8 bits	33ksps	100µA*	✔	✔
LTC1098	8 bits	33ksps	100µA*	✔	✔
LTC1196	8 bits	1Msps	8µA		✔
LTC1198	8 bits	750ksps	8µA*	✔	✔
LTC1286	**12 bits**	**12.5ksps**	**250µA***	✔	✔
LTC1298	**12 bits**	**11.1.ksps**	**340µA***	✔	✔

*Auto shutdown reduces supply current at lower rates

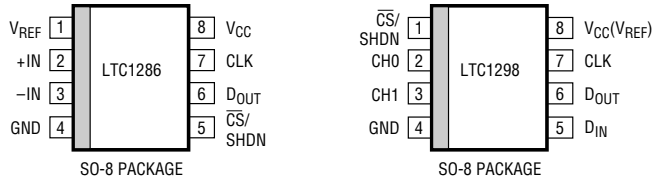


Figure 2. The extremely small size of these converters makes them popular in compact designs

of 1ksps, the supply current drops to around 20 microamps. During long idle periods when no conversions are being requested, the supply current is zero.

Benefits

Lowest Power Dissipation and Auto-Shutdown

No 12-bit ADCs offer lower power dissipation than the LTC1286/LTC1298. The power dissipation automatically adjusts to the sample rate as needed. When converting rapidly, the converter stays on continuously, but when the conversion rate drops, the auto-shutdown reduces the power to give the lowest possible overall power dissipation (see Figure 3). Battery-powered designs will benefit tremendously from this automatic power optimization. It is totally transparent to the user.

Good DC Performance

The DC specs include excellent differential non-linearity (DNL) of ±3/4 LSB, as required by pen-screen and other monitoring applications. No missing codes are guaranteed over temperature.

Tiny Configuration

You can't find a smaller 12-bit ADC anywhere. The tiny SO-8 design is even more attractive because it can be used with a single, surface mount bypass capacitor (1µF or less). The serial interface saves board space and package pins on the processor. A sample configuration is shown in Figure 4. For ratiometric applications, such as the pen screen, the reference input can be tied to the sensor drive. In these cases, an external voltage reference is not required. For absolute reference applications, the devices can be used with an external reference, which sets the span of the ADCs. The ADCs can be powered directly from the external reference if desired, eliminating the need for a separate voltage regulator.

Low Cost Solution

Reaching the required size and power levels provides only two-thirds of the solution. The final area is cost. To keep system cost low, the ADC contains everything required except the reference (which is not necessary in many target applications). The serial port makes a very space-efficient interface and significantly reduces cost in isolated applications. The high-impedance analog inputs can digitize many sensors and signals directly without needing buffer amplifiers. Finally, the ADCs themselves are very attractively priced, making them the ideal choice for new designs.

Conclusion

The new LTC1286 and LTC1298 are the lowest power, smallest 12-bit ADCs anywhere. They can make the job of the designer of hand-held instruments much easier by solving the A/D conversion problem in the space, power, and cost budget required. They will find their way into many applications in this exciting new area. LT

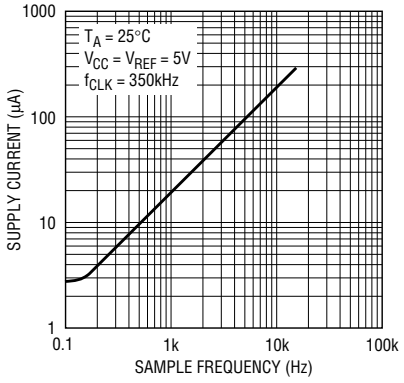


Figure 3. Automatic power shutdown between conversions saves power as sample rate is reduced

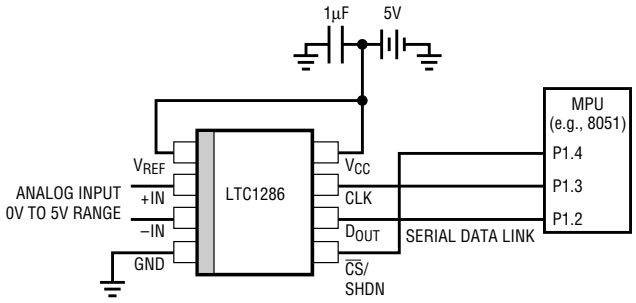


Figure 4. The SO-8 package, serial I/O and no external components make this the smallest possible ADC configuration

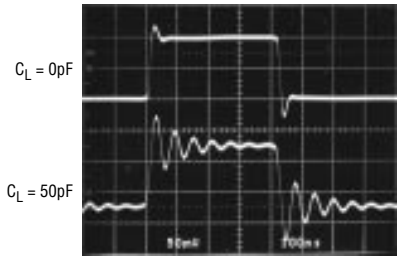


Figure 2. Medium-speed, non-LTC op amp shown with C_L = 0pF and C_L = 50pF. V_s = ±15 V, A_v = +1, R_L = 5K

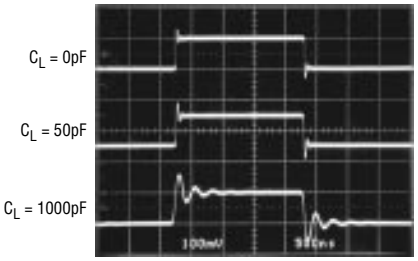


Figure 3. LT1355 voltage-feedback amplifier shown with C_L = 0pF, C_L = 50pF and C_L = 1000pF. V_S = ±5V, A_V = +1, R_L = 5K

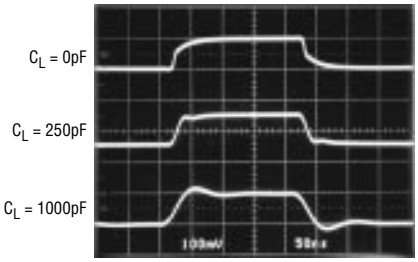


Figure 4. LT1206 current-feedback amplifier shown with C_L = 0pF, C_L = 250pF and C_L = 1000pF. V_S = ±15V, A_V = +1, R_F = 3K, R_L = 5K, C_{COMP} = 0.01µF

C-Load™, continued from page 1

become unstable with even small amounts of capacitance. Figure 2 shows an example of a competitor's medium-speed device, which is sensitive to capacitive loading. With the 5kΩ load, the transient response shows no sign of instability, but when 50pF is paralleled with the 5kΩ, the response exhibits considerable ringing. With a 75pF load, the device oscillates.

By comparison, the transient responses of the 12MHz LT1355 voltage-feedback amplifier and the 60MHz LT1206 current-feedback amplifier (Figures 3 and 4) show the improvement in stability achieved by C-Load™ op amps. Each device maintains a stable transient response, even with 1000pF of C_{LOAD}.

The Solution— Maintaining Stability

LTC's new family of voltage-feedback amplifiers adjusts the frequency response of the op amp to maintain adequate phase margin regardless of the capacitive load. Thus, the amplifiers cannot oscillate. These C-Load™ amplifiers are great in systems where the load is not fixed or is ill defined. Examples include driving coaxial cables that may be unterminated, driving twisted-pair transmission lines, and buffering the inputs of sampling A-to-D converters that present time varying impedances. Table 1 lists LTC's *unconditionally stable* voltage-feedback C-Load™ amplifiers. Table 2 lists other voltage-feedback C-Load™ amplifiers that are stable with loads up to 10,000pF.

All LTC op amps that allow the bandwidth to be adjusted as a function of the capacitive load can be stabilized. This approach is feasible on current-feedback amplifiers where the bandwidth is set by the external feedback resistor. The proper value of feedback resistor is selected for the desired C_L. Graphs of feedback resistor versus C_L for values up to 1000pF appear on the data sheets of most of the current-feedback amplifiers in the LTC catalog. The LT1206 current-feedback amplifier provides the additional enhancement of an internal compensation network around the output stage, which can be connected with an external bypass capacitor. This current-feedback amplifier has a 250mA output-current capability and can easily drive loads up to 10,000pF. Table 3 lists LTC's current-feedback amplifiers that can be stabilized with a simple modification to the feedback resistor.

How Amplifiers are Made Stable with All Capacitive Loads

The basic approach used to accommodate all capacitive loads is to first create a high-frequency, high-gain amplifier in a single gain stage, using LTC's advanced, complementary-bipolar process. To this amplifier, we add a network that effectively senses the amplifier's C_L and adjusts the bandwidth, and therefore the phase margin, accordingly.

The C-Load™ block diagram in Figure 5 illustrates this approach. The input voltage is converted to differential currents by a transconductance stage. The differential currents are then mirrored off each

Table 1. Unity-gain stable C-Load™ amplifiers stable with all capacitive loads

Singles	Duals	Quads	GBW (MHz)	I_S/Amp (mA)
LT1200	LT1201	LT1202	11	1
LT1220	——	——	45	8
LT1224	LT1208	LT1209	45	7
LT1354	LT1355	LT1356	12	1
LT1357	LT1358	LT1359	25	2
LT1360	LT1361	LT1362	50	4
LT1363	LT1364	LT1365	70	6

Table 2. Unity-gain stable C-Load™ amplifiers stable with $C_L \leq$ 10,000pF

Singles	Duals	Quads	GBW (MHz)	I_S/Amp (mA)
LT1012	——	——	0.6	0.4
——	LT1112	LT1114	0.65	0.32
LT1097	——	——	0.7	0.35
——	LT1457	——	2.0	1.6

Table 3. Current-feedback amplifiers with adjustable bandwidth

Singles	Duals	Quads	GBW (MHz)	I_S/Amp (mA)
LT1217	——	——	10	1
LT1223	——	——	100	6
LT1227	——	——	140	10
——	LT1229	LT1230	100	6
LT1252	——	——	100	10
LT1206	——	——	60	20

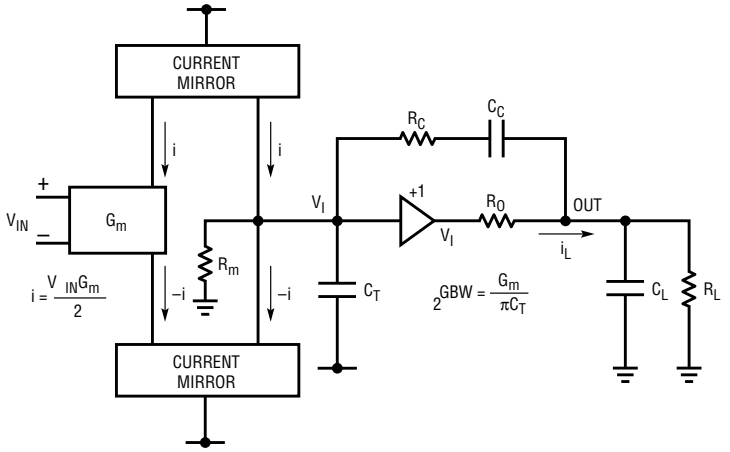


Figure 5. Block diagram of C-Load™ amplifier

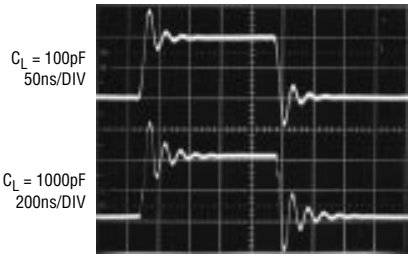


Figure 6. LT1360 shown with C_L = 100pF and C_L = 1000pF. V_{IN} = 100mVp-p, V_S = ±15V, A_V = +1, R_L = 5K

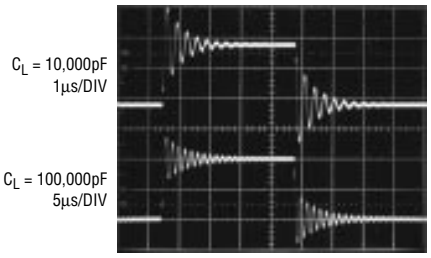


Figure 7. LT1360 shown with C_L = 10,000pF and C_L = 100,000pF. V_{IN} = 100mVp-p, V_S = ±15V, A_V = +1, R_L = 5K

supply rail to the high impedance node V_I. The output impedance of the mirrors is high, so the gain, $G_m \times R_m$, is typically greater than 10,000. The capacitor C_T and the output impedance of the current mirrors R_m form the dominant pole for the amplifier. The bandwidth is determined by the input transconductance G_m and the compensation capacitor C_T, as noted previously. A unity-gain buffer with an output impedance R_O isolates the high-impedance node from the load. Phase shifts through the mirrors and the input and output stages add to the 90 degrees from the dominant pole, resulting in a phase margin of 40–60 degrees, depending on the particular amp.

The network R_CC_C exploits bootstrapping to adjust the amplifier compensation as a function of output loading. Looking at the block diagram, observe that the voltage that appears across the network is the voltage drop across the output impedance I_LR_L. With no load on the output, no voltage differential appears across the network, so no current flows through the network and the network does not affect the frequency response of the amplifier. The heavier the output loading, the greater the current in the network and the larger the effect of the network. At the limit, with very heavy loads and at frequencies near the unity-gain cross, the network R_CC_C appears effectively in parallel with the compensation capacitor C_T. The overall effect of R_CC_C on the response is to reduce the bandwidth and to add a pole-zero pair as C_L is increased. The bandwidth reduction improves the phase margin by moving the unity-gain cross away from the output pole, and the added pole-zero pair compensates for some of the phase lag. The added zero ensures that the total phase lag can never exceed 180 degrees (corresponding to zero phase margin), even for very large load capacitances, and that the amplifier remains stable.

Figures 6 and 7 show a set of transient responses illustrating the effect of the compensation network. The device, the LT1360 (a 50MHz amplifier) is loaded with 100pF, 1000pF, 10,000pF (0.01µF), and 100,000pF (0.1µF). As the capacitive loading is increased, the transient responses show increasing overshoots and ringing, but, as discussed previously, some phase margin is always maintained, even for a 0.1µF load.

Conclusions

Linear Technology has developed families of medium- and high-speed amplifiers that are much easier to apply than their predecessors. Stable operation with capacitive loads can be achieved without critical external components or loss of output drive. These C-Load™ operational amplifiers are designed to be the next generation of standard amplifiers because they are stable under any capacitive loading condition. They are ideal for applications where the load is not well defined, and can simplify even low frequency designs by ensuring stability under all conditions of loading. LT

DESIGN IDEAS

A Simple 300mA NiCad Battery Charger 17
Randy G. Flatness

A Perfectly Temperature-Compensated Battery Charger 18
Mitchell Lee and Kevin Vasconcelos

All-Surface-Mount, Programmable VPP Generator for PCMCIA.... 19
Jon A. Dutra

Clock-Tunable Bandpass Filter Operates to 160kHz in Single-Supply Systems 20
Philip Karantzalis

A Fully Isolated, Quad, 4A High-Side Switch..... 21
Milton Wilcox

A Single-Cell Barometer 22
Jim Williams and Steve Pietkiewicz

LT1074/LT1076 Adjustable 0V to 5V Power Supply 23
Kevin Vasconcelos

Clock-Synchronized Switching Regulator has Coherent Noise 24
Jim Williams, Sean Gold, and Steve Pietkiewicz

Isolated High-Side Driver 25
James Herr

Using Super Op Amps to Push Technological Frontiers: an Ultra-Pure Oscillator 26
Dale Eagar

High Efficiency 5V to 3.3V/1.25A Converter 29
Randy G. Flatness

RS485 Repeater Extends System Capability 30
Mitchell Lee

±5V Converter Uses Off-the-Shelf, Surface-Mount Coil 32
Mitchell Lee and Kevin Vasconcelos

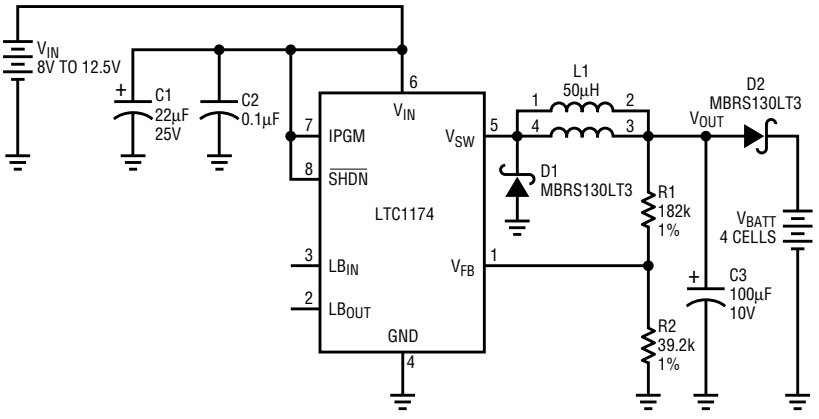
A Simple 300mA NiCad Battery Charger

by Randy G. Flatness

Low-current battery charger circuits are required in hand-held products such as palmtop, pen-based, and fingertip computers. The charging circuitry for these applications must use surface mount components and consume minimal board space. The circuit shown in Figure 1 meets both of these requirements.

The circuit shown in Figure 1 uses an LTC1174 to control the charging circuit. A fully self-contained switching regulator IC, the LTC1174 contains both a power switch and the control circuitry (constant off-time controller, reference voltage, error amplifier, and protection circuitry). The internal power switch is a P-channel MOSFET transistor in a common source configuration; consequently, when the switch turns on, the LTC1174's V_{SW} pin is connected to the input voltage. This power switch handles peak currents of 600mA. The LTC1174's architecture allows the LTC1174 to achieve 100% duty cycle, forcing the internal P-channel MOSFET on 100% of the time.

When the batteries are being charged, the resistor divider network (R1 and R2) forces the LTC1174's feedback pin (V_{FB}) below 1.25V, causing the LTC1174 to operate at the maximum output current. An internal 100mΩ resistor senses this current and sets it at approximately 300mA, according to equation 1 (shown on the schematic). When the batteries are disconnected, the error amplifier drives the feedback pin to 1.25V, limiting the output voltage to 7.0V. Diode D2 prevents the batteries from discharging through the divider network when the charger is shut down. In shut-down mode, less than 10 microamps of supply current is drawn from the input supply.



C1 = AVX (TA) TPSD226M025R0200 ESR = 0.200 I_{RMS} = 0.775A
C3 = AVX (TA) TPSD107M010R0100 ESR = 0.100 I_{RMS} = 1.095A
D1, D2 = MOTOROLA SCHOTTKY VBR = 30V
L1 = COILTRONICS CTX50-2P DCR = 0.212 IDC = 0.729A TYPE 52 CORE

COILTRONICS (407) 241-7876

$V_{OUT} = 1.25V \bullet (1 + R1/R2) = 7.0V$

$$\text{FAST CHARGE} \approx 0.6A - \frac{(V_{BATT} + 0.6V) \bullet 4\mu s}{2 \bullet L} \quad \text{(EQ.1)}$$

Figure 1. Four cell, 300mA, LTC1174 battery charger implemented with all surface-mount components

A Perfectly Temperature-Compensated Battery Charger

by Mitchell Lee and Kevin Vasconcelos

Battery charging circuits are usually greeted with a yawn, but this lead-acid charger offers a combination of features that sets it apart from all others. It incorporates a low-dropout regulator, temperature compensation, dual-rate charging, true negative ground, and consumes zero standby current.

The LT1083 family of linear regulators exhibits dropout characteristics of less than 1.5V, as compared to 2.5V in standard regulators. A smaller regulator drop allows for lower input voltages and less power dissipation in the regulator. In this application the regulator is used to control charging voltage and limit maximum charging current.

The temperature compensation employed in this circuit, unlike diode-based straight-line approximations, follows the true curvature of a lead-acid cell. This prevents over- or under-charging of the battery during periods of extended low or high ambient temperatures. Temperature compensation is conveniently provided by a Tempsistor® as shown in Figure 1. The Tempsistor is used to generate a temperature-dependent current, which, in turn, adjusts the charger's output voltage to match that of the battery. The match is within 100mV for a 12V battery over a range of –10 degrees C to +60 degrees C. The best place for the Tempsistor is directly under the battery, with the battery resting on a pad of styrofoam.

Q1 provides a low voltage disconnect function, which reduces the charger standby current to zero. When the input voltage (from a rectified transformer) is available, Q1 is biased ON and Q2 is turned ON. Q2 connects the various current paths on the output of the regulator to ground, activating the charging circuitry. If the input voltage is removed, Q1 and Q2 turn off, and all current paths from the battery to ground (except for the load, of course) are interrupted. This prevents unnecessary battery drain when the charging source is not available.

A dual-rate charging characteristic is achieved by means of a current-sense resistor (R_S) and a sense comparator (LT1012). If the battery-charge current exceeds the float-current threshold of $10mV/R_S$, the comparator pulls the gate of Q3 low, increasing the output voltage by 600mV. This sets the charging voltage to 14.4V at 25 degrees C. After the battery reaches full charge, the

continued on page 31

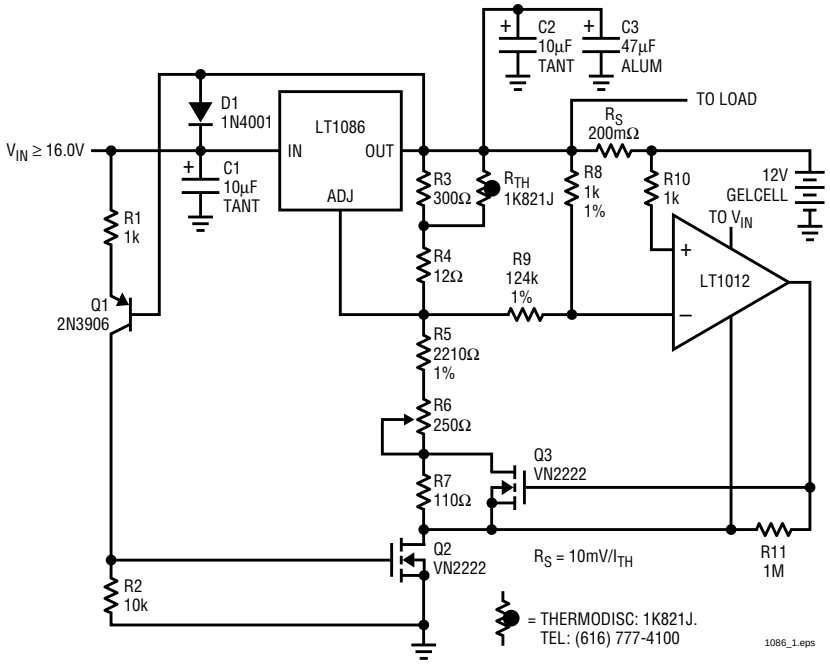


Figure 1. Battery charger follows temperature coefficient of a lead-acid cell very accurately

Tempsistor® is a registered trademark of Thermodisc Inc.

All-Surface-Mount, Programmable 0, 3.3V, 5V, and 12V VPP Generator for PCMCIA

by Jon A. Dutra

Generating the VPP voltage for a PCMCIA port in laptop computers has become more complicated with PCMCIA standard 2.0. The VPP line must come up to +5V initially until the card "tupple" tells the card its type and VPP voltage. For example, a 3.3V SRAM card must have VPP adjusted to 3.3V. If it is a flash memory card, +12V must be supplied during programming. During card insertion, zero volts is desirable to unconditionally prevent latch-up. Shutdown supply current must be as low as possible, and the supply must not overshoot. This Design Idea presents a circuit (Figure 1) that meets these specifications. The same topology could be useful for generating other programmable supplies.

The circuit uses the LT1107 micropower DC-to-DC converter with a single surface-mount transformer. The LT1107 features an I_{LIM} pin which enables direct control of maximum inductor current. This allows use of a smaller transformer without risk of saturation. The LT1111 could also be used, with a reduction in output power.

Circuit Operation

The circuit is basically a gated-oscillator flyback topology. The SET pin of the LT1107 is held at 1.25V by negative feedback. Summing currents into the SET pin to zero for the three different output states yields three equations with three unknown resistor values. The resistor values are easily solved for using Mathametica, MathCad, or classical techniques.

Output noise is reduced by using the auxiliary gain block (AGB) in the feedback path. This added gain effectively reduces the hysteresis of the comparator and tends to randomize output noise. With a low ESR capacitor for C1, output noise is below 30mV over the output load range.

Output power increases with $V_{BATTERY}$, from about 1.4W out with 5V in to about 2W out with 8V or more. Efficiency is 62% to 76% over a broad output power range. No minimum load is required.

Component Selection

Substantial current flows through C_{IN} and C_{OUT}. Most tantalum capacitors are not rated for current flow and can result in field failures. Using a rated tantalum or rated electrolytic will result in longer system life.

Shutdown

The circuit is shut down by using two sections of the CD4066 in parallel as a high-side switch. Alternatively, simply disabling the logic supply to the V_{IN} and I_{LIM} nodes of the LT1107 will shut it down. This drops quiescent current from the $V_{BATTERY}$ input below 2µA. When the device is shut down, V_{OUT} drops to zero volts.

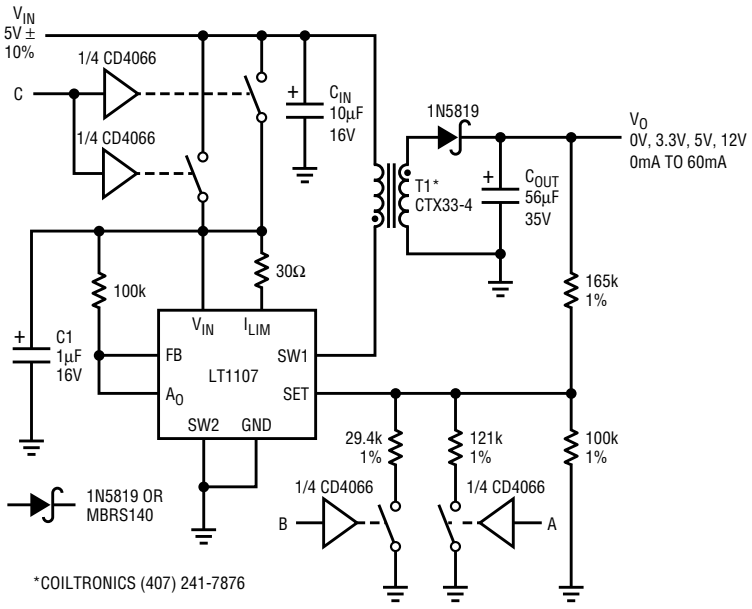


Figure 1. Schematic diagram for VPP generator

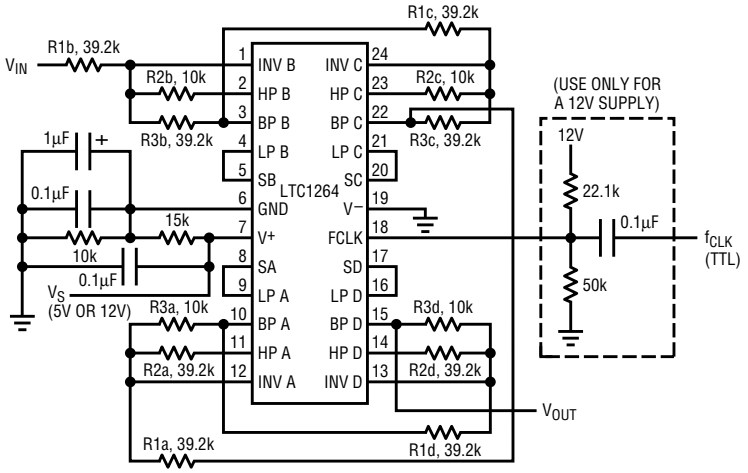
Clock-Tunable Bandpass Filter Operates to 160kHz in Single-Supply Systems

by Philip Karantzalis

When the only available power supply in a system is 5V or 12V and a precision bandpass filter is needed at cutoff frequencies greater than 20kHz, the LTC1264 switched-capacitor active-filter building block can be configured to realize an eighth-order bandpass filter accurate to ±1% or better over temperature (–40 degrees C to 85 degrees C). Figure 1 is a schematic diagram of an eighth-order bandpass filter tunable with a TTL clock signal to any center frequency up to 70kHz with a 5V supply or to 100kHz with a 12V supply. The clock-frequency-to-center-frequency ratio is 20:1. The gain response for a 50kHz bandpass filter is shown in Figure 2 and the input dynamic range with a 5V supply is shown in Figure 3.

The passband frequency range (the frequency range where the filter's attenuation is 3dB or less) is equal to the center frequency divided by ten. The stopband attenuation reaches 60dB at twice the center frequency and at one-half the center frequency. The typical gain variation at the center frequency is ±0.5dB at 25 degrees C and ±1.5dB over temperature. (Note that an additional ±0.4dB should be added to account for the gain variation due to the 1% resistors). If the operating temperature range is 25 degrees C (±20 degrees C) and the power supply voltage can be controlled to ±2%, the center frequency can be extended to 90kHz for a 5V supply or 160kHz for a 12V supply. Note that the gain error for center frequencies greater than 70kHz with a 5V supply and greater than 100kHz with a 12V supply increases from 1dB to 7dB. Therefore, the value of resistor R1 for each LTC1264 section should be increased to reduce the error to ±1dB (see the table in Figure 1).

If the power supply for this filter is a switching regulator, the regulator's output noise can appear at the filter's output if the center frequency of the filter is tuned to the noise frequency of the regulator. This is due to the filter's low power-supply rejection near its center frequency. The LTC1264 is not a low-power device. The typical quiescent current is 11mA with a 5V supply or 18mA with a 12V supply.



V_S	f_{CENTER}	R1 (EACH SECTION)
5V	80kHz	42.2k
5V	90kHz	47.5k
12V	120kHz	40.2k
12V	140kHz	42.2k
12V	160kHz	47.5k

Figure 1. Single-supply bandpass filter

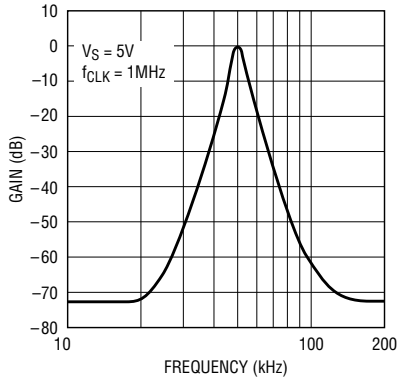


Figure 2. LTC1264 single 5V supply, 50kHz bandpass response

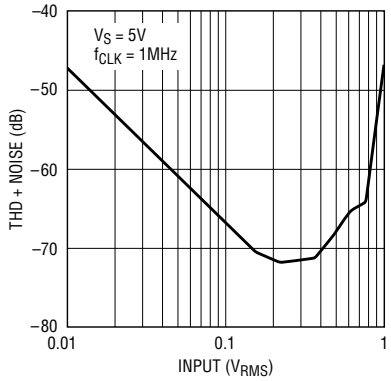


Figure 3. Dynamic range vs. input signal. LTC1264 single 5V supply, 50kHz bandpass filter

A Fully Isolated, Quad, 4A High-Side Switch

by Milton Wilcox

High-side switching in hostile environments often requires isolation to protect the controlling logic from transients on the "dirty" power ground. The circuit shown in Figure 1 drives and protects four low $R_{DS(ON)}$ power MOSFET switches over a wide operating supply range. The LT1161 drivers are protected from transients of up to 60V on the supply pins and 75V on the gate pins. Fault indication is provided by an inexpensive logic gate.

Each of the four LT1161 switch channels has a completely self-contained charge pump, which drives the gate of the N-channel MOSFET switch 12V above the supply rail when the corresponding input pin is taken high. The specified MOSFET device types have a maximum $R_{DS(ON)}$ of 28mΩ, resulting in a total switch drop (including sense resistor) of only 0.15V at 4A output current.

The LT1161 independently protects and restarts each MOSFET. It senses drain current via the voltage drop across a current shunt R_S. When the current in one switch exceeds approximately 6A (62mV/0.01Ω), the switch is turned off without affecting the other switches. The switch remains off for 50ms (set by external timing capacitor C_T), after which the LT1161 automatically attempts to restart it. If the fault is still present, this cycle repeats until the fault is removed, thus protecting the MOSFET. Current shunts are readily available in both through-hole and surface-mount case styles. AN53 has additional information on shunts.

The highest MOSFET dissipation occurs with a "soft short" (one in which the current is above the normal operating level, but still below the current-limit threshold). This can cause dissipation in Figure 1's circuit to rise, in the worst case, to 2W, requiring modest heatsinking. When an output is directly shorted to ground, the average dissipation is very low because the MOSFET conducts only during brief restart attempts.

Fault indication is provided by a low-cost exclusive-NOR gate. In normal operation, a low on the LT1161 input forces a low on the output, and a high forces a high. If an input is high and the corresponding output is low (i.e., short circuited), the output of the exclusive-NOR gate activates the isolated fault output. Similarly, by adding resistor R_{OL}, the low-input/high-output state can be used to diagnose an open-load condition. Adjusting the value of R_{OL} sets the output current at which the load is considered to be open. For example, in Figure 1, with V_{SUPPLY} = 24V, a fault would be indicated if the load could not sink 10mA.

Figure 1's circuit is ideal for driving resistive or inductive loads, such as solenoids. However, the circuit can be tailored for capacitive or high inrush loads as well. Consult the LT1161 data sheet for information on programming current limit, delay time, and automatic-restart period to handle other loads. The LT1161 is available in both DIP and surface-mount packaging.

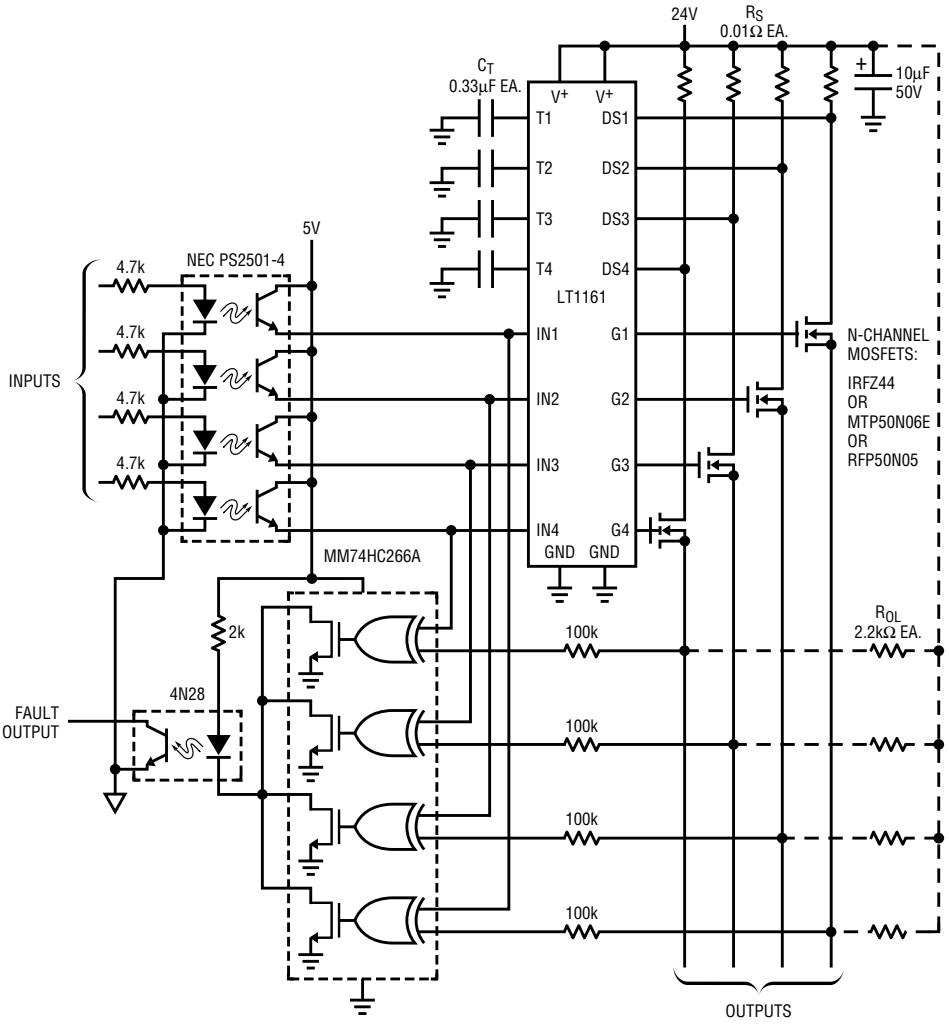


Figure 1. Protected quad high-side switch has isolated inputs and fault output

A Single-Cell Barometer

by Jim Williams and
Steve Pietkiewicz

Figure 1, a complete barometric pressure signal conditioner, operates from a single 1.5V battery. Until recently, high accuracy and stability have been obtainable only with bonded strain gage and capacitively based transducers, which are quite expensive. This design, using a recently introduced semiconductor transducer, achieves .01"Hg (inches of mercury) uncertainty over time and temperature. The 1.5V powered operation permits portable application.

The 6kΩ transducer (T1) requires precisely 1.5mA of excitation, necessitating a relatively high voltage drive. A1's positive input senses T1's current by monitoring the voltage drop across the resistor string in T1's return path. A1's negative input is fixed by the 1.2V LT1004 reference. A1's output biases the 1.5V powered LT1110 switching regulator. The LT1110's switching produces two outputs from L1. Pin 4's rectified and filtered output powers A1 and T1. A1's output, in turn, closes a feedback loop at the regulator. This loop generates whatever voltage step-up is required to force precisely 1.5mA through T1. This arrangement provides the required high-voltage drive while minimizing power consumption. This occurs because the switching regulator produces only enough voltage to satisfy T1's current requirements.

L1 pins 1 and 2 source a boosted, fully floating voltage, which is rectified and filtered. This potential powers A2. Because A2 floats with respect to T1, it can look differentially across T1's outputs, pins 10 and 4. In practice, pin 10 becomes "ground" and A2 measures pin 4's output with respect to this point. A2's gain-scaled output is the circuit's output, conveniently scaled at 3.000V = 30.00"Hg.

To calibrate the circuit, adjust R1 for 150mV across the 100Ω resistor in T1's return path. This sets T1's current to the manufacturer's specified calibration point. Next, adjust R2 at a scale factor of 3.000V = 30.00"Hg. If R2 cannot capture the calibration, reselect the 200kΩ resistor in series with it. If a pressure standard is not available, the transducer is supplied with individual calibration data, permitting circuit calibration.

This circuit, compared to a high-order pressure standard, maintained .01"Hg accuracy over months with widely varying ambient pressure shifts. Changes in pressure, particularly rapid ones, correlated quite nicely to changing weather conditions. Additionally, because .01"Hg corresponds to about 10 feet of altitude at sea level, driving over hills and freeway overpasses becomes quite interesting. The circuit pulls 14mA from the battery, allowing about 250 hours operation from one D cell.

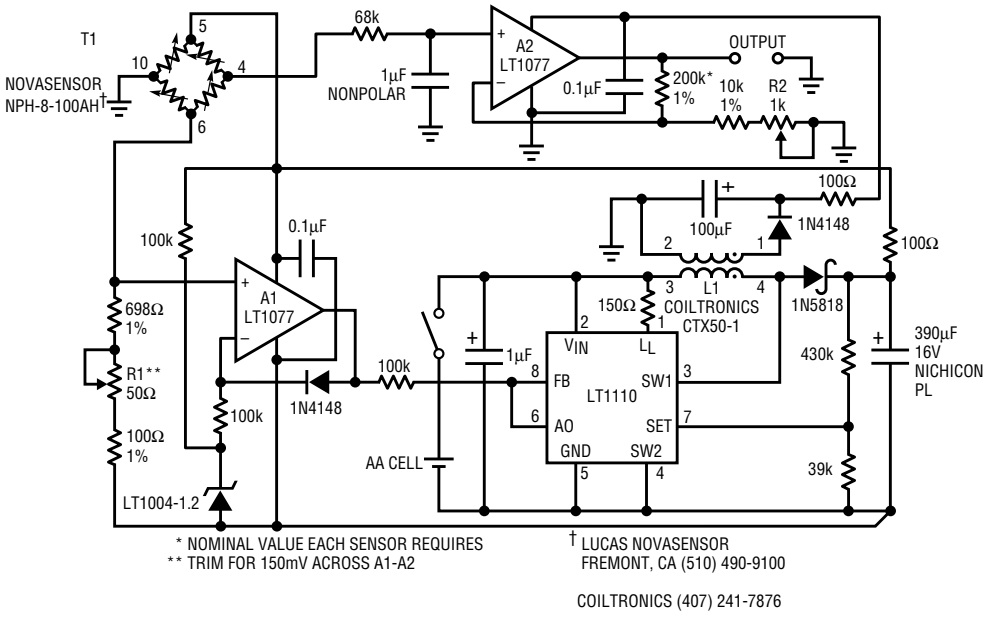


Figure 1. Schematic diagram: single-cell barometer

LT1074/LT1076 Adjustable 0V to 5V Power Supply

by Kevin Vasconcelos

Linear regulator ICs are commonly used in variable power supplies. Common types, such as the 317, can be adjusted as low as 1.25V in single-supply applications. At low output voltages, power losses in these regulators can be a problem. For example, if an output current of 1.5A is required at 1.25V from an input of 8V, the regulator dissipates more than 10W. Figure 1 shows a DC-to-DC converter that functionally replaces a linear regulator in this application. The converter not only eliminates power loss as a concern, but can be adjusted for output voltages as low as 25mV while still delivering an output current of 1.5A.

The circuit of Figure 1 employs a basic positive-buck topology with one exception: a control voltage is applied through R4 to the feedback summing node at pin 1 of the LT1076 switching regulator IC, allowing the output to be adjusted from 0 to approximately 6V. This encompasses the 3.3V and 5V logic-supply ranges as well as battery-pack combinations of one to four D cells.

As R4 is driven from 0V to 5V by the buffer (U1), more or less current is required from R2 to satisfy the loop's desire to hold the feedback summing point at 2.37V. This forces the converter's output to swing over the range of 0V to 6V.

Figure 2 shows a comparison of power losses for a linear regulator and the circuit of Figure 1. The load current is 1.5A in both cases, although the LT1076 is capable of 1.75A guaranteed output current in this application, and 2A typical. If more current is required, the LT1074 can be substituted for the LT1076. This change accommodates outputs up to 5A, but at the expense of a heftier diode and coil (D1, L1). An MBR735 and Coiltronics CTX50-2-52 are recommended for 5A service.

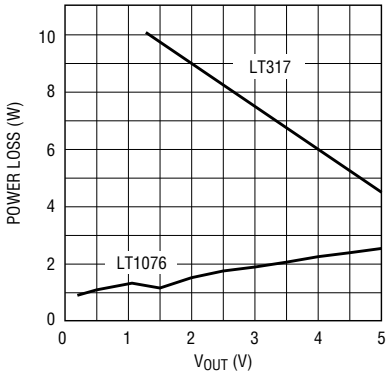


Figure 2. Power loss comparison: linear regulator vs. Figure 1's circuit

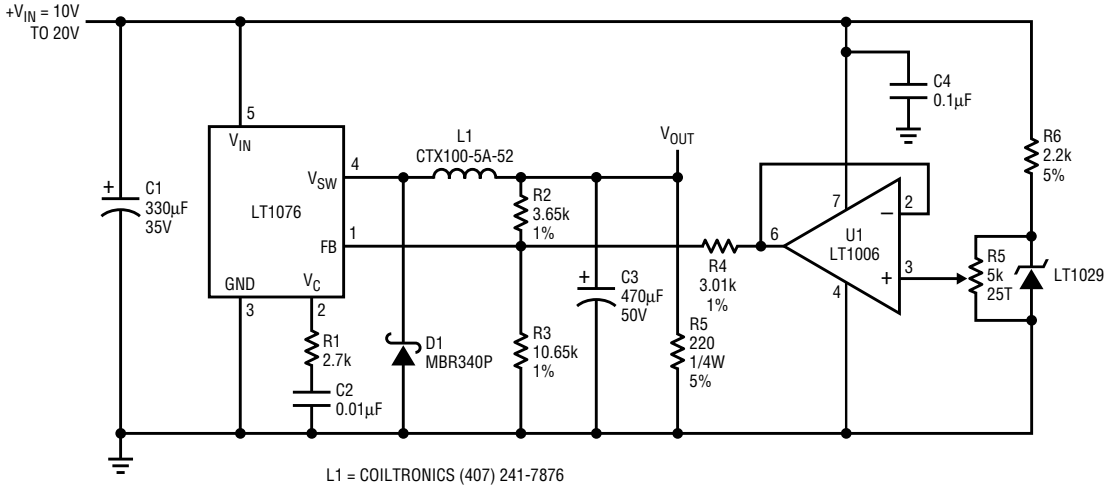


Figure 1. Adjustable LT1074/1076 0V to 5V power supply

Clock-Synchronized Switching Regulator has Coherent Noise

by Jim Williams, Sean Gold, and Steve Pietkiewicz

Gated-oscillator-type switching regulators permit high efficiency over extended ranges of output current. These regulators achieve this desirable characteristic by using a gated-oscillator architecture instead of a clocked pulse-width modulator. This eliminates the "housekeeping" currents associated with the continuous operation of fixed-frequency designs. Gated-oscillator regulators simply self-clock at whatever frequency is required to maintain the output voltage. Typically, loop-oscillation frequency ranges from a few hertz into the kilohertz region, depending upon the load.

This asynchronous, variable frequency operation seldom creates problems; some systems, however, are sensitive to this characteristic. The circuit in Figure 1 slightly modifies a gated-oscillator-type switching regulator by synchronizing its loop-oscillation frequency to the system's clock. In this fashion the oscillation frequency and its attendant switching noise, although variable, are made coherent with system operation.

Circuit operation is best understood by temporarily ignoring the flip-flop and assuming that the LT1107 regulator's A_{OUT} and FB pins are connected. When the output voltage decays, the set pin drops below V_{REF}, causing A_{OUT} to fall. This causes the internal comparator to switch high, biasing the oscillator and output transistor into conduction. L1 receives pulsed drive, and its flyback events are deposited into the 100µF capacitor via the diode, restoring output voltage. This overdrives the set pin, causing the IC to switch off until another cycle is required.

The frequency of this oscillatory cycle is load dependent and variable. If a flip-flop is interposed in the A_{OUT}–FB pin path, as shown, the frequency is synchronized to the system clock. When the output decays far enough (trace A, Figure 2) the A_{OUT} pin (trace B) goes low. At the next clock pulse (trace C) the flip-flop Q2 output (trace D) sets low, biasing the comparator-oscillator. This turns on the power switch (V_{SW} pin is trace E), which pulses L1. L1 responds in flyback fashion, depositing its energy into the output capacitor to maintain

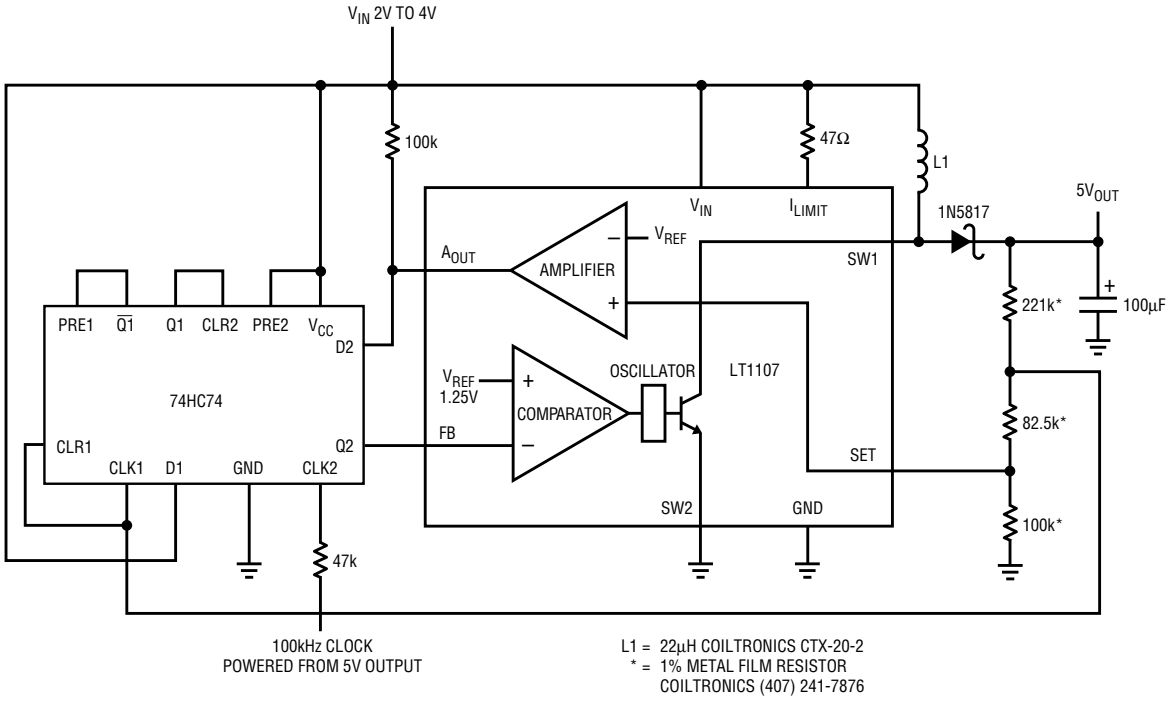


Figure 1. A synchronizing flip-flop forces switching regulator noise to be coherent with the clock

output voltage. This operation is similar to the previously described case, except that the sequence is forced to synchronize with the system clock by the flip-flop's action. Although the resulting loop's oscillation frequency is variable, it, and all its attendant switching noise, are synchronous and coherent with the system clock.

Because of its sampled nature, this clocked loop may not start. To ensure start-up, the flip-flop's remaining section is connected as a buffer. The CLR1–CLK1 line monitors output voltage via the resistor string. If the circuit does not start, Q1 is asserted, CLR2 sets, and loop operation commences. Although the circuit shown is a step-up type, any switching regulator configuration can use this technique. LT

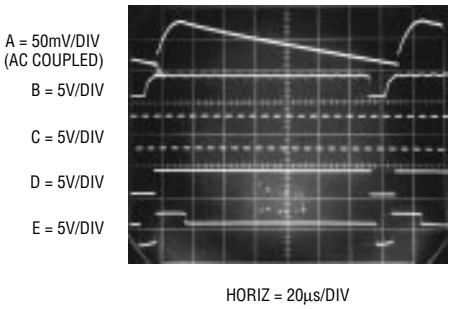


Figure 2. Waveforms for the clock-synchronized switching regulator. The regulator switches (trace E) only on clock transitions (trace C), resulting in clock-coherent output noise (trace A)

An Isolated High-Side Driver

by James Herr

Introduction

The LTC1146 low-power digital isolator draws only 70µA of supply current with V_{IN} = 5V. Its low supply current feature is well suited for battery-powered systems that require isolation, such as an isolated high-side driver. The LTC1146A is rated at 2500V_{RMS} and is UL approved. The LTC1146 is intended for less stringent applications. It is rated at 500VDC.

Theory of Operation

Opto-isolators available today require supply currents in the milliampere range even for low-speed operation (less than 20kHz). This high supply current is another drain on the battery. Figure 1 shows the alternative of using an LTC1146A to drive an external power MOSFET (IRF840) at speeds to 20kHz with V+ = 300V.

The input pin of LTC1146A must be driven with a signal that swings at least 3 volts (referred to GND1, which is a floating ground). The O_S pin outputs a square wave corresponding to the input signal, but with a time delay. The amplitude of the output square wave is equal to the potential at the V_{CC} pin. The TL4426 is a high-speed MOSFET driver used here to supply gate-drive current to the power MOSFET. The power supply to the LTC1146A and the TL4426 is bootstrapped from a 13V supply referred to system ground. C1 supplies the current to both the LTC1146A and the TL4426 when the power MOSFET is being turned on. Its value should be increased when the input signal's ON time increases. D3 prevents the output from swinging negative due to stray inductance. If the output goes below ground, the gate-to-source voltage of the IRF840 rises. This high potential could damage the power MOSFET. The output slew rate should be limited to 1000V/µs to prevent glitches on the O_S output of the LTC1146A. LT

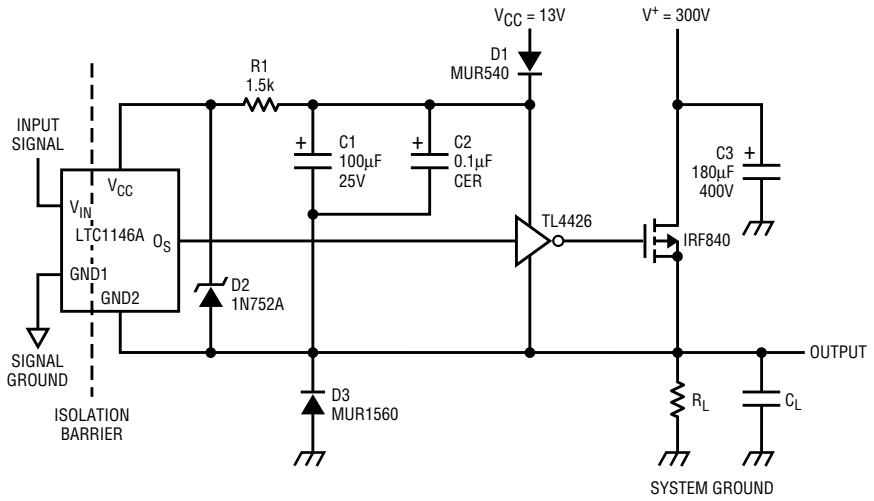


Figure 1. Isolated high-side driver schematic diagram

Using Super Op Amps to Push Technological Frontiers: an Ultra-Pure Oscillator

by Dale Eagar

The advent of high-speed op amps allows the implementation of circuits that were impossible just a few years ago. This design idea describes a new topology that makes use of these new high-speed circuits and makes astounding improvements in their performance. An oscillator using such op amps has distortion limits beyond our ability to measure.

An Ultra-Low-Distortion, 10kHz Sine-Wave Source for Calibration of 16-Bit or Higher Analog-to-Digital Converters

The path to low distortion in an amplifier or an oscillator begins with amplifiers with the lowest possible open-loop distortion and lots of excess-open loop gain in the frequency band of interest. The next step is closing the loop, thereby reducing open-loop distortion by an amount approximately equal to the loop gain. This is not easy, as certain stability criteria must be met by an amplifier that isn't an oscillator or by an oscillator that oscillates at a specified frequency.

The trick used in this circuit is to build an amplifier that has excessive gain where it is needed but no excess gain or phase shift where it isn't. In many applications the band from DC to 100kHz requires the above mentioned high gain; the gain should fall off when the open-loop gain falls through unity (around 5MHz). How this is done in the flesh (silicon) is shown here.

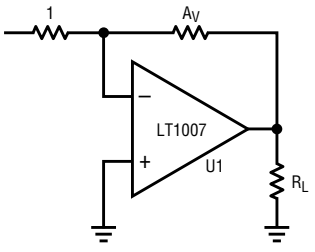


Figure 1. Conventional inverting op amp topology

Circuit Operation and Circuit Evolution

A standard inverting amplifier topology, as shown in Figure 1, has a finite open-loop gain in the frequency band of interest (see Figure 2), with some open-loop harmonic distortion (about –60dB), and an open-loop output impedance of about 70 ohms.

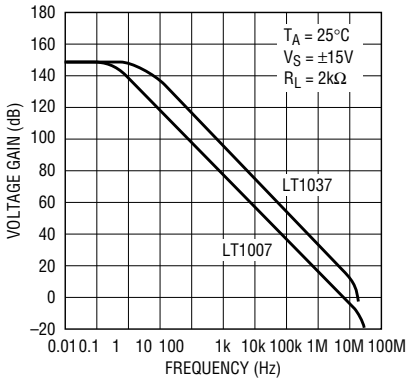


Figure 2. Voltage gain vs. frequency

The amplifier shown in Figure 1 can achieve low distortion, but since the circuit has a limited loop gain, the curative effects of feedback can only be taken so far. The designer must also be careful to ensure that R_L is many times higher than the open-loop output impedance of U1.

Figure 3's circuit makes several improvements over the circuit of Figure 1. First, the open-loop gain of U1 is multiplied by $A_V(f)$, the gain of the composite amplifier stage A1. Second, the input impedance of A1 can be made very high, further improving both open-loop gain of U1, and the open-loop harmonic distortion of U1.

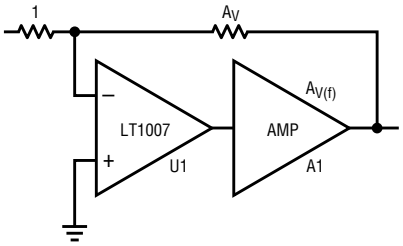


Figure 3. LT1007 followed by composite amplifier A1

Third, the output voltage swing of U1 is decreased, keeping its output circuitry in its lowest distortion area.

The composite circuit, A1, consists of three sections. The first section, as seen in Figure 4, has the gain/phase plot shown in Figure 6. Note the high gain at 10kHz (60dB), and the gain of 6dB at 5MHz, with only 17 degrees of phase contribution. In fact, this looks so nice that you might ask, "why not use two?," and thus reduce your distortion by an additional 60dB?

The second section, shown in Figure 5, has the gain/phase plot shown in Figure 7. Note that here the gain doesn't change significantly, but the phase is positive just where we want it (1–5MHz) to allow a very stable system to be built.

The third section, as you might guess, is the same as the first. In sum, the gain/phase plot of the composite amplifier A1 is shown in

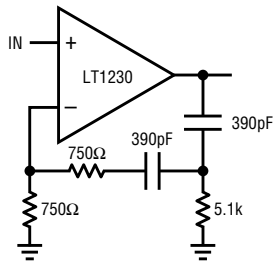


Figure 4. First section of composite amplifier A1

Figure 8. Note the gain, which is in excess of 120db at 10kHz, and the total phase contribution of about –20 degrees at 5MHz. The complete gain block is shown in Figure 9.

Super Gain-Block Oscillator Circuitry

When A1, as described above, is connected with U1, as shown in Figure 3, the resulting circuit is not only unity-gain stable, but has open-loop gain of 180dB at 10kHz (yes, 1 billion). This means that the closed-loop harmonic distortion can easily be kept in the region of "parts per billion."

A Wien bridge oscillator with harmonic distortion in the parts per billion is shown in Figure 10. The super op amps S1 and S2 are the previously described composite amplifiers as shown in Figure 9. Note that the output is taken between the two outputs of S1 and S2. This topology gives the best signal-to-noise ratio, in addition to balancing the power supply currents and their harmonics. Taking the output from one amplifier's output to ground is also valid.

To align the circuit, first center the output amplitude adjustment potentiometer. Next, adjust the gain trim for oscillation while also adjusting the output amplitude for 5Vp-p output (single ended). Next, adjust the gain trim to 1Vp-p at the output of the LT1228. Finally, connect a spectrum analyzer to the output of the LT1228 and adjust the second harmonic trim potentiometer for a null in the second harmonic of the oscillator frequency. The measurement of the harmonic distortion of this oscillator defies all of our resources, but appears to be well into the parts-per-billion range. LT

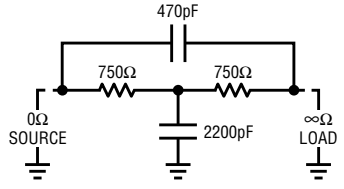


Figure 5. Second section of composite amplifier A1

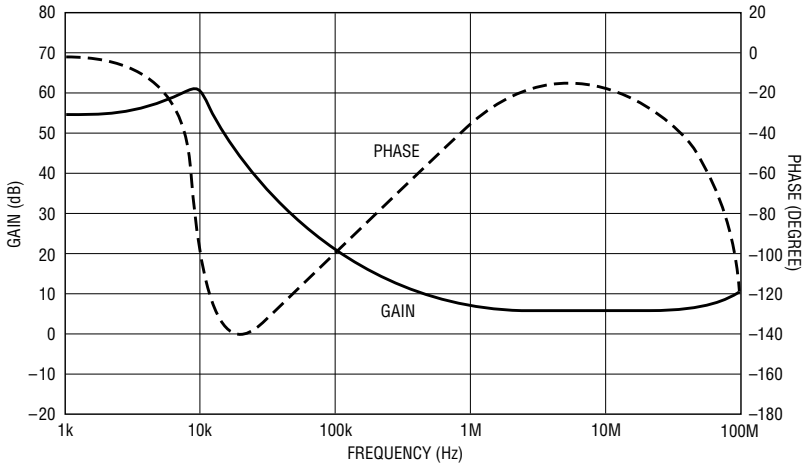


Figure 6. Gain/phase response of circuit shown in Figure 4

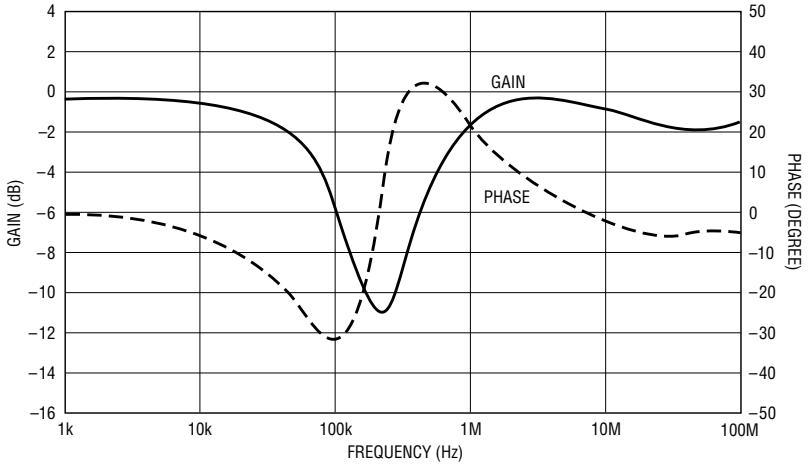


Figure 7. Gain/phase response of circuit shown in Figure 5

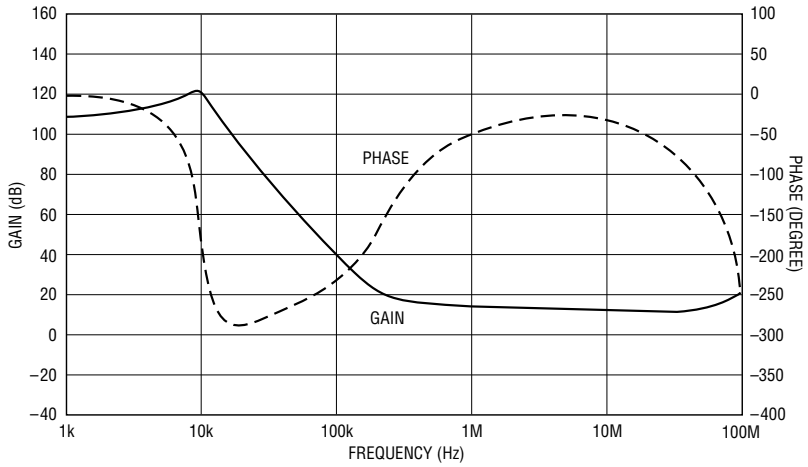


Figure 8. Gain/phase response of composite amplifier A1 (shown in Figure 3)

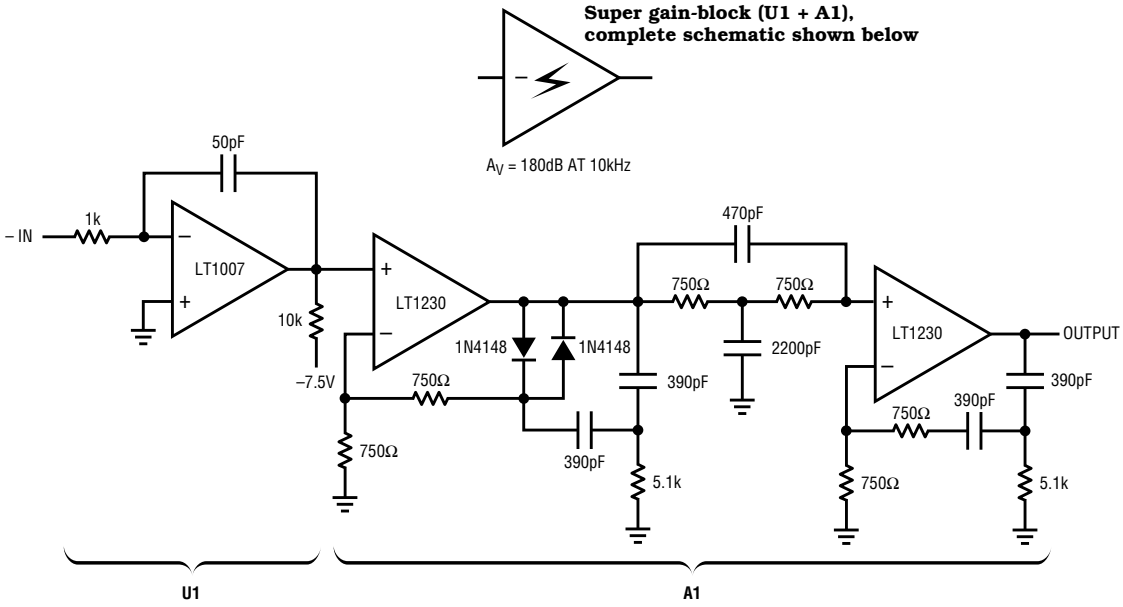


Figure 9. Schematic diagram—super gain-block S1 and S2

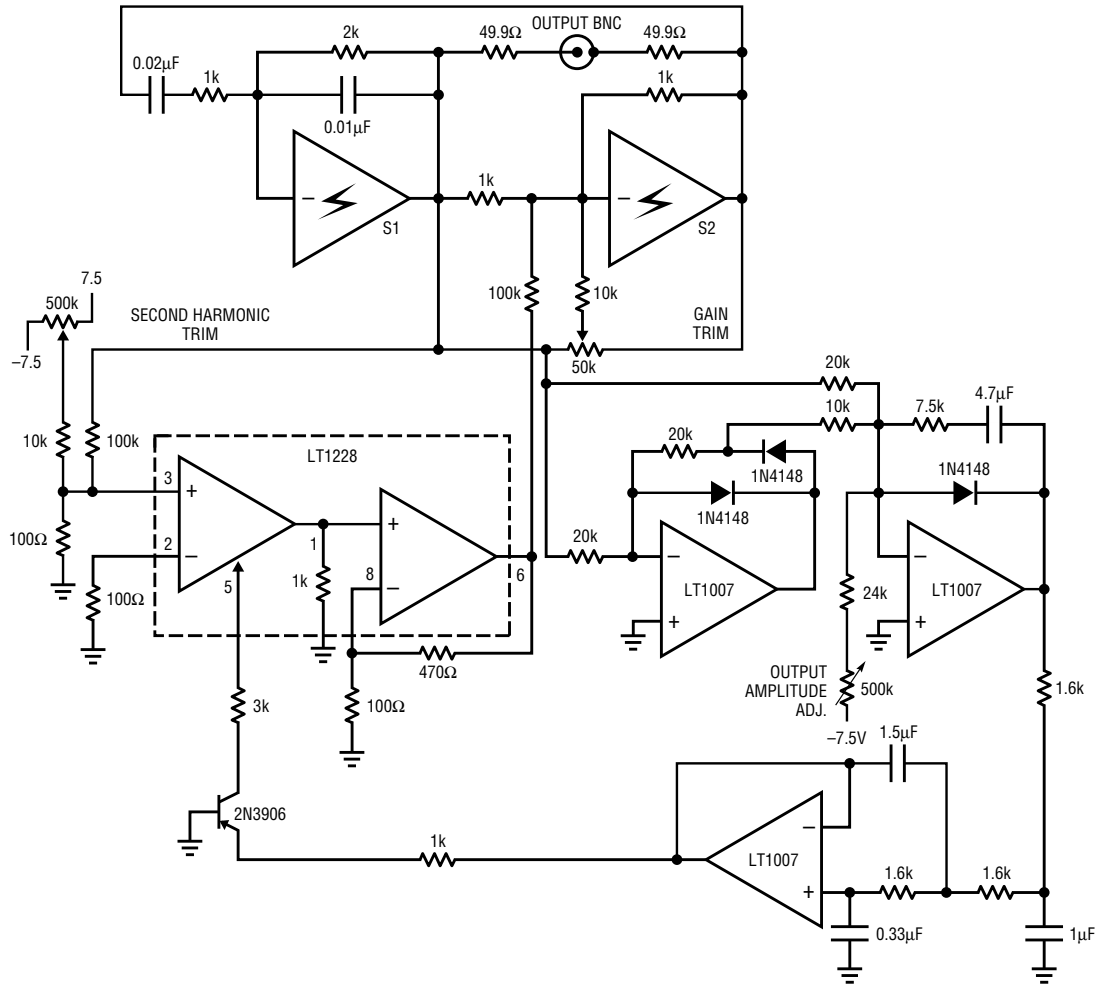


Figure 10. Schematic diagram—Wien bridge oscillator with distortion in the parts-per-billion range

High Efficiency 5V to 3.3V/1.25A Converter in 0.6 Square Inches

by Randy G. Flatness

The next generation of notebook and desktop computers will incorporate a growing number of 3.3V ICs along with 5V devices. As the number of 3.3V devices increases, the current requirements increase. Typically, a high-current 5V supply is already available. Thus, the problem is reduced to deriving 3.3V from 5V at high efficiency in a small amount of board space.

High efficiency is mandatory in these applications since converting 5V to 3.3V at 1.25A using a linear regulator would require dissipating over 2W. This is an unnecessary waste of power and board space for heatsinking.

The LTC1147 SO-8 switching-regulator controller accomplishes the 5V to 3.3V conversion with high efficiencies over a wide load current range. The circuit shown in Figure 1 provides 3.3V at efficiencies greater than 90% from 50mA to 1.25A. Using all surface-mount components and a low value of inductance (10µH) for L1, the circuit of Figure 1 occupies only 0.6 square inches of PC board area. The efficiency of the circuit in Figure 1 is plotted in Figure 2.

At an output current of 1.25A the efficiency is 90.4%; this means only 0.4W are lost. This lost power is distributed among R_{SENSE}, L1, and the power MOSFETs; thus heatsinking is not required.

The LTC1147 series of controllers use constant off-time current-mode architecture to provide clean start-up, accurate current limit, and excellent line and load regulation. To maximize the operating efficiency at low output currents, Burst Mode™ operation is used to reduce switching losses.

The P-channel MOSFET in the circuit of Figure 1 will be ON 2/3 of the time with an input voltage of 5V. Hence, this device should be carefully selected to obtain the best performance. This design uses an Si9433DY for optimum efficiency; for lower cost, an Si9340DY can be used at a slight reduction in performance.

The circuit in Figure 1 has a no-load current of only 160µA. In shutdown with pin 6 held high (above 2V), the quiescent current is reduced to less than 20µA with the MOSFET held off. Although the circuit in Figure 1 is specified at a 5V input voltage, the circuit will function from 4V to 10V.

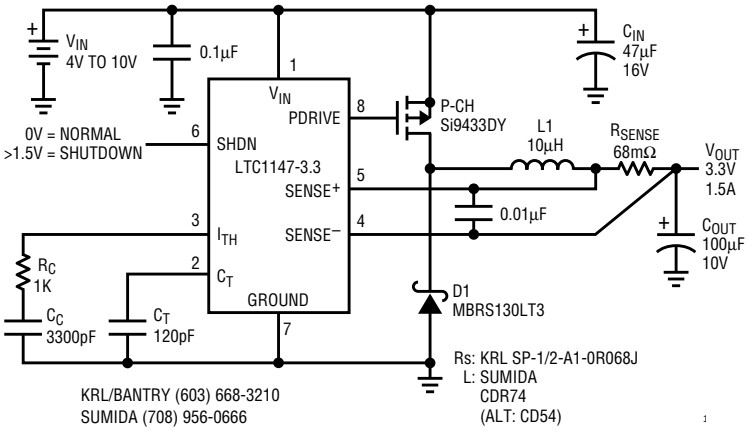


Figure 1. High-efficiency controller converts 5V to 3.3V in minimum board area

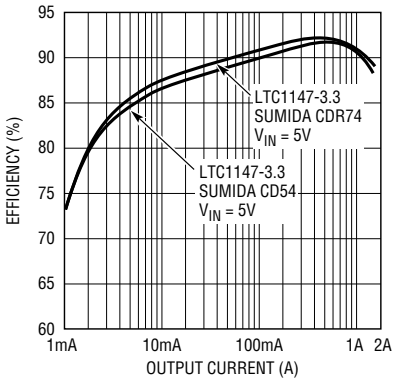


Figure 2. 5V to 3.3V conversion efficiency

RS485 Repeater Extends System Capability

by Mitchell Lee

RS485 data communications are specified for distances of up to 4000 feet. This limit is the consequence of losses in the twisted pair used to carry the data signals. Beyond 4000 feet, skin effect and dielectric losses take their toll, attenuating the signal beyond use.

If greater distances must be covered, some means of repeating the data is necessary. One method is to terminate a long run of cable with a microprocessor-based node capable of relaying data to yet another length of cable.

A simpler solution is shown in Figure 1. Two RS485 transceivers are connected back-to-back so as to relay incoming data from either side to the other. A pair of cross-coupled one-shots furnish a means of "flow control" so that one and only one transmitter is turned on at any given time. Incoming data is sensed by detecting a 1–0 transition at the output of either idling receiver. The first receiver to spot such a transition triggers its associated one-shot, which, in turn, activates the opposite transmitter and ensures smooth data flow from one side to the other. At the same time, the one-shot locks out the other receiver/transmitter/one-shot combination, so that only one data path is open.

The one-shot is retriggered by successive 1–0 transitions and start bits, holding the data path in this configuration. The one-shot time constant is set slightly greater than the interval between any two start bits. When the received data stops, the line idles high, producing a 1 at the receiver's output. The one-shot resets, returning the opposite transceiver to the receive mode—ready for any subsequent data flow.

In order to allow adequate time for the one-shot to reset, the software protocol must wait one word length after the end of any data transmission before responding to a call or initiating a new conversation. As shown, the repeater is set up for 100k baud data rates and an 8-bit word length (plus start and stop bits).

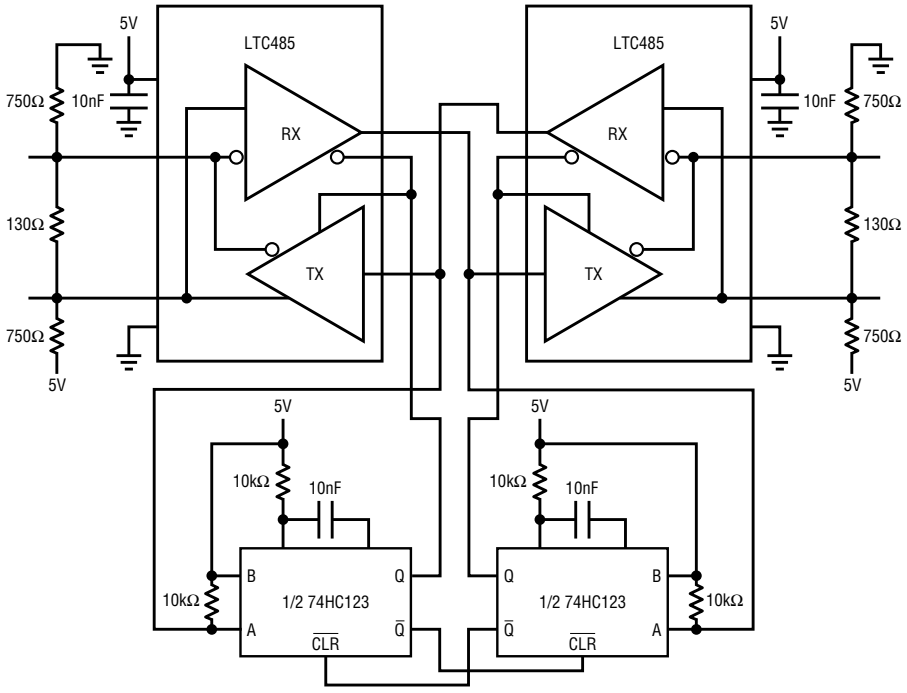


Figure 1. RS485 repeater schematic diagram

Notebook Power Supply, continued from page 7

that determine the maximum input voltage of the circuit are the power MOSFETs, the LTC1142, and the input capacitors. With the LTC1142 replaced by an LTC1142HV, an 18V typical (20V maximum) input voltage is allowable. Since the gate-drive voltages supplied by the LTC1142 and LTC1142HV are from ground to V_{IN}, the input voltage must not exceed the maximum V_{GS} of the MOSFETs. The MOSFETs specified in Figure 2 have an absolute maximum of 20V, matching that of the LTC1142HV.[1] Finally, the input capacitor's voltage rating will also have to be increased above 25V.

Conclusion

The LTC1142/LTC1142HV are ideal for supplying dual 3.3V and 5V output voltages with high efficiencies over a wide load-current range. High performance current-mode architectures with Burst Mode™ operation provide an extremely well behaved and highly efficient solution. With the addition of an auxiliary winding and an LT1121, an additional 12V output can be derived, making a complete power supply for notebook computers (shown in Figure 3) or other battery-operated devices. For additional high efficiency circuits, see Application Note 54. LT

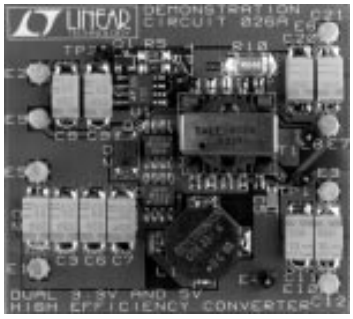


Figure 3. Demonstration board photograph

[1] For improved efficiency, C_{T5} should be changed to 270pF.

LTC1065 continued from page 12

performance shown by curve A holds for cutoff frequencies below about 14kHz. Above 14kHz the dynamic range will be limited mainly by distortion, as shown by curve B.

Conclusions

The LTC1065 offers significant advantages over exisiting monolithic lowpass filters. The AC specifications offer device matching in both amplitude and phase, eliminating cumbersome trimming and calibration. The internal oscillator eliminates the need for an external clock and the associated problems of routing a digital signal into an analog PC board area. At cutoff frequencies below 14kHz, the dynamic range of the filter allows operation in 14-bit systems. The filter's DC accuracy eliminates the need for offset adjustment, even in systems that do not require such accuracy. Finally, the LTC1065 can handle DC input voltages with up to 12 bits of gain linearity. A fine filter indeed. LT

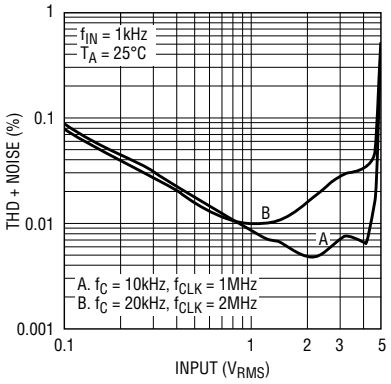


Figure 8. THD + noise vs. input voltage (V_s = ±7.5 V)

Charger, continued from page 18

current will fall below the 10mV/R_S threshold and the LT1012 will short out R7, reducing the output by 600mV to a float level of 13.8V. Both the float and charging voltages can be trimmed by R6; R7 sets the 600mV difference between them.

With the charging source connected, the sense resistor R_S measures only battery current. This eliminates the tendency found in some schemes for the charger to trip on load current.

Table 1 simplifies the selection of an appropriate regulator for batteries of up to 48 Ampere-hours (Ah). The selection is based on providing a minimum available charge current of at least C/4, where C represents the battery's Ampere-hour capacity. The next larger regulator may be required in applications where sustained load currents of greater than C/10 are expected.

If you want to set the trip current to an exact figure, the current shunt (R_S) can be calculated as R_S = 10mV/I_{TH}. For a threshold of C/100 this reduces to R_S = 1/C. LT

Table 1. The regulator should be chosen to provide at least C/4 charging current

Battery Capacity	Device	Maximum Charging Current	Float Current Threshold	Sense Resistor (Shunt)
≤3Ah	LT1117	0.8A	20mA	500mΩ
3–6Ah	LT1086	1.5A	50mA	200mΩ
6–12Ah	LT1085	3.2A	100mA	100mΩ
12–24Ah	LT1084	5.5A	200mA	50mΩ
24–48Ah	LT1083	8.0A	400mA	25mΩ

±5V Converter Uses Off-the-Shelf, Surface-Mount Coil

by Mitchell Lee and
Kevin Vasconcelos

Single-output switching regulator circuits can often be adapted to multiple-output configurations with a minimum of changes, but these transformations usually call for custom-wound inductors. A new series of standard inductors,[1] featuring quadrifilar windings allows power supply designers to take advantage of these modified circuits, but without the risks of a custom magnetics development program.

The circuit shown in Figure 1 fulfills a recent customer requirement for a 9V to 12V input, 5V/800mA and –5V/100mA output converter. It employs a 1:1 overwinding on what is ostensively a buck converter, to provide a –5V output. The optimum solution would be a bifilar-wound coil with heavy-gauge wire for the main 5V output and smaller wire for the overwinding. To avoid a custom coil design, an off-the-shelf JUMBO-PAC™ quadrifilar-wound coil is used. This family of coils is wound with 1:1:1:1 sections. In the application of Figure 1, three sections are paralleled for the main 5V winding and the remaining section is used for the –5V output. This concentrates the copper where it is needed most—on the high current output.

Efficiency with the outputs loaded at 500mA and –50mA is over 80%. Minimum recommended load on the –5V output is 1 or 2mA, and the –5V load current must always be less than the 5V load current.

[1] Coiltronics Inc. JUMBO-PAC™ (407) 241-7876

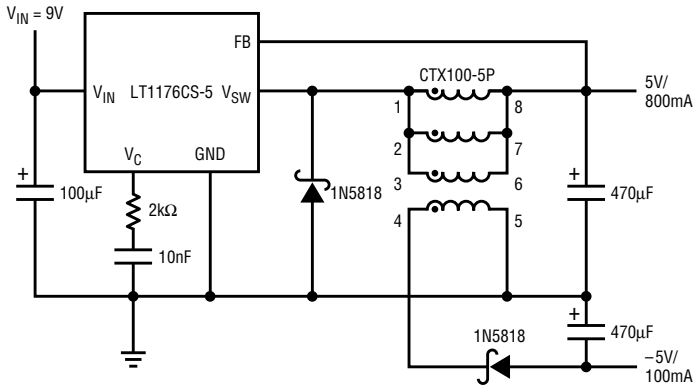


Figure 1. 5V Buck converter with –5V overwinding

Reconfigurable CMOS EIA562/RS232 and RS485 Transceivers

by Dave Dwelley

The LTC1322 and LTC1335 are low-power CMOS, two-port transceivers. Each port can be operated as either an EIA562 transceiver or an RS485 transceiver by changing the logic state at the mode-select pin. The LTC1322 and LTC1335 have two EIA562 transceivers and one RS485 transceiver per port.

Figure 1 shows RS422 and EIA562 interfaces using the LTC1322. Figure 2 shows RS485 and EIA562 interfaces using the LTC1335. Figure 3 shows RS485 and RS232 interfaces using the LTC1322 and two zener diodes, operating from +5 and ±12 volt supplies. A LocalTalk®/AppleTalk® interface using the LTC1335 is shown in Figure 4. An RS422 cable repeater application is shown in Figure 5. Figure 6 shows an interface level translation from EIA562/RS232 to RS422 levels.

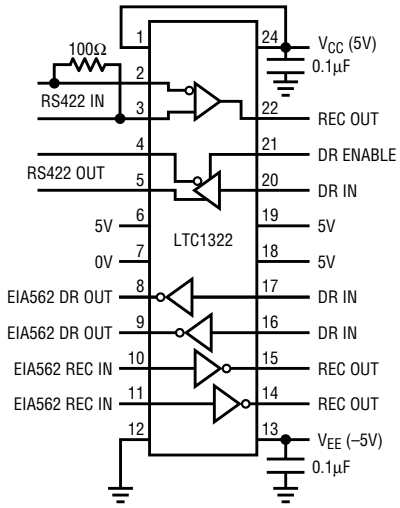


Figure 1.

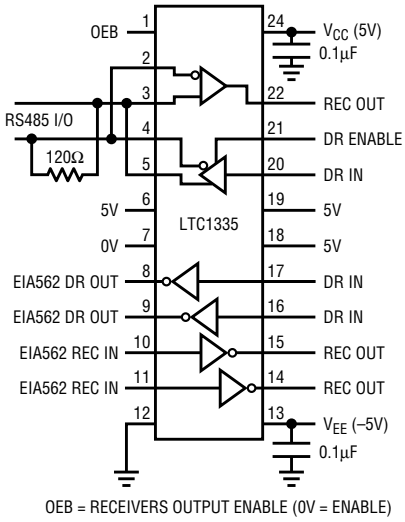


Figure 2.

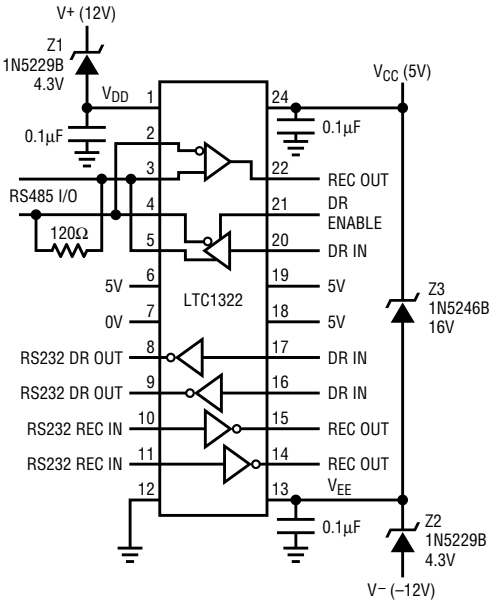


Figure 3.

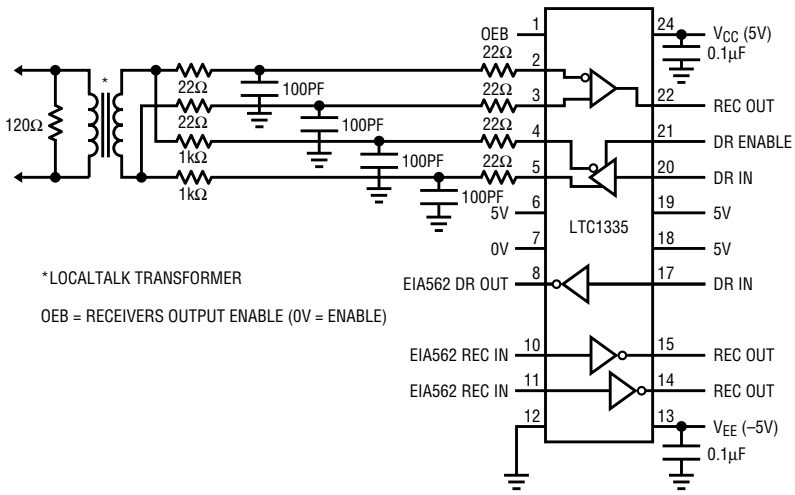


Figure 4.

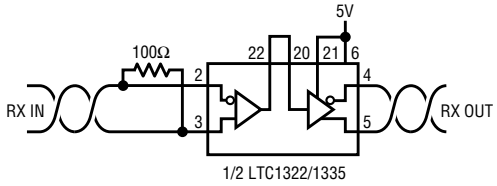


Figure 5.

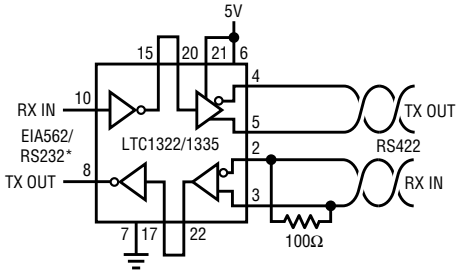


Figure 6.

LocalTalk® and AppleTalk® are registered trademarks of Apple Computer, Inc.

New Device Cameos

LTC1323 Single 5V AppleTalk® Transceiver

The LTC1323 operates from a single 5V supply with 2.4mA quiescent current when active and 1µA in shutdown mode. The device is similar to the LTC1320, but includes a charge pump to generate a –5V supply using three external capacitors. One differential transceiver drives the AppleTalk® network, and a single-ended driver and two single-ended receivers can be used to generate the handshaking signals. The charge-pump disable mode can be used to turn off all circuitry and drop I_{CC} to 65µA with one single-ended receiver remaining alive. The shutdown mode drops I_{CC} further to 1µA.

All driver outputs go into three-state mode when disabled, during shutdown, during charge pump disable mode, or when the power is off. Both the driver outputs and receiver inputs are protected against ESD damage to ±10kV. The LTC1323 is available in the 24-pin SOL package.

LTC1338 Ultra-Low-Power RS232 Transceiver

The LTC1338 five driver, three receiver RS232 transceiver is designed for 5V systems and draws only 500µA quiescent supply current, the industry's lowest power consumption.

The charge pump requires only four space-saving 0.1µF capacitors. The transceiver operates at speeds up to 120k baud with a 2500pF, 3kΩ load. It withstands repeated ESD strikes of up to ±10kV using the human body model.

The transceiver operates in one of the four modes: NORMAL, RECEIVER ALIVE, RECEIVER DISABLE, and SHUTDOWN. In NORMAL or RECEIVER DISABLE mode, supply current is only 500µA with all RS232 outputs unloaded. In SHUTDOWN mode, the supply current is reduced to below 1µA. In RECEIVER ALIVE mode, all three receivers are kept alive and the supply current is 50µA. All RS232 outputs assume high impedance states in SHUTDOWN or RECEIVER ALIVE modes or when the power is off. The receiver outputs assume high impedance states in RECEIVER DISABLE or SHUTDOWN modes.

The LTC1338 is available in 28-pin DIP, SSOP, and SOIC packages.

LTC1382, LTC1383, LTC1384 and LTC1385 RS232/RS562 Transceiver

Four new RS232/RS562 transceivers, each with two drivers and two receivers, expand LTC's line of interface circuits for PC-compatible applications. All four feature 240µA quiescent current, ±10kV ESD protection on the RS232 line pins, operation to 120k baud, and on-chip charge pump circuitry. The charge pump requires only four space-saving 0.1µF capacitors.

The LTC1382 is designed for 5V systems. In SHUTDOWN mode, all RS232 outputs assume high impedance states and the supply current is below 1µA.

The LTC1383 is similar to the LTC1382, but is available in space-saving 16-pin packages. The LTC1383 does not include a SHUDOWN mode.

The LTC1384 is another variation of LTC1382, featuring an additional RECEIVER OUTPUT DISABLE mode and two receivers alive in SHUTDOWN mode. The supply current is 35µA in SHUTDOWN mode.

The LTC1385 is designed for 3.3V systems. The transceiver has low-power SHUTDOWN and DRIVER DISABLE modes. In SHUTDOWN mode, all RS562 outputs assume high impedance states and the supply current drops below 1µA. In DRIVER DISABLE mode two receivers are kept alive and I_{CC} is only 35µA.

The LTC1382, LTC1384, and LTC1385 are available in 18-pin DIP and SOIC packages. The LTC1383 is available in 16-pin DIP and narrow SOIC packages.

Introducing the LTC1044A

The LTC1044A is a new addition to Linear Technology's growing family of CMOS, switched-capacitor voltage inverters. Compatible with the ICL7660 and LTC1044, this device gives the user an immediate solution to higher voltage applications. The voltage range in battery-powered applications can be extended, as the maximum operating supply voltage is now 12V. The inverting function ($V_{OUT} = -V_{IN}$) requires only two non-critical external capacitors. Other functions that can be implemented include doubling ($V_{OUT} = 2V_{IN}$), division ($V_{OUT} = V_{IN}/2$) or multiplication ($V_{OUT} = \pm nV_{IN}$).

High-Voltage, CMOS, Switched-Capacitor Voltage Inverter

The LTC1144 is the newest member of Linear Technology's family of CMOS, switched-capacitor voltage inverters. It boasts a wide input operating voltage range of 2V to 18V. The LTC1144 provides an easy high voltage upgrade to the ICL7660 or LTC1044. Only two non-critical external 10 microfarad capacitors are needed to generate a negative supply, such as a –15V supply from 15V. A shutdown pin has also been provided. The LTC1144 also has a BOOST pin that will shift the internal oscillator frequency from 10kHz to outside the audio band. Special internal circuitry and processing makes this part resistant to latch-up.

LTC1148HV, LTC1142HV: Ultra-High-Efficiency, Synchronous Step-Down Controllers

The single-output LTC1148HV and dual-output LTC1142HV synchronous switching regulator controllers now are available with a 20V maximum input voltage. This extends the range of applications to include 10–12 cell battery packs.

Both devices use current-mode architecture with Burst Mode™ operation to provide extremely high operating efficiency, typically greater than 90%, over the entire load range. They extend battery life by providing high efficiencies at load currents from a few milliamps (when the device is in standby or sleep mode) to amps (under full power conditions).

Each regulator employs a pair of external complementary MOSFETs and a user-programmable current-sense resistor for setting the operating current level. The LTC1142/LTC1148 families are ideal for applications requiring single or dual 3.3V and 5V supplies with the highest conversion efficiencies.

LTC7541A: 12-Bit Multiplying, Current-Output DAC

The LTC7541A is a 12-bit, current-output, four-quadrant multiplying D/A converter. It is a superior, pin-compatible replacement for the industry standard AD7541A.

INL and DNL are 1/2LSB maximum, less than 1/4LSB typical. Gain error is as low as 1LSB max, so true 12-bit absolute accuracy is obtained without trimming. For applications requiring high stability, INL temperature coefficient is typically less than .001LSB/°C and gain error is less .005LSB/°C.

As a multiplying DAC, the LTC7541A handles bipolar inputs outside the supply rails with better than –90dB THD. This makes the part suitable for programmable amplifiers and for digitally programmable attenuators and filters. For single-supply systems, the part can be connected in voltage-output mode, which yields outputs from 0V to the reference voltage.

Improvements in the LTC part include reduced sensitivity to op amp V_{OS}, TTL compatibility at 5V and 15V, and better latch-up and ESD resistance. Parasitic diodes between digital inputs and V_{DD} have been removed, easing power sequencing restrictions.

The LTC7541A comes in commercial, industrial, and military grades, and is available in DIP or surface-mount SO-18 packages.

LT1251, LT1256: 40MHz Video Fader and DC Gain Controlled Amplifier

The LT1251/LT1256 is a two input, one output, 40MHz current feedback amplifier with a linear control circuit that determines the mix of each input to the output. These parts make excellent electronically controlled variable gain amplifiers, filters, mixers and faders. The only external components required are the supply bypass capacitors and the feedback resistors. Both parts will operate on all supplies from ±2.5V (or single 5V) to ±15V (or single 30V).

In the simplest configuration, a 2.5V full scale voltage sets a 0V to 2.5V control input range, and two equal feedback resistors set the maximum gain at unity. Absolute gain accuracy is trimmed at wafer sort to minimize part to part variations. The circuit is completely temperature compensated.

The LT1251 includes circuitry that eliminates the need for accurate control signals around zero and full scale. For control signals of less than 2% or greater than 98% the LT1251 sets one input completely off and the other on. This is ideal for fader applications. The LT1256 does not have this snap on/off characteristic and operates linearly over the complete control range. The LT1256 is recommended for applications requiring more than 20dB of linear control range. LT

For further information on the above or any other devices mentioned in this issue of Linear Technology, use the reader service card or call the LTC literature-service number: 1-800-4-LINEAR. Ask for the pertinent data sheets and application notes.

LTC in the News...

LTC Posts Record Quarter

Robert H. Swanson, Jr., President and CEO of Linear Technology Corporation, announced that net sales for LTC's first quarter ended September 26, 1993 increased by 34% over the first quarter of the previous year. The company posted record high sales for $45,040,000 for the first quarter of fiscal 1994 compared to $33,602,000 for the same quarter of fiscal year 1993.

Net income performance for the company also increased to a new record level of $11,808,000 or $0.32 per share (55% over the first quarter of last year). Linear Technology also increased its cash dividend by 20%.

According to Robert H. Swanson, President and CEO, "This was our strongest summer quarter ever as we again reached record levels of financial performance. In essence, it is expert knowledge, delivered in the form of analog integrated circuits, that we market and sell.

Business Week in its November 1, 1993 report on "250 Companies on the Move" included LTC as one of two semiconductor companies. In its September 20, 1993 issue, *Fortune Magazine* selected Linear Technology for inclusion in the publication's very prestigious "Companies to Watch" section. Among "1993 Preferred Component Suppliers" *Electronic Buyers News* placed LTC in their October 18, 1993 list of the top Linear IC sellers.

For the fifth straight year *Forbes Magazine* included Linear Technology on its list of the "Best 200 small companies in America."

Finally, on November 30, 1993, *Investor's Business Daily* published a feature story headlined "Linear Technology Enjoys Strong Demand for Vital Links." The story makes the point that LTC is a source of "high-performance linear solutions to the practical problems faced by manufacturers. The company initially markets its solutions to customers' system designers and component engineers." LT

DESIGN TOOLS

Applications on Disk

NOISE DISK
This IBM-PC (or compatible) progam allows the user to calculate circuit noise using LTC op amps, determine the best LTC op amp for a low noise application, display the noise data for LTC op amps, calculate resistor noise, and calculate noise using specs for any op amp.
Available at no charge.

SPICE MACROMODEL DISK
This IBM-PC (or compatible) high density diskette contains the library of LTC op amp SPICE macromodels. The models can be used with any version of SPICE for general analog circuit simulations. The diskette also contains working circuit examples using the models, and a demonstration copy of PSPICE™ by MicroSim.
Available at no charge.

Technical Books

1990 Linear Databook — This 1440 page collection of data sheets covers op amps, voltage regulators, references, comparators, filters, PWMs, data conversion and interface products (bipolar and CMOS), in both commercial and military grades. The catalog features well over 300 devices. $10.00

1992 Linear Databook Supplement — This 1248 page supplement to the *1990 Linear Databook* is a collection of all products introduced since then. The catalog contains full data sheets for over 140 devices. The *1992 Linear Databook Supplement* is a companion to the *1990 Linear Databook*, which should not be discarded. $10.00

Linear Applications Handbook — 928 pages full of application ideas covered in depth by 40 Application Notes and 33 Design Notes. This catalog covers a broad range of "real world" linear circuitry. In addition to detailed, systems-oriented circuits, this handbook contains broad tutorial content together with liberal use of schematics and scope photography. A special feature in this edition includes a 22 page section on SPICE macromodels. $20.00

1993 Linear Applications Handbook Volume II — Continues the stream of "real world" linear circuitry initiated by the *1990 Handbook*. Similar in scope to the 1990 edition, the new book covers Application Notes 41 through 54 and Design Notes 33 through 69. Additionally, references and articles from non-LTC publications that we have found useful are also included. $20.00

Interface Product Handbook — This 200 page handbook features LTC's complete line of line driver and receiver products for RS232, RS485, RS423, RS422 and AppleTalk® applications. Linear's particular expertise in this area involves low power consumption, high numbers of drivers and receivers in one package, 10kV ESD protection of RS232 devices and surface mount packages.
Available at no charge.

Monolithic Filter Handbook — This 234 page book comes with a disk which runs on PCs. Together, the book and disk assist in the selection, design and implementation of the right switched capacitor filter circuit. The disk contains standard filter responses as well as a custom mode. The handbook contains over 20 data sheets, Design Notes and Application Notes. $40.00

SwitcherCAD Handbook — This 144 page manual, including disk, guides the user through SwitcherCAD—a powerful PC software tool which aids in the design and optimization of switching regulators. The program can cut days off the design cycle by selecting topologies, calculating operating points and specifying component values and manufacturer's part numbers. $20.00

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