Linear Technology Chronicle

November 1996 — *A Showcase of Linear Technology's Focus Products* — Vol. 5 No. 11

Products of the Month

Software-Selectable Multiprotocol Chip Set Simplifies Data Networking Interface Design

The **LTC®1343** multiprotocol transceiver and companion **LTC1344** cable terminator form a complete software-selectable multiprotocol serial port, operating from a single 5V supply. This is the first integrated solution to pass the stringent NET1 and NET2 tests of the European Telecommunications Institute.

The LTC1343 contains four drivers and four receivers and the configuration logic to do protocol selection, loopback testing as well as turning on and off the echo clock and the low power shutdown mode. The LTC1343/LTC1344 can be used in both DTE and DCE equipment. The LTC1344 cable terminator contains six switchable resistive terminations to configure a single DB-25 connector for up to eight different serial protocols. Two LTC1343 transceivers and a single LTC1344 terminator form a DTE or DCE interface port, capable of supporting RS232 (V.28), RS423 (V.10), EIA530, EIA530-A, RS449, V.35, V.36 and X.21 protocols that are both NET1 and NET2 compliant. This chip set is ideal for space limited networking applications and supports all major telecom protocols for remote access serial ports.

In a typical application, the first LTC1343 is connected to the clock and data signal lines along with the diagnostic LL (local loop-back) and TM (test mode) signals. The second LTC1343 is connected to the control signal lines along with the diagnostic RL (remote loop-back) signals. Switching between modes is simple—just three mode select pins are required for both the LTC1343 and LTC1344, as shown in Figure 1. The mode pins are latched internally to allow sharing of the select lines between multiple interface ports. DTE or DCE is set with one pin, as is the designation for whether the transceiver is used for data and clock signals or control signals. This greatly simplifies the task of switching eight different types of serial ports to the same DB-25 connector, as shown in Figure 2. Other routing tasks, such as loop-back testing or echo clocking, are also easily performed.

The LTC1343 is packaged in a 44-lead SSOP and the LTC1344 in a 28-lead SSOP. Together they eliminate the switches, relays and jumpers normally required to switch between drivers, receivers and associated termination schemes. The three chips together occupy only 8 cm^2 of board area, ideal for space constrained applications. For a data sheet and evaluation samples of this multiprotocol chip set, contact your local Linear Technology sales office.

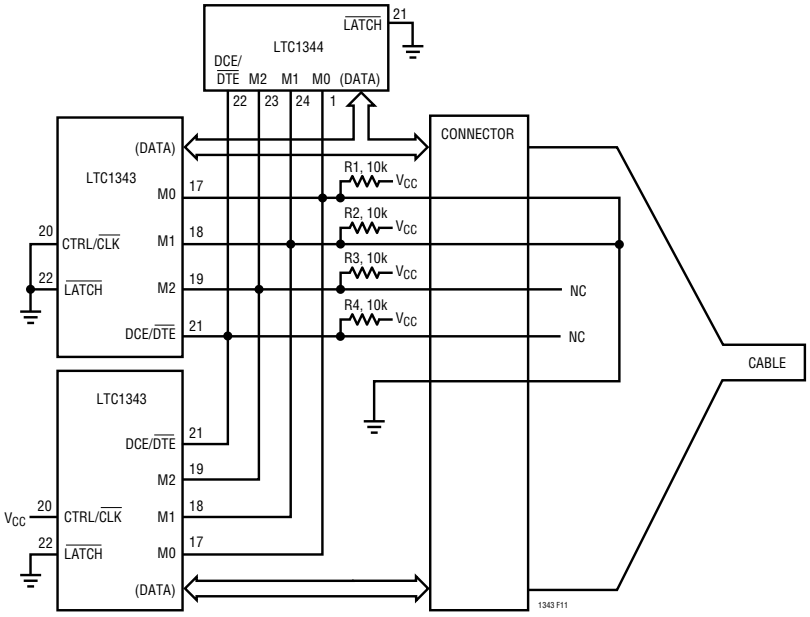

Figure 1. The LTC1343 and LTC1344 Address the Problem of Easily Switching the Terminations for Different Protocols Using a Single Connector. Here it is Configured for Single Port DCE and V.35

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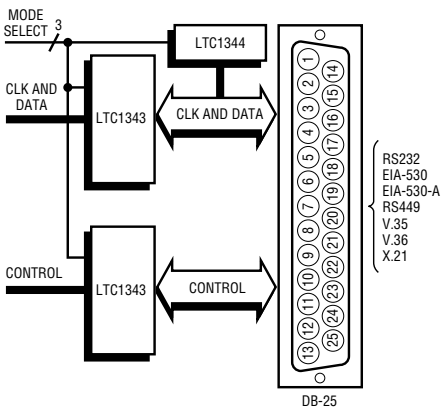

Figure 2. Single 5V Complete Multiprotocol Serial Port

Controller IC Allows Safe Hot Swapping of Circuit Boards

The **LTC1421** hot swap controller safely limits the inrush currents that can destroy components and traces on circuit boards and prevents glitches that disrupt the system bus when a circuit board is plugged into a live backplane. The device can turn on up to three board supply voltages at programmable rates. The LTC1421 is ideal for backplanes and rack systems that must run continuously or cannot tolerate glitches on the supply rails when inserting or removing circuit boards. It is appropriate for power systems supplying 3V/5V, 5V/±12V or even –48V/5V telecom voltages.

The key to controlling the inrush current is the user-programmable power-up rate. An external capacitor sets the timing for the ramp-up of the positive FET voltages resulting in the switches being turned on slowly and the current being held to an acceptable level. A sense resistor in series with the FETs, shown in Figure 1, is used to detect excessive current levels. Both positive FETs are ramped up at the same rate, with the higher voltage FET kept above the lower voltage FET to prevent power sequencing problems.

The chip includes undervoltage lockout and a voltage comparator to generate a reset signal. Voltage levels can be monitored using the uncommitted comparator and the 1.232V reference.

Power management functions include data bus disable, reset input, system reset and power good signals. During board insertion or removal, the disable signal can be used to halt the system bus by putting the bus buffer in a high impedance state. The reset input allows recycling the power with a pushbutton or external signal. The reset output and power good output signals are used by the processor for general power management functions.

The LTC1421 controller provides warning signals when power fails, the circuit breaker has tripped or when the switches have been turned off. Separate controls are available for power-on reset or disabling the data lines.

The LTC1421 is available in the 24-pin SO and SSOP packages. For a data sheet and evaluation samples, contact your local Linear Technology sales office.

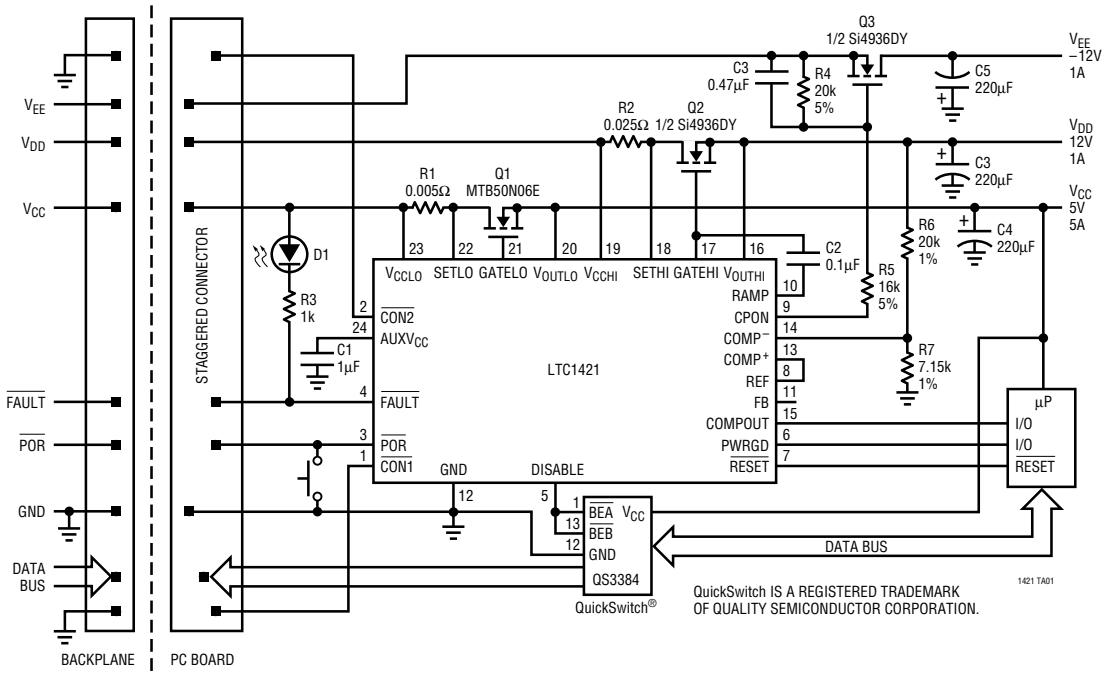

Figure 1. The LTC1421 Can Drive Three N-Channel MOSFETs That Switch the Power from the Backplane to the Circuit Board. Resistors in Series with the Power FETs Sense Excessive Current Levels

First Dual 12-Bit Voltage Output DAC in SO-8 Runs on 3V Supply

The **LTC1446L** is a dual 12-bit voltage output digital-to-analog converter that is complete with two rail-to-rail voltage output amplifiers, a 1.22V bandgap voltage reference and a 3-wire cascadable serial interface, all packed into an 8-pin SO package. The maximum differential nonlinearity (DNL) is only ±0.5LSB. It consumes just 2mW from a single 3V supply making it the best solution for portable and battery-powered equipment. Better than 12-bit monotonicity over temperature makes the LTC1446L ideal for feedback control applications such as industrial control loops and general purpose trim pots.

The 2.5V output voltage is guaranteed even with a reduced supply of 2.7V. The DAC outputs drive capacitive loads of up to 1000pF. Power-on reset insures the DACs start in a known state after power up, easing initial processor overhead. Figure 1 shows a typical application for the LTC1446L.

The excellent typical differential nonlinearity (DNL) of 0.2LSB (Figure 2) not only guarantees 12-bit monotonic performance but also provides exceptional performance in closed loop control systems. The LTC1446L's 3-wire serial interface allows several dual DACs to be daisy-

Continued on page 3

Application of the Month

Micropower Dual JFET Op Amps Feature pA Input Bias Currents and C-Load Drive Capability

The LT®1462/LT1463 low input bias currents make them a natural for amplifying low level signals from high impedance transducers. The 1pA input bias current contributes only 0.4fA/√Hz of current noise or 0.4nV/√Hz voltage noise with a 1MΩ source impedance. A 1MΩ impedance's thermal noise of 130nV/√Hz dominates the op amp's noise, showing that even with high source impedances, the LT1462/LT1463 contribute very little to total input-referred noise. Taking advantage of these features, Figure 1's photodiode logging amplifier uses two LT1462 duals or an LT1463 quad. Here, the photodiode current is converted to a voltage by the first op amp and D1 and amplified by the first, second and third logarithmic compression amplifiers. A DC feedback path comprising R8, R9, C6 and Q1 is active only for no-light conditions. Q1 is off when light is present, isolating the photodiode from C6. When feedback is needed, a small filtered current through R8 prevents the op amp outputs from saturating when no signal is present as shown in Figure 2.

The LT1462/LT1463 family is especially suited for piezo transducer conditioning, strain gauge weight scales, very low droop track-and-holds, wide dynamic range photodiode amplifiers and other applications that benefit from pA input bias current. The family also exhibits very low noise current, important to circuits such as low frequency filters. These op amps allow high value resistors to be used with easily obtainable, low value precision capacitors to set a filter's frequency characteristics without compromising noise performance.

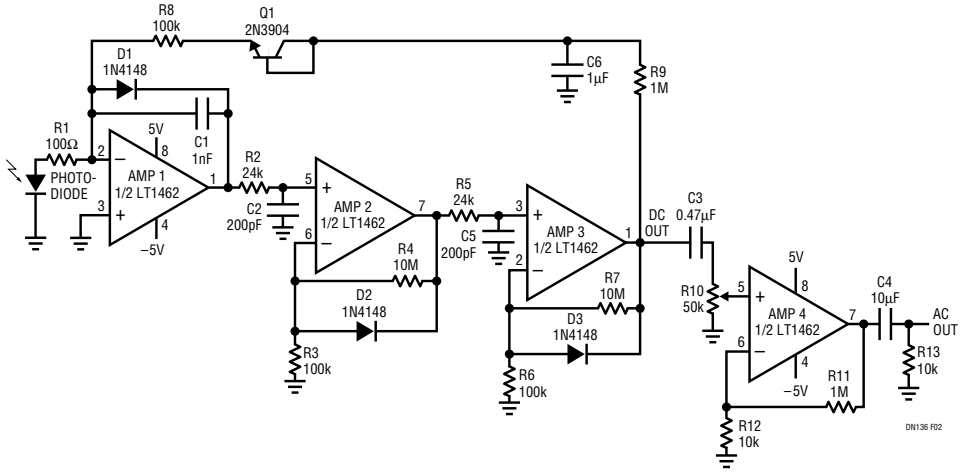

Figure 1. This Logging Photodiode Amplifier Takes Advantage of the LT1462's 1pA Input Bias Current to Amplify the Low Level Signal from the Photodiode's High Source Impedance

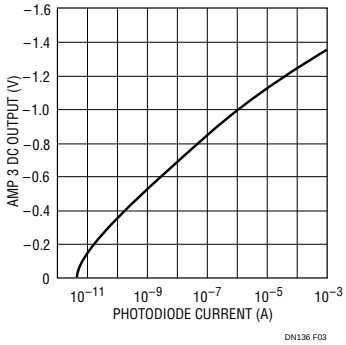

Figure 2. Logging Photodiode Amplifier DC Output

LTC1446L from page 2

chained to save board space and is compatible with SPI, QSPI and MICROWIRE™ protocols.

The LTC1446L is available in 8-lead SO and PDIP packages screened to the commercial and industrial temperature ranges. Contact your local Linear Technology sales office for a data sheet and evaluation samples.

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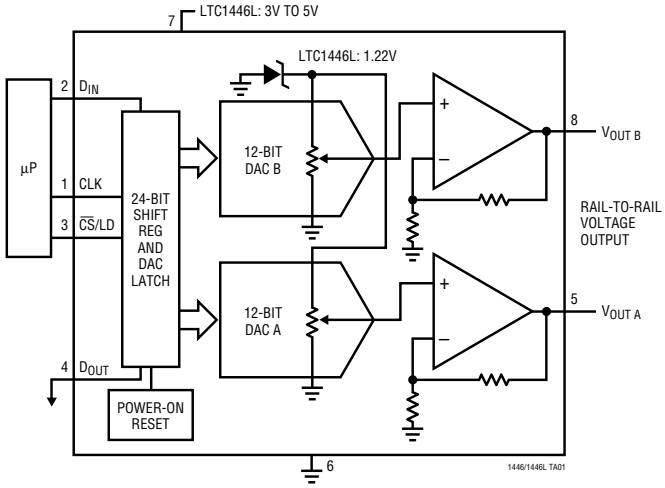

Figure 1. The LTC1446L Dual 12-Bit DAC is the First in an 8-Pin SO Package to Operate with a Single 3V Supply

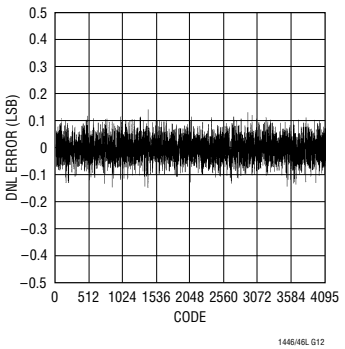

Figure 2. Typical Differential Nonlinearity vs Input Code for LTC1446L is Only ±0.2LSB. Maximum DNL is ±0.5LSB

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Dual DAC Adds Features to Single 5V Supply, 12-Bit Family

The **LTC1454** is a dual 12-bit DAC that consumes 3.5mW (typ) from a single 5V supply and has a differential nonlinearity (DNL) of only ±0.5LSB. This makes it ideal for feedback control applications such as industrial control loops and general trim pots. The low power consumption and high integration make the LTC1454 an excellent choice for portable or battery-powered equipment.

The LTC1454 contains two 12-bit DACs with rail-to-rail output amplifiers, a 3-wire, cascadable serial interface and a 2.048V bandgap voltage reference. Offset error is only ±18mV (max). The LTC1454 has an asynchronous Clear pin which resets all DACs to zero scale. A unity/2X gain select pin lets the user set the gain of the output amplifiers. The on-chip reference is available for external circuitry and is not internally connected, allowing a user specified reference input.

The rail-to-rail amplifiers have improved capacitive load handling over competing devices and swing to 4.095V full scale even when running on a 4.5V supply. The serial I/O is cascadable which reduces interface hardware when multiple DACs are used. Power-on reset insures the DACs start in a known state after power up and Clear resets the DAC to zero scale asynchronously. For a data sheet and evaluation samples of this high performance ADC, contact your local Linear Technology sales office.

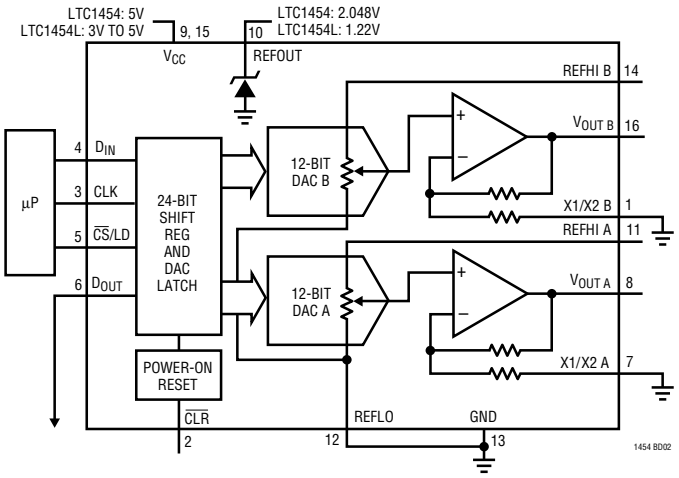

Figure 1. LTC1454 Dual 12-Bit Rail-to-Rail DAC Offers Many Features in Its 16-pin SO Package.

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