Complete 10-Bit Data Acquisition System with On Board Reference

FEATURES

- On Board 5V Precision Buried Zener Reference
- Software Controlled 6 Channel Multiplexer
- Differential and Single Ended Input Capability
- Built-In Sample and Hold for Single Ended Inputs
- Analog Inputs Common Mode to Both Supply Rails
- Single Supply (7.2V to 40V) or Split Supply Operation
- 10 Bit Unipolar or 9 Bit Plus Sign Bipolar
- 2's Complement Output Coding on Bipolar Conversions
- Direct Interface to Most Microprocessor Serial Data Ports Including Mortorola SPI, Hitachi SCI and National MICROWIRE/PLUS*
- Software Interface to Other Microprocessor Parallel Ports
- MSB or LSB First Data

KEY SPECIFICATIONS

■ Resolution	10 Bits
■ Linearity Error	±0.5LSB (0.05% FSR) Max
■ Total Unadjusted Error	±0.15% FSR
■ Conversion Time	20μs
■ Sampling Rate	25kHz
■ Supply Current	4.7mA Max, 2.3mA Typ
■ Full Scale Error Temperature Drift (B Grade)	23ppm/°C Max

*MICROWIRE/PLUS is a trademark of National Semiconductor.

DESCRIPTION

The LTC1095 is a complete data acquisition component which contains a serial I/O, successive approximation A/D converter, a 6 channel multiplexer, a sample and hold, and an on board reference. It uses LTCMOS™ switched capacitor technology to perform either 10 bit unipolar, or 9 bit plus sign bipolar A/D conversions. The 6 channel input multiplexer can be software configured for either single ended or differential inputs (or combinations thereof). The on chip sample and hold is included for all single ended input channels. The LTC1095 is specified as a complete system. This specification includes the error contribution of the A/D, MUX, S&H, and reference.

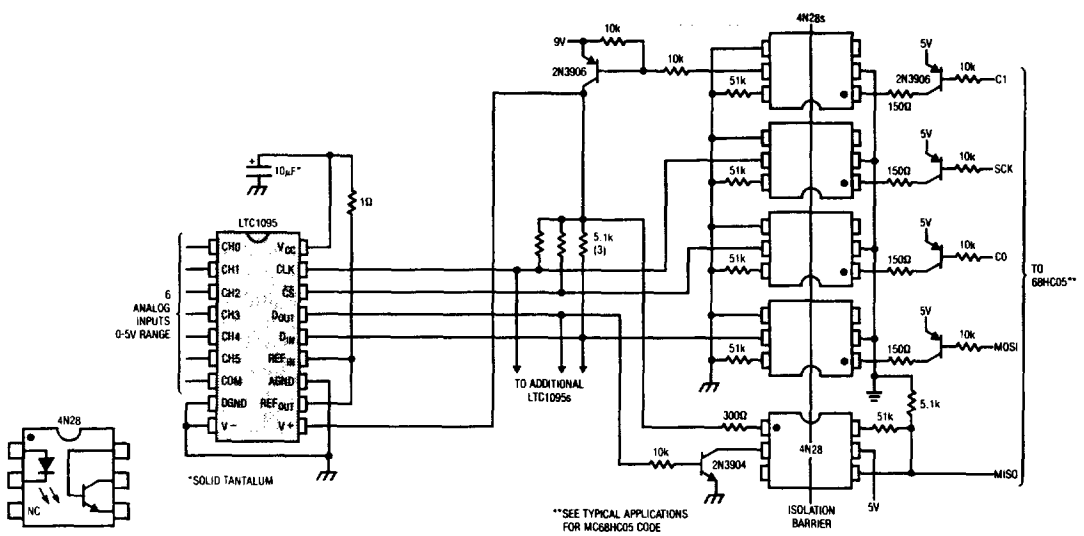
The serial I/O is designed to be compatible with industry standard serial interfaces. It allows either MSB or LSB first data and automatically provides 2's complement output coding in the bipolar mode. This allows easy interface to shift registers and a variety of processors.

All grades of the LTC1095 have guaranteed maximum offset and linearity errors of ±0.5LSB over the full operating temperature range. The LTC1095B is specified with gain error less than ±0.1% maximum.

The LTC1095C is specified with a gain error limit of ±0.2% FSR maximum.

TYPICAL APPLICATIONS

Micropower, 500V Opto Isolated, Multichannel, 10-Bit Data Acquisition System

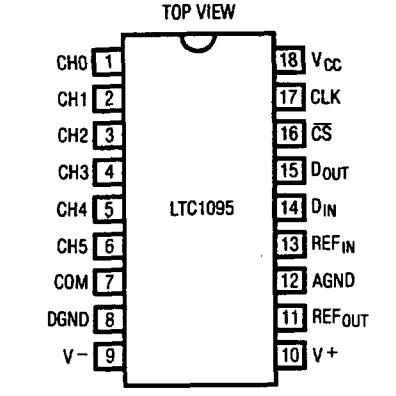


ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage (V^+) to GND 40V
Supply Voltage (V_{CC}) to GND or V^- 12V
Negative Supply Voltage (V^-) ..... –6V to GND
Voltage
  Analog and Reference Inputs .. (V^-) – 0.3V to V_{CC} + 0.3V
  Digital Inputs ..... – 0.3V to 12V
  Digital Outputs ..... – 0.3V to V_{CC} + 0.3V
Power Dissipation 500mW
Operating Temperature Range
  LTC1095BC, LTC1095CC ..... 0°C to 70°C
  LTC1095BM, LTC1095CM ..... –55°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



J PACKAGE
18-LEAD CERAMIC DIP

N PACKAGE
18-LEAD PLASTIC DIP

ORDER PART NUMBER

LTC1095BMJ
LTC1095CMJ
LTC1095BCJ
LTC1095CCJ
LTC1095BCN
LTC1095CCN

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 3)

(With internal reference)

PARAMETER	CONDITIONS (See Schematic of Figure 1)		LTC1095B MIN	LTC1095B TYP	LTC1095B MAX	LTC1095C MIN	LTC1095C TYP	LTC1095C MAX	UNITS
Offset Error		●			±0.5			±0.5	LSB
Linearity Error	(Notes 4 and 5)	●			±0.5			±0.5	
Gain Error	(Note 4)				±0.1			±0.2	%FSR
	Commercial Range	●			±0.15			±0.3	
	Military Range	●			±0.2			±0.4	
Total Unadjusted Error	(Notes 4 and 6)				±0.15			±0.25	%FSR
	Commercial Range	●			±0.2			±0.35	
	Military Range	●			±0.25			±0.45	
Full Scale Error Temperature Coefficient	Commercial Grade	●		(Note 9)			(Note 9)		ppm/°C
	Military Grade (Note 10)	●			23			45	

INTERNAL REFERENCE CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		LTC1095B MIN	LTC1095B TYP	LTC1095B MAX	LTC1095C MIN	LTC1095C TYP	LTC1095C MAX	UNITS
Output Voltage				5.000			5.000		V
Output Voltage Temperature Coefficient				2			5		ppm/°C
Line Regulation	$7.2V \le V^+ \le 10V$			4	12		4	12	ppm/V
		●			20			20	
	$10V \le V^+ \le 40V$			2	6		2	6	
		●			10			10	
Load Regulation (Sourcing Current)	$0 \le \lvert I_{REF\,OUT} \rvert \le 10mA$			10	25		10	25	ppm/mA
		●			40			40	
Load Regulation (Sinking Current)	$0 \le \lvert I_{REF\,OUT} \rvert \le 10mA$			60	150		60	150	
		●			200			200	

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1095B/LTC1095C MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	$V_{CC} = 5.25V$	●	2.0			V
V_{IL}	Low Level Input Voltage	$V_{CC} = 4.75V$	●			0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●			2.5	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0V$	●			−2.5	μA
V_{OH}	High Level Output Voltage	$V_{CC} = 4.75V$, $I_O = 10\mu A$			4.7		V
		$I_O = 360\mu A$	●	2.4	4.0		V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.75V$, $I_O = 1.6mA$	●			0.4	V
I_{OZ}	Hi-Z Output Leakage	$V_{OUT} = V_{CC}$, $\overline{CS}$ High	●			3	μA
		$V_{OUT} = 0V$, $\overline{CS}$ High	●			−3	μA
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$			−10		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$			10		mA
I_{CC}	Positive Supply Current	$\overline{CS}$ High, REF^+ Open	●		1.0	2.5	mA
$I_{REF\,IN}$	Reference Input Current	$REF_{IN} = 5V$	●		0.5	1.0	mA
I^-	Negative Supply Current	$\overline{CS}$ High	●		1	50	μA
I^+	On Chip Reference Current	$V^+ = 10V$ REF_{OUT} Open	●		0.8	1.2	mA
	Reference Input Resistance				10		kΩ
	Analog and REF Input Range	(Note 7)		$(V^-) - 0.05V$ to $V_{CC} + 0.05V$			V
	On Channel Leakage Current (Note 8)	On Channel = 5V, Off Channel = 0V	●			1	μA
		On Channel = 0V, Off Channel = 5V	●			−1	
	Off Channel Leakage Current (Note 8)	On Channel = 5V, Off Channel = 0V	●			−1	μA
		On Channel = 0V, Off Channel = 5V	●			1	

9

AC CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1095B/LTC1095C MIN	TYP	MAX	UNITS
t_{SMPL}	Analog Input Sample Time	See Operating Sequence			1.5		CLK Cycles
t_{CONV}	Conversion Time	See Operating Sequence			10		CLK Cycles
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Data Valid	See Parameter Measurement Section	●		400	850	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Parameter Measurement Section	●		180	450	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enabled	See Parameter Measurement Section	●		160	450	ns
t_{hDO}	Time Output Data Remains Valid After CLK↓				150		ns
t_f	D_{OUT} Fall Time	See Parameter Measurement Section	●		90	300	ns
t_r	D_{OUT} Rise Time	See Parameter Measurement Section	●		60	300	ns
C_{IN}	Input Capacitance	Analog Inputs On Channel			65		pF
		Off Channel			5		pF
		Digital Inputs			5		pF

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND, AGND, and REF^- wired together (unless otherwise noted).

Note 3: $V_{CC} = 5V$, $REF_{IN} = REF_{OUT}$, $V^+ = 10V$, $I_{REF\,OUT} = 0$, $V^- = 0V$ for unipolar mode and $-5V$ for bipolar mode, CLK = 0.5MHz unless otherwise specified. The ● indicates specs which apply over the full operating temperature range; all other limits and typicals $T_A = 25°C$.

Note 4: These specs apply for both unipolar and bipolar modes. In bipolar mode, one LSB is equal to the bipolar input span ($2REF_{IN}$) divided by 1024. For example, when $REF_{IN} = 5V$, 1LSB (bipolar) = 2(5V)/1024 = 9.77mV.

Note 5: Linearity error is specified between the actual end points of the A/D transfer curve.

Note 6: Total unadjusted error includes offset, full scale, linearity, multiplexer, reference and hold step errors.

Note 7: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below V^- or one diode drop above V_{CC}. Be careful during testing at low V_{CC} levels (4.5V), as high level reference or analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for inputs near full-scale. This spec allows 50mV forward bias of either diode. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over initial tolerance, temperature variations and loading.

Note 8: Channel leakage current is measured after the channel selection.

Note 9: For commercial grade parts with tested and specified T.C. consult the factory.

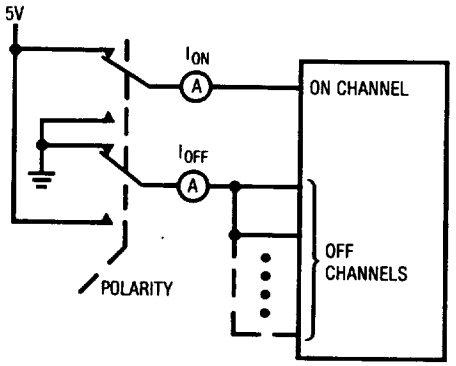
Note 10: This is specified for both unipolar and bipolar modes via the "box" method. The lowest of three readings (T_{MIN}, T_{ROOM}, T_{MAX}) subtracted from the highest and divided by $T_{MAX} - T_{MIN}$ is guaranteed to be less than the specified T.C. These numbers are guaranteed by the MIL range gain error test limits. For tighter T.C. specifications, consult the factory.

RECOMMENDED OPERATING CONDITIONS

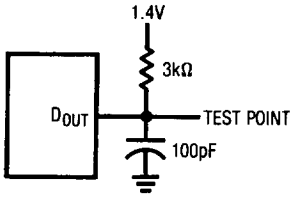
SYMBOL	PARAMETER	CONDITIONS	LTC1095B/LTC1095C MIN	MAX	UNITS
V_{CC}	Supply Voltage		4.5	10	V
V^-	Negative Supply Voltage	$V_{CC} = 5V$	−5.5	0	V
f_{CLK}	Clock Frequency	$V_{CC} = 5V$	0.01	0.5	MHz
t_{CYC}	Total Cycle Time		18 CLK Cycles + 2μs		
t_{hDI}	Hold Time, D_{IN} After SCLK↑	$V_{CC} = 5V$	150		ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$↓ Before CLK↑	$V_{CC} = 5V$	1		μs
t_{suDI}	Setup Time, D_{IN} Stable Before CLK↑	$V_{CC} = 5V$	400		ns
t_{WHCLK}	CLK High Time	$V_{CC} = 5V$	0.8		μs
t_{WLCLK}	CLK Low Time	$V_{CC} = 5V$	1		μs
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfer Cycles	$V_{CC} = 5V$	2		μs
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer		18		CLK Cycles

TEST CIRCUITS

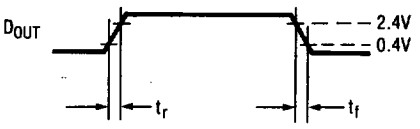
On and Off Channel Leakage Current



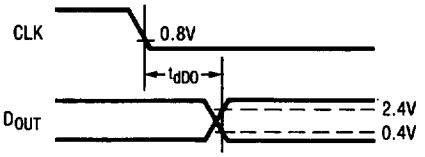
Load Circuit for t_{dDO}, t_r, and t_f



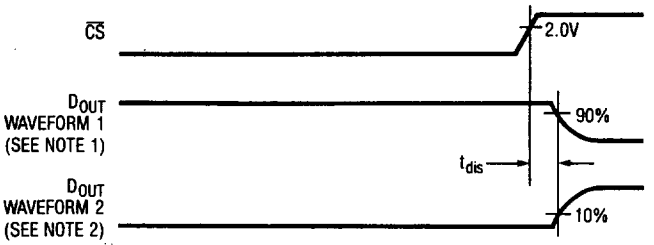
Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r, t_f



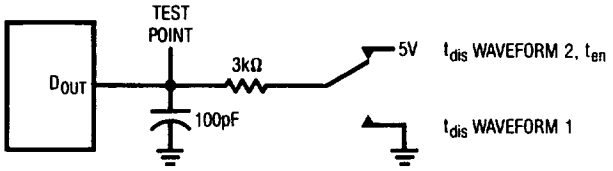
Voltage Waveforms for D_{OUT} Delay Time, t_{dDO}



Voltage Waveforms for t_{dis}



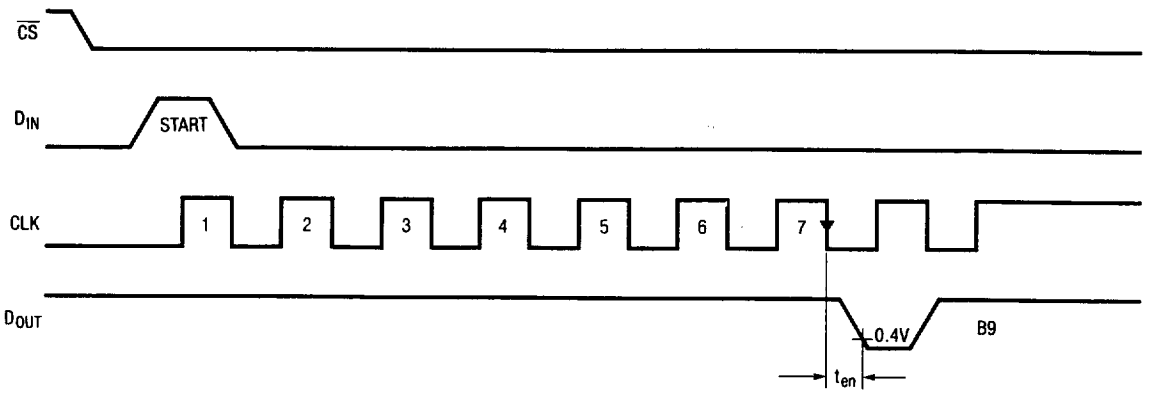
Load Circuit for t_{dis} and t_{en}



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

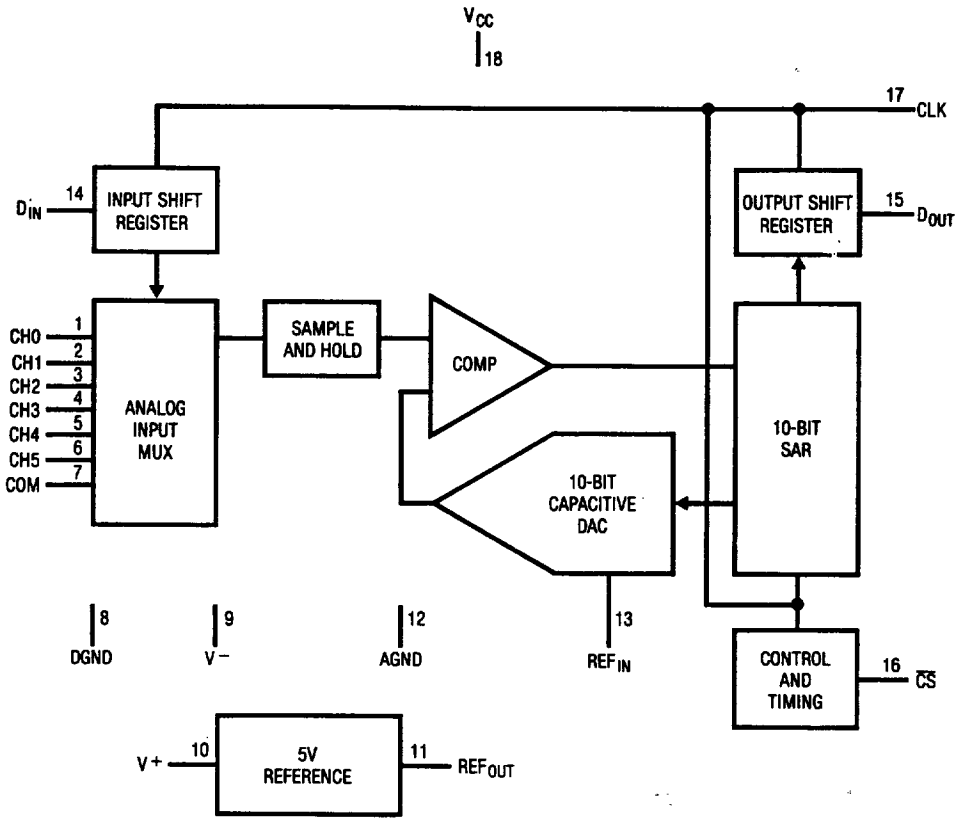
Voltage Waveforms for t_{en}



PIN FUNCTIONS

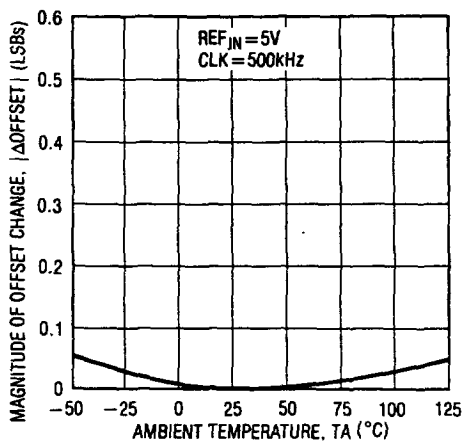
LTC1095 #	PIN	FUNCTION	DESCRIPTION
1-6	CH0-CH5	Analog Inputs	The analog inputs must be free of noise with respect to AGND.
7	COM	Common	The common pin defines the zero reference point for all single ended inputs. It must be free of noise and is usually tied to the analog ground plane.
8	DGND	Digital Ground	This is the ground for the internal logic. Tie to the ground plane.
9	V^-	Negative Supply	Tie V^- to most negative potential in the circuit. (Ground in single supply applications.)
10	V^+	Reference Supply	Supply pin for on board reference.
11	REF_{OUT}	Reference Output	Output of on board reference.
12	AGND	Analog Ground	AGND should be tied directly to the analog ground plane.
13	REF_{IN}	Reference Input	The reference input must be kept free of noise with respect to AGND.
14	D_{IN}	Data Input	The A/D configuration word is shifted into this input.
15	D_{OUT}	Digital Data Output	The A/D conversion result is shifted out of this output.
16	$\overline{CS}$	Chip Select Input	A logic low on this input enables the LTC1095.
17	CLK	Shift Clock	This clock synchronizes the serial data transfer.
18	V_{CC}	Positive Supply	This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

BLOCK DIAGRAM

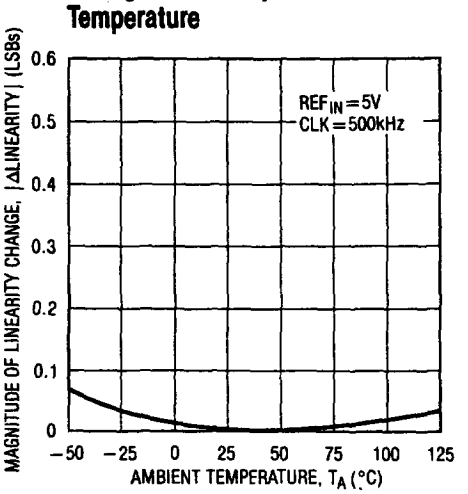


TYPICAL PERFORMANCE CHARACTERISTICS

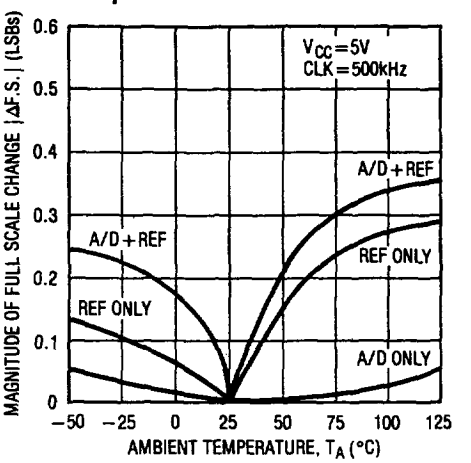
Change in Offset Error vs Temperature



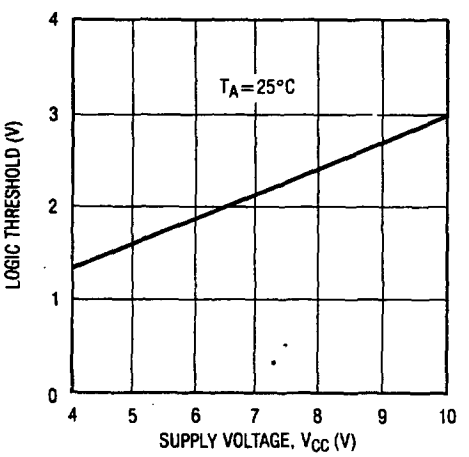
Change in Linearity Error vs Temperature



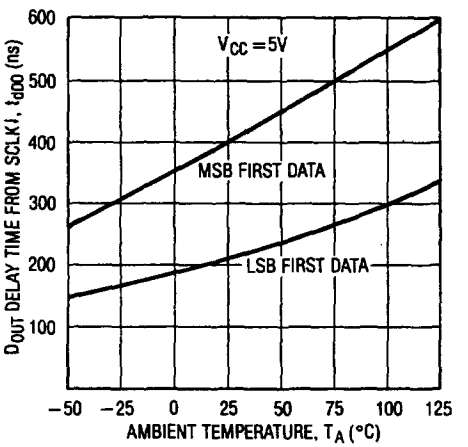
Change in Full Scale Error vs Temperature



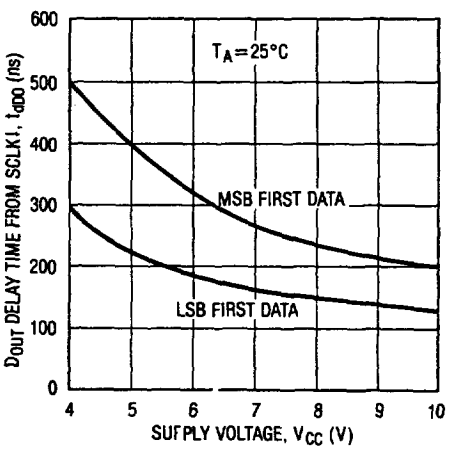
Digital Input Logic Threshold vs V_{CC} Supply Voltage



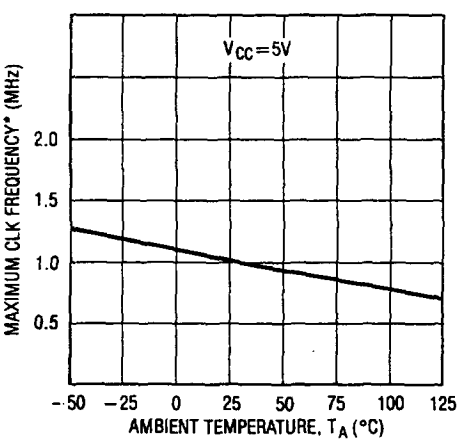
D_{OUT} Delay Time vs Temperature



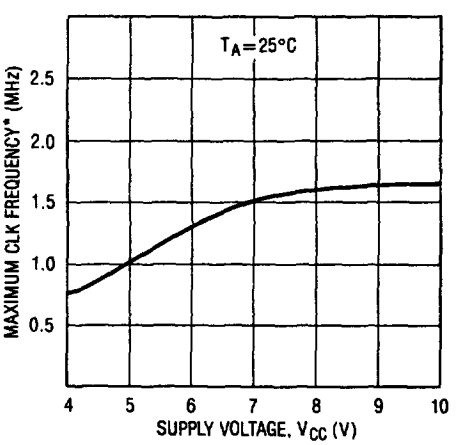
D_{OUT} Delay Time vs V_{CC} Supply Voltage



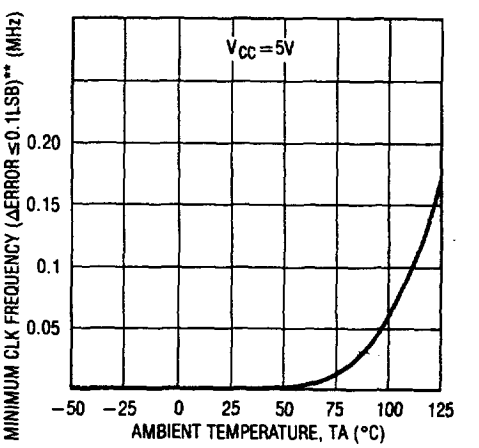
Maximum Clock Rate vs Temperature



Maximum Clock Rate vs V_{CC} Supply Voltage



Minimum Clock Rate vs Temperature

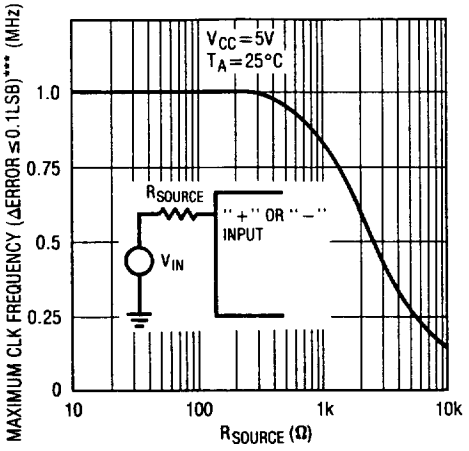


*MAXIMUM CLK FREQUENCY REPRESENTS THE HIGHEST FREQUENCY AT WHICH CLK CAN BE OPERATED (WITH 50% DUTY CYCLE) WHILE STILL PROVIDING 100ns SETUP TIME FOR THE DEVICE RECEIVING THE D_{OUT} DATA.

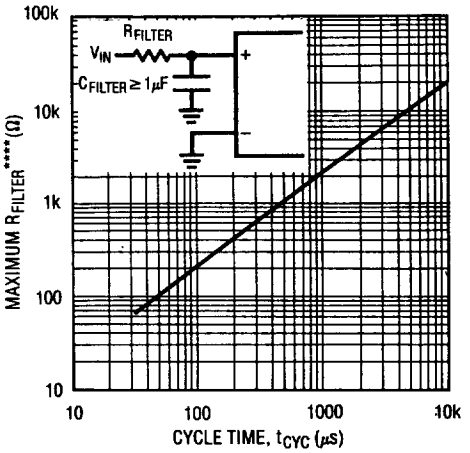
**AS THE CLK FREQUENCY IS DECREASED FROM 500kHz, MINIMUM CLK FREQUENCY (ΔERROR ≤0.1LSB) REPRESENTS THE FREQUENCY AT WHICH A 0.1LSB SHIFT IN ANY CODE TRANSITION FROM ITS 500kHz VALUE IS FIRST DETECTED.

TYPICAL PERFORMANCE CHARACTERISTICS

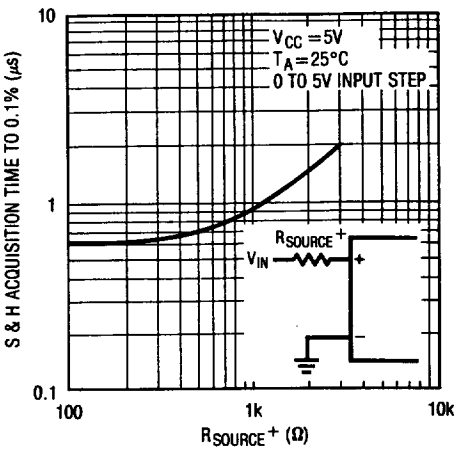
Maximum Clock Rate vs Source Resistance



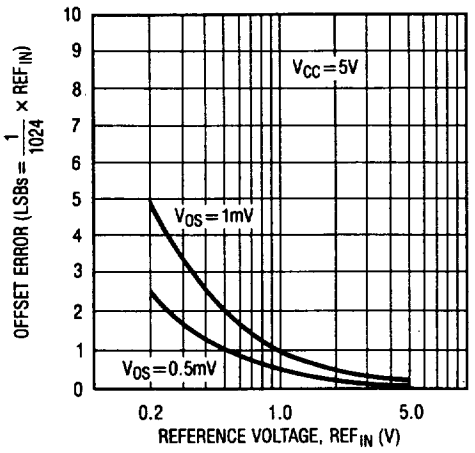
Maximum Filter Resistor vs Cycle Time



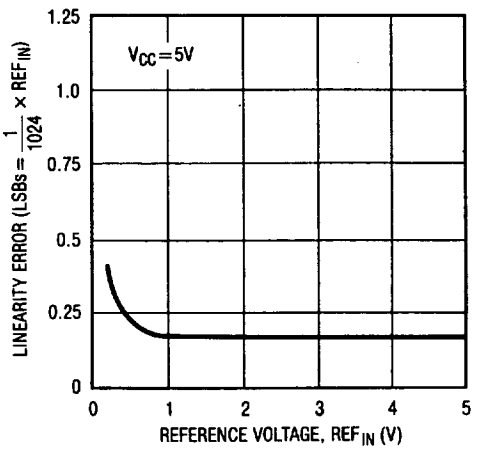
Sample and Hold Acquisition Time vs Source Resistance



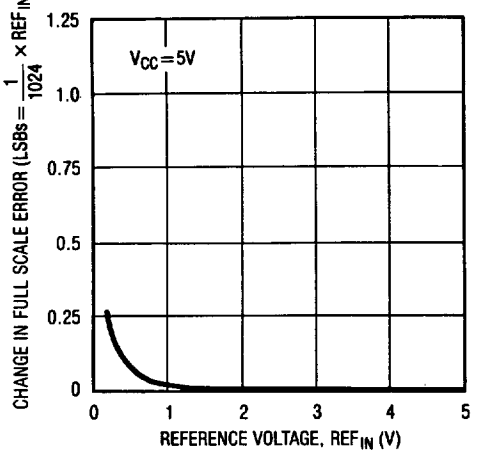
Unadjusted Offset Error vs Reference Voltage



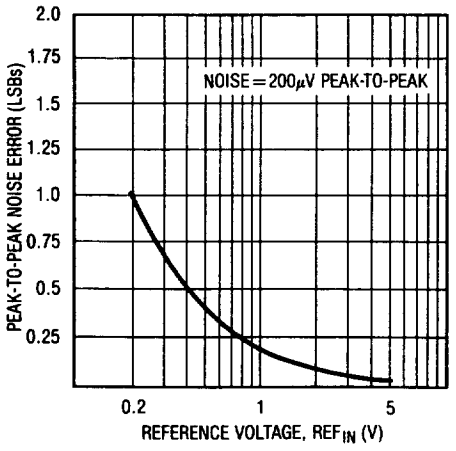
Linearity Error vs Reference Voltage



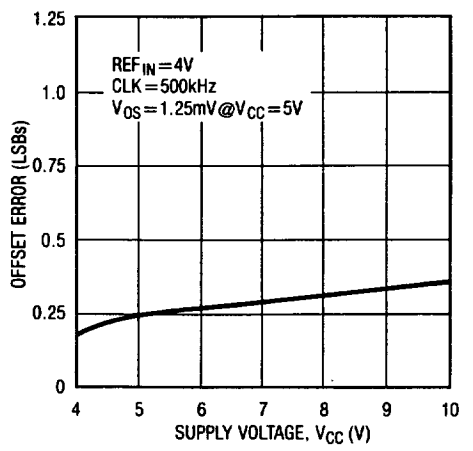
Change in Full Scale Error vs Reference Voltage



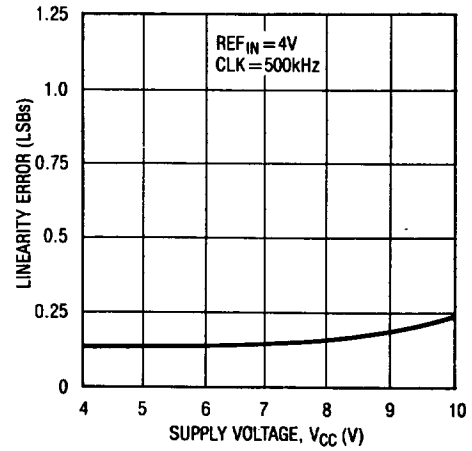
Noise Error vs Reference Voltage



Offset Error vs Supply Voltage



Linearity Error vs Supply Voltage

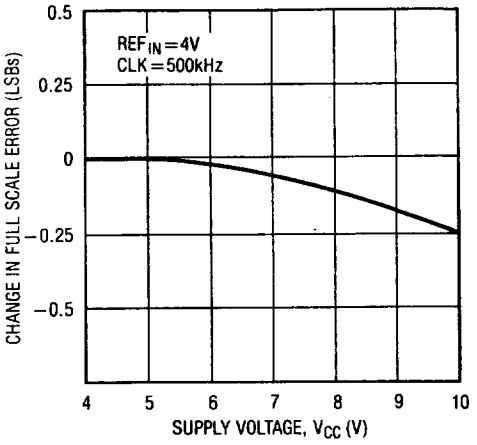


***AS THE CLK FREQUENCY AND SOURCE RESISTANCE ARE INCREASED, MAXIMUM CLK FREQUENCY (ΔERROR ≤ 0.1LSB) REPRESENTS THE FREQUENCY AT WHICH A 0.1LSB SHIFT IN ANY CODE TRANSITION FROM ITS 500kHz, 0Ω VALUE IS FIRST DETECTED.

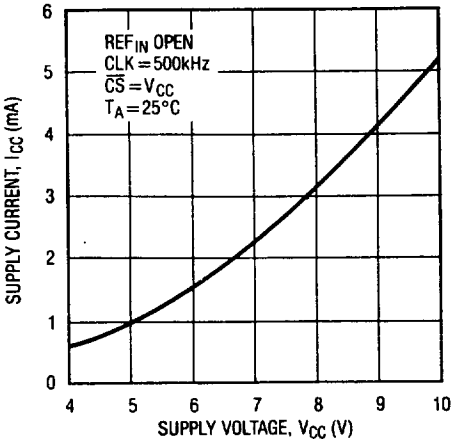
****MAXIMUM R_{FILTER} REPRESENTS THE FILTER RESISTOR VALUE AT WHICH A 0.1LSB CHANGE IN FULL-SCALE ERROR FROM ITS VALUE AT $R_{FILTER} = 0$ IS FIRST DETECTED.

TYPICAL PERFORMANCE CHARACTERISTICS

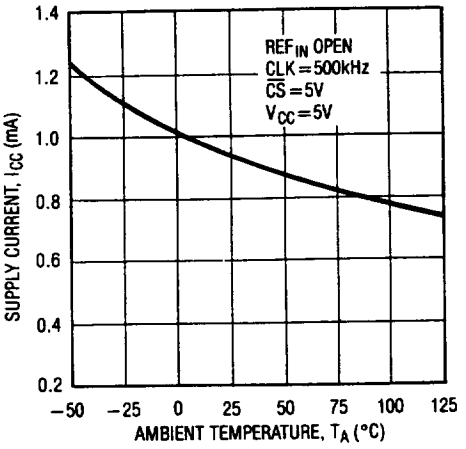
Change in Full Scale Error vs V_{CC} Supply Voltage



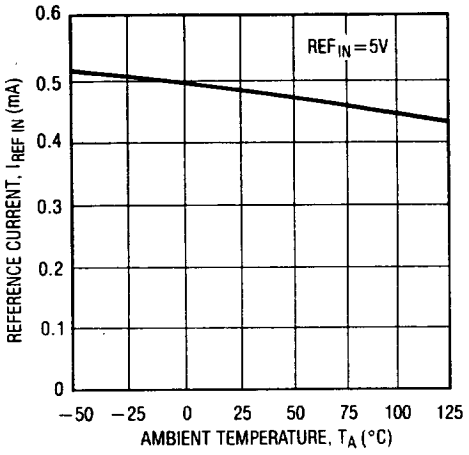
V_{CC} Supply Current vs Supply Voltage



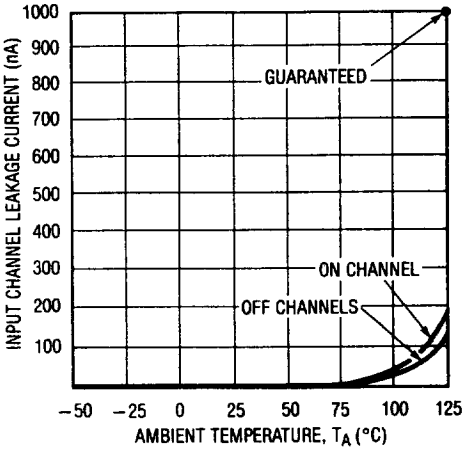
V_{CC} Supply Current vs Temperature



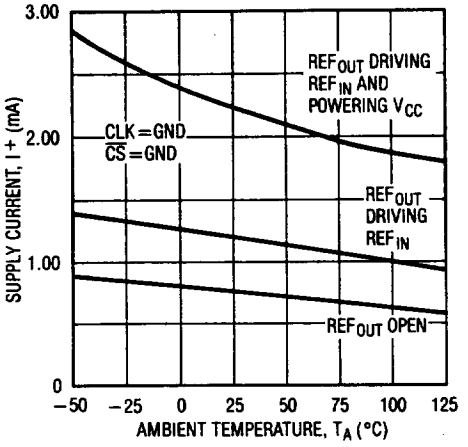
Reference Current vs Temperature



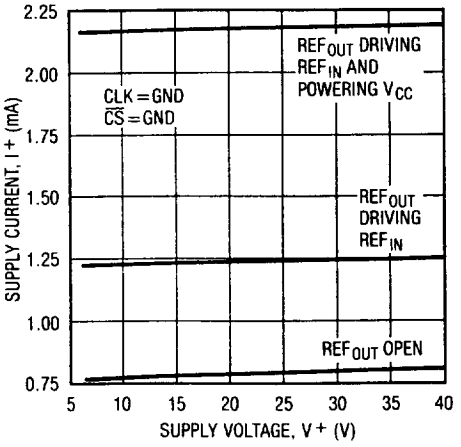
Input Channel Leakage Current vs Temperature



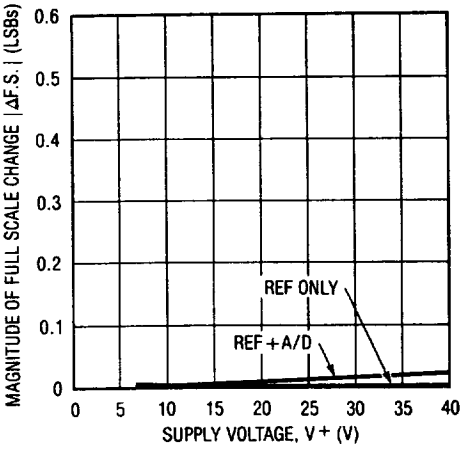
V+ Supply Current vs Temperature



V+ Supply Current vs Supply Voltage



Change in Full Scale Error vs V+ Supply Voltage



9

APPLICATIONS INFORMATION

The LTC1095 is a data acquisition component which contains the following functional blocks:

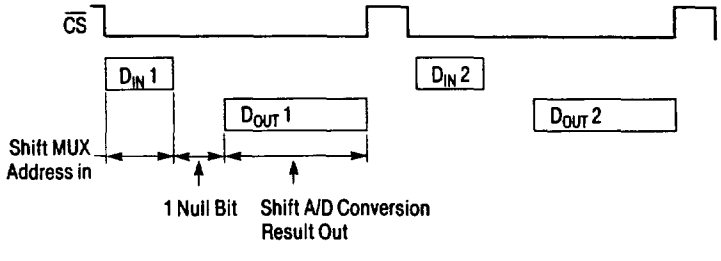
1. 10-bit successive approximation A/D converter
2. Analog multiplexer (MUX)
3. Sample and hold (S&H)
4. Synchronous, half duplex serial interface
5. Control and timing logic
6. On board reference

DIGITAL CONSIDERATIONS

1. Serial Interface

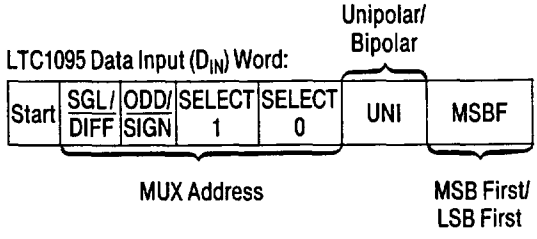
The LTC1095 communicates with microprocessors and other external circuitry via a synchronous, half duplex, four wire serial interface (see Operating Sequence). The clock (CLK) synchronizes the data transfer with each bit being transmitted on the falling CLK edge and captured on the rising CLK edge in both transmitting and receiving systems. The LTC1095 first receives input data and then transmits back the A/D conversion result (half duplex). Because of the half duplex operation, D_{IN} and D_{OUT} may be tied together allowing transmission over just 3 wires: $\overline{CS}$, CLK and DATA (D_{IN}/D_{OUT}).

Data transfer is initiated by a falling chip select ($\overline{CS}$) signal. After $\overline{CS}$ falls the LTC1095 looks for a start bit. After the start bit is received, a 6-bit input word is shifted into the D_{IN} input which configures the LTC1095 and starts the conversion. After one null bit, the result of the conversion is output on the D_{OUT} line. At the end of the data exchange $\overline{CS}$ should be brought high. This resets the LTC1095 in preparation for the next data exchange.



2. Input Data Word

The LTC1095 clocks data into the D_{IN} input on the rising edge of the clock. The input data word is defined as follows:



Start Bit

The first "logical one" clocked into the D_{IN} input after $\overline{CS}$ goes low is the start bit. The start bit initiates the data transfer. The LTC1095 will ignore all leading zeros which precede this logical one. After the start bit is received, the remaining bits of the input word will be clocked in. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle.

APPLICATIONS INFORMATION

Multiplexer (MUX) Address

The bits of the input word following the START bit assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the + and – signs in the selected row of the following tables. In single ended mode, all input channels are measured with respect to COM.

LTC1095 Channel Selection

MUX ADDRESS				DIFFERENTIAL CHANNEL SELECTION					
SGL/DIFF	ODD/SIGN	SELECT 1	0	0	1	2	3	4	5
0	0	0	0	+	–				
0	0	0	1			+	–		
0	0	1	0					+	–
0	0	1	1	NOT USED					
0	1	0	0	–	+				
0	1	0	1			–	+		
0	1	1	0					–	+
0	1	1	1	NOT USED					

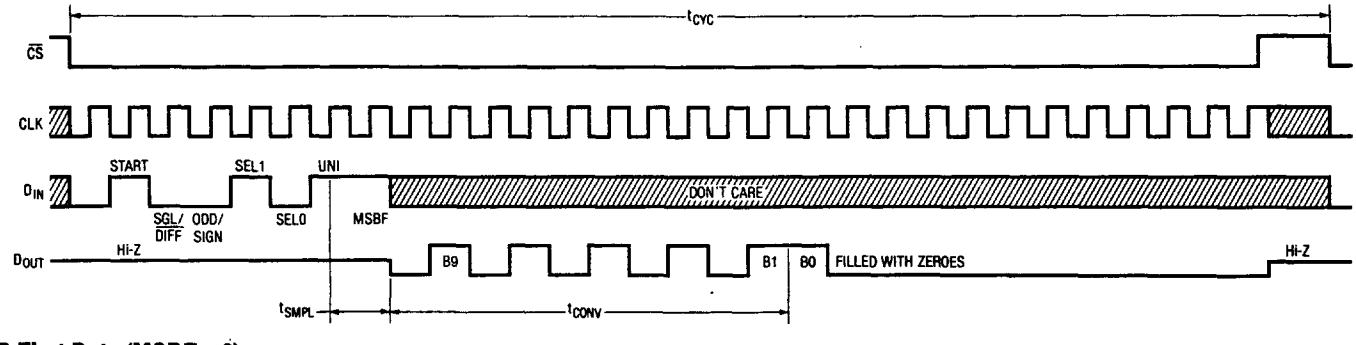
MUX ADDRESS				SINGLE ENDED CHANNEL SELECTION						
SGL/DIFF	ODD/SIGN	SELECT 1	0	0	1	2	3	4	5	COM
1	0	0	0	+						–
1	0	0	1			+				–
1	0	1	0					+		–
1	0	1	1	NOT USED						
1	1	0	0		+					–
1	1	0	1				+			–
1	1	1	0						+	–
1	1	1	1	NOT USED						

MSB First/LSB First (MSBF)

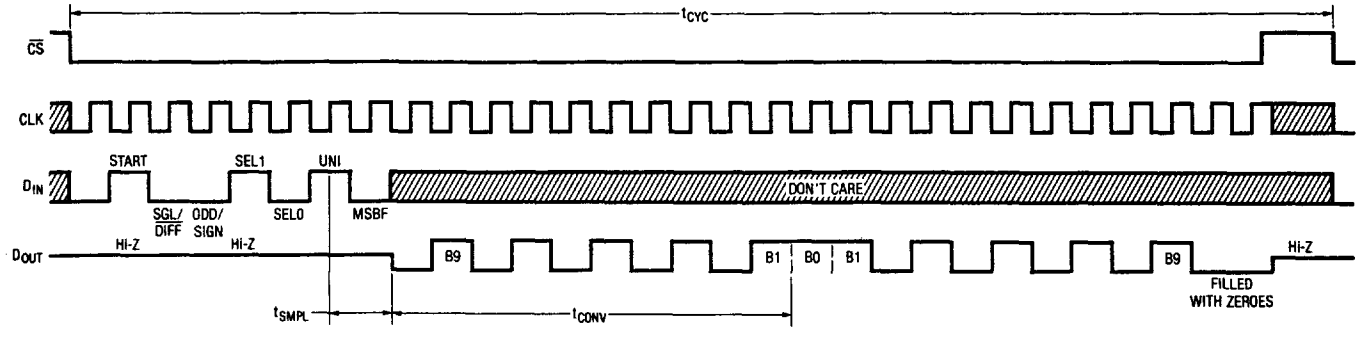
The output data of the LTC1095 is programmed for MSB first or LSB first sequence using the MSBF bit. When the MSBF bit is a logical one, data will appear on the D_{OUT} line in MSB first format. Logical zeros will be filled in indefinitely following the last data bit to accommodate longer word lengths required by some microprocessors. When the MSBF bit is a logical zero, LSB first data will follow the normal MSB first data on the D_{OUT} line. (See operating sequence).

LTC1095 Operating Sequence
Example: Differential Inputs (CH4 +, CH5 –), Unipolar Mode

MSB First Data (MSBF = 1)



LSB First Data (MSBF = 0)



9

APPLICATIONS INFORMATION

Unipolar/Bipolar (UNI)

The UNI bit of the LTC1095 determines whether the conversion will be unipolar or bipolar. When UNI is a logical one, a unipolar conversion will be performed on the selected input voltage. When UNI is a logical zero, a bipolar conversion will result. The input span and code assignment for each conversion type are shown in the figures below.

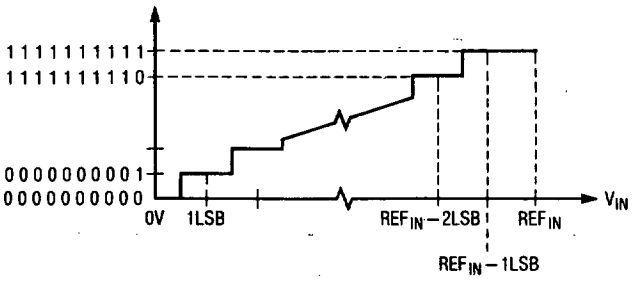
Unipolar Output Code (UNI = 1)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (REF_{IN} = 5V)
1111111111	REF_{IN} – 1LSB	4.9951V
1111111110	REF_{IN} – 2LSB	4.9902V
•	•	•
•	•	•
•	•	•
0000000001	1LSB	0.0049V
0000000000	0V	0V

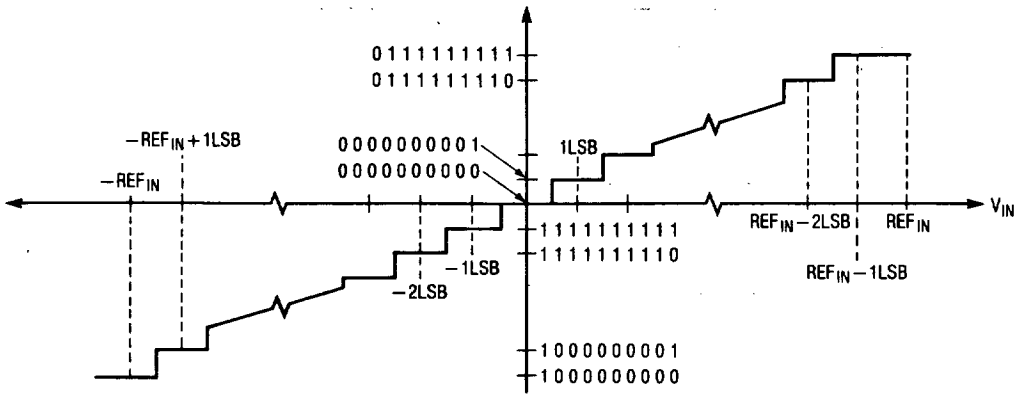
Bipolar Output Code (UNI = 0)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (REF_{IN} = 5V)
0111111111	REF_{IN} – 1LSB	4.9902V
0111111110	REF_{IN} – 2LSB	4.9805V
•	•	•
•	•	•
•	•	•
0000000001	1LSB	0.0098V
0000000000	0V	0V
1111111111	– 1LSB	– 0.0098V
1111111110	– 2LSB	– 0.0195V
•	•	•
•	•	•
•	•	•
1000000001	$-(REF_{IN})$ + 1LSB	– 4.9902V
1000000000	$-(REF_{IN})$	– 5.000V

Unipolar Transfer Curve (UNI = 1)



Bipolar Transfer Curve (UNI = 0)



APPLICATIONS INFORMATION

3. Accommodating Microprocessors with Different Word Lengths

The LTC1095 will fill zeroes indefinitely after the transmitted data until $\overline{CS}$ is brought high. At that time the D_{OUT} line is disabled. This makes interfacing easy to MPU serial ports with different transfer increments including 4 bits (e.g., COP400) and 8 bits (e.g., SPI and MICROWIRE/PLUS).

Figure 1 shows examples of LTC1095 input and output words for 4-bit and 8-bit processors. A complete data exchange can be implemented with two 4-bit MPU outputs and three inputs in 4-bit systems and one 8-bit output and two inputs in 8-bit systems. The resulting data winds up left justified in the MPU with zeroes automatically filled in the unused low order bits by the LTC1095. In section 5 another example is given using the MC68HC05C4 which positions data right justified inside the MPU.

4. Operation with D_{IN} and D_{OUT} Tied Together

The LTC1095 can be operated with D_{IN} and D_{OUT} tied together. This eliminates one of the lines required to communicate to the MPU. Data is transmitted in both directions on a single wire. The processor pin connected to this data line should be configurable as either an input or an output. The LTC1095 will take control of the data line and drive it low on the 7th falling CLK edge after the start bit is received (see Figure 2). Therefore the processor port line must be switched to an input before this happens, to avoid a conflict.

In the next section, an example is made of interfacing the LTC1095 with D_{IN} and D_{OUT} tied together to the Intel 8051 MPU.

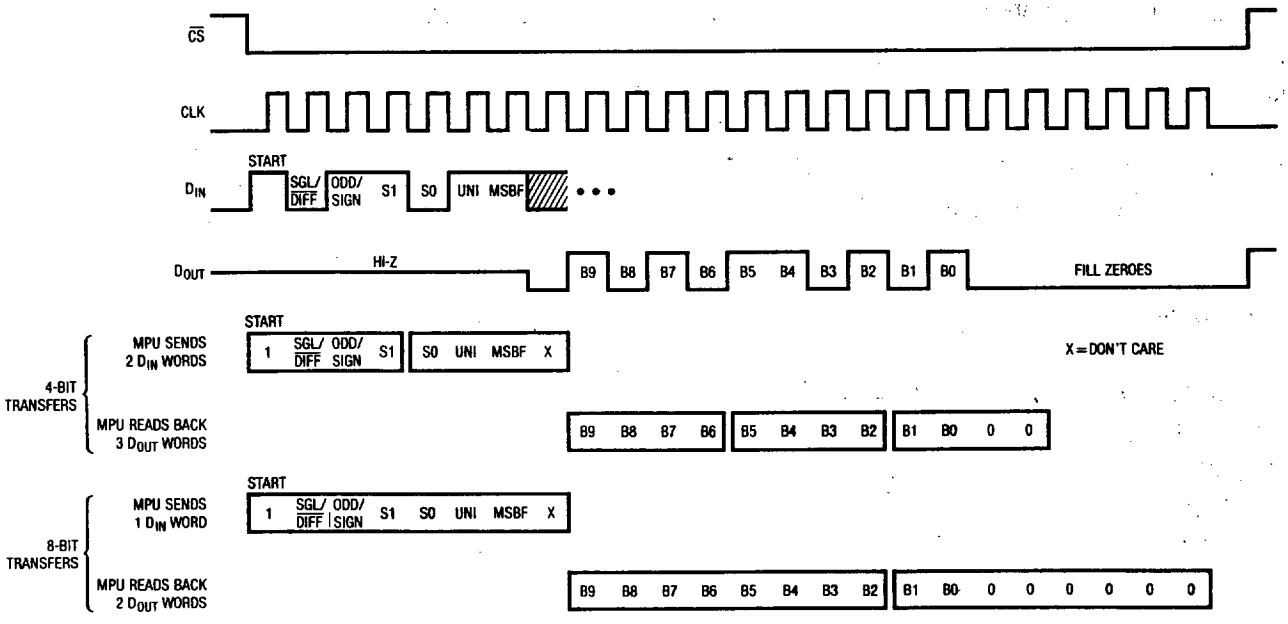


Figure 1. LTC1095 Input and Output Word Arrangments for 4-Bit and 8-Bit Serial Port Microprocessors

APPLICATIONS INFORMATION

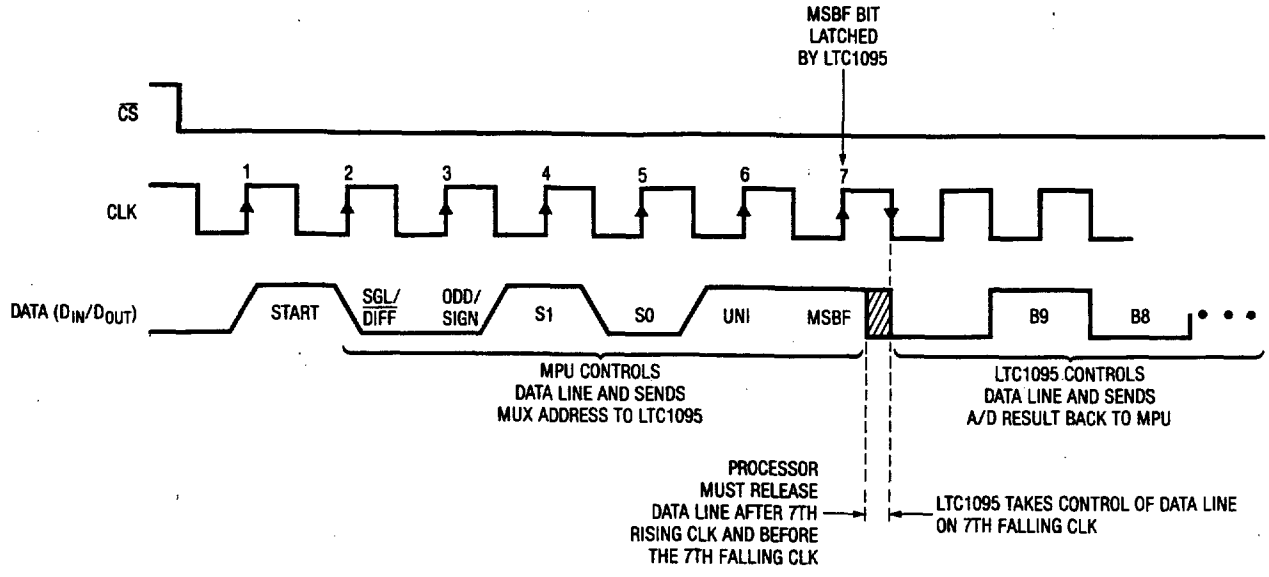


Figure 2. LTC1095 Operation with D_{IN} and D_{OUT} Tied Together

5. Microprocessor Interfaces

The LTC1095 can interface directly (without external hardware) to most popular microprocessor (MPU) synchronous serial formats (see Table 1). If an MPU without a dedicated serial port is used, then 3 or 4 of the MPU's parallel port lines can be programmed to form the serial link to the LTC1095. Included here are one serial interface example and one example showing a parallel port programmed to form the serial interface.

Motorola SPI (MC68HC05C4, MC68HC11)

The MC68HC05C4 has been chosen as an example of an MPU with a dedicated serial port. This MPU transfers data MSB first and in 8-bit increments. With three 8-bit transfers, the A/D result is read into the MPU. The first 8-bit transfer sends the start bit and the SGL/$\overline{\text{DIFF}}$ bit of the D_{IN} word to the LTC1095. The second 8-bit transfer clocks the remaining D_{IN} word bits, and B9 and B8 of the A/D conversion result. The third transfer clocks the remaining D_{OUT} bits into the μP.

ANDing the most significant byte with 03 Hex clears the 6 most significant bits. Notice how the position of the start bit in the first MPU transmit word is used to position the A/D result right justified in two memory locations.

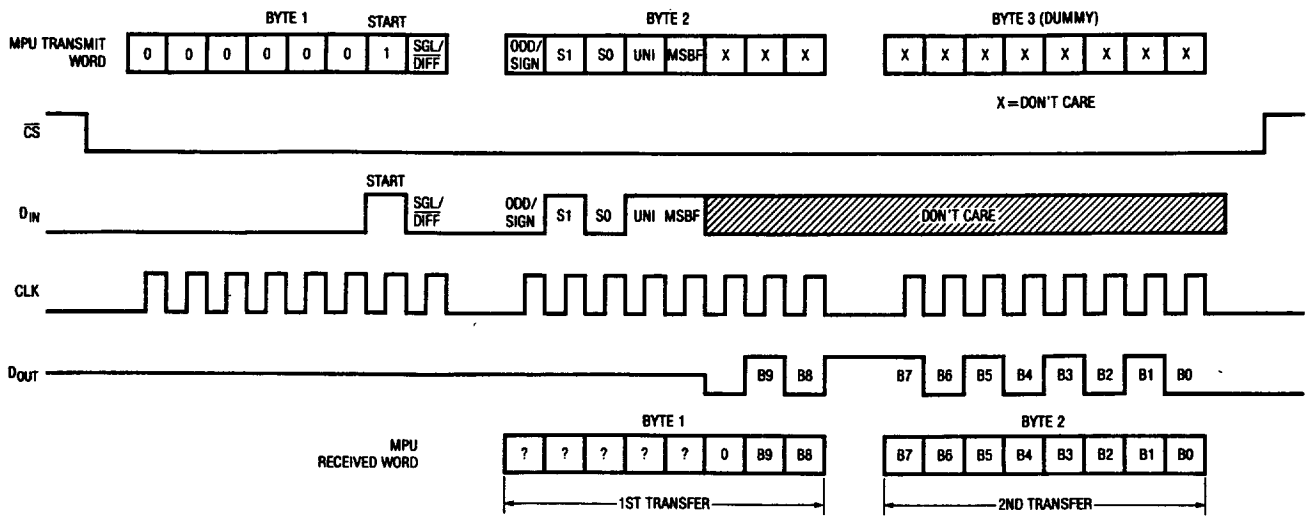
Table 1. Microprocessors with Hardware Serial Interfaces Compatible with the LTC1095

PART NUMBER	TYPE OF INTERFACE
Motorola	
MC6805S2, S3	SPI
MC68HC11	SPI
MC68HC05	SPI
RCA	
CDP68HC05	SPI
Hitachi	
HD6305	SCI Synchronous
HD63705	SCI Synchronous
HD6301	SCI Synchronous
HD63701	SCI Synchronous
HD6303	SCI Synchronous
HD64180	CSI/O
National Semiconductor	
COP400 Family	MICROWIRE†
COP800 Family	MICROWIRE/PLUS†
NS8050U	MICROWIRE/PLUS
HPC16000 Family	MICROWIRE/PLUS
Texas Instruments	
TMS7002	Serial Port
TMS7042	Serial Port
TMS70C02	Serial Port
TMS70C42	Serial Port
TMS32011*	Serial Port
TMS32020	Serial Port
TMS320C25*	Serial Port

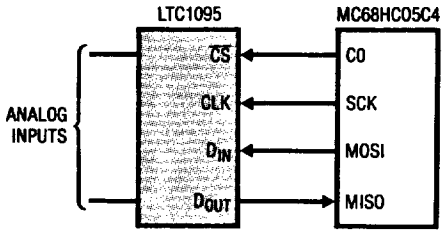
*Requires external hardware
†MICROWIRE and MICROWIRE/PLUS are trademarks of National Semiconductor Corp.

APPLICATIONS INFORMATION

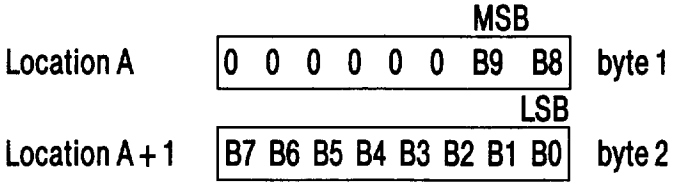
Data Exchange Between LTC1095 and MC68HC05C4



Hardware and Software Interface to Motorola MC68HC05C4 Microcontroller



D_{OUT} from LTC1095 stored in MC68HC05C4 RAM



LABEL	MNEMONIC	COMMENTS
START	BCLRn	Bit 0 Port C goes low ($\overline{CS}$ goes low)
	LDA	Load LTC1095 D_{IN} word into Acc.
	STA	Load LTC1095 D_{IN} word into SPI from Acc. Transfer begins.
	TST	Test status of SPIF
	BPL	Loop to previous instruction if not done with transfer
	LDA	Load next LTC1095 D_{IN} word into Acc.
	STA	Load LTC1095 D_{IN} word into SPI from Acc. Transfer begins.
	TST	Test status of SPIF
	BPL	Loop to previous instruction if not done with transfer
	LDA	Load contents of SPI data register into Acc. (D_{OUT} MSBs)
	STA	Start next SPI cycle
	AND	Clear 6 MSBs of first D_{OUT} word
	STA	Store in memory location A (MSBs)
	TST	Test status of SPIF
	BPL	Loop to previous instruction if not done with transfer
	BSETn	Set B0 of Port C ($\overline{CS}$ goes high)
	LDA	Load contents of SPI data register into Acc. (D_{OUT} LSBs)
	STA	Store in memory location A + 1 (LSBs)

9

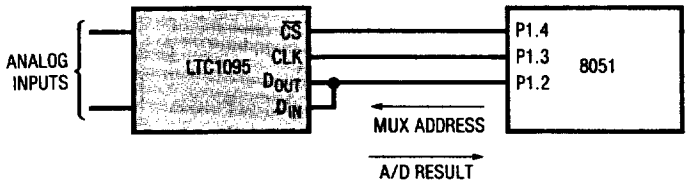
APPLICATIONS INFORMATION

Interfacing to the Parallel Port of the Intel 8051 Family

The Intel 8051 has been chosen to demonstrate the interface between the LTC1095 and parallel port microprocessors. Normally the $\overline{CS}$, CLK and D_{IN} signals would be generated on 3 port lines and the D_{OUT} signal read on a 4th port line. This works very well. However, we will demonstrate here an interface with the D_{IN} and D_{OUT} of the LTC1095 tied together as described in section 4. This saves one wire.

The 8051 first sends the start bit and MUX address to the LTC1095 over the data line connected to P1.2. Then P1.2 is reconfigured as an input (by writing to it a one) and the 8051 reads back the 10-bit A/D result over the same data line.

Hardware and Software Interface to 8051 Microcontroller

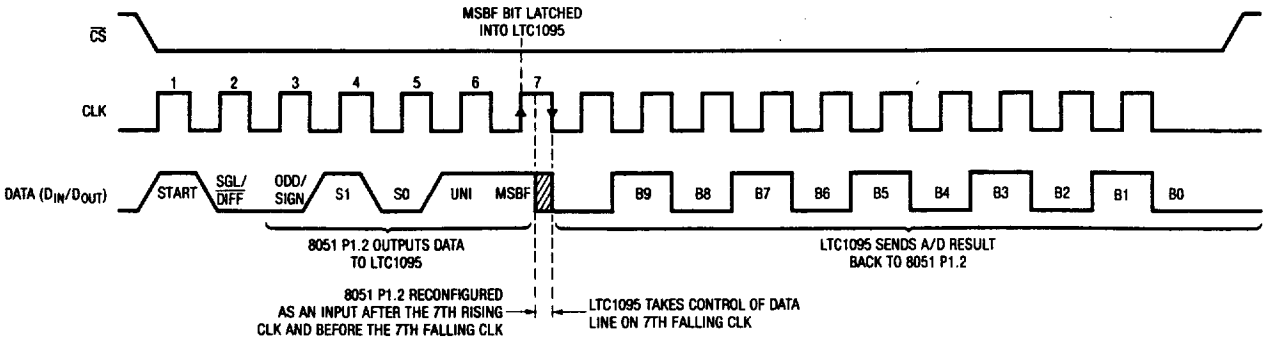


LABEL	MNEMONIC	OPERAND	COMMENTS
	MOV	A, #FFH	D_{IN} word for LTC1095
	SETB	P1.4	Make sure $\overline{CS}$ is high
	CLR	P1.4	$\overline{CS}$ goes low
	MOV	R4, #07	Load counter
LOOP 1	RLC	A	Rotate D_{IN} bit into Carry
	CLR	P1.3	CLK goes low
	MOV	P1.2, C	Output D_{IN} bit to LTC1095
	SETB	P1.3	CLK goes high
	DJNZ	R4, LOOP 1	Next bit
	MOV	P1, #04	Bit 2 becomes an input
	CLR	P1.3	CLK goes low
	MOV	R4, #09	Load counter
LOOP	MOV	C, P1.2	Read data bit into Carry
	RLC	A	Rotate data bit into Acc.
	SETB	P1.3	CLK goes high
	CLR	P1.3	CLK goes low
	DJNZ	R4, LOOP	Next bit
	MOV	R2, A	Store MSBs in R2
	MOV	C, P1.2	Read data bit into Carry
	SETB	P1.3	CLK goes high
	CLR	P1.3	CLK goes low
	CLR	A	Clear Acc.
	RLC	A	Rotate data bit from Carry to Acc.
	MOV	C, P1.2	Read data bit into Carry
	RRC	A	Rotate right into Acc.
	RRC	A	Rotate right into Acc.
	MOV	R3, A	Store LSBs in R3
	SETB	P1.4	$\overline{CS}$ goes high

D_{OUT} from LTC1095 stored in 8051 RAM

	MSB							LSB
R2	B9	B8	B7	B6	B5	B4	B3	B2
R3	B1	B0	0	0	0	0	0	0

Data Exchange Between LTC1095 and 8051



APPLICATIONS INFORMATION

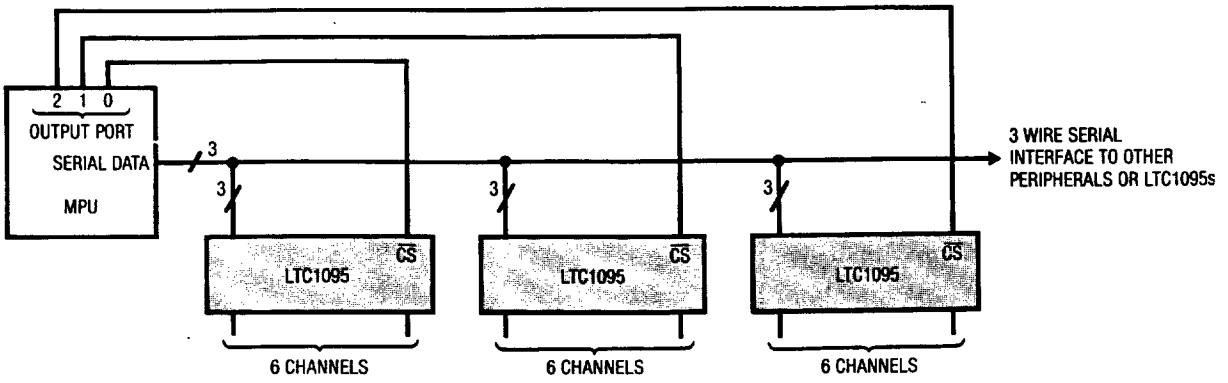


Figure 3. Several LTC1095s Sharing One 3 Wire Serial Interface

Sharing the Serial Interface

The LTC1095 can share the same 2 or 3 wire serial interface with other peripheral components or other LTC1095s (see Figure 3). In this case, the $\overline{CS}$ signals decide which LTC1095 is being addressed by the MPU.

ANALOG CONSIDERATIONS

1. Grounding

The LTC1095 should be used with an analog ground plane and single point grounding techniques.

The AGND pin should be tied directly to this ground plane.

The DGND pin of the LTC1095 can also be tied directly to this ground plane because minimal digital noise is generated within the chip itself.

The V_{CC} pin should be bypassed to the ground plane with a 4.7μF tantalum with leads as short as possible. The V^- pin should be bypassed with a 0.1μF ceramic disk. For single supply applications, V^- can be tied to the ground plane.

It is also recommended that the COM pin be tied directly to the ground plane. All analog inputs should be referenced directly to the single point ground. Digital inputs and outputs should be shielded from and/or routed away from the reference and analog circuitry.

Figure 4 shows an example of an ideal LTC1095 ground plane design for a two sided board. Of course this much ground plane will not always be possible, but users should strive to get as close to this ideal as possible.

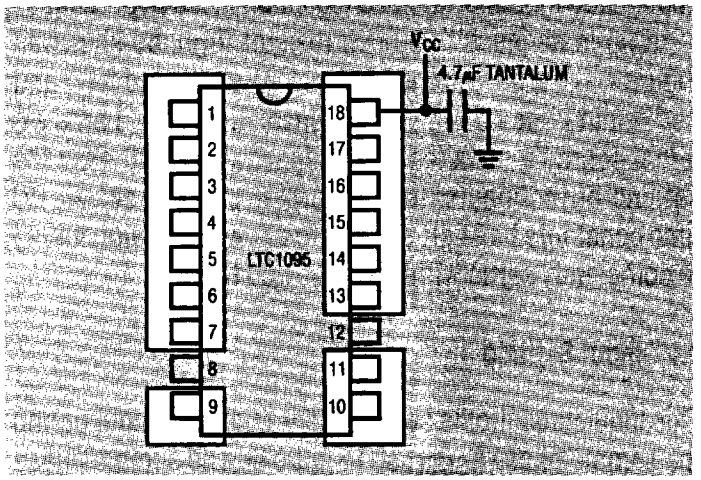


Figure 4. Example Ground Plane for the LTC1095

9

APPLICATIONS INFORMATION

2. Bypassing

For good performance, V_{CC} must be free of noise and ripple. Any changes in the V_{CC} voltage with respect to analog ground during a conversion cycle can induce errors or noise in the output code. V_{CC} noise and ripple can be kept below 1mV by bypassing the V_{CC} pin directly to the analog ground plane with a 4.7µF tantalum with leads as short as possible. Figures 5 and 6 show the effects of good and poor V_{CC} bypassing.

3. Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1095 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. However, if large source resistances are used or if slow settling op amps drive the inputs, care must be taken to insure that the transients caused by the current spikes settle completely before the conversion begins.

Source Resistance

The analog inputs of the LTC1095 look like a 60pF capacitor (C_{IN}) in series with a 500Ω resistor (R_{ON}) as shown in Figure 7. C_{IN} gets switched between the selected "+" and "–" inputs once during each conversion cycle. Large external source resistances and capacitances will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle within the allowed time.

"+" Input Settling

This input capacitor is switched onto the "+" input during the sample phase (t_{SMPL}, see Figure 8). The sample phase is the 1 1/2 CLK cycles before the conversion starts. The voltage on the "+" input must settle completely within this sample time. Minimizing R_{SOURCE}^+ and C1 will improve the input settling time. If large "+" input source resistance must be used, the sample time can be increased by using a slower CLK frequency. With the minimum possible sample time of 3µs, **R_{SOURCE}^+ <2k and C1<20pF will provide adequate settling.**

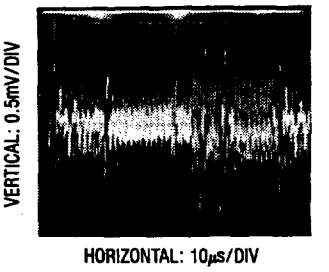


Figure 5. Poor V_{CC} Bypassing. Noise and Ripple Can Cause A/D Errors.

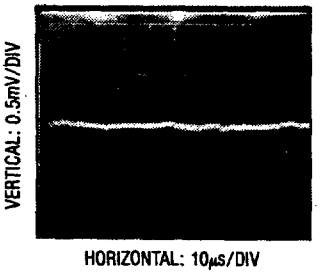


Figure 6. Good V_{CC} Bypassing Keeps Noise and Ripple On V_{CC} Below 1mV

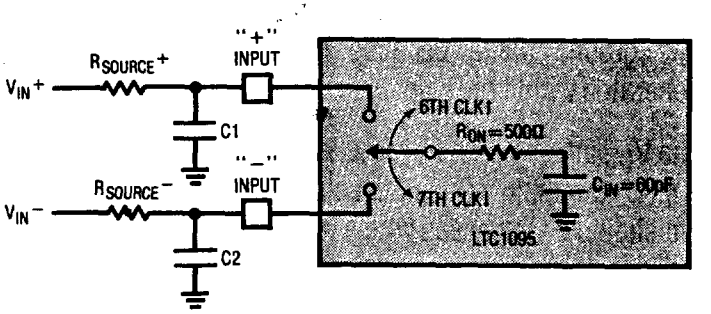


Figure 7. Analog Input Equivalent Circuit

APPLICATIONS INFORMATION

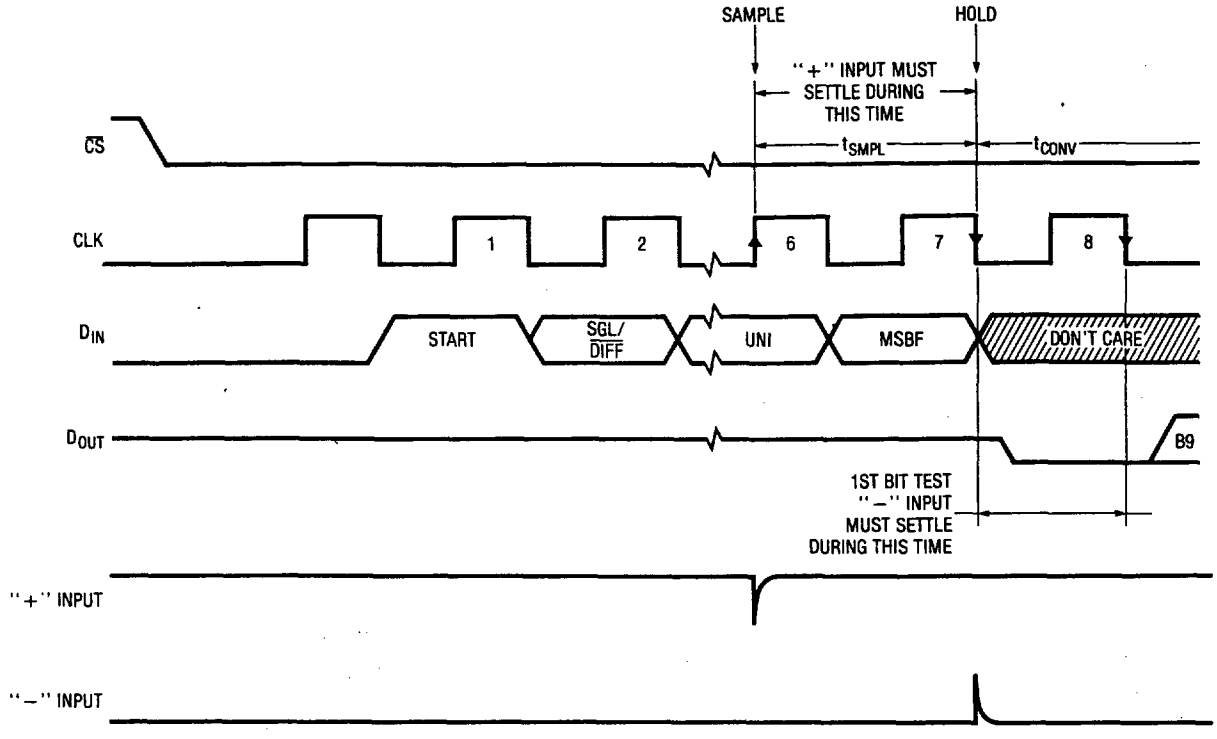


Figure 8. "+" and "–" Input Settling Windows

"–" Input Settling

At the end of the sample phase the input capacitor switches to the "–" input and the conversion starts (see Figure 8). During the conversion, the "+" input voltage is effectively "held" by the sample and hold and will not affect the conversion result. However, it is critical that the "–" input voltage settle completely during the first CLK cycle of the conversion time and be free of noise. Minimizing R_{SOURCE}^- and C2 will improve settling time. If large "–" input source resistance must be used, the time allowed for settling can be extended by using a slower CLK frequency. At the maximum CLK rate of 500kHz, **R_{SOURCE}^- <1kΩ and C2<20pF will provide adequate settling.**

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time (see Figure 8). Again, the "+" and "–" input sampling times can be extended as described above to accommodate slower op amps. Most op amps including the LT1006 and LT1013 single supply op amps, can be made to settle well even with the minimum settling windows of 3μs ("+" input) and 2μs ("–" input) which occur at the maximum clock rate of 500kHz. Figures 9 and 10 show examples of adequate and poor op amp settling.

9

APPLICATIONS INFORMATION

RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 11. For large values of C_F (e.g., 1μF), the capacitive input switching currents are averaged into a net DC current. Therefore, a filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 60pF \times V_{IN}/t_{CYC}$ and is roughly proportional to V_{IN}. When running at the minimum cycle time of 38μs, the input current equals 8μA at $V_{IN} = 5V$. In this case, a filter resistor of 50Ω will cause 0.1LSB of full-scale error. If a larger filter resistor must be used, errors can be eliminated by increasing the cycle time as shown in the typical curve of Maximum Filter Resistor vs Cycle Time.

Input Leakage Current

Input leakage currents can also create errors if the source resistance gets too large. For instance, the maximum input leakage specification of 1μA (at 125°C) flowing through a source resistance of 1kΩ will cause a voltage drop of 1mV or 0.2LSB. This error will be much reduced at lower temperatures because leakage drops rapidly (see typical curve of Input Channel Leakage Current vs Temperature).

4. Sample and Hold

Single Ended Inputs

The LTC1095 provides a built-in sample and hold (S&H) function for signals acquired in the single ended mode. This sample and hold allows conversion of rapidly varying signals (see typical curve of S&H Acquisition Time vs Source Resistance). The input voltage is sampled during the t_{SMPL} time as shown in Figure 8. The sampling interval begins as the bit preceding the MSBF bit is shifted in and continues until the falling CLK edge after the MSBF bit is received. On this falling edge, the S&H goes into hold mode and the conversion begins.

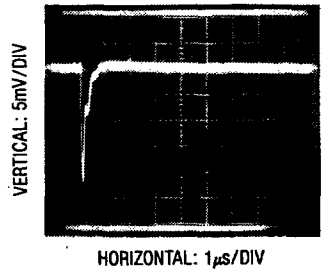


Figure 9. Adequate Settling of Op Amp Driving Analog Input

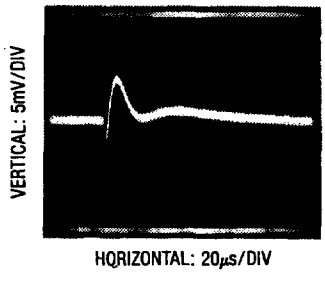


Figure 10. Poor Op Amp Settling Can Cause A/D Errors

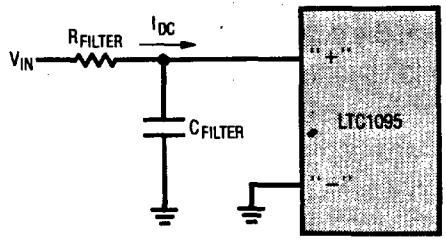


Figure 11. RC Input Filtering

APPLICATIONS INFORMATION

Differential Inputs

With differential inputs, the A/D no longer converts just a single voltage but rather the difference between two voltages. In this case, the voltage on the selected "+" input is still sampled and held and therefore may be rapidly time varying just as in single ended mode. However, the voltage on the selected "–" input must remain constant and be free of noise and ripple throughout the conversion time. Otherwise, the differencing operation may not be performed accurately. The conversion time is 10 CLK cycles. Therefore, a change in the "–" input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the "–" input this error would be:

$$V_{ERROR(MAX)} = V_{PEAK} \times 2 \times \pi \times f(\text{"}-\text{"}) \times 10/f_{CLK}$$

Where f("–") is the frequency of the "–" input voltage, V_{PEAK} is its peak amplitude and f_{CLK} is the frequency of the CLK. In most cases V_{ERROR} will not be significant. For a 60Hz signal on the "–" input to generate a 1/4LSB error (1.25mV) with the converter running at CLK = 500kHz, its peak value would have to be 150mV.

5. Internal Reference

The LTC1095 contains an internal precision 5V buried zener reference which is capable of supplying the full scale reference for the converter when connected as shown in Figure 15. With its 10mA output current the reference can also power the A/D and other external circuitry to provide a TTL input/TTL output system running off a single 7.2V–40V supply (see Figure 16).

6. Reference Input

The voltage on the reference input of the LTC1095 defines the voltage span of the A/D converter. The reference input looks primarily like a 10kΩ resistor to ground but will have transient capacitive switching currents due to the switched capacitor conversion technique (see Figure 12). During each bit test of the conversion (every CLK cycle), a capacitive current spike will be generated on the reference pin by the A/D. These current spikes settle quickly and do not cause a problem. However, if slow settling circuitry is used to drive the reference input, care must be taken to ensure that transients caused by these current spikes settle completely during each bit test of the conversion.

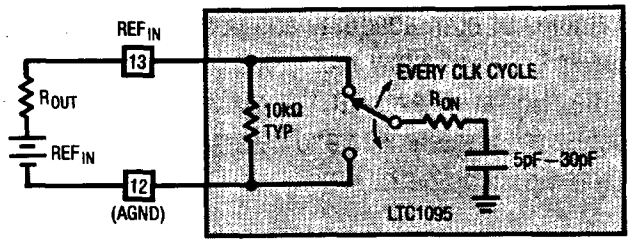


Figure 12. Reference Input Equivalent Circuit

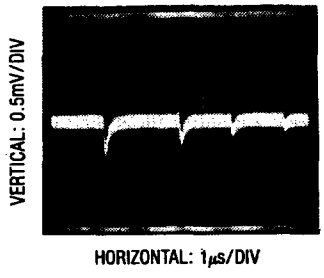


Figure 13. Adequate Reference Settling

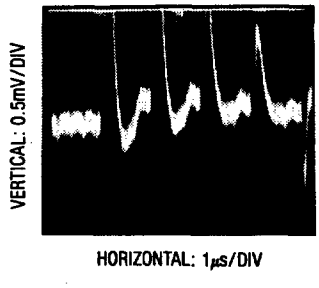


Figure 14. Poor Reference Settling Can Cause A/D Errors

9

APPLICATIONS INFORMATION

When driving the reference input, three things should be kept in mind:

1. The source resistance (R_{OUT}) driving the reference input should be low (less than 1Ω) to prevent DC drops caused by the 1mA maximum reference current ($I_{REF\ IN}$).
2. Transients on the reference input caused by the capacitive switching currents must settle completely during each bit test (each CLK cycle). Figures 13 and 14 show examples of both adequate and poor settling. Using a slower CLK will allow more time for the reference to settle. However, even at the maximum CLK rate of 500kHz most references and op amps can be made to settle within the 2μs bit time.
3. It is recommended that REF_{IN} be tied to REF_{OUT} as shown in Figure 15.

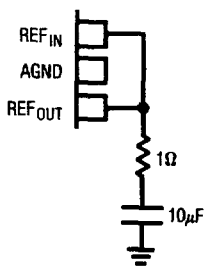


Figure 15. Suggested Circuit for REF_{IN} Tied to REF_{OUT}

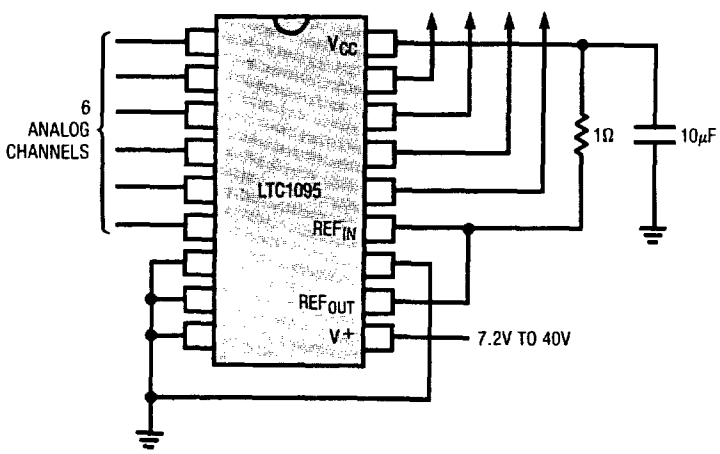


Figure 16. LTC1095 Single Supply Operation

7. Reduced Reference Operation

The LTC1095 can operate with reference voltages below 1V, by dividing down the 5V reference output voltage as shown in Figure 17.

The effective resolution of the LTC1095 will be increased by reducing the input span of the converter. The LTC1095 exhibits good linearity and gain over a wide range of reference voltages (see typical curves of Linearity and Full Scale Error vs Reference Voltage). However, care must be taken when operating at low values of $V_{REF\ IN}$ because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. The following factors must be considered when operating at low $V_{REF\ IN}$ values.

1. Offset
2. Noise
3. Conversion speed (CLK frequency)

Offset with Reduced Reference Voltages

The offset of the LTC1095 has a larger effect on the output code when the A/D is operated with reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Unadjusted Offset Error vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of V_{OS}. For example, a

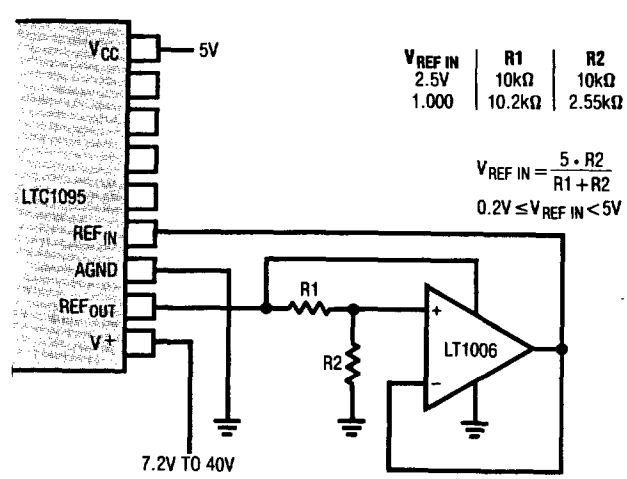


Figure 17. Operating LTC1095 on Reduced Reference Voltage

APPLICATIONS INFORMATION

V_{OS} of 0.5mV which is 0.1LSB with a 5V reference becomes 0.5LSB with a 1V reference and 2.5LSBs with a 0.2V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the "–" input to the LTC1095.

Noise with Reduced Reference Voltages

The total input referred noise of the LTC1095 can be reduced to approximately 200μV peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference input. This noise is insignificant with a 5V reference but will become a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Noise Error vs Reference Voltage shows the LSB contribution of this 200μV of noise.

For operation with a 5V reference, the 200μV noise is only 0.04LSB peak-to-peak. In this case, the LTC1095 noise will contribute virtually no uncertainty to the output code. However, for reduced references, the noise may cause undesirable jitter in the output code. For example, with a 1V reference, this same 200μV noise is 0.2LSB peak-to-peak. This will reduce the range of input voltages, over which a stable output code can be achieved, by 0.2LSB. If the reference is further reduced to 200mV, the 200μV noise becomes equal to one LSB and a stable code may be difficult to achieve. In this case, averaging readings may be necessary.

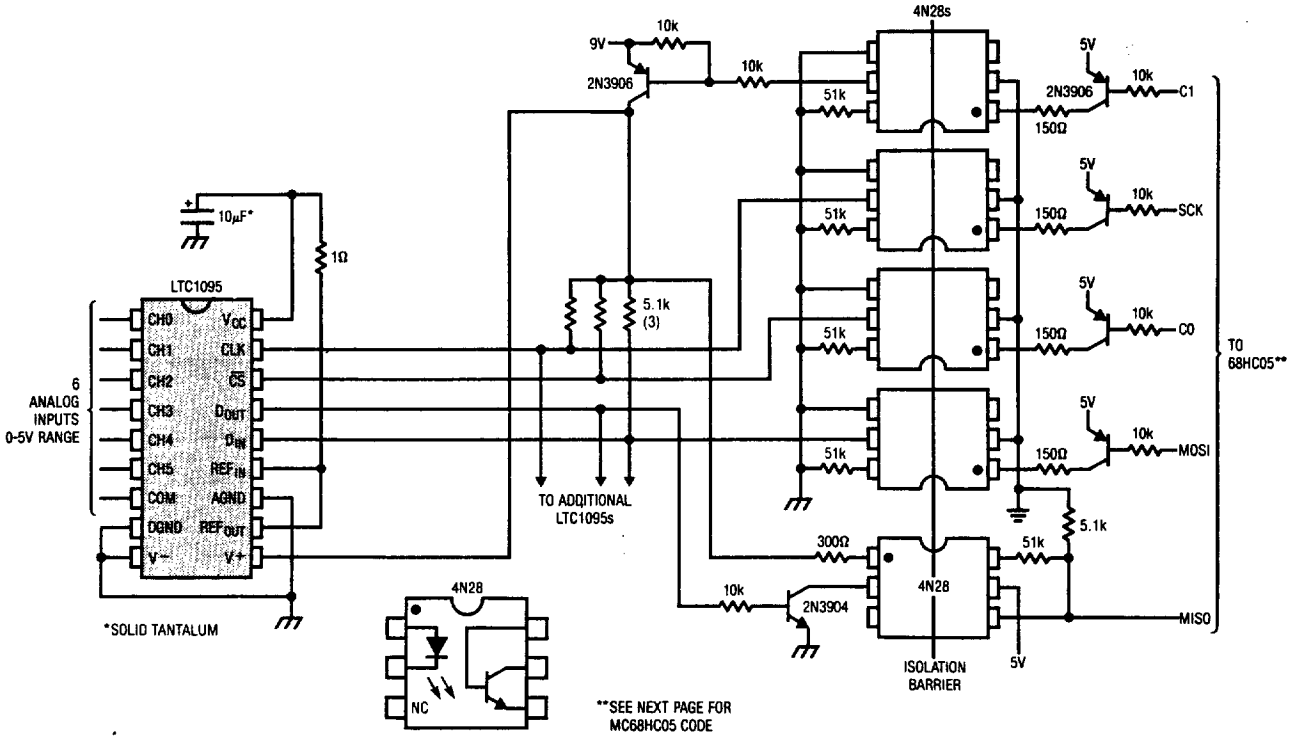
This noise data was taken in a very clean setup. Any setup induced noise (noise or ripple on: V_{CC}, REF_{IN}, V_{IN} or V^-) will add to the internal noise. The lower the reference voltage to be used, the more critical it becomes to have a clean, noise-free setup.

Conversion Speed with Reduced Reference Voltages

With reduced reference voltages, the LSB step size is reduced and the LTC1095 internal comparator overdrive is reduced. Therefore, it may be necessary to reduce the maximum CLK frequency when low reference voltages are used.

TYPICAL APPLICATIONS

Micropower, 500V Opto Isolated, Multichannel, 10-Bit Data Acquisition System



TYPICAL APPLICATIONS

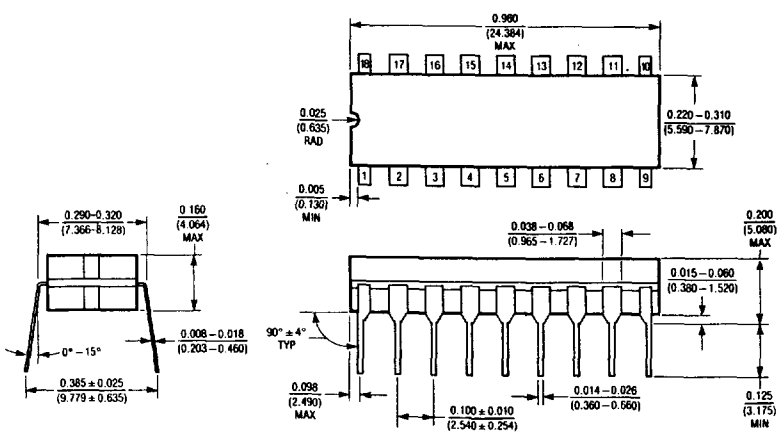
68HC05 Code Communicates with LTC1095 through Opto-Isolators

LABEL	MNEMONIC	OPERAND	COMMENTS
	ORG	$100	
	CLRX		Clear X register
	LDA	#$1F	CH0
	STA	$50	CH0 address
	LDA	#$9F	CH1
	STA	$51	CH1 address
	LDA	#$3F	CH2
	STA	$52	CH2 address
	LDA	#$BF	CH3
	STA	$53	CH3 address
	LDA	#$5F	CH4
	STA	$54	CH4 address
	LDA	#$DF	CH5
	STA	$55	CH5 address
	LDA	#$53	Data for SPCR
	STA	$0A	Load data into SPCR
	LDA	#$FF	Data for DDR
	STA	$06	Configure PORT C DDR
START	BCLR	1,$02	C1 (PWR OFF) goes low
	LDA	#$FF	Load counter
T1	DECA		Decrement Acc.
	BNE	T1	
	LDA	#$FF	Load counter
T2	DECA		Decrement Acc.
	BNE	T2	
	LDA	#$FF	Load counter
T3	DECA		Decrement Acc.
	BNE	T3	
	LDA	#$FF	Load counter

LABEL	MNEMONIC	OPERAND	COMMENTS
T4	DECA		Decrement Acc.
	BNE	T4	
START1	BCLR	0,$02	C0 ($\overline{CS}$) goes low
	LDA	#$03	D_{IN} prefix start and SGL
	STA	$0C	Start transfer
TEST2	TST	$0B	Test if done
	BPL	TEST2	If not try again
	LDA	$50,X	Put D_{IN} word in Acc.
	STA	$0C	Start transfer
TEST	TST	$0B	Test if done
	BPL	TEST	If not try again
	LDA	#0C	Load MSBs in Acc.
	STA	$60,X	Store MSBs in $60 + X
SKIP	LDA	#$FF	Insure 1's output last
	STA	$0C	Start next transfer
TEST1	TST	$0B	Test if done
	BPL	TEST1	If not try again
	BSET	0,$02	C0 ($\overline{CS}$) goes high
	LDA	$0C	Put LSBs in Acc.
	STA	$70,X	Put LSBs in $70 + x
SKIP1	INCX		Increment X register
	CPX	#$06	Check if done
	BNE	START1	
	BSET	1,$02	Set C1 (PWR OFF)
	CLRX		Reset counter
	JMP		Start next loop

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J Package
18-Lead Ceramic DIP



N Package
18-Lead Plastic DIP