Dual, Precision JFET Input Op Amp

FEATURES

- **Handles 10,000pF Capacitive Load**
- 450µV Max Offset Voltage
- 1200µV Max Offset Voltage in S8 Package
- **50pA Bias Current at 70°C**
- 13nV/√Hz Voltage Noise
- 4V/µs Slew Rate
- 4µV/°C Drift
- 130dB Channel Separation

APPLICATIONS

- Sample-and-Hold (Drives Large Hold Capacitors)
- A/D and D/A Converters
- Photodiode Amplifiers
- Voltage-to-Frequency Converters

DESCRIPTION

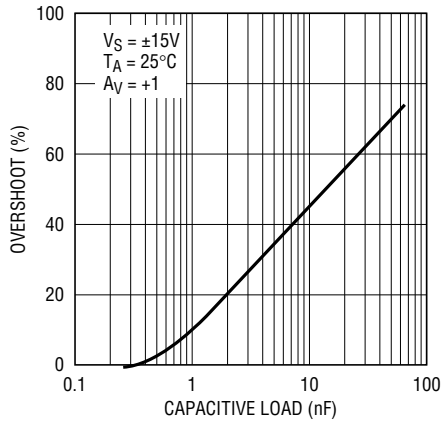
The LT1457 is a dual, JFET input op amp optimized for handling large capacitive loads in combination with precision performance.

Precision specifications include 220µV offset voltage in plastic and surface mount packages. At 70°C input bias current is 50pA, input offset current is 20pA. Channel separation is 130dB.

Other dual JFET input op amps from Linear Technology include the LT1057, which is three times faster than the LT1457 but at the expense of significantly lower capacitive load handling capability; and the LT1113 with 4.5nV/√Hz voltage noise.

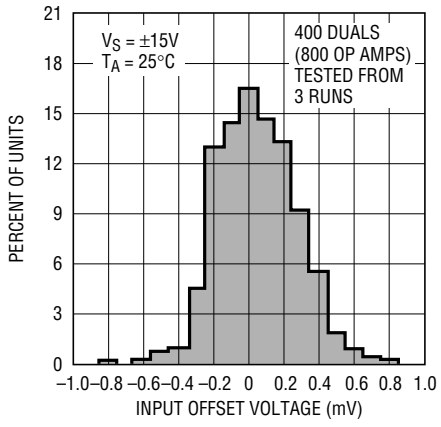
TYPICAL PERFORMANCE CHARACTERISTICS

Capacitive Load Handling



LT11457• TA01

Input Offset Voltage Distribution S8 Package

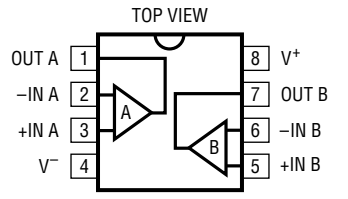


LT1457 • TA02

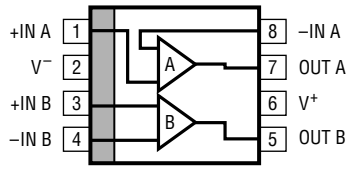
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Differential Input Voltage ..... ±40V
Input Voltage ..... Equal to Supply Voltages
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP
T_{JMAX} = 115°C, θ_{JA} = 130°C/W



S8 PACKAGE
8-LEAD PLASTIC SOIC

NOTE: THIS PIN CONFIGURATION DIFFERS FROM THE 8-LEAD DIP PIN LOCATIONS. INSTEAD, IT FOLLOWS THE INDUSTRY STANDARD LT1013DS8 SO PACKAGE CONFIGURATION.

T_{JMAX} = 130°C, θ_{JA} = 190°C/W

ORDER PART NUMBER
LT1457ACN8 LT1457CN8
LT1457S8
S8 PART MARKING
1457

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_S = ±15V, T_A = 25°C, V_{CM} = 0V unless otherwise noted. (Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1457AC MIN	LT1457AC TYP	LT1457AC MAX	LT1457C/LT1457S8 MIN	LT1457C/LT1457S8 TYP	LT1457C/LT1457S8 MAX	UNITS
V_{OS}	Input Offset Voltage	LT1457AC/C LT1457S8		150	450		200 220	800 1200	µV µV
I_{OS}	Input Offset Current	Fully Warmed Up		3	40		4	50	pA
I_B	Input Bias Current	Fully Warmed Up		±5	±50		±7	±75	pA
	Input Resistance-Differential -Common-Mode	 V_{CM} = –11V to 8V V_{CM} = 8V to 11V		10^{12} 10^{12} 10^{11}			10^{12} 10^{12} 10^{11}		Ω Ω Ω
	Input Capacitance			4			4		pF
e_n	Input Noise Voltage	0.1Hz to 10Hz		2.0			2.1		μV_{P-P}
e_n	Input Noise Voltage Density	f_O = 10Hz f_O = 1kHz (Note 2)		26 13	 22		28 14	 24	nV/√Hz nV/√Hz
i_n	Input Noise Current Density	f_O = 10Hz, 1kHz (Note 3)		1.5	4		1.8	6	fA/√Hz
A_{VOL}	Large-Signal Voltage Gain	V_O = ±10V, R_L = 2k V_O = ±10V, R_L = 1k	150 120	350 250		100 80	300 220		V/mV V/mV
	Input Voltage Range		±10.5	14.3 –11.5		±10.5	14.3 –11.5		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±10.5V	86	100		82	98		dB
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V to ±18V	88	103		86	102		dB
V_{OUT}	Output Voltage Swing	R_L = 2k	±12	±13		±12	±13		V
SR	Slew Rate		2	4		2	4		V/µs

ELECTRICAL CHARACTERISTICS

V_S = ±15V, T_A = 25°C, V_{CM} = 0V unless otherwise noted. (Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1457AC MIN	LT1457AC TYP	LT1457AC MAX	LT1457C/LT1457S8 MIN	LT1457C/LT1457S8 TYP	LT1457C/LT1457S8 MAX	UNITS
GBW	Gain-Bandwidth Product	(Note 5)	1.0	1.7		1.0	1.7		MHz
I_S	Supply Current Per Amplifier			1.8	3.0		1.8	3.0	mA
	Channel Separation	DC to 5kHz, V_{IN} = ±10V		132			130		dB

ELECTRICAL CHARACTERISTICS

V_S = ±15V, V_{CM} = 0V, 0°C ≤ T_A ≤ 70°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1457AC MIN	LT1457AC TYP	LT1457AC MAX	LT1457C/LT1457S8 MIN	LT1457C/LT1457S8 TYP	LT1457C/LT1457S8 MAX	UNITS
V_{OS}	Input Offset Voltage	LT1457AC/C	●		250	900		330	1500	µV
		LT1457S8	●					400	1900	µV
	Average Temperature Coefficient of Input Offset Voltage (Note 4)		●		3	10		4	16	µV/°C
I_{OS}	Input Offset Current	Warmed Up, T_A = 70°C			18	150		20	250	pA
I_B	Input Bias Current	Warmed Up, T_A = 70°C			±50	±250		±60	±350	pA
A_{VOL}	Large-Signal Voltage Gain	V_O = ±10V, R_L = 2k	●	70	220		50	200		V/mV
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±10.4V	●	85	98		80	96		dB
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V to ±18V	●	87	102		84	100		dB
V_{OUT}	Output Voltage Swing	R_L = 2k	●	±12	±12.8		±12	±12.8		V
I_S	Supply Current Per Amplifier		●			3.2			3.2	mA
		T_A = 70°C			1.7			1.7		mA

ELECTRICAL CHARACTERISTICS

V_S = ±15V, V_{CM} = 0V, –40°C ≤ T_A ≤ 85°C, unless otherwise noted. (Note 6)

SYMBOL	PARAMETER	CONDITIONS		LT1457AC MIN	LT1457AC TYP	LT1457AC MAX	LT1457C/LT1457S8 MIN	LT1457C/LT1457S8 TYP	LT1457C/LT1457S8 MAX	UNITS
V_{OS}	Input Offset Voltage	LT1457AC/C	●		350	1100		400	1800	µV
		LT1457S8	●					500	2300	µV
	Average Temperature Coefficient of Input Offset Voltage		●		3	10		4	16	µV/°C
I_{OS}	Input Offset Current	Warmed Up, T_A = 85°C			0.1	0.5		0.1	0.6	nA
I_B	Input Bias Current	Warmed Up, T_A = 85°C			±0.2	±0.7		±0.2	±0.9	nA
A_{VOL}	Large-Signal Voltage Gain	V_O = ±10V, R_L = 2k	●	40	120		30	110		V/mV
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±10.4V	●	84	97		80	95		dB
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±17V	●	86	100		83	98		dB
V_{OUT}	Output Voltage Swing	R_L = 2k	●	±12	±12.7		±12	±12.6		V
I_S	Supply Current Per Amplifier	T_A = – 40°C				3.8			3.8	mA
		T_A = 85°C			1.7			1.7		mA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Typical parameters are defined as the 60% yield of distributions of individual amplifiers; i.e., out of 100 LT1457s (200 op amps) typically 120 will be better than the indicated specification.

Note 2: This parameter is tested on a sample basis only.

Note 3: Current noise is calculated from the formula: $i_n = (2qI_b)^{1/2}$, where $q = 1.6 \times 10^{-19}$ coulomb. The noise of source resistors up to 1GΩ swamps the contribution of current noise.

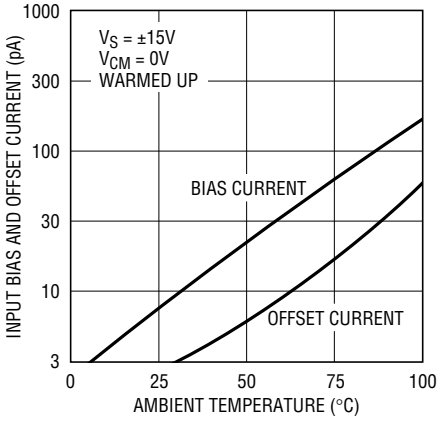
Note 4: This parameter is not 100% tested.

Note 5: Gain-Bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.

Note 6: The LT1457 is not tested and not quality-assurance-sampled at –40°C and at 85°C. These specifications are guaranteed by design, correlation, and/or inference from 0°C, 25°C, and 70°C tests.

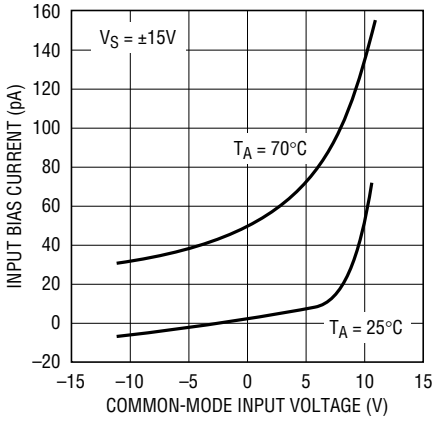
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias and Offset Current vs Temperature



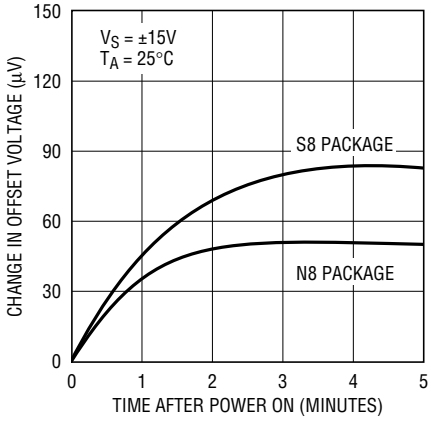
LT1457 • TPC01

Input Bias Current Over the Common-Mode Range



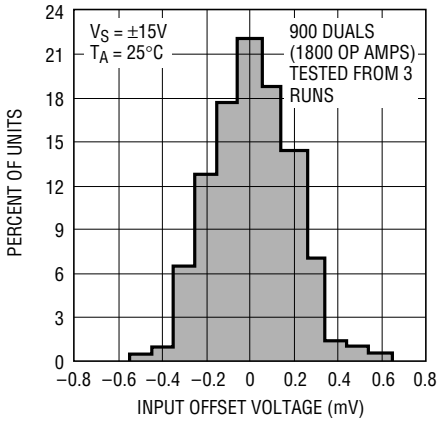
LT1457 • TPC02

Warm-Up Drift



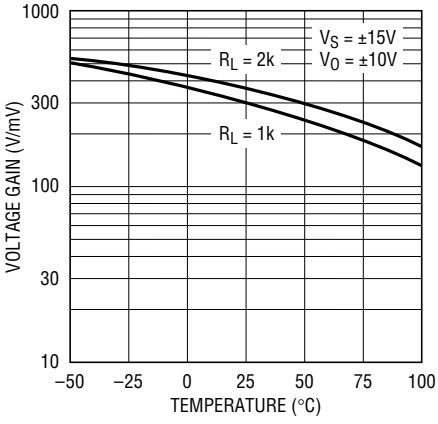
LT1457 • TPC03

Input Offset Voltage Distribution N8 Package



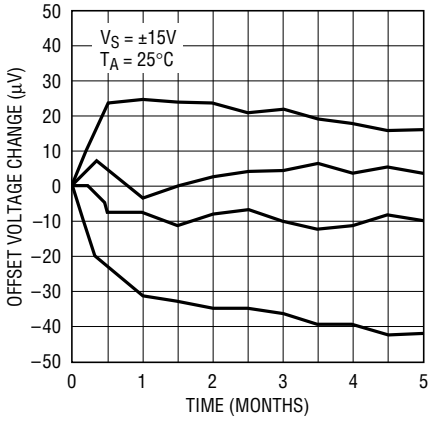
LT1457 • TPC04

Voltage Gain vs Temperature



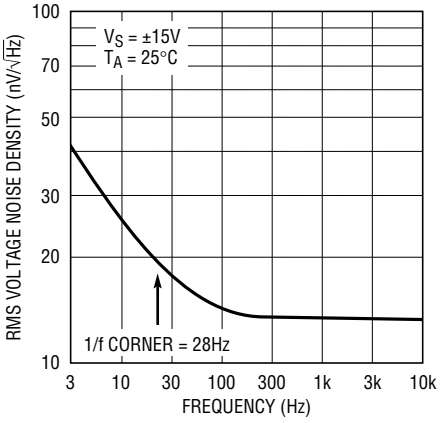
LT1457 • TPC05

Long Term Drift of Representative Units



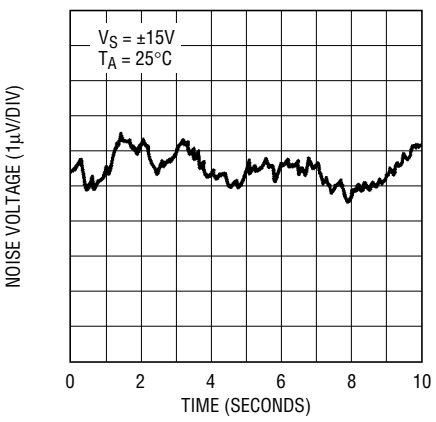
LT1457 • TPC06

Voltage Noise vs Frequency



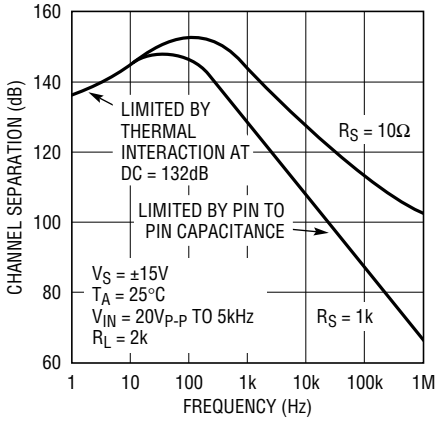
LT1457 • TPC07

0.1Hz to 10Hz Noise



LT1457 • TPC08

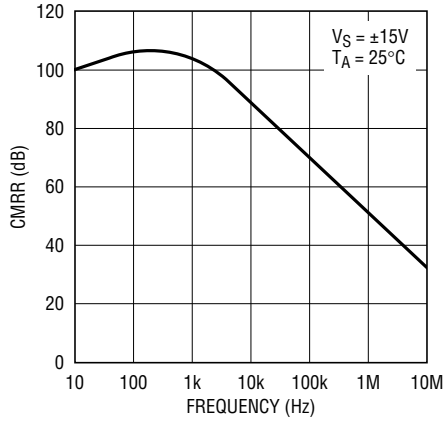
Channel Separation vs Frequency



LT1457 • TPC09

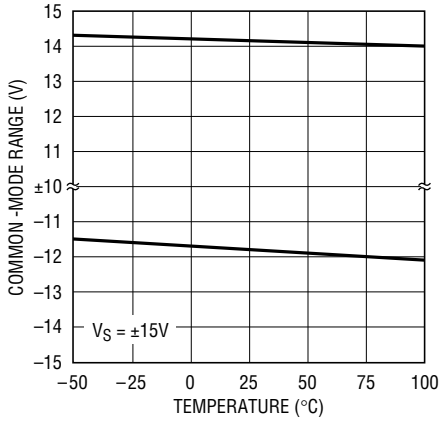
TYPICAL PERFORMANCE CHARACTERISTICS

Common-Mode Rejection Ratio vs Frequency



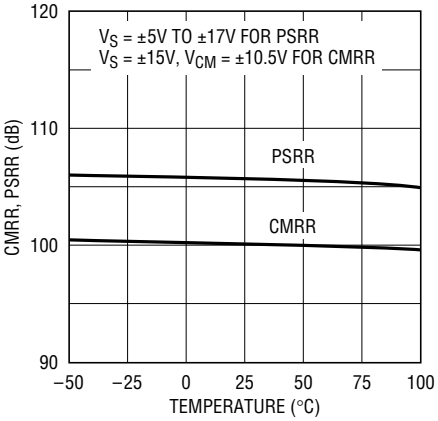
LT1457• TPC10

Common-Mode Range vs Temperature



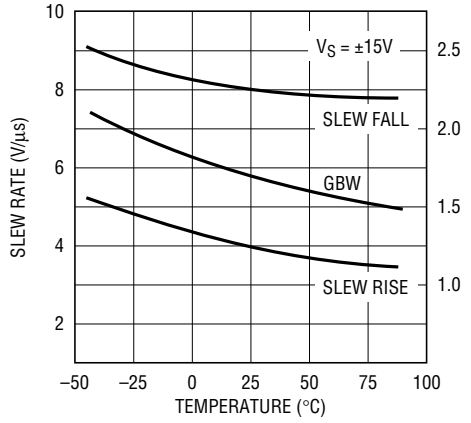
LT1457 • TPC11

Common-Mode and Power Supply Rejections vs Temperature



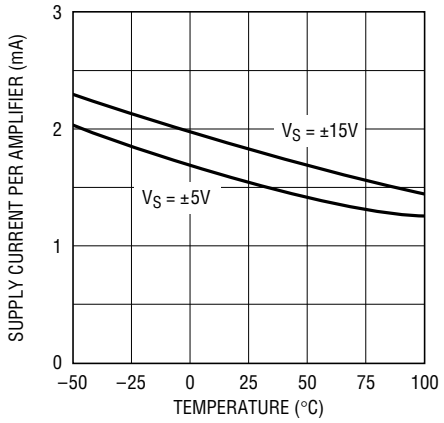
LT1457 • TPC12

Slew Rate, Gain-Bandwidth Product vs Temperature



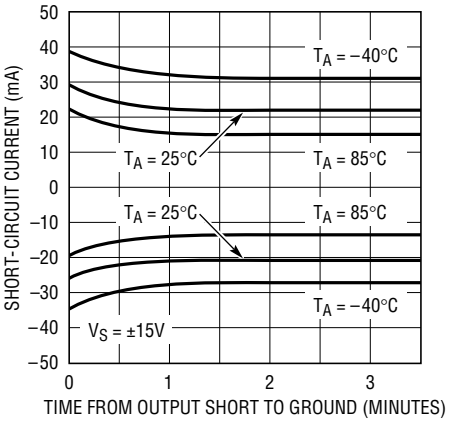
LT1457 • TPC18

Supply Current vs Temperature



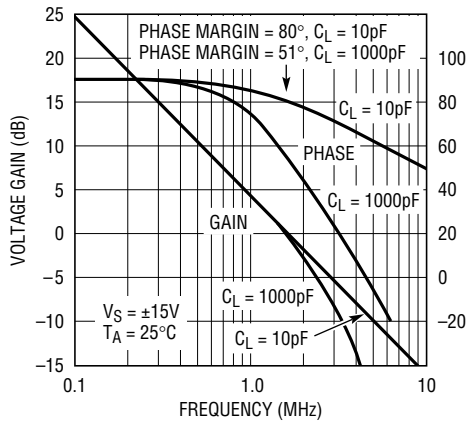
LT1457 • TPC14

Short-Circuit Current vs Time (One Output Shorted to Ground)



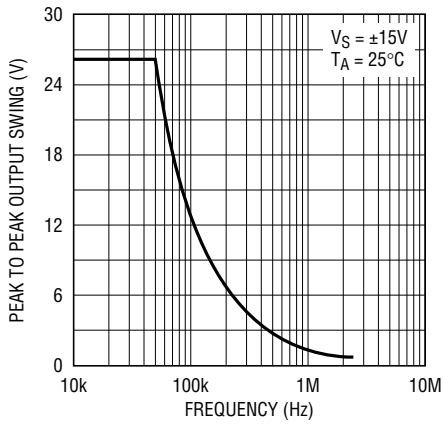
LT1457 • TPC15

Gain, Phase vs Frequency



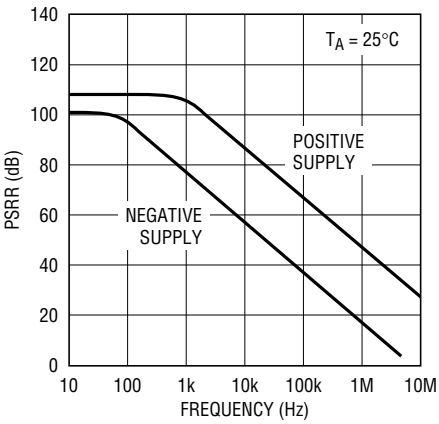
LT1457 • TPC16

Undistorted Output Swing vs Frequency



LT11457• TPC17

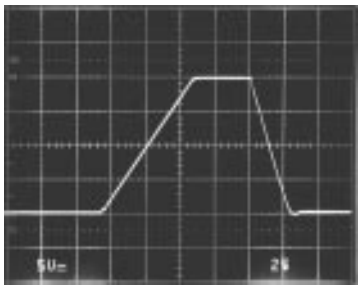
Power Supply Rejection Ratio vs Frequency



LT1457• TPC13

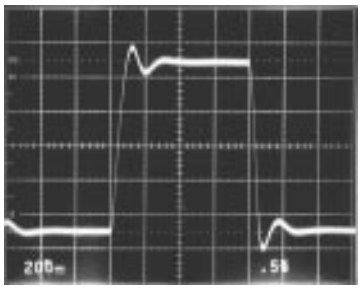
TYPICAL PERFORMANCE CHARACTERISTICS

Large-Signal Response
A_V = 1, C_L = 100pF



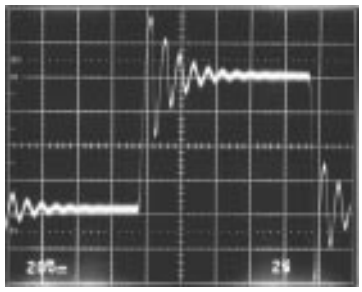
LT1457 TPC19

Small-Signal Response
A_V = 1, C_L = 1000pF



LT1457 TPC20

Small-Signal Response
A_V = 1, C_L = 10,000pF



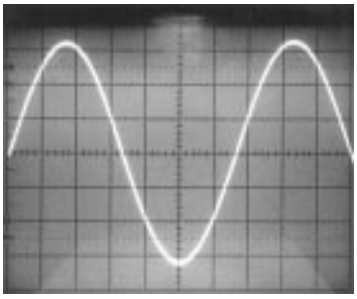
LT1457 TPC21

APPLICATIONS INFORMATION

Phase Reversal Protection

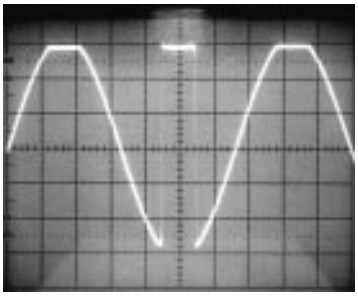
Most industry standard JFET input single, dual, and quad op amps (e.g., LF156, LF351, LF353, LF411, LF412, OP-15, OP-16, OP-215, and TL084) exhibit phase reversal at the output when the negative common-mode limit at the input is exceeded (i.e., below –12V with ±15V supplies). The photos show a ±16V sine wave input (A), the response of an LF412A in the unity gain follower mode (B), and the response of the LT1457 (C).

The phase reversal of photo (B) can cause lock-up in servo systems. The LT1457 does not phase-reverse due to a unique phase reversal protection circuit.



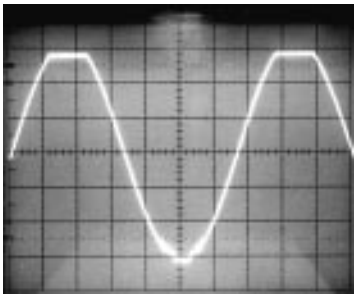
LT1457 AI01

(A) ±16V Sine Wave Input



LT1457 AI02

(B) LF412A Output



LT1457 AI03

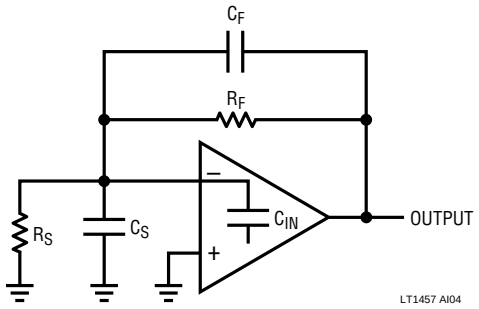
(C) LT1457 Output

All Photos 5V/Div Vertical Scale, 50μs/Div Horizontal Scale

APPLICATIONS INFORMATION

High Speed Operation

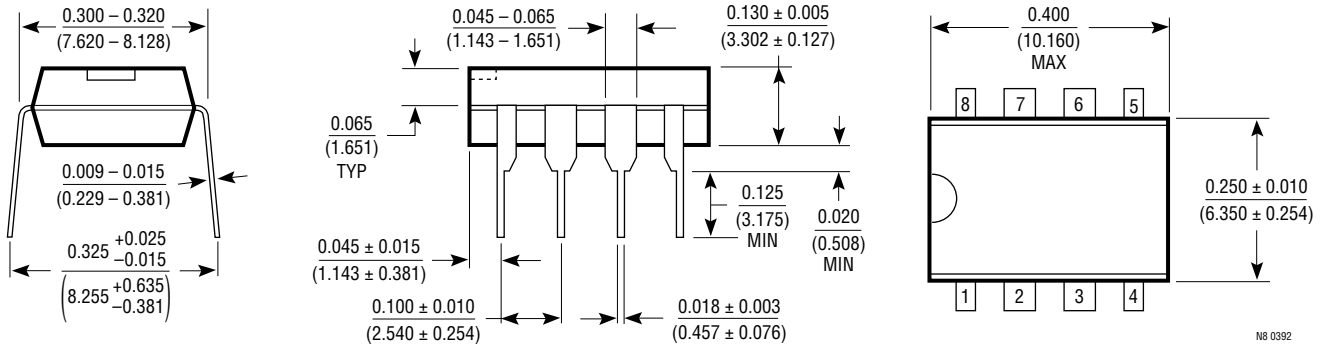
When the feedback around the op amp is resisitive (R_F), a pole will be created with R_F, the source resistance and capacitance (R_S, C_S), and the amplifier input capacitance ($C_{IN} \approx 4pF$). In low closed loop gain configurations and with R_S and R_F in the kilohm range, this pole can create excess phase shift and even oscillation on high speed amplifiers. Because the LT1457's phase margin is very high, this problem is minimal. However, a small capacitor (C_F) in parallel with R_F eliminates this problem. With $R_S(C_S + C_{IN}) = R_FC_F$, the effect of the feedback pole is completely removed.



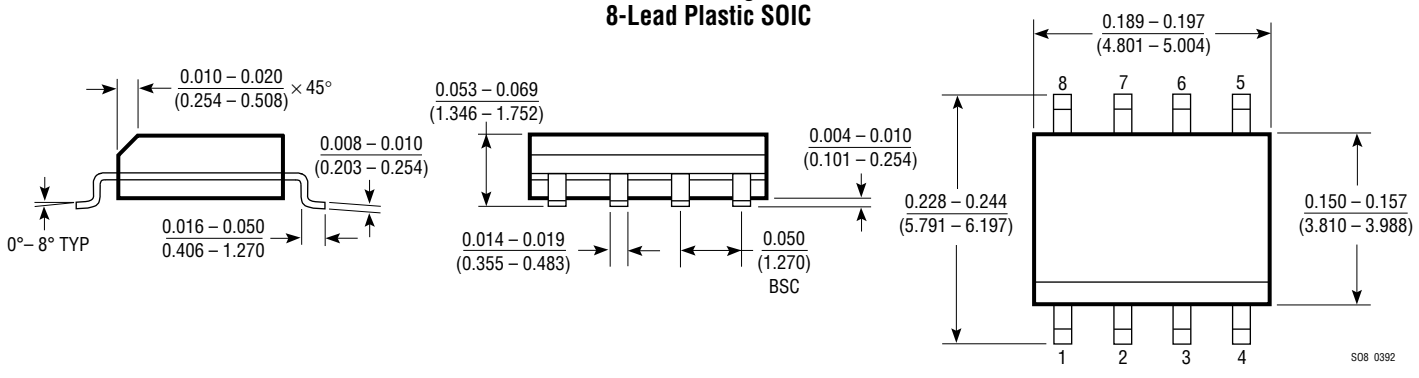
PACKAGE DESCRIPTION

Dimension in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead Plastic DIP



S8 Package
8-Lead Plastic SOIC



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