INITIAL RELEASE
Final Electrical Specifications

LTC1450/LTC1450L

Parallel Input, 12-Bit Rail-to-Rail Micropower DACs in SSOP

December 1995

FEATURES

- 12-Bit Resolution
- **Buffered True Rail-to-Rail Voltage Output**
- 3V Operation (LTC1450L) I_{CC}: 250µA Typ
- 5V Operation (LTC1450) I_{CC}: 400µA Typ
- Parallel 12-Bit or 8 + 4-Bit Double Buffered Digital Input
- Internal Reference
- Output Buffer Configurable to Gain of 1 or 2
- Configurable as a Multiplying DAC
- Internal Power-On Reset
- **Maximum DNL Error: 0.5LSB**

APPLICATIONS

- Digital Calibration
- Industrial Process Control
- Automatic Test Equipment
- Arbitrary Function Generators
- Battery-Powered Data Conversion Products

DESCRIPTION

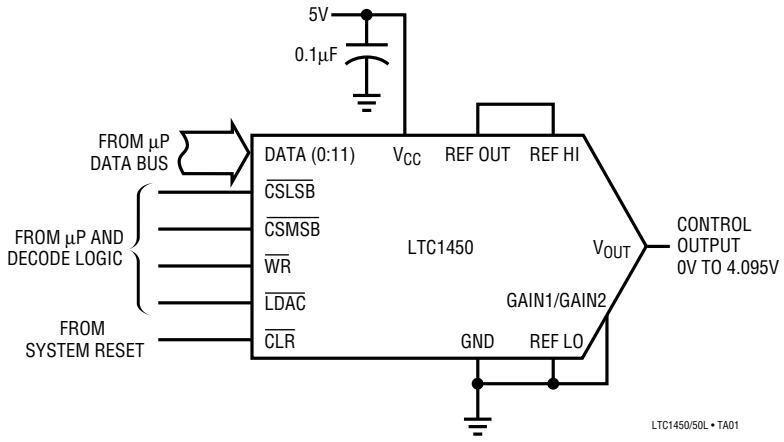
The LTC®1450/LTC1450L are complete single supply, rail-to-rail voltage output, 12-bit digital-to-analog converters (DACs) in a 24-pin SSOP or PDIP package. They include an output buffer amplifier, reference and a double buffered parallel digital interface.

The LTC1450 operates from a 4.5V to 5.5V supply. The output can be configured for 4.095V or 2.048V full-scale. It has a 2.048V internal reference.

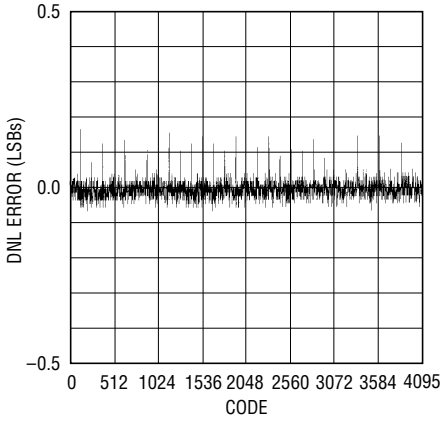
The LTC1450L operates from a 2.7V to 5.5V supply. The output can be configured for 2.5V or 1.22V full-scale. It has a 1.22V internal reference.

The LTC1450/LTC1450L offer true stand-alone performance. In addition, the reference output, high and low reference inputs and gain setting resistor are brought to pins for maximum flexibility.

TYPICAL APPLICATION



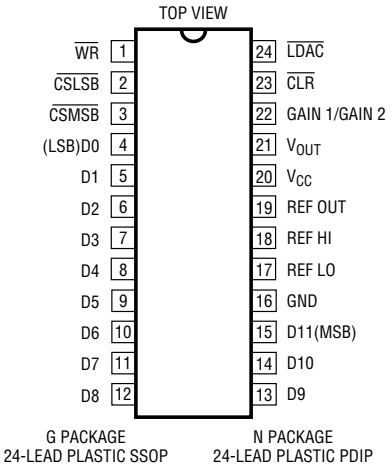
Differential Nonlinearity vs Input Code



ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ..... –0.5V to 7.5V
TTL Input Voltage ..... –0.5V to 7.5V
V_{OUT} ..... –0.5V to V_{CC} + 0.5V
REF OUT ..... –0.5V to V_{CC} + 0.5V
Maximum Junction Temperature ..... 125°C
Operating Temperature Range
Commercial ..... 0°C to 70°C
Industrial ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
24-LEAD PLASTIC SSOP

N PACKAGE
24-LEAD PLASTIC PDIP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W (G)
T_{JMAX} = 125°C, θ_{JA} = 58°C/W (N)

ORDER PART NUMBER

LTC1450CG
LTC1450CN
LTC1450IG
LTC1450IN
LTC1450LCG
LTC1450LCN
LTC1450LIG
LTC1450LIN

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5V to 5.5V (LTC1450), 2.7V to 5.5V (LTC1450L), internal or external reference ($V_{REF\ OUT} \leq V_{CC}/2$), V_{OUT} unloaded, REF OUT = REF HI, REF LO = GND = GAIN 1/GAIN 2, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DAC							
	Resolution		●	12			Bits
DNL	Differential Nonlinearity	Guaranteed Monotonic (Note 1)	●			±0.5	LSB
INL	Integral Nonlinearity	T_A = 25°C				±3.5	LSB
		(Note 1)	●			±4.0	LSB
V_{OS}	Offset Error	T_A = 25°C				±12	mV
			●			±18	mV
V_{OS} TC	Offset Error Temperature Coefficient				±15		µV/°C
V_{FS}	Full-Scale Voltage	Using Internal Reference, LTC1450, T_A = 25°C		4.065	4.095	4.125	V
		Using Internal Reference, LTC1450	●	4.045	4.095	4.145	V
		External 2.048V Reference, LTC1450	●	4.075	4.095	4.115	V
		Using Internal Reference, LTC1450L, T_A = 25°C		2.470	2.500	2.530	V
		Using Internal Reference, LTC1450L	●	2.460	2.500	2.540	V
		External 1.22V Reference, LTC1450L	●	2.480	2.500	2.520	V
V_{FS} TC	Full-Scale Voltage Temperature Coefficient	Using Internal Reference, LTC1450			±0.10		LSB/°C
		Using External Reference, LTC1450/LTC1450L			±0.02		LSB/°C
		Using Internal Reference, LTC1450L			±0.10		LSB/°C
Reference Output (REF OUT)							
	Reference Output Voltage	LTC1450L	●	1.195	1.220	1.245	V
		LTC1450	●	2.008	2.048	2.088	V
	Reference Output Temperature Coefficient				±0.08		LSB/°C
	Reference Line Regulation		●		0.7	±2	LSB/V
	Reference Load Regulation	$0 \leq I_{OUT} \leq 100\mu A$, LTC1450L	●		0.6	±3.0	LSB
		LTC1450	●		0.2	±1.5	LSB
	Short-Circuit Current	REF OUT Shorted to GND	●			80	mA

ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5V to 5.5V (LTC1450), 2.7V to 5.5V (LTC1450L), internal or external reference ($V_{REF\ OUT} \leq V_{CC}/2$), V_{OUT} unloaded, REF OUT = REF HI, REF LO = GND = GAIN 1/GAIN 2, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Input (REF LO = GND)							
	REF HI Input Range	$V_{REF\ HI} \leq V_{CC} - 1.5V$ $V_{REF\ LO} \leq V_{CC} - 1.5V$	● ●			$V_{CC}/2$ $V_{CC}/2$	V V
	REF HI Input Resistance		●	8	18	30	kΩ
	REF HI Input Capacitance				15		pF
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance, LTC1450L LTC1450	● ●	2.7 4.5		5.5 5.5	V V
I_{CC}	Supply Current	$4.5V \leq V_{CC} \leq 5.5V$ (Note 4) LTC1450 $2.7V \leq V_{CC} \leq 5.5V$ (Note 4) LTC1450L	● ●	300 150	400 250	620 500	μA μA
Op Amp DC Performance							
	Short-Circuit Current Low	V_{OUT} Shorted to GND	●			100	mA
	Short-Circuit Current High	V_{OUT} Shorted to V_{CC}	●			120	mA
	Output Impedance to GND	Input Code = 0	●		40	120	Ω
AC Performance							
	Voltage Output Slew Rate	(Note 2)	●	0.5	1.0		V/μs
	Voltage Output Settling Time	(Notes 2, 3) to ±0.5LSB			14		μs
	Digital Feedthrough	$\overline{LDAC}$ = 1			1.5		(nV)(s)
	AC Feedthrough	REF HI = 1kHz, $2V_{P-P}$			–95		dB
SINAD	Signal-to-Noise + Distortion	REF HI = 1kHz, $2V_{P-P}$ (Code: All 1's)			85		dB
Digital I/O							
V_{IH}	Digital Input High Voltage	V_{CC} = 3V, LTC1450L V_{CC} = 5V, LTC1450	● ●	2.2 2.4			V V
V_{IL}	Digital Input Low Voltage	V_{CC} = 3V, LTC1450L V_{CC} = 5V, LTC1450	● ●			0.8 0.8	V V
I_{LEAK}	Digital Input Leakage	V_{CC} = 5V, V_{IN} = GND to V_{CC}	●			±10	μA
C_{IN}	Digital Input Capacitance	Guaranteed by Design. Not Subject to Test	●			10	pF
Switching Characteristics							
t_{CS}	$\overline{CS}$ (MSB or LSB) Pulse Width	V_{CC} = 3V, LTC1450L V_{CC} = 5V, LTC1450	● ●	40 40			ns ns
t_{WR}	$\overline{WR}$ Pulse Width	V_{CC} = 3V, LTC1450L V_{CC} = 5V, LTC1450	● ●	40 40			ns ns
t_{CWS}	$\overline{CS}$ to $\overline{WR}$ Setup	V_{CC} = 3V, LTC1450L V_{CC} = 5V, LTC1450	● ●	0 0			ns ns
t_{CWH}	$\overline{CS}$ to $\overline{WR}$ Hold	V_{CC} = 3V, LTC1450L V_{CC} = 5V, LTC1450	● ●	0 0			ns ns
t_{DWS}	Data Valid to $\overline{WR}$ Setup	V_{CC} = 3V, LTC1450L V_{CC} = 5V, LTC1450	● ●	40 40			ns ns
t_{DWH}	Data Valid to $\overline{WR}$ Hold	V_{CC} = 3V, LTC1450L V_{CC} = 5V, LTC1450	● ●	0 0			ns ns
t_{LDAC}	$\overline{LDAC}$ Pulse Width	V_{CC} = 3V, LTC1450L V_{CC} = 5V, LTC1450	● ●	40 40			ns ns
t_{CLR}	$\overline{CLR}$ Pulse Width	V_{CC} = 3V, LTC1450L V_{CC} = 5V, LTC1450	● ●	40 40			ns ns

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to code 4095 (full-scale).

Note 2: Load is 5kΩ in parallel with 100pF.

Note 3: DAC switched all 1's and the code corresponding to V_{OS} for the part, i.e., LTC1450: code 18.

Note 4: Digital inputs at 0V or V_{CC}.

PIN FUNCTIONS

$\overline{WR}$ (Pin 1): Write Input (Active Low). Used with $\overline{CSMSB}$ and/or $\overline{CSLSB}$ to load data into the input latches.

$\overline{CSLSB}$ (Pin 2): Chip Select Least Significant Byte (Active Low). Used with $\overline{WR}$ to load data into the LSB input latches. Can be connected to $\overline{CSMSB}$ for simultaneous loading of both sets of input latches on a 12-bit bus.

$\overline{CSMSB}$ (Pin 3): Chip Select Most Significant Byte (Active Low). Used with $\overline{WR}$ to load data into the MSB input latches. Can be connected to $\overline{CSLSB}$ for simultaneous loading of both sets of input latches on a 12-bit bus.

D0 to D7 (Pins 4 to 11): Input data for the Least Significant Byte. Loaded into LSB input latch when; $\overline{WR}$ = 0 and $\overline{CSLSB}$ = 0.

D8, D9, D10, D11 (Pins 12, 13, 14, 15): Input data for the Most Significant Byte. Loaded into MSB input latch when; $\overline{WR}$ = 0 and $\overline{CSMSB}$ = 0. Can be connected to D0 to D3 for multiplexed operation on an 8-bit bus.

GND (Pin 16): Ground.

REF LO (Pin 17): Lower input terminal of the DAC's internal resistor string. Typically connected to Analog Ground. An input code of (000_H) will connect the output buffer to this end.

REF HI (Pin 18): Upper input terminal of the DAC's internal resistor string. Typically connected to REF OUT. An input code of (FFF_H) will connect the output buffer to 1LSB from this end.

REF OUT (Pin 19): Reference Output. Output of the internal 2.048V/1.22V reference. Connect to REF HI to drive internal DAC resistor string.

V_{CC} (Pin 20): The positive power supply input. $4.5V \leq V_{CC} \leq 5.5V$ (LTC1450) and $2.7V \leq V_{CC} \leq 5.5V$ (LTC1450L). Requires a bypass capacitor to ground.

V_{OUT} (Pin 21): Voltage Output. Buffered DAC output.

GAIN 1/GAIN 2 (Pin 22): Gain Setting Resistor Pin. Connect to GND for G = 2 or to V_{OUT} for G = 1.

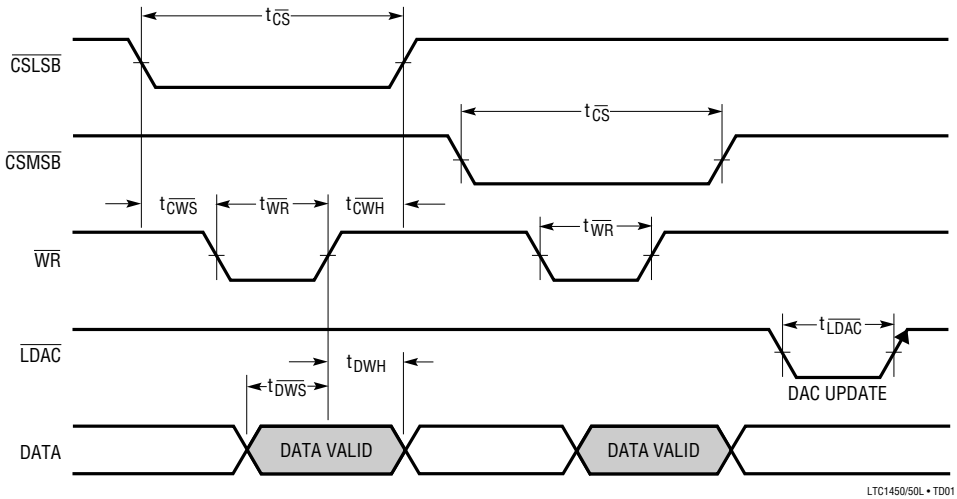
$\overline{CLR}$ (Pin 23): Clear Input (Active Low). A low on this pin resets all internal latches to 0s.

$\overline{LDAC}$ (Pin 24): Load DAC (Active Low). Used to transfer the contents of the input latches to the DAC latches which updates the output voltage.

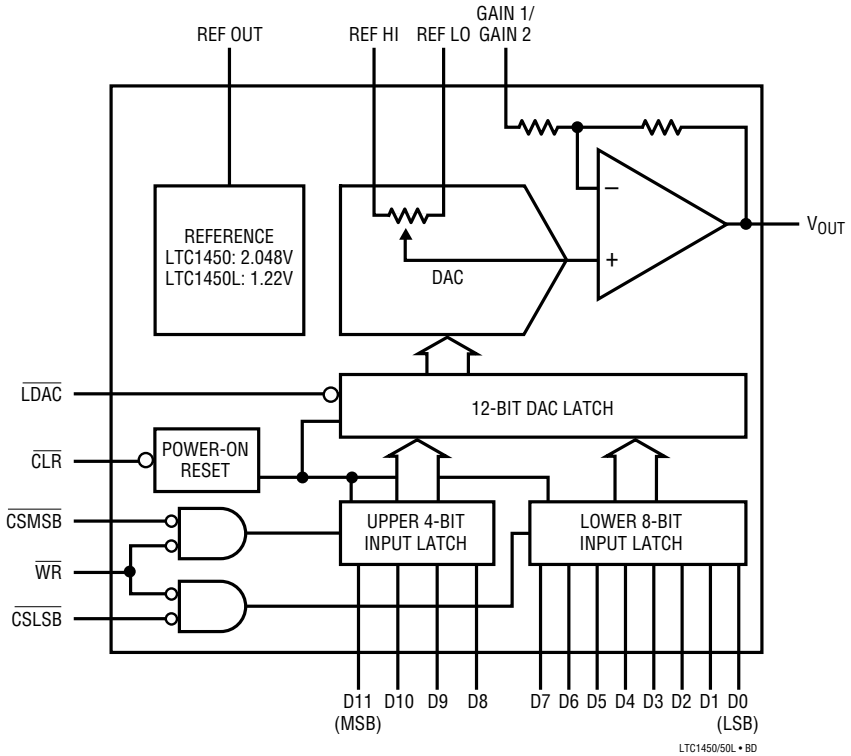
DIGITAL INTERFACE TRUTH TABLE

$\overline{CLR}$	$\overline{CSMSB}$	$\overline{CSLSB}$	$\overline{WR}$	$\overline{LDAC}$	FUNCTION
H	H	L	L	H	Loads the 8LSBs into the input latch
H	H	L	↑	H	Latches the 8LSBs into the input latch
H	H	↑	L	H	Latches the 8LSBs into the input latch
H	L	H	L	H	Loads the 4MSBs into the input latch
H	L	H	↑	H	Latches the 4MSBs into the input latch
H	↑	H	L	H	Latches the 4MSBs into the input latch
H	H	H	H	L	Loads the input latch data into the DAC latch
H	H	H	H	↑	Latches the input latch data into the DAC latch
H	L	L	L	L	Loads input data into DAC latches (latches transparent)
H	L	L	L	↑	Latches input data into DAC latches
L	X	X	X	X	All zeros loaded into input and DAC latches

TIMING DIAGRAM



BLOCK DIAGRAM



DEFINITIONS

Resolution (n): Resolution is defined as the number of digital input bits (n). It defines the number of DAC output states (2^n) that divide the full-scale range. The resolution does not imply linearity.

Full-Scale Voltage (V_{FS}): This is the output of the DAC when all bits are set to 1.

Voltage Offset Error (V_{OS}): The theoretical voltage at the output when the DAC is loaded with all zeros. The output amplifier can have a true negative offset, but because the part is operated from a single supply, the output cannot go below zero. If the offset is negative, the output will remain near 0V resulting in the transfer curve shown in Figure 1.

The offset of the part is measured at the code that corresponds to the maximum offset specification:

$$V_{OS} = V_{OUT} - [(Code)(V_{FS})/(2^n - 1)]$$

Least Significant Bit (LSB): One LSB is the ideal voltage difference between two successive codes.

$$LSB = (V_{FS} - V_{OS})/(2^n - 1) = (V_{FS} - V_{OS})/4095$$

Nominal LSBs:

LTC1450 LSB = 4.095V/4095 = 1mV
LTC1450L LSB = 2.5V/4095 = 0.610mV

Integral Nonlinearity (INL): End-point INL is the maximum deviation from a straight line passing through the end points of the DAC transfer curve. Because the part operates from a single supply and the output cannot go below zero, the linearity is measured between full scale and the code corresponding to the maximum offset specification. The INL error at a given input code is calculated as follows:

$$INL = [V_{OUT} - V_{OS} - (V_{FS} - V_{OS})(code/4095)]/LSB$$

V_{OUT} = The output voltage of the DAC measured at the given input code

Differential Nonlinearity (DNL): DNL is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. The DNL error between any two codes is calculated as follows:

$$DNL = (\Delta V_{OUT} - LSB)/LSB$$

ΔV_{OUT} = The measured voltage difference between two adjacent codes

Digital Feedthrough: The glitch that appears at the analog output caused by AC coupling from the digital inputs when they change state. The area of the glitch is specified in (nV)(s).

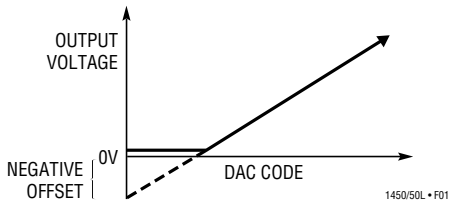


Figure 1. Effect of Negative Offset

OPERATION

Parallel Interface

The data on the input of the DAC is loaded into the DAC's input latches when Chip Select ($\overline{CSLSB}$ and/or $\overline{CSMSB}$) and $\overline{WR}$ are at a logic low. The data that is loaded into the input latches will depend on which of the Chip Selects are at a logic low (see Digital Interface Truth Table). If $\overline{WR}$ and $\overline{CSLSB}$ are both low and $\overline{CSMSB}$ is high, then only data on the 8LSBs (D0 to D7) is loaded into the input latches. Similarly if $\overline{WR}$ and $\overline{CSMSB}$ are both low and $\overline{CSLSB}$ is high then only data on the 4MSBs (D8 to D11) is loaded into the input latches. Data is loaded into both the Least Significant Data Bits (D0 to D7) and the Most Significant Bits (D8 to D11) at the same time if $\overline{WR}$, $\overline{CSLSB}$ and $\overline{CSMSB}$ are low.

The input data is latched into the input latches on the rising edge of either the $\overline{WR}$ or one of the Chip Selects. The $\overline{WR}$ transition high will latch the data in both input latches. A rising edge on $\overline{CSMSB}$ will latch data bits D8 to D11. A rising edge on $\overline{CSLSB}$ will latch data bits D0 to D7.

Once data is loaded into the input latches, it can be loaded into the DAC latch. This will update the analog voltage output of the DAC. The DAC latch is loaded by a logic low on $\overline{LDAC}$. The data that is loaded into the DAC latch will be latched on the rising edge of $\overline{LDAC}$.

When $\overline{WR}$, $\overline{CSLSB}$, $\overline{CSMSB}$ and $\overline{LDAC}$ are all low the latches are transparent and data on pins D0 to D11 loads directly into the DAC latch.

Reference

The LTC1450 includes an internal 2.048V reference, giving the LTC1450 a full-scale range of 4.095V in the gain of 2 configuration. The LTC1450L has an internal 1.22V reference with a full-scale range of 2.5V and a gain of 2.05 in the gain of 2 configuration. The internal reference in the LTC1450 and LTC1450L is not internally connected to the DAC's reference resistor string but is provided on an adjacent pin for flexibility. Because the internal reference is not internally connected to the DAC resistor string, an external reference can be used or the resistor string can be driven with an external source in multiplying configuration. The external reference or source must be capable of driving the 8k minimum DAC ladder resistance.

DAC Ladder Resistor String

The high and low end of the DAC ladder resistor string (REF HI and REF LO respectively) are not connected internally on this part. Typically REF HI will be connected to REF OUT and REF LO will be connected to GND. This will give the LTC1450 a full-scale range of 4.095V. The full-scale range for the LTC1450L will be 2.5V

Either of these pins can be driven up to V_{CC} – 1.5V when using the buffer in the gain of 1 configuration. The resistor string pins can be driven to $V_{CC}/2$ when the buffer is in the gain of 2 configuration (2.05 for the LTC1450L). The resistance between these two pins is typically 18k (8k min).

Voltage Output

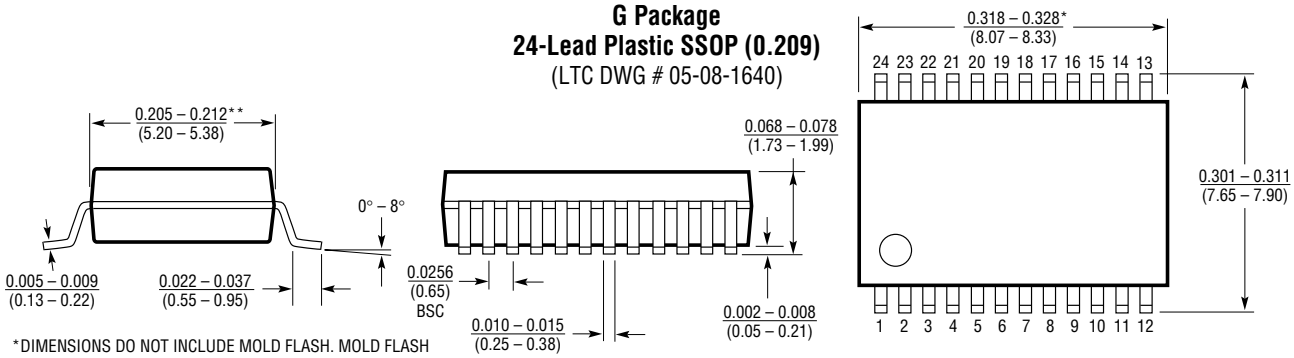
The output buffer for the LTC1450/LTC1450L can be configured for two different gain settings. By tying the GAIN 1/GAIN 2 pin to GND the gain is set to 2 (2.05 for the LTC1450L). By tying the GAIN 1/GAIN 2 pin to V_{OUT} the gain is set to one.

The LTC1450 family's rail-to-rail buffered output can source or sink 5mA over the entire operating temperature range while pulling to within 300mV of the positive supply voltage or GND. The output swings to within a few millivolts of either supply rail when unloaded and has an equivalent output resistance of 40Ω when driving a load to the rails.

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

G Package
24-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)

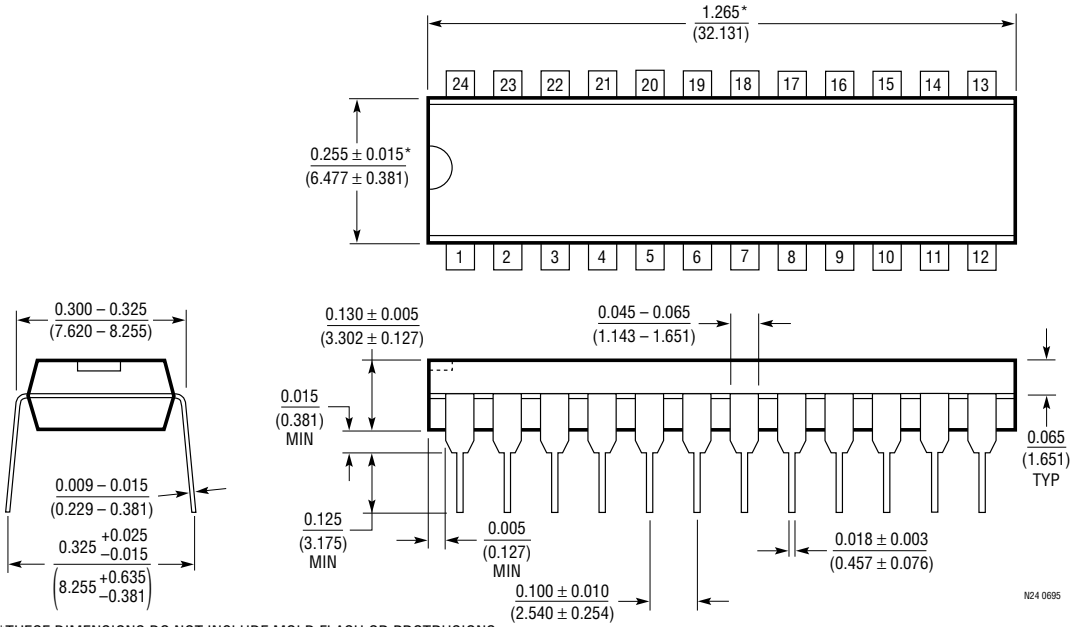


*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

G24 SSOP 0595

N Package
24-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



N24 0695

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1257	Complete Serial I/O V_{OUT} 12-Bit DAC	5V to 15V Single Supply in 8-Pin SO and PDIP
LTC1451/LTC1452/LTC1453	Complete Serial I/O V_{OUT} 12-Bit DACs	3V/5V Single Supply, Rail-to-Rail in 8-Pin SO and PDIP
LTC7541A	Parallel I/O Multiplying 12-Bit DAC	12-Bit Wide Input
LTC7543/LTC8143	Serial Multiplying 12-Bit DACs	Daisy-Chainable, Flexible Analog and Digital Interface
LTC8043	Serial Multiplying 12-Bit DAC	8-Pin SO and PDIP

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