

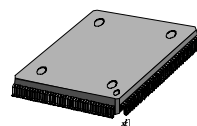
## KS7301B

## DIGITAL CAMERA PROCESSOR

### GENERAL DESCRIPTION

KS7301B is a CMOS IC designed for Digital Camcorder System. This Processor is Compatible for NTSC/PAL & Hi-band/Normal Camcorder System.

160-QFP-2424



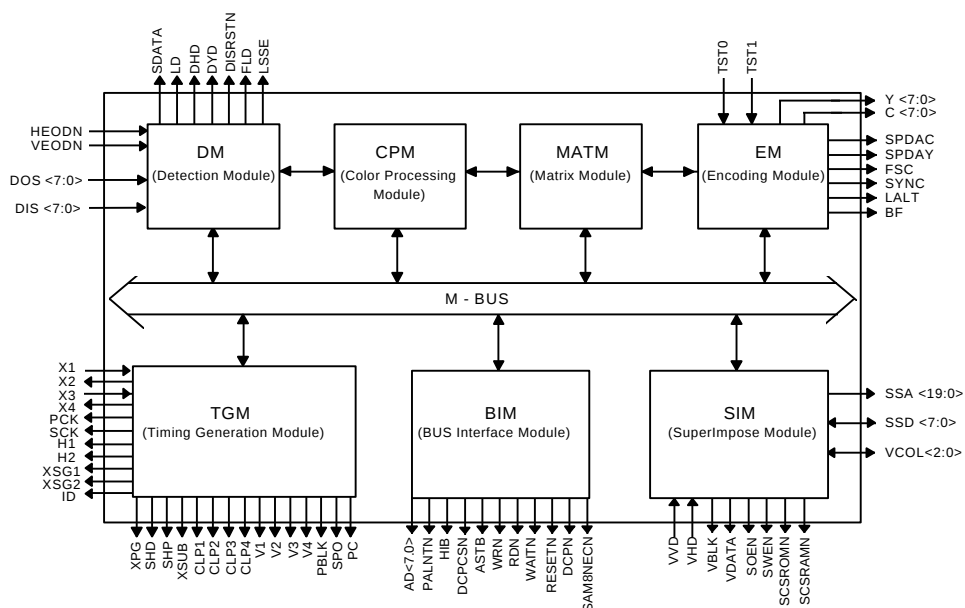
### FEATURES

- Luminance & Chroma Signal Procession
- Built in Timing Generator
- Built in Sync. Generator
- Built in Memory for Detection Part (16bit\* 64 word\*2 page)
- Built in 1H delay line (1H \*2, 8 bit \*910)
- Built in Encoder for PAL/NTSC
- Built in DIS Interface Block
- Built in Super Impose function
- Built in Title Mix Block
- Compatible with NORMAL/Hi - Band System
- Built in Micro controller Interface Block

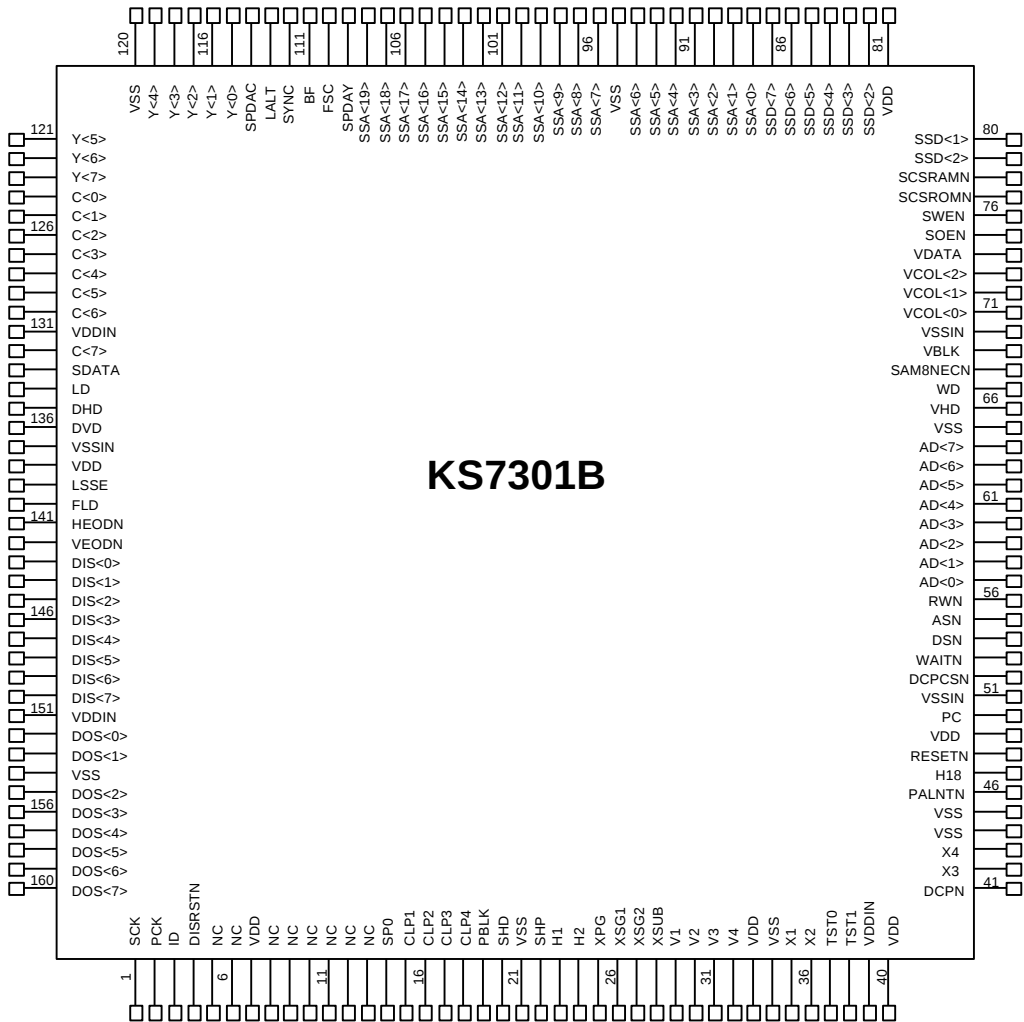
### ORDERING INFORMATION

| Device  | Package      | Operating Temperature |
|---------|--------------|-----------------------|
| KS7301B | 160-QFP-2424 | -20°C ~ +75°C         |

### BLOCK DIAGRAM



PIN CONFIGURATION



## PIN DESCRIPTIONS

| No. | Symbol  | I/O | Description                            | Remark |
|-----|---------|-----|----------------------------------------|--------|
| 1   | SCK     | O   | Secondary Pipe Line clock ( PCK/2 )    |        |
| 2   | PCK     | O   | Main Pipe Line Clock                   | *1     |
| 3   | ID      | O   | CCD Line ID Signal                     |        |
| 4   | DISRSTN | O   | DZE Reset Signal ( Active Low )        |        |
| 5   | NC      | -   | No connection                          |        |
| 6   | NC      | -   | No connection                          |        |
| 7   | VDD     | -   | I/O Power supply                       |        |
| 8   | NC      | -   | No connection                          |        |
| 9   | NC      | -   | No connection                          |        |
| 10  | NC      | -   | No connection                          |        |
| 11  | NC      | -   | No connection                          |        |
| 12  | NC      | -   | No connection                          |        |
| 13  | NC      | -   | No connection                          |        |
| 14  | SP0     | O   | A/D Converter Sampling Clock           |        |
| 15  | CLP1    | O   | Clamp Pulse 1                          |        |
| 16  | CLP2    | O   | Clamp Pulse 2                          |        |
| 17  | CLP3    | O   | Clamp Pulse 3                          |        |
| 18  | CLP4    | O   | Clamp Pulse 4                          |        |
| 19  | PBLK    | O   | Video Pre - Blanking Pulse             |        |
| 20  | SHD     | O   | Data Sampe & Hold Pulse For CDS        |        |
| 21  | VSS     | -   | Ground                                 |        |
| 22  | SHP     | O   | Pre-Charge Sample & Hold Pulse For CDS |        |
| 23  | H1      | O   | Horizontal Driving Pulse 1 For CCD     |        |
| 24  | H2      | O   | Horizontal Driving Pulse 2 For CCD     |        |
| 25  | XPG     | O   | Pre-Charge Gate Pulse For CCD          |        |
| 26  | XSG1    | O   | Read Out Pulse 1 For CCD               |        |
| 27  | XSG2    | O   | Read Out Pulse 2 For CCD               |        |
| 28  | XSUB    | O   | Discharge Pulse For CCD                |        |
| 29  | V1      | O   | Vertical Driving Pulse 1 For CCD       |        |
| 30  | V2      | O   | Vertical Driving Pulse 2 For CCD       |        |
| 31  | V3      | O   | Vertical Driving Pulse 3 For CCD       |        |
| 32  | V4      | -   | Vertical Driving Pulse 4 For CCD       |        |
| 33  | VDD     | -   | I/O Power Supply                       |        |
| 34  | VSS     | I   | Ground                                 |        |
| 35  | X1      | O   | Main X-tal Input                       | *2     |
| 36  | X2      | I   | Main X-tal Output                      |        |
| 37  | TST0    | I   | IC Test pin                            | *3     |
| 38  | TST1    | -   | IC Test Output                         | *3     |
| 39  | VDDIN   | -   | Power Supply (INTERNAL)                |        |
| 40  | VDD     | I   | Power Supply For X - tal               |        |

## PIN DESCRIPTIONS (Continued)

| No. | Symbol          | I/O | Description                                          | Remark |
|-----|-----------------|-----|------------------------------------------------------|--------|
| 41  | DCPN            | I   | IC Test Pin                                          | *3     |
| 42  | X3              | I   | 4Fsc X - tal Input For PAL (17.73447MHz)             |        |
| 43  | X4              | O   | 4Fsc X - tal Output For PAL                          |        |
| 44  | V <sub>SS</sub> | -   | Ground X - tal                                       |        |
| 45  | V <sub>SS</sub> | -   | Ground                                               |        |
| 46  | PALNTN          | I   | PAL/NTSC Mode Select ion Pin                         |        |
| 47  | HI8             | I   | 760H/510H CCD Mode Selection Pin                     |        |
| 48  | RESETN          | I   | IC Reset Input                                       |        |
| 49  | V <sub>DD</sub> | -   | I/O Power Supply                                     |        |
| 50  | PC              | O   | Phase Comparator Output Of PAL PLL                   | *4     |
| 51  | VSSIN           | -   | Ground (INTRENAL)                                    |        |
| 52  | DCPCSN          | I   | DCP Chip Select Pin (Low Active)                     |        |
| 53  | WAITN           | O   | Wait For Micom Interface (Low Active)                |        |
| 54  | DSN(RDN)        | I   |                                                      | *5     |
| 55  | ASN(AS)         | I   |                                                      | *6     |
| 56  | RWN             | I   |                                                      | *7     |
| 57  | AD<0>           | I/O | Micro controller Address / Data Bus I / O            |        |
| 58  | AD<1>           | I/O |                                                      |        |
| 59  | AD<2>           | I/O |                                                      |        |
| 60  | AD<3>           | I/O |                                                      |        |
| 61  | AD<4>           | I/O |                                                      |        |
| 62  | AD<5>           | I/O |                                                      |        |
| 63  | AD<6>           | I/O |                                                      |        |
| 64  | AD<7>           | I/O |                                                      |        |
| 65  | VSS             | -   | Ground                                               |        |
| 66  | VHD             | I   | VCR Part HD Pulse (VCR PB Mode Title Mix)            |        |
| 67  | VVD             | I   | VCR Part VD Pulse (VCR PB Mode Title Mix)            |        |
| 68  | SAM8NECH        | I   | Microcontroller Type Select Pin (SAM8:High, NEC:Low) |        |
| 69  | VBLK            | O   | Title Blank Signal For VCR PB Mode Title Mix         |        |
| 70  | VSSIN           | -   | Ground (INTERNAL)                                    |        |
| 71  | VCOL<0>         | O   | Title Color Signal For VCR PB Mode Title Mix         |        |
| 72  | VCOL<1>         | O   |                                                      |        |
| 73  | VCOL<2>         | O   |                                                      |        |
| 74  | VDATA           | O   | Title Data Enable Signal For VCR PB Mode Title Mix   |        |
| 75  | SOEN            | O   | ROM Enable For Superimpose ( Low Active )            |        |
| 76  | SWEN            | O   | RAM Enable For Superimpose ( Low Active )            |        |
| 77  | SCSROMN         | O   | ROM Chip Select For Superimpose ( Low Active )       |        |
| 78  | SCSRAMN         | O   | RAM Chip Select For Superimpose ( Low Active )       |        |
| 79  | SSD<0>          | I/O | Memory Interface Data I/O For Superimpose            |        |
| 80  | SSD<1>          | I/O |                                                      |        |

## PIN DESCRIPTIONS (Continued)

| No. | Symbol  | I/O | Description                                           | Remark |
|-----|---------|-----|-------------------------------------------------------|--------|
| 81  | VDD     | -   | Power supply For I/O                                  |        |
| 82  | SSD<2>  | I/O | Memory Interface Data I/O For Superimpose             |        |
| 83  | SSD<3>  | I/O |                                                       |        |
| 84  | SSD<4>  | I/O |                                                       |        |
| 85  | SSD<5>  | I/O |                                                       |        |
| 86  | SSD<6>  | I/O |                                                       |        |
| 87  | SSD<7>  | I/O |                                                       |        |
| 88  | SSA<0>  | O   | Memory Interface Address Output For Superimpose       |        |
| 89  | SSA<1>  | O   |                                                       |        |
| 90  | SSA<2>  | O   |                                                       |        |
| 91  | SSA<3>  | O   |                                                       |        |
| 92  | SSA<4>  | O   |                                                       |        |
| 93  | SSA<5>  | O   |                                                       |        |
| 94  | SSA<6>  | O   |                                                       |        |
| 95  | VSS     | -   | Ground                                                |        |
| 96  | SSA<7>  | O   | Memory Interface Address Output For Superimpose       |        |
| 97  | SSA<8>  | O   |                                                       |        |
| 98  | SSA<9>  | O   |                                                       |        |
| 99  | SSA<10> | O   |                                                       |        |
| 100 | SSA<11> | O   |                                                       |        |
| 101 | SSA<12> | O   | Memory Interface Address Output For Superimpose       |        |
| 102 | SSA<13> | O   |                                                       |        |
| 103 | SSA<14> | O   |                                                       |        |
| 104 | SSA<15> | O   |                                                       |        |
| 105 | SSA<16> | O   |                                                       |        |
| 106 | SSA<17> | O   |                                                       |        |
| 107 | SSA<18> | O   |                                                       |        |
| 108 | SSA<19> | O   |                                                       |        |
| 109 | SPDAY   | O   | D/A Converter Sampling Clock For Y Signal (PCK)       |        |
| 110 | FSC     | O   | Chroma Subcarrier (NTSC : 3.7595MHz, PAL : 4.4336MHz) |        |
| 111 | BF      | O   | Burst Flag Pulse                                      |        |
| 112 | SYNC    | O   | Video Composite SYNC signal                           |        |
| 113 | LALT    | O   | Line Alternate Pulse For PAL                          |        |
| 114 | SPDAC   | O   | D/A Converter Sampling Clock for C Signal (4Fsc)      |        |
| 115 | Y<0>    | O   | Y Video Signal Output                                 |        |
| 116 | Y<1>    | O   |                                                       |        |
| 117 | Y<2>    | O   |                                                       |        |
| 118 | Y<3>    | O   |                                                       |        |
| 119 | Y<4>    | O   |                                                       |        |
| 120 | VSS     | -   | Ground                                                |        |

## PIN DESCRIPTIONS (Continued)

| No. | Symbol | I/O | Description                                     | Remark |
|-----|--------|-----|-------------------------------------------------|--------|
| 121 | Y<5>   | O   | Y Video Signal Output                           |        |
| 122 | Y<6>   | O   |                                                 |        |
| 123 | Y<7>   | O   |                                                 |        |
| 124 | C<0>   | O   | C Video Signal Output                           |        |
| 125 | C<1>   | O   |                                                 |        |
| 126 | C<2>   | O   |                                                 |        |
| 127 | C<3>   | O   |                                                 |        |
| 128 | C<4>   | O   |                                                 |        |
| 129 | C<5>   | O   |                                                 |        |
| 130 | C<6>   | O   |                                                 |        |
| 131 | VDDIN  | -   | Power supply (INTERNAL)                         |        |
| 132 | C<7>   | O   | C Video Signal Output                           |        |
| 133 | SDATA  | O   | DZE Interface Serial Data                       |        |
| 134 | LD     | O   | DZE Interface Load Signal                       |        |
| 135 | DHD    | O   | HD signal for DIS                               |        |
| 136 | DVD    | O   | VD signal for DIS                               |        |
| 137 | VSSIN  | -   | Ground (INTERNAL)                               |        |
| 138 | VDD    | -   | Power supply For I/O                            |        |
| 139 | LSSE   | O   | Low Shutter Speed Enable                        |        |
| 140 | FLD    | O   | Video Field Signal                              |        |
| 141 | HEODN  | I   | Chroma S1, S2 Pixel Control (Default : High)    |        |
| 142 | VEODN  | I   | Chroma 2R-G, G-2B Line Control (Default : High) |        |
| 143 | DIS<0> | I/O | CCD Video Input Signal                          |        |
| 144 | DIS<1> | I/O |                                                 |        |
| 145 | DIS<2> | I/O |                                                 |        |
| 146 | DIS<3> | I/O |                                                 |        |
| 147 | DIS<4> | I/O |                                                 |        |
| 148 | DIS<5> | I/O |                                                 |        |
| 149 | DIS<6> | I/O |                                                 |        |
| 150 | DIS<7> | I/O |                                                 |        |
| 151 | VDDIN  | -   | Power supply (INTERNAL)                         |        |
| 152 | DOS<0> | I   | DZE Video Input Signal                          |        |
| 153 | DOS<1> | I   |                                                 |        |
| 154 | VSS    | -   | Ground                                          |        |
| 155 | DOS<2> | I   | DZE Video Input Signal                          |        |
| 156 | DOS<3> | I   |                                                 |        |
| 157 | DOS<4> | I   |                                                 |        |
| 158 | DOS<5> | I   |                                                 |        |
| 159 | DOS<6> | I   |                                                 |        |
| 160 | DOS<7> | I   |                                                 |        |

**< REMARK >****\*1. Main Pipe Line Clock**

510H: NTSC 1820/3fh, PAL 18 6/3fh  
760H: NTSC 910fh, PAL 908fh

**\*2. Main X-tal Input**

NTSC:28.63636MHz, PAL:28,375Mhz

**\*3. IC Test Pin**

( TST1, TST0, DCPN)  
( 0,0,0 ) : TEST ( CPM )  
( 0,0,1 ) : TEST ( MATM )  
( 0,1,0 ) : TEST ( TGM )  
( 0,1,1 ) : TEST ( SIM )  
( 1,0,0 ) : TEST ( DC LOW )  
( 1,0,1 ) : TEST ( DC HIGH )  
( 1,1,0 ) : NORMAL  
( 1,1,1 ) : RESERVED

**\*4. Phase Comparator Output Of PAL PLL**

Include Charge Pump Part

**\*5. SAM 8 Mode : Data Strobe Signal Input ( Low Active )**

NEC Mode : Read Enable ( Low Active )

**\*6. Address Strobe For Micom Interface**

SAM 8 : Low Active, NEC : High Active

**\*7. SAM 8 Mode : Read / Write Enable Read : High, Write : Low )**

NEC Mode : Write Enable ( Low Active )

**ABSOLUTE MAXIMUM RATINGS** (Ta=25°C)

| Characteristics       | Symbol           | Value                     | Unit |
|-----------------------|------------------|---------------------------|------|
| Supply Voltage        | V <sub>DD</sub>  | -0.5~6.5                  | V    |
| Input Voltage         | V <sub>IN</sub>  | -0.5~V <sub>DD</sub> +0.5 | V    |
| Output Voltage        | V <sub>OUT</sub> | -0.5~V <sub>DD</sub> +0.5 | V    |
| Power Dissipation     | P <sub>D</sub>   | 1                         | W    |
| Operating Temperature | T <sub>OPR</sub> | -20~+75                   | °C   |
| Storage Temperature   | T <sub>STG</sub> | -65~+150                  | °C   |

**ELECTRICAL CHARACTERISTICS**(V<sub>CC</sub>=5V, Ta = 25°C, unless otherwise specified )

| Characteristics          | Symbol           | Test Condition        | Min                  | Typ | Max                | Unit | Remark |
|--------------------------|------------------|-----------------------|----------------------|-----|--------------------|------|--------|
| Supply Voltage           | V <sub>DD</sub>  | -                     | 4.5                  | 5.0 | 5.5                | V    |        |
| Input Leakage Current    | I <sub>I</sub>   | -                     | -                    | -   | 1                  | μA   |        |
| Output Leakage Current   | I <sub>LO</sub>  | -                     | -                    | -   | 1                  | μA   |        |
| Operating Current        | I <sub>CC</sub>  | V <sub>DD</sub> =5V   | -                    | 140 | 180                | mA   |        |
| High-Level Input Voltage | V <sub>IH</sub>  | -                     | 0.8V <sub>DD</sub>   | -   | V <sub>DD</sub>    | V    |        |
| Low-Level Input Voltage  | V <sub>IL</sub>  | -                     | 0                    | -   | 0.2V <sub>DD</sub> | V    |        |
| Output High Voltage 1    | V <sub>OH1</sub> | I <sub>OH</sub> =-2mA | V <sub>DD</sub> -0.5 | -   | -                  | V    | *1     |
| Output Low Voltage 1     | V <sub>OL1</sub> | I <sub>OL</sub> =4mA  | -                    | -   | 0.45               | V    | *1     |
| *Output High Voltage 2   | V <sub>OH2</sub> | I <sub>OH</sub> =-4mA | V <sub>DD</sub> -0.5 | -   | -                  | V    | *2     |
| *Output Low Voltage 2    | V <sub>OL2</sub> | I <sub>OL</sub> =8mA  | -                    | -   | 0.45               | V    | *2     |
| **Output High Voltage 3  | V <sub>OH3</sub> | I <sub>OH</sub> =-8mA | V <sub>DD</sub> -0.5 | -   | -                  | V    | *3     |
| **Output Low Voltage 3   | V <sub>OL3</sub> | I <sub>OL</sub> =8mA  | -                    | -   | 0.45               | V    | *3     |

\*: XPG, SHP, SHD Pulse

\*\*: H1, H2 Pulse

\*1 : IO=2mA

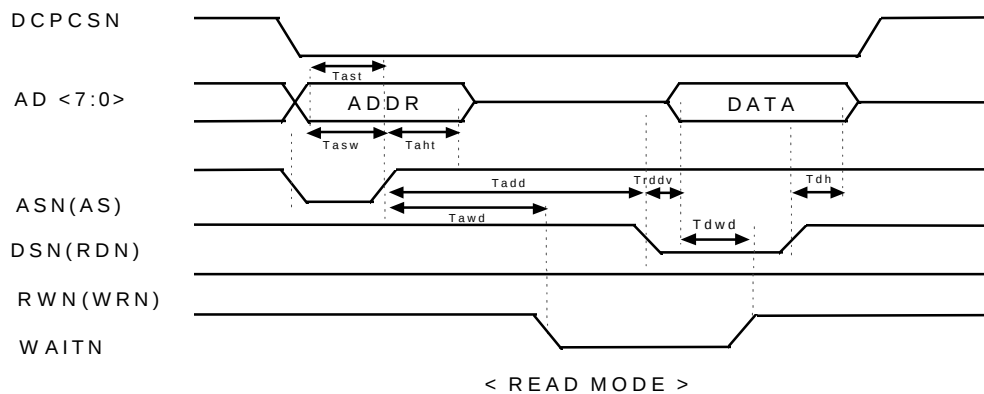
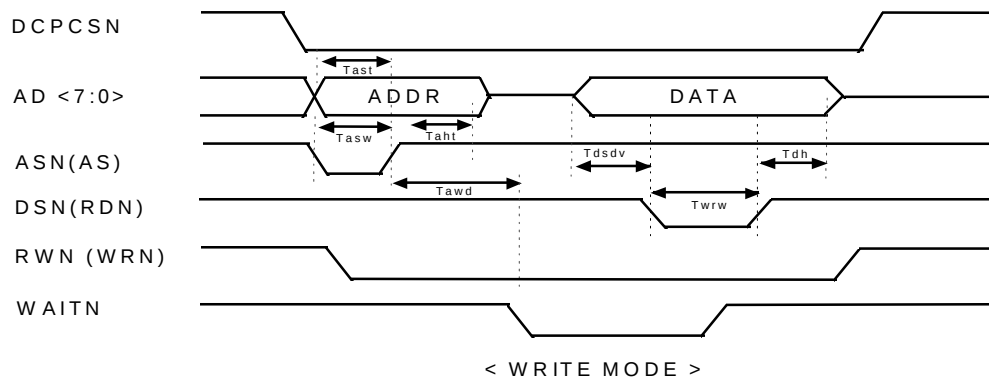
\*2 : IO=4mA

\*3 : IO=8mA

## Micro controller Interface I : for SAVB ( PIN68A → HIGH )

| Characteristics      | Symbol | Min | Typ | Max | Unit | Remark |
|----------------------|--------|-----|-----|-----|------|--------|
| Address setup time   | Tast   | 15  | -   | -   | nsec | -      |
| Address hold time    | Taht   | 35  | -   | -   | nsec | -      |
| ASTB pulse width     | Tasw   | 35  | -   | -   | nsec | -      |
| ASTB, WAITN distance | Tawd   | -   | -   | 35  | nsec | -      |
| DSN delay from Data  | Tdsdy  | 35  | -   | -   | nsec | Write  |
| WRN width            | Twrw   | 400 | -   | -   | nsec | -      |
| Data hold time       | Tdh    | 0   | -   | -   | nsec | -      |
| Data delay from DSN  | Trdrv  | -   | -   | 270 | nsec | Read   |
| Data, WAITN distance | Tdwd   | 35  | -   | -   | nsec | -      |
| ASN, DSN distance    | Tadd   | -   | -   | 140 | nsec | Read   |

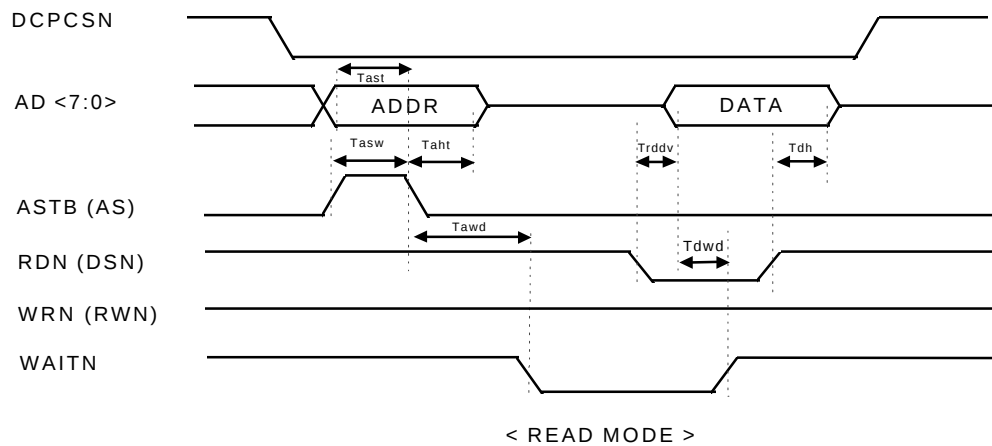
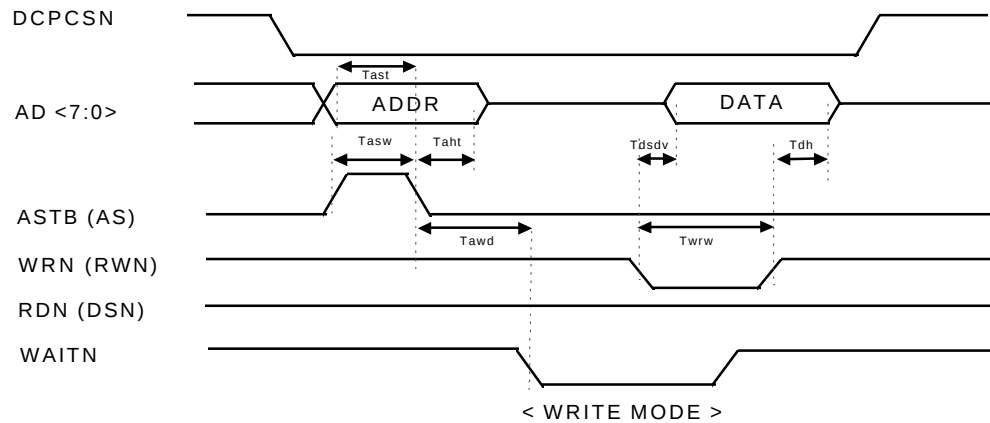
## Micro controller Interface I : for SAM8 ( PIN68 → HIGH )



## Micro controller Interface II: for SAVB (PIN68 → LOW)

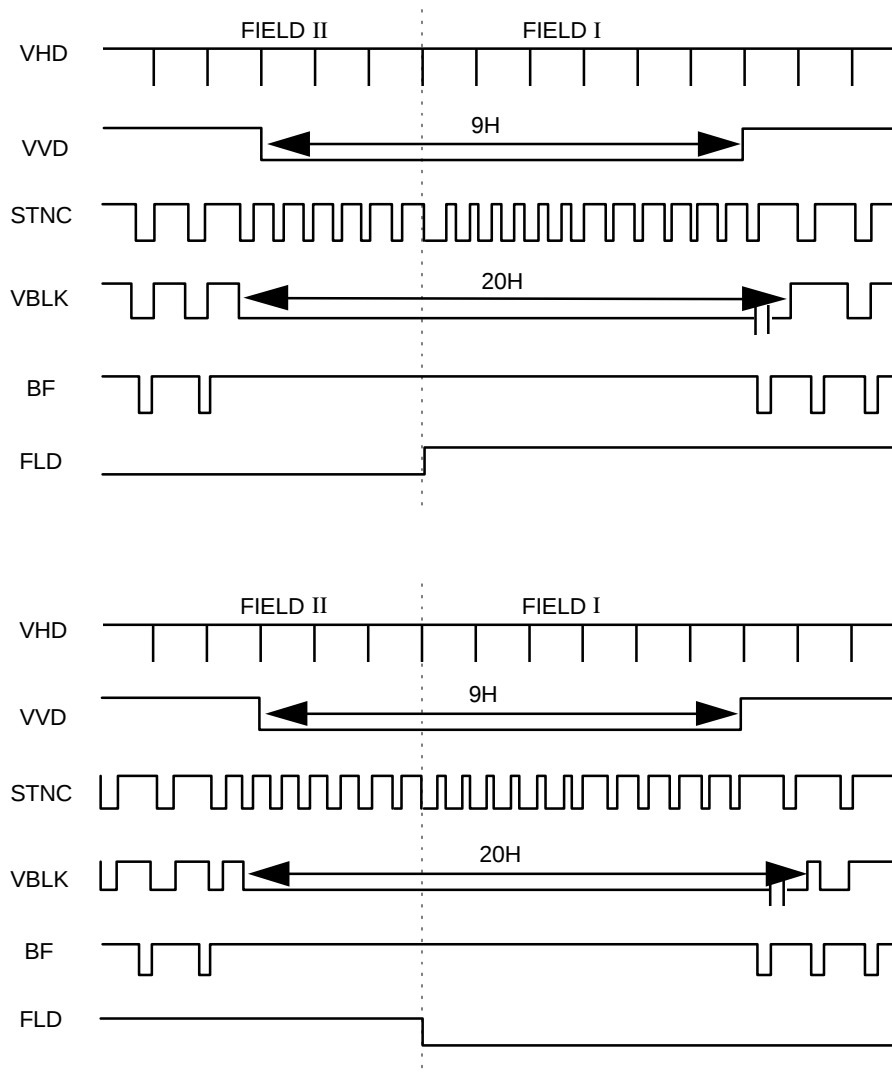
| Characteristics      | Symbol | Min | Typ | Max | Unit | Remark |
|----------------------|--------|-----|-----|-----|------|--------|
| Address setup time   | Tast   | 15  | -   | -   | nsec | -      |
| Address hold time    | Taht   | 35  | -   | -   | nsec | -      |
| ASTB pulse width     | Tasw   | 35  | -   | -   | nsec | -      |
| ASTB, WAITN distance | Tawd   | -   | -   | 35  | nsec | -      |
| Data delay from DSN  | Tdsdy  | 35  | -   | 100 | nsec | Write  |
| WRN width            | Twrw   | 400 | -   | -   | nsec | -      |
| Data hold time       | Tdh    | 0   | -   | -   | nsec | -      |
| Data delay from RDN  | Trdrv  | -   | -   | 270 | nsec | Read   |
| Data, WAITN distance | Tdwd   | 35  | -   | -   | nsec | -      |
| ASN, DSN distance    | Tadd   | -   | -   | 140 | nsec | Read   |

## Micro controller Interface II : for NEC (PIN68 → LOW)

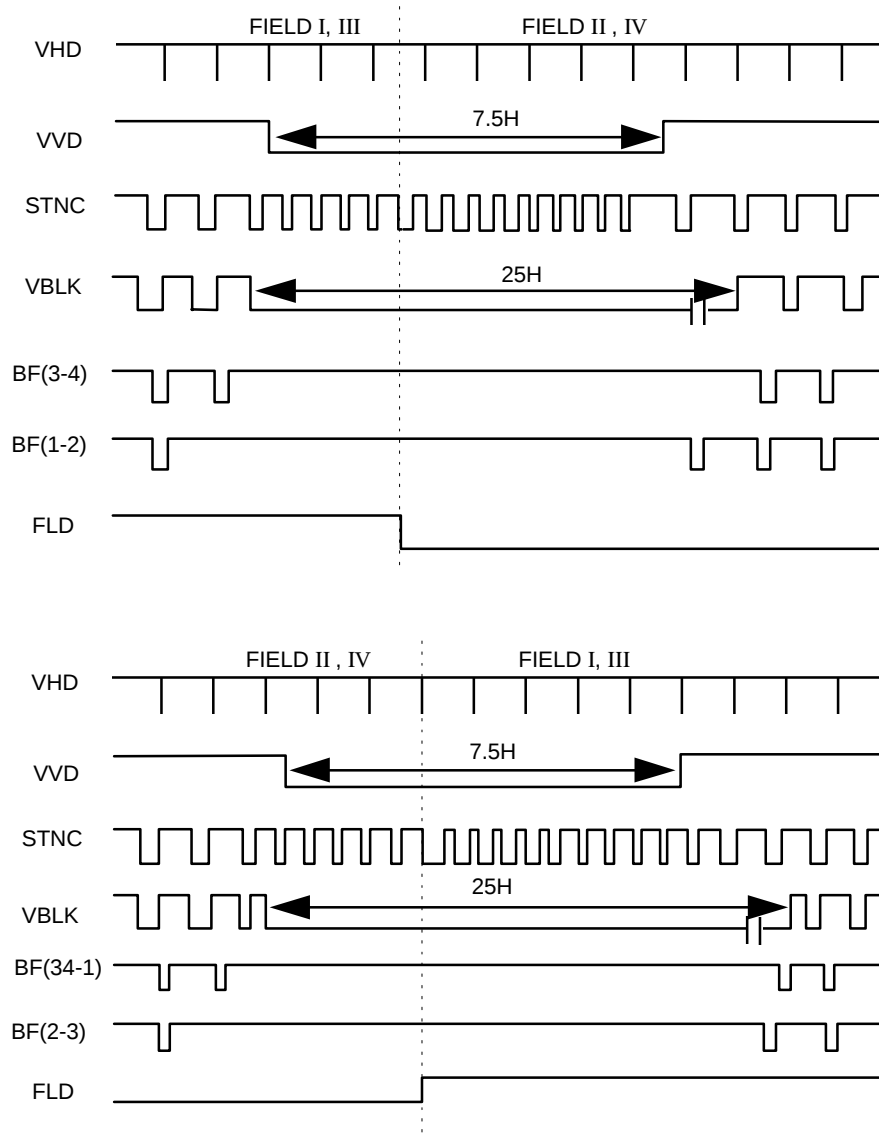


## Vertical Timing for SYNC signal

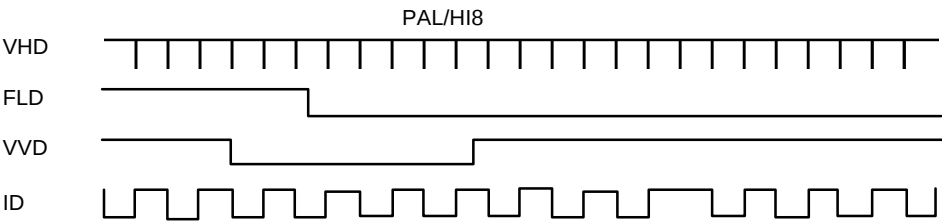
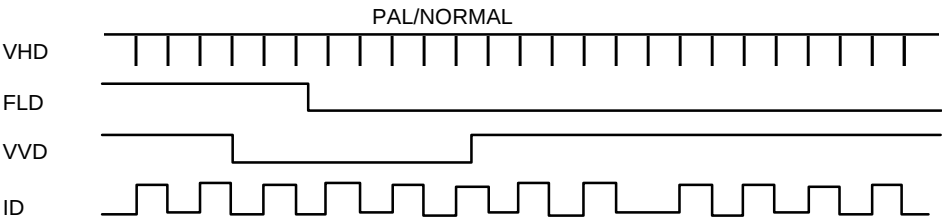
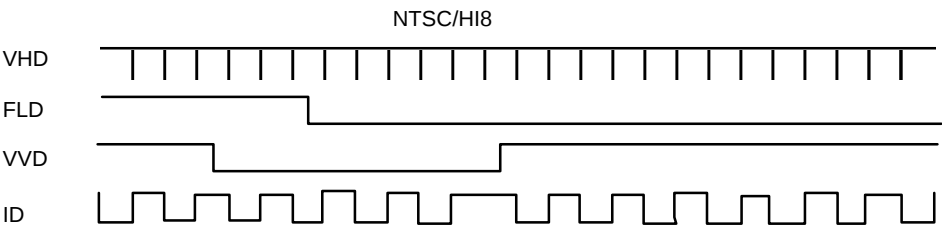
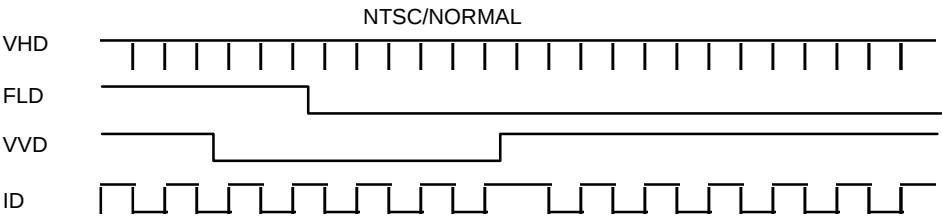
(1) NTSC



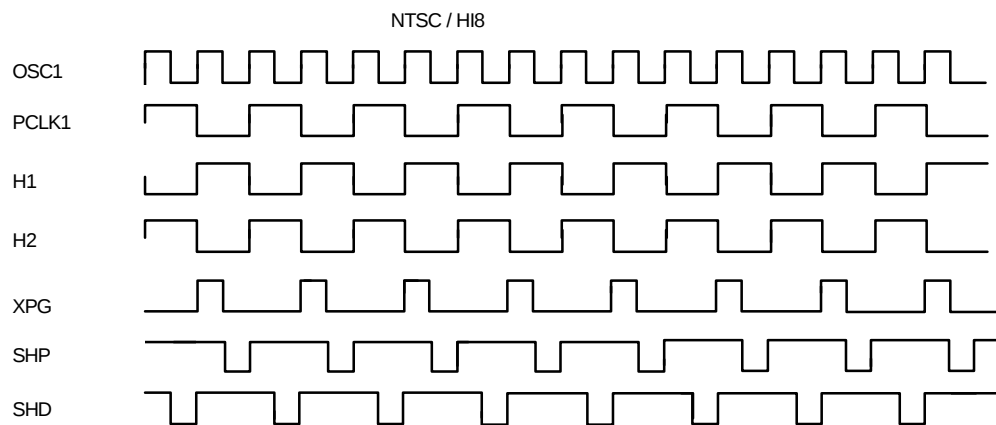
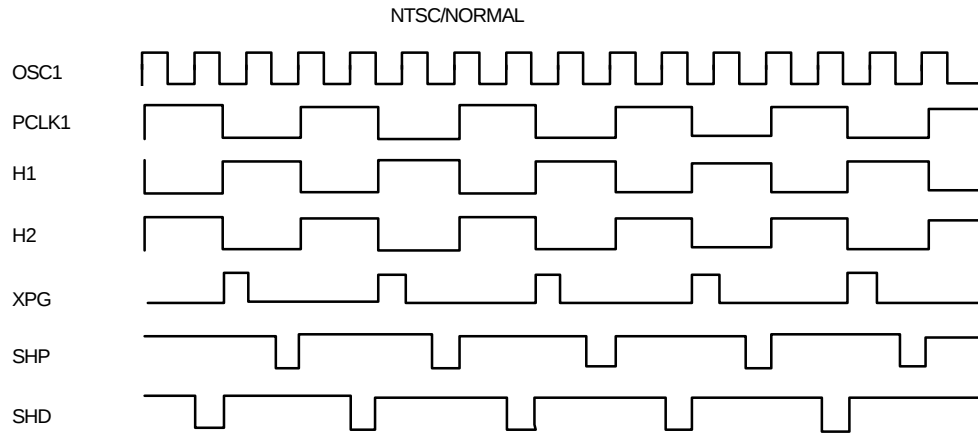
(2) PAL



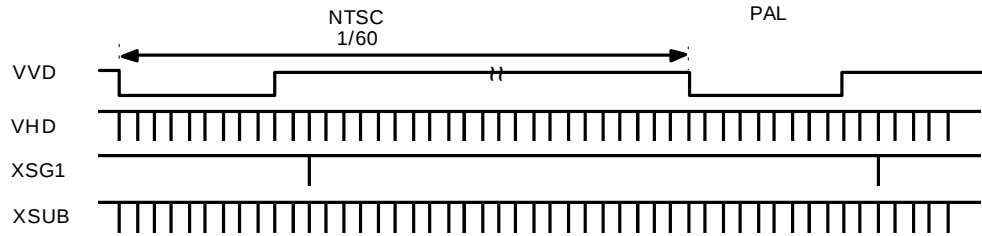
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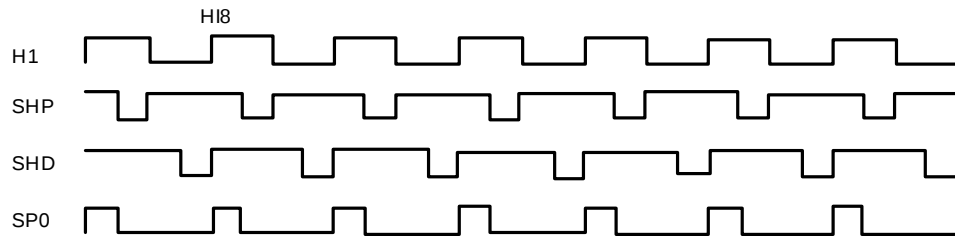
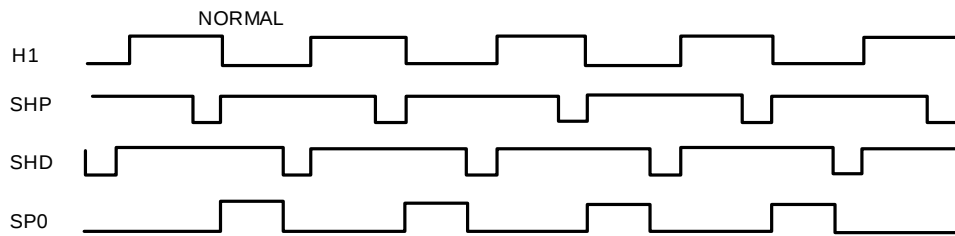
SHP, SHD, H1, H2



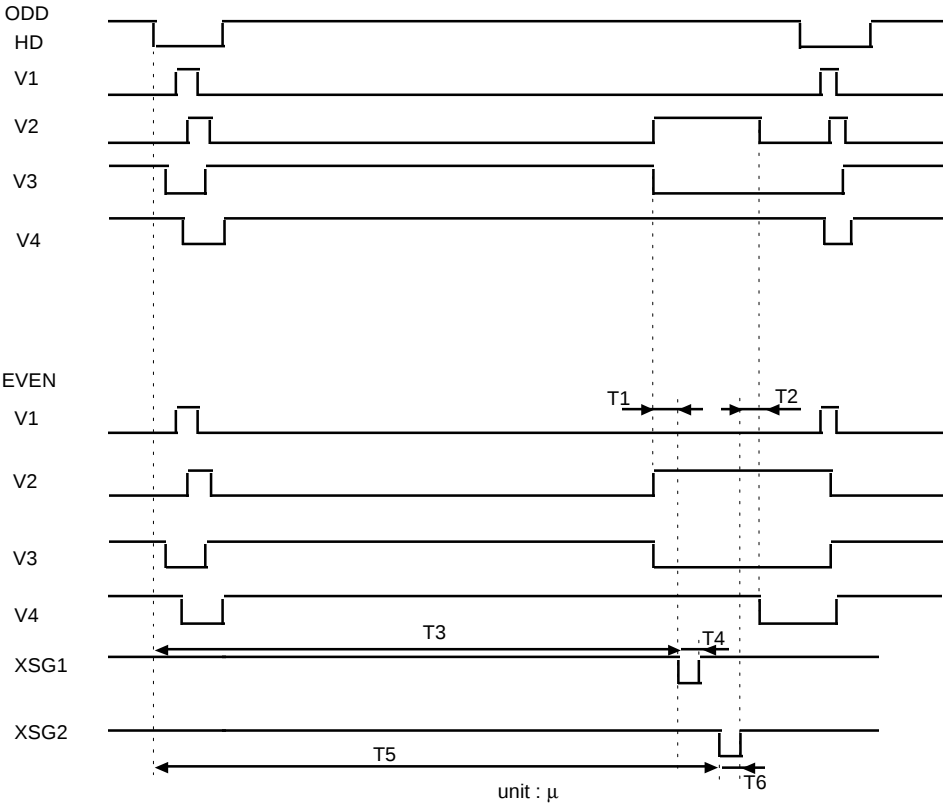
XSUB (1 / 10000 sec Low Shutter Speed Mode )



SPO

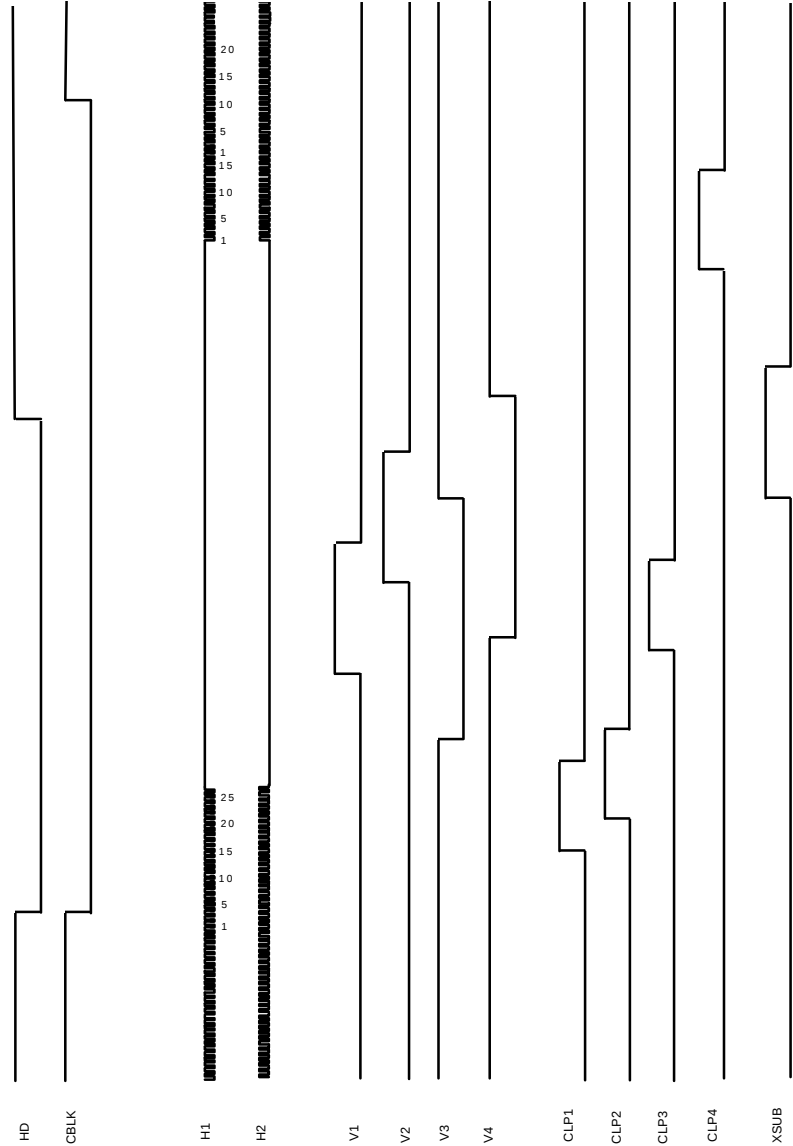


Horizontal Timing of V1 - V4, XSG1,XSG2

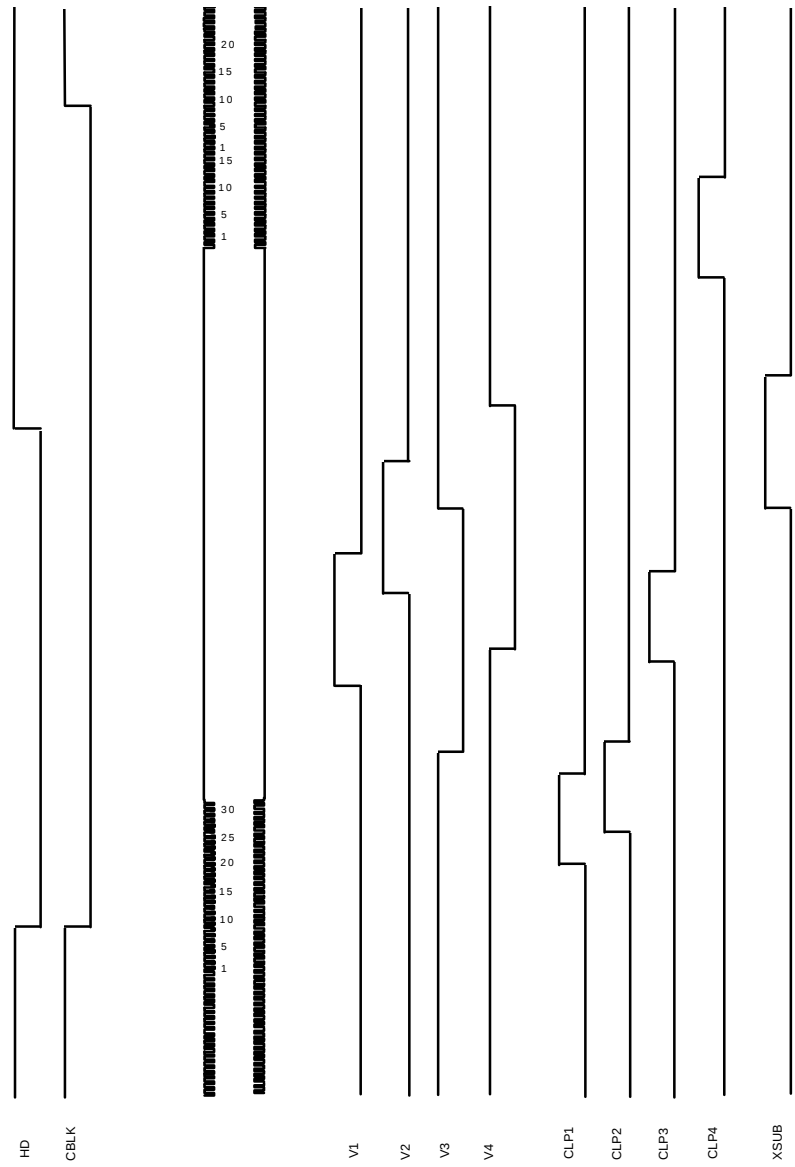


|    | Normal | HI18 |
|----|--------|------|
| T1 | 1.1    | 1.6  |
| T2 | 2      | 2.5  |
| T3 | 39.5   | 42.2 |
| T4 | 2.5    | 2.5  |
| T5 | 43.5   | 47.2 |
| T6 | 2.5    | 2.5  |

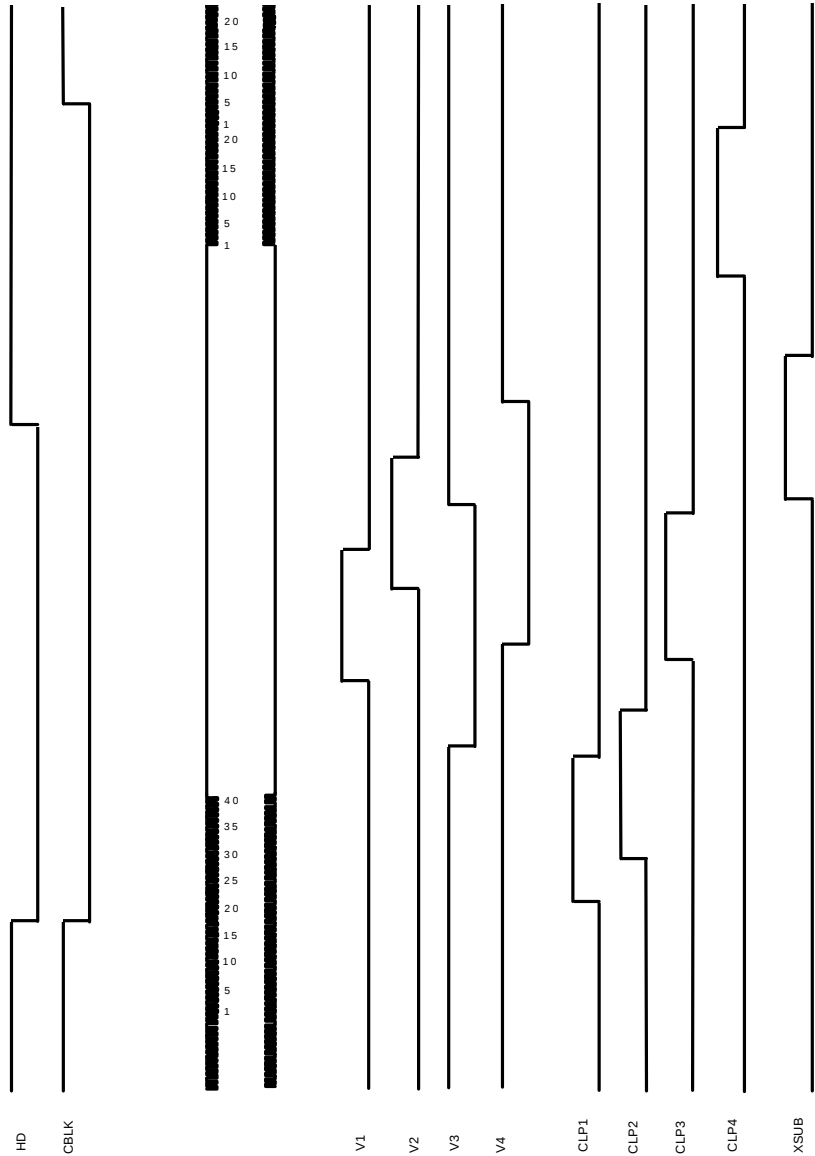
Horizontal Timing For CCD(NTSC/NORMAL)



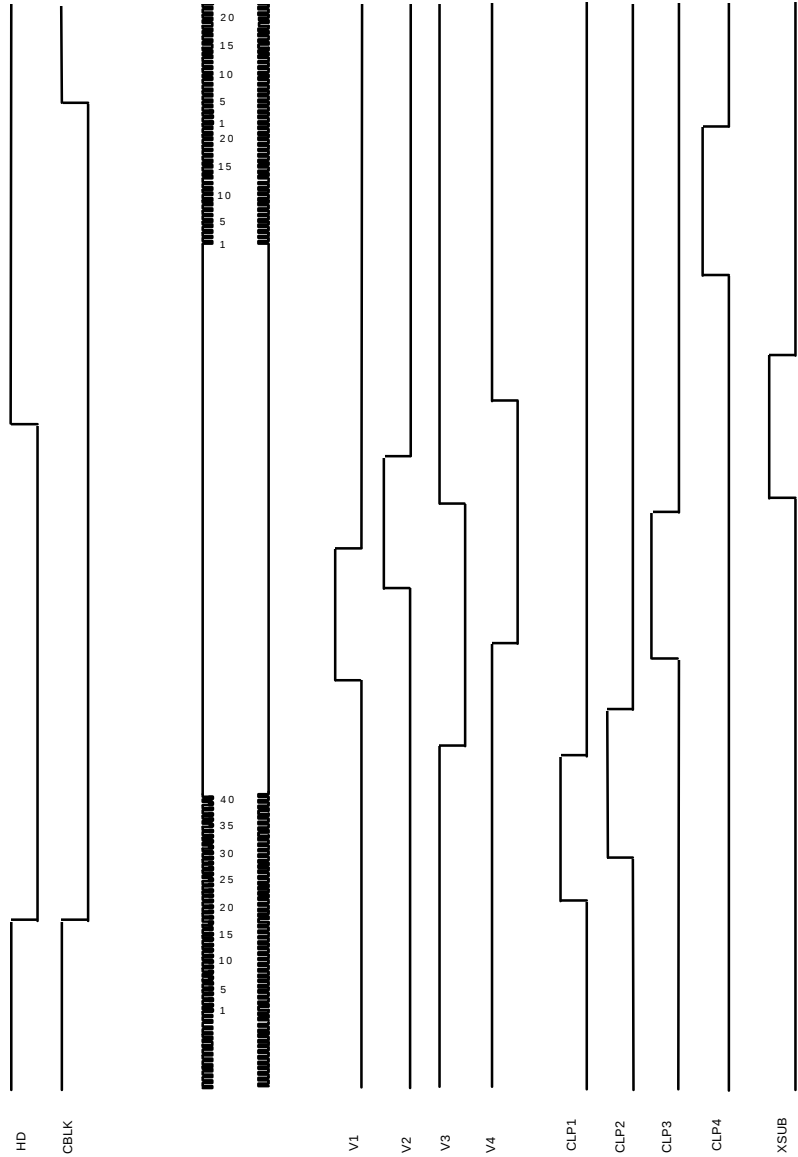
Horizontal Timing For CCD(PAL/NORMAL)



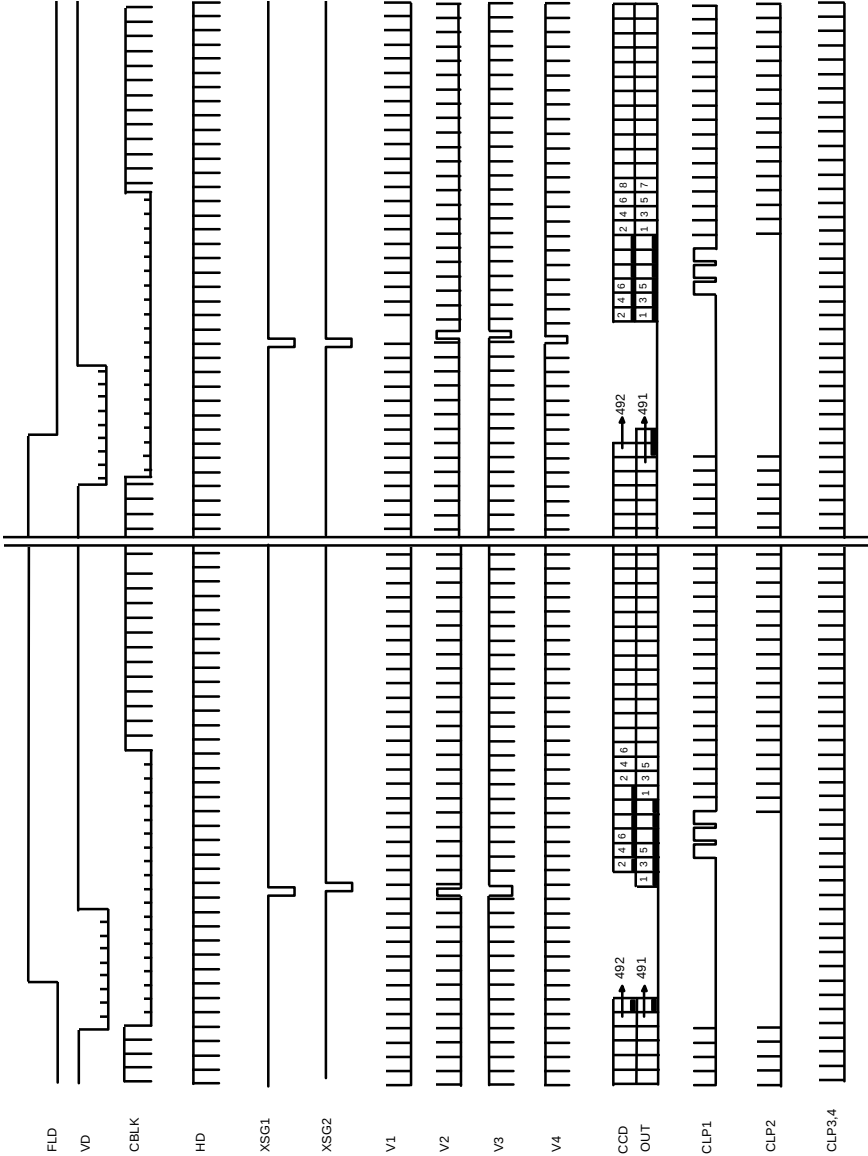
Horizontal Timing For CCD(NTSC/H18)



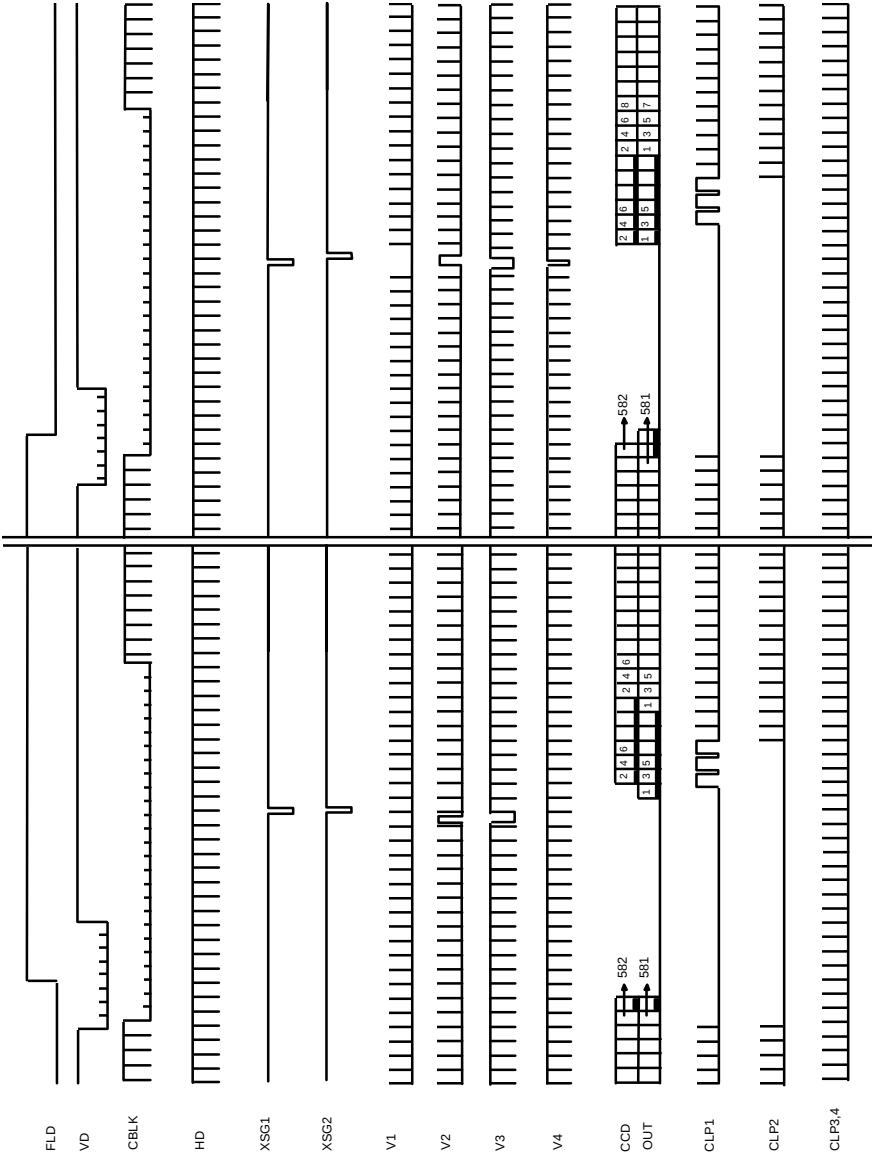
Horizontal Timing For CCD(PAL/Hi8)



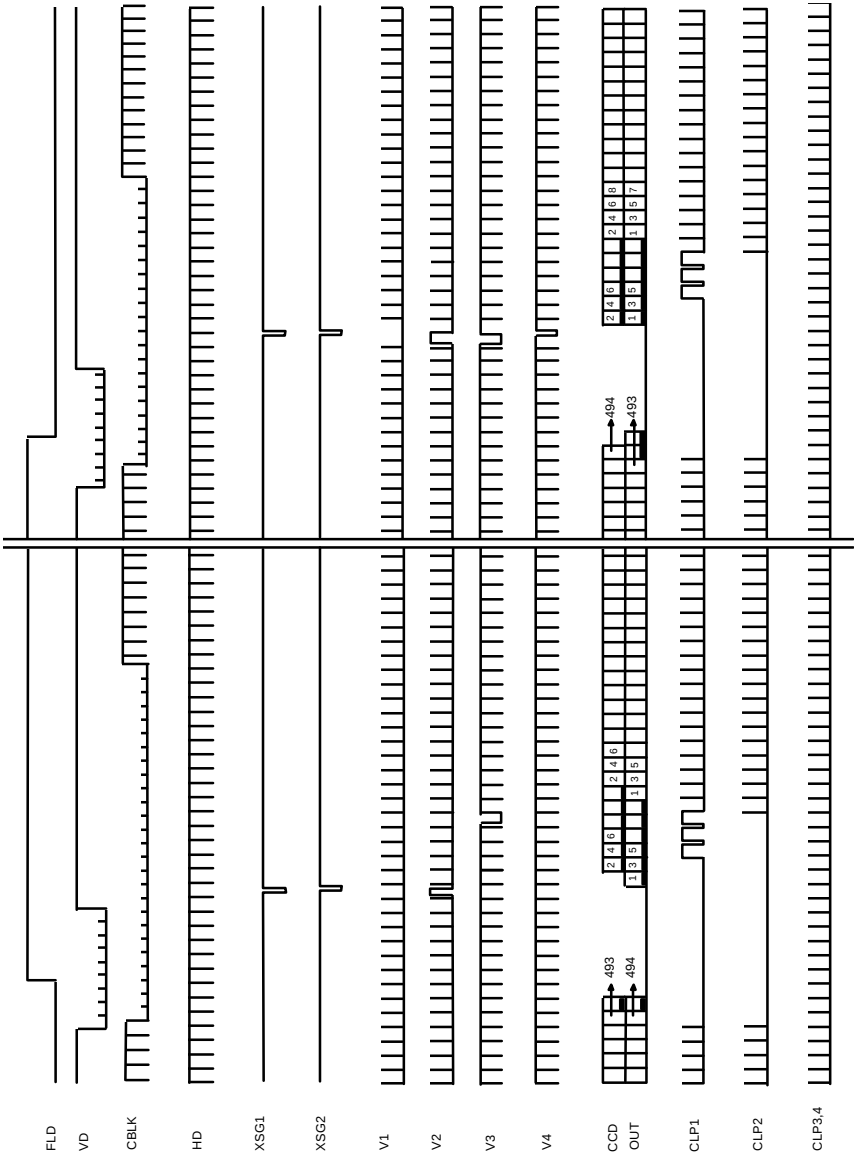
Vertical Timing For CCD(NTSC/NORMAL)



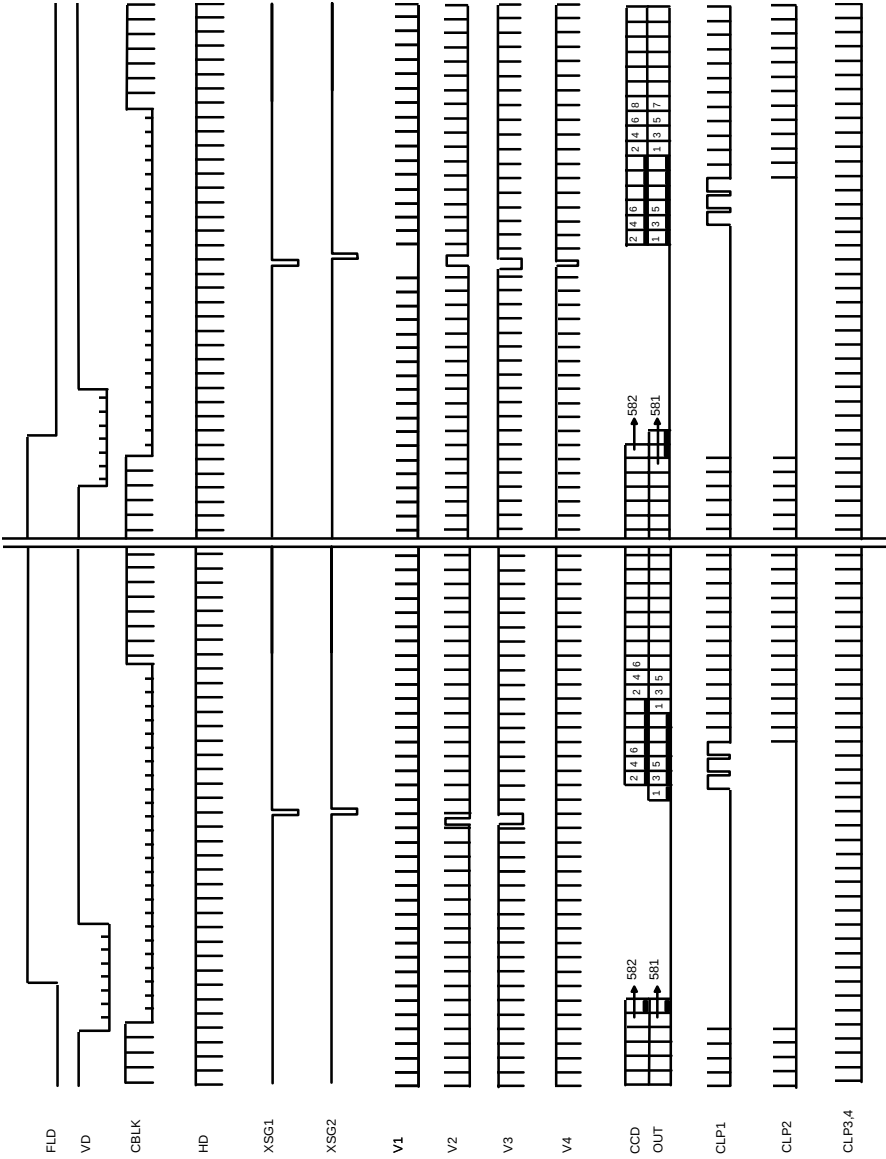
Vertical Timing For CCD(PAL/NORMAL)



Vertical Timing For CCD(NTSC/H18)



Vertical Timing For CCD(PAL/Hi8)



## REGISTER MAPPING

| REGISTER NAME | ADDRESS NO.(HEX) | BITS | MODE | DESCRIPTION                                                                                                                                                                                                                                                                                                                                   |        |       |      |      |      |    |     |    |
|---------------|------------------|------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-------|------|------|------|----|-----|----|
| BST           | 00               | 3    | R    | <div>DCP Status Register</div> <div><table><tr><td>7~3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>----</td><td>PN</td><td>Hi8</td><td>SB</td></tr></table><div><div>High : Superimpose Busy<br/>Low : Superimpose Standby</div><div>High : Hi8 Mode<br/>Low : Normal Mode</div><div>High : PAL Mode<br/>Low : NTSC Mode</div></div></div> | 7~3    | 2     | 1    | 0    | ---- | PN | Hi8 | SB |
| 7~3           | 2                | 1    | 0    |                                                                                                                                                                                                                                                                                                                                               |        |       |      |      |      |    |     |    |
| ----          | PN               | Hi8  | SB   |                                                                                                                                                                                                                                                                                                                                               |        |       |      |      |      |    |     |    |
| DADR          | 20               | 6    | W    | <div>Detection RAM Address Pointing Register</div> <div>Just with assignment Start point, increasing the 64 step Address automatically.<br/>To read the first small picture, set the Address value to 00(HEX)<br/>(LSB 6 bit using)</div>                                                                                                     |        |       |      |      |      |    |     |    |
| DMDL          | 21               | 8    | R/W  | <div>Detection Data Register</div> <div><table><tr><td>15 ~ 8</td><td>7 ~ 0</td></tr><tr><td>DMDH</td><td>DMDL</td></tr></table></div>                                                                                                                                                                                                        | 15 ~ 8 | 7 ~ 0 | DMDH | DMDL |      |    |     |    |
| 15 ~ 8        | 7 ~ 0            |      |      |                                                                                                                                                                                                                                                                                                                                               |        |       |      |      |      |    |     |    |
| DMDH          | DMDL             |      |      |                                                                                                                                                                                                                                                                                                                                               |        |       |      |      |      |    |     |    |
| DMDH          | 22               | 8    | R/W  | Read cycle achieve which of DMDH → DMDL Register in AE/AF/AWB detection Data                                                                                                                                                                                                                                                                  |        |       |      |      |      |    |     |    |
| DCMD          | 23               | 8    | W    | Command Register                                                                                                                                                                                                                                                                                                                              |        |       |      |      |      |    |     |    |

|     |     |     |     |    |     |     |     |
|-----|-----|-----|-----|----|-----|-----|-----|
| 7   | 6   | 5   | 4   | 3  | 2   | 1   | 0   |
| FS1 | FS2 | R/B | R/W | PG | ADC | DIS | PHC |

High : AF Peak-hold Data Detection  
Low : AF Integration Data Detection

High : DIS On  
Low : DIS Off

High : Odd Clock Delay  
Low : Even Clock Delay

High : Page 1 Micom Read  
Low : Page 0 Micom Read

High : Detection RAM Read  
Low : Detection RAM Write

High : AWB R-Y Data Detection  
Low : AWB B-Y Data Detection

High : AE Mode  
Low : AF2 Mode

High : AWB Mode  
Low : AF1 Mode

| REGISTER NAME | ADDRESS NO.(HEX) | BITS                 | MODE | DESCRIPTION                                                                                                                                                                                                                                                                                                                         |   |     |     |   |      |                      |
|---------------|------------------|----------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|-----|-----|---|------|----------------------|
| DDIS          | 27               | 8                    | WR   | DZE Mode Control Register                                                                                                                                                                                                                                                                                                           |   |     |     |   |      |                      |
| COV1          | 40               | 8                    | WR   | Knee Delta Coeff. Register ( Default : Hex 00 )<br>Range : 0 ~ 255( FF )                                                                                                                                                                                                                                                            |   |     |     |   |      |                      |
| COV2          | 41               | 8                    | WR   | Knee Coeff. Register ( Half value of Knee Point )<br>Range : 0 ~ 255( FF )                                                                                                                                                                                                                                                          |   |     |     |   |      |                      |
| CAG           | 42               | 8                    | WR   | Aperture Gain Register<br>Range : 0 ~ 255( FF )                                                                                                                                                                                                                                                                                     |   |     |     |   |      |                      |
| CC0A          | 43               | 8                    | WR   | Color Coeff.1 Register ( Default : 0.12 )<br>Range : 0 ~ 6dB( FF )                                                                                                                                                                                                                                                                  |   |     |     |   |      |                      |
| CC0B          | 44               | 8                    | WR   | Color Coeff.2 Register ( Default : 0.2 )<br>Range : 0 ~ 6dB( FF )                                                                                                                                                                                                                                                                   |   |     |     |   |      |                      |
| CAKP          | 45               | 8                    | WR   | Knee Point Value<br>Range : 0 ~ 255( FF )                                                                                                                                                                                                                                                                                           |   |     |     |   |      |                      |
| CNSL          | 46               | 8                    | WR   | Aperture Noise Slice Level<br>Range : 0 ~ 255( FF )                                                                                                                                                                                                                                                                                 |   |     |     |   |      |                      |
| CAPS          | 47               | 7                    | WR   | <div>Bdge Chroma Suppress</div> <div><table><tr><td>7</td><td>6-5</td><td>4-0</td></tr><tr><td>-</td><td>Gain</td><td>Suppress Limit Level</td></tr></table><div><div></div><div>00: X1<br/>01: X 1/2<br/>10: X 1/4<br/>11: X 2</div></div><div>Deciding the amount of Max, Suppress by fixing the suppress Limit Level</div></div> | 7 | 6-5 | 4-0 | - | Gain | Suppress Limit Level |
| 7             | 6-5              | 4-0                  |      |                                                                                                                                                                                                                                                                                                                                     |   |     |     |   |      |                      |
| -             | Gain             | Suppress Limit Level |      |                                                                                                                                                                                                                                                                                                                                     |   |     |     |   |      |                      |
| CRC0          | 48               | 8                    | WR   | Cr(=2R-G) Gain<br>Range : 0 ~ 6 dB ( FF )                                                                                                                                                                                                                                                                                           |   |     |     |   |      |                      |
| CBC0          | 49               | 8                    | WR   | Cb(=G-2B) Gain<br>Range : 0 ~ 6 dB ( FF )                                                                                                                                                                                                                                                                                           |   |     |     |   |      |                      |
| CGC0          | 4A               | 8                    | WR   | YL Gain<br>Range : 0 ~ 6 dB ( FF )                                                                                                                                                                                                                                                                                                  |   |     |     |   |      |                      |
| CUTH          | 4B               | 5                    | WR   | Superimpose RAM Mode Input Data High Threshold<br>Range : 0 ~ 32 ( 1F )                                                                                                                                                                                                                                                             |   |     |     |   |      |                      |
| CLTH;         | 4C               | 5                    | WR   | Superimpose RAM Mode Input Data Low Threshold<br>Range : 0 ~ 32 ( 1F )                                                                                                                                                                                                                                                              |   |     |     |   |      |                      |

| REGISTER NAME | ADDRESS NO.(HEX) | BITS | MODE | DESCRIPTION                                                                                                                                                                    |
|---------------|------------------|------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MRPW          | 60               | 8    | WR   | Red Pre-white Balance Coeff.<br>Range : 0 ~ 18dB ( FF ) 0dB : HEX 20                                                                                                           |
| MGPW          | 61               | 8    | WR   | Green Pre-white Balance Coeff.<br>Range : 0 ~ 18dB ( FF ) 0dB : HEX 20                                                                                                         |
| MBPW          | 62               | 8    | WR   | Blue Pre-white Balance Coeff.<br>Range : 0 ~ 18dB ( FF ) 0dB : HEX 20                                                                                                          |
| MRWB          | 63               | 8    | WR   | Red White Balance Coeff.<br>Range : 0 ~ 18dB ( FF ) 0dB : HEX 20                                                                                                               |
| MBWB          | 64               | 8    | WR   | Blue White Balance Coeff.<br>Range : 0 ~ 18dB ( FF ) 0dB : HEX 20                                                                                                              |
| MDSCR         | 65               | 8    | WR   | RGB Black Balance Coeff. (2°C Data)<br>Range : -127(HEX 81) ~ +127 (HEX 7F )                                                                                                   |
| MDSCR         | 66               | 8    | WR   |                                                                                                                                                                                |
| MDSCR         | 67               | 8    | WR   |                                                                                                                                                                                |
| MRHC          | 68               | 8    | WR   | R-Y Hue Control Value (MRHC*[B-Y])<br>Range : -(B-Y) ~ +(B-Y)<br>MSB 7 : Sign bit<br>LSB 0 ~ 6 : Absolute Value                                                                |
| MBHC          | 69               | 8    | WR   | B-Y Hue Control Value (MBHC*[R-Y])<br>Range : -(R-Y) ~ +(R-Y)<br>MSB 7 : Sign bit<br>LSB 0 ~ 6 : Absolute Value                                                                |
| MRYG          | 6A               | 8    | WR   | R-Y Gain<br>Range : 0~18dB (FF) 0dB : HEX 20                                                                                                                                   |
| MBYG          | 6B               | 8    | WR   | B-Y Gain<br>Range : 0 ~ 18dB (FF) 0dB : HEX 20                                                                                                                                 |
| MA1C          | 6C               | 8    | WR   | Color difference signal Matrix Coeff<br>Range : 0 ~ 1 dB ( FF )<br>Recommand Value: MA1C : 0.7 (HEX B3)<br>MB1C : 0.3 (HEX 4d)<br>MA2C : 0.11 (HEX 1C)<br>MB2C : 0.89 (HEX E4) |
| MB1C          | 6D               | 8    | WR   |                                                                                                                                                                                |
| MA2C          | 6E               | 8    | WR   |                                                                                                                                                                                |
| MB2C          | 6F               | 8    | WR   |                                                                                                                                                                                |

| REGISTER NAME | ADDRESS NO.(HEX) | BITS | MODE | DESCRIPTION                                                                                                                     |
|---------------|------------------|------|------|---------------------------------------------------------------------------------------------------------------------------------|
| EHSBY         | A0               | 8    | WR   | B-Y axis direction Burst Level (2'C Data)<br>Range : -128(HEX 80) ~ + 127 (HEX 7F)<br>MSB 7 : Sign bit<br>LSB 6 ~ 0 : 2'C Value |
| EHSRY         | A1               | 8    | WR   | R-Y axis direction Burst Level (2'C Data)<br>Range : -128(HEX 80) ~ + 127 (HEX 7F)<br>MSB 7 : Sign bit<br>LSB 6 ~ 0 : 2'C Value |
| ECFAD         | A2               | 8    | WR   | Chroma Fade Control Value<br>Range : 0 ~ 6dB ( FF ) 0dB : HEX 80                                                                |
| EWCLP         | A3               | 8    | WR   | White Clip Level<br>Range : 0 ~ 255                                                                                             |
| EYFAD         | A4               | 8    | WR   | Luminance Fade Control Value<br>Range : 0 ~ 18dB ( FF ) 0dB : HEX 80                                                            |
| ESET          | A5               | 8    | WR   | Set-up Level<br>Range : 0 ~ 255 ( FF )                                                                                          |
| EBLK          | A6               | 8    | WR   | Blanking Level<br>Range : 0 ~ 255 ( FF )                                                                                        |
| ECMD1         | A7               | 8    | W    | Command Register                                                                                                                |

|    |     |     |     |     |     |    |    |
|----|-----|-----|-----|-----|-----|----|----|
| 7  | 6   | 5   | 4   | 3   | 2   | 1  | 0  |
| EN | DVR | DAC | DAY | AR1 | AR0 | PS | NP |

1 : Negative Effect  
0 : Normal Operation

1 : Output Pin Disable  
0 : Normal Operation

00 : Normal Operation  
01 : step16 Art Freeze  
10 : step 8 Art Freeze  
11 : step 4 Art Freeze

1 : Y D/A Clock Inverting  
0 : Normal Operation

1 : Digital VCR Interface Mode  
0 : Normal Operation

1 : Digital VCR Interface Mode  
0 : Normal Operation

1 : Y/C Output Enable  
0 : Y/C Output Disable

|       |    |   |   |              |
|-------|----|---|---|--------------|
| ECMD2 | A8 | 5 | W | Delay Adjust |
|-------|----|---|---|--------------|

|       |                                         |                                    |
|-------|-----------------------------------------|------------------------------------|
| 7~5   | 4, 3                                    | 2~0                                |
| - - - | Title Y/C delay daj.<br>Range : 0~3 PCK | Y/C delay adj.<br>Range : 0~3 PCLK |

| REGISTER NAME | ADDRESS NO.(HEX) | BITS | MODE | DESCRIPTION           |
|---------------|------------------|------|------|-----------------------|
| TCMD1         | 10               | 7    | W    | Shutter Speed Control |

|   |     |     |     |     |     |     |     |
|---|-----|-----|-----|-----|-----|-----|-----|
| 7 | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| - | TSE | SS1 | SS0 | HS3 | HS2 | HS1 | HS0 |

0000 : 1/60 sec (PAL 1/50 sec)  
0001 : 1/85 sec  
0010 : 1/125 sec  
0011 : 1/185 sec  
0100 : 1/250 sec  
0101 : 1/375 sec  
0110 : 1/500 sec  
0111 : 1/750 sec  
1000 : 1/1000 sec  
1001 : 1/1500 sec  
1010 : 1/2000 sec  
1111 : 1/2500 sec  
1100 : 1/4000 sec  
1101 : 1/6000 sec  
1110 : 1/10000 sec  
1111 : Flicker Mode

00 : 1/30 sec  
01 : 1/15 sec  
10 : 1/8 sec  
11 : 1/4 sec

0 : Normal  
1 : Low Shutter Speed enable

| REGISTER NAME | ADDRESS NO.(HEX) | BITS | MODE | DESCRIPTION         |
|---------------|------------------|------|------|---------------------|
| ECMD2         | 11               | 1    | W    | Flickerless Control |

|   |   |   |   |   |   |   |     |
|---|---|---|---|---|---|---|-----|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0   |
| - | - | - | - | - | - | - | FLM |

High : NTSC 1/120 sec, PAL 1/100 sec  
Low : Flickerless Mode Off

| REGISTER NAME | ADDRESS NO.(HEX) | BITS | MODE | DESCRIPTION                  | REMARK |
|---------------|------------------|------|------|------------------------------|--------|
| SCMD          | 80               | 8    | W    | Superimpose Command Register |        |

#### Superimpose Instruction Set Format

|     |     |     |     |                      |   |   |   |
|-----|-----|-----|-----|----------------------|---|---|---|
| 7   | 6   | 5   | 4   | 3                    | 2 | 1 | 0 |
| FIL | OUT | CT1 | CT0 | Sub Instruction Code |   |   |   |

#### 1) TYPE 0 (CT1=0, CT2=0) : Environmental Instruction

|   |   |   |   |   |    |    |    |
|---|---|---|---|---|----|----|----|
| 7 | 6 | 5 | 4 | 3 | 2  | 1  | 0  |
| - | - | 0 | 0 | - | C2 | C1 | C0 |

\* NML Conditions :

-. ROM : 0  
 -. TOG : 0  
 -. MEDi : 0  
 -. SWAP : 0  
 -. PB : 0  
 -. TST : 0  
 -. DMA : 0  
 -. WRN : 0

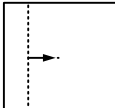
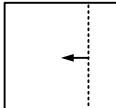
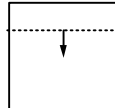
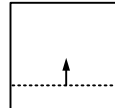
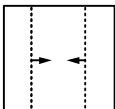
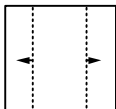
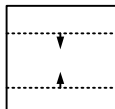
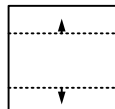
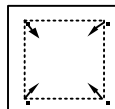
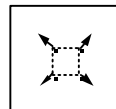
000 : ---  
 001 : NML  
 010 : STOP  
 011 : TOG  
 100 : MEDi  
 101 : ROM  
 110 : SWAP  
 111 : ---

#### 2) TYPE 1 (CT1=0, CT0=0) : Configure Environment 1 (R/W, SCOLL)

|   |   |   |   |   |    |    |    |
|---|---|---|---|---|----|----|----|
| 7 | 6 | 5 | 4 | 3 | 2  | 1  | 0  |
| - | - | 0 | 1 | - | C2 | C1 | C0 |

000 : ----  
 001 : READ  
 010 : WRITE  
 011 : SCi  
 100 : SCo  
 101 : ----  
 110 : ----  
 111 : ----

Occur Superimpose Busy Flag '1' while sci, sco operation Mode.  
 And, impossible to excute the other superimpose intermediate in this status.  
 (About for 4 seconds)

| REGISTER NAME                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | ADDRESS NO.(HEX) | BITS | MODE | DESCRIPTION | REMARK |    |    |   |   |   |   |   |   |     |     |   |   |    |    |    |    |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|------|------|-------------|--------|----|----|---|---|---|---|---|---|-----|-----|---|---|----|----|----|----|
| 3) TYPE2 ( CT1 = 1, CT2 = 0 ) : Environmental Instruction                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                  |      |      |             |        |    |    |   |   |   |   |   |   |     |     |   |   |    |    |    |    |
| <div><table><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>FIL</td><td>OUT</td><td>1</td><td>0</td><td>F3</td><td>F2</td><td>F1</td><td>F0</td></tr></table><div><div><div>0 : Normal Wiper<br/>1 : Inverse Wiper</div><div>0 : Normal<br/>1 : FILL Mode</div></div><div><div>0000 : ---<br/>0001 : F1<br/>0010 : F2<br/>0011 : F3<br/>0100 : F4<br/>0101 : F5<br/>0110 : F6<br/>0111 : F7<br/>1000 : F8<br/>1001 : F9<br/>1010 : F10<br/>1011 : ---<br/>1100 : ---<br/>1101 : ---<br/>1110 : ---<br/>1111 : ---</div></div></div><div><div><div><div></div><div></div><div></div><div></div></div><div><div></div><div></div><div></div><div></div><div></div><div></div></div></div><div><p>* Occur Superimpose Busy Flag '1' while wiper operation Mode. And impossible to excute the other superimpose intermediate in this status (About for 4 seconds)</p></div></div></div> |                  |      |      |             |        | 7  | 6  | 5 | 4 | 3 | 2 | 1 | 0 | FIL | OUT | 1 | 0 | F3 | F2 | F1 | F0 |
| 7                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 6                | 5    | 4    | 3           | 2      | 1  | 0  |   |   |   |   |   |   |     |     |   |   |    |    |    |    |
| FIL                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | OUT              | 1    | 0    | F3          | F2     | F1 | F0 |   |   |   |   |   |   |     |     |   |   |    |    |    |    |
| 4) TYPE 3 ( CT1 = 1, CT0 = 1 ) : Configure Environment 3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                  |      |      |             |        |    |    |   |   |   |   |   |   |     |     |   |   |    |    |    |    |
| <div><table><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>-</td><td>-</td><td>1</td><td>1</td><td>-</td><td>C2</td><td>C1</td><td>C0</td></tr></table><div><div>000 : ---<br/>001 : PB<br/>010 : TST1<br/>011 : DMA<br/>100 : WRN<br/>101 : ---<br/>110 : ---<br/>111 : ---</div></div></div>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                  |      |      |             |        | 7  | 6  | 5 | 4 | 3 | 2 | 1 | 0 | -   | -   | 1 | 1 | -  | C2 | C1 | C0 |
| 7                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 6                | 5    | 4    | 3           | 2      | 1  | 0  |   |   |   |   |   |   |     |     |   |   |    |    |    |    |
| -                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | -                | 1    | 1    | -           | C2     | C1 | C0 |   |   |   |   |   |   |     |     |   |   |    |    |    |    |

| REGISTER NAME                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | ADDRESS NO.(HEX) | BITS   | MODE   | DESCRIPTION                                      | REMARK |     |     |   |   |   |   |   |   |     |     |     |   |     |     |     |     |     |     |        |     |   |   |        |        |   |   |        |        |   |   |        |   |   |   |        |   |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|--------|--------|--------------------------------------------------|--------|-----|-----|---|---|---|---|---|---|-----|-----|-----|---|-----|-----|-----|-----|-----|-----|--------|-----|---|---|--------|--------|---|---|--------|--------|---|---|--------|---|---|---|--------|---|
| SCOL                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 81               | 7      | R/W    | Super impose Color Status Register               |        |     |     |   |   |   |   |   |   |     |     |     |   |     |     |     |     |     |     |        |     |   |   |        |        |   |   |        |        |   |   |        |   |   |   |        |   |
| <div><table><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>C02</td><td>C01</td><td>C00</td><td>-</td><td>ROM</td><td>SWP</td><td>TOG</td><td>FIL</td></tr></table><div><div>0 : Medi off<br/>1 : Medi on</div><div>0 : Toggle off<br/>1 : Toggle on</div><div>0 : Swap off<br/>1 : Swap on</div><div>0 : RAM Mode<br/>1 : ROM Mode</div><div>000 : Blank<br/>001 : Blue<br/>010 : Red<br/>011 : Magenta<br/>100 : Green<br/>101 : Cyan<br/>110 : Yellow<br/>111 : White</div></div></div> |                  |        |        |                                                  |        | 7   | 6   | 5 | 4 | 3 | 2 | 1 | 0 | C02 | C01 | C00 | - | ROM | SWP | TOG | FIL |     |     |        |     |   |   |        |        |   |   |        |        |   |   |        |   |   |   |        |   |
| 7                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 6                | 5      | 4      | 3                                                | 2      | 1   | 0   |   |   |   |   |   |   |     |     |     |   |     |     |     |     |     |     |        |     |   |   |        |        |   |   |        |        |   |   |        |   |   |   |        |   |
| C02                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | C01              | C00    | -      | ROM                                              | SWP    | TOG | FIL |   |   |   |   |   |   |     |     |     |   |     |     |     |     |     |     |        |     |   |   |        |        |   |   |        |        |   |   |        |   |   |   |        |   |
| * MSB [7 ~ 5] Color status bit is READ/WRITE, all other bits are READ only                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                  |        |        |                                                  |        |     |     |   |   |   |   |   |   |     |     |     |   |     |     |     |     |     |     |        |     |   |   |        |        |   |   |        |        |   |   |        |   |   |   |        |   |
| SDAT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 82               | 8      | R/W    | Data Register (Buffer of using at DMA test mode) |        |     |     |   |   |   |   |   |   |     |     |     |   |     |     |     |     |     |     |        |     |   |   |        |        |   |   |        |        |   |   |        |   |   |   |        |   |
| SPG                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 83               | 3      | WR     | Setting RAM mode stage                           |        |     |     |   |   |   |   |   |   |     |     |     |   |     |     |     |     |     |     |        |     |   |   |        |        |   |   |        |        |   |   |        |   |   |   |        |   |
| <div><table><tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>PG1</td><td>PG0</td><td>SWP</td></tr></table><table><tr><td>PG1</td><td>PG2</td><td>Normal</td><td>Hi8</td></tr><tr><td>0</td><td>0</td><td>Page 0</td><td>Page 0</td></tr><tr><td>0</td><td>1</td><td>Page 1</td><td>Page 1</td></tr><tr><td>1</td><td>0</td><td>Page 2</td><td>-</td></tr><tr><td>1</td><td>1</td><td>Page 3</td><td>-</td></tr></table></div>             |                  |        |        |                                                  |        | 7   | 6   | 5 | 4 | 3 | 2 | 1 | 0 | -   | -   | -   | - | -   | PG1 | PG0 | SWP | PG1 | PG2 | Normal | Hi8 | 0 | 0 | Page 0 | Page 0 | 0 | 1 | Page 1 | Page 1 | 1 | 0 | Page 2 | - | 1 | 1 | Page 3 | - |
| 7                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 6                | 5      | 4      | 3                                                | 2      | 1   | 0   |   |   |   |   |   |   |     |     |     |   |     |     |     |     |     |     |        |     |   |   |        |        |   |   |        |        |   |   |        |   |   |   |        |   |
| -                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | -                | -      | -      | -                                                | PG1    | PG0 | SWP |   |   |   |   |   |   |     |     |     |   |     |     |     |     |     |     |        |     |   |   |        |        |   |   |        |        |   |   |        |   |   |   |        |   |
| PG1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | PG2              | Normal | Hi8    |                                                  |        |     |     |   |   |   |   |   |   |     |     |     |   |     |     |     |     |     |     |        |     |   |   |        |        |   |   |        |        |   |   |        |   |   |   |        |   |
| 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 0                | Page 0 | Page 0 |                                                  |        |     |     |   |   |   |   |   |   |     |     |     |   |     |     |     |     |     |     |        |     |   |   |        |        |   |   |        |        |   |   |        |   |   |   |        |   |
| 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 1                | Page 1 | Page 1 |                                                  |        |     |     |   |   |   |   |   |   |     |     |     |   |     |     |     |     |     |     |        |     |   |   |        |        |   |   |        |        |   |   |        |   |   |   |        |   |
| 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 0                | Page 2 | -      |                                                  |        |     |     |   |   |   |   |   |   |     |     |     |   |     |     |     |     |     |     |        |     |   |   |        |        |   |   |        |        |   |   |        |   |   |   |        |   |
| 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 1                | Page 3 | -      |                                                  |        |     |     |   |   |   |   |   |   |     |     |     |   |     |     |     |     |     |     |        |     |   |   |        |        |   |   |        |        |   |   |        |   |   |   |        |   |

| REGISTER NAME                                                                                                               | ADDRESS NO.(HEX) | BITS   | MODE | DESCRIPTION                                                                                | REMARK |         |        |     |          |        |        |
|-----------------------------------------------------------------------------------------------------------------------------|------------------|--------|------|--------------------------------------------------------------------------------------------|--------|---------|--------|-----|----------|--------|--------|
| SADR00                                                                                                                      | 84               | 8      | WR   | ROM image 0 address register (20Bit)                                                       |        |         |        |     |          |        |        |
| SADR01                                                                                                                      | 85               | 8      | WR   |                                                                                            |        |         |        |     |          |        |        |
| SADR02                                                                                                                      | 86               | 4      | WR   |                                                                                            |        |         |        |     |          |        |        |
| SADR10                                                                                                                      | 87               | 8      | WR   | ROM image 1 address register (20Bit)                                                       |        |         |        |     |          |        |        |
| SADR11                                                                                                                      | 88               | 8      | WR   |                                                                                            |        |         |        |     |          |        |        |
| SADR12                                                                                                                      | 89               | 4      | WR   |                                                                                            |        |         |        |     |          |        |        |
| SADR20                                                                                                                      | 8A               | 8      | WR   | ROM image 2 address register (20Bit)                                                       |        |         |        |     |          |        |        |
| SADR21                                                                                                                      | 8B               | 8      | WR   |                                                                                            |        |         |        |     |          |        |        |
| SADR22                                                                                                                      | 8C               | 4      | WR   |                                                                                            |        |         |        |     |          |        |        |
| SADR30                                                                                                                      | 8D               | 8      | WR   | ROM image 3 address register (20Bit)                                                       |        |         |        |     |          |        |        |
| SADR31                                                                                                                      | 8E               | 8      | WR   |                                                                                            |        |         |        |     |          |        |        |
| SADR32                                                                                                                      | 8F               | 4      | WR   |                                                                                            |        |         |        |     |          |        |        |
| SADR40                                                                                                                      | 90               | 8      | WR   | ROM image 4 address register (20Bit)                                                       |        |         |        |     |          |        |        |
| SADR41                                                                                                                      | 91               | 8      | WR   |                                                                                            |        |         |        |     |          |        |        |
| SADR42                                                                                                                      | 92               | 4      | WR   |                                                                                            |        |         |        |     |          |        |        |
| <table><tr><td>23 ~ 16</td><td>15 ~ 8</td><td>4~0</td></tr><tr><td>* SADR02</td><td>SADR01</td><td>SADR00</td></tr></table> |                  |        |      |                                                                                            |        | 23 ~ 16 | 15 ~ 8 | 4~0 | * SADR02 | SADR01 | SADR00 |
| 23 ~ 16                                                                                                                     | 15 ~ 8           | 4~0    |      |                                                                                            |        |         |        |     |          |        |        |
| * SADR02                                                                                                                    | SADR01           | SADR00 |      |                                                                                            |        |         |        |     |          |        |        |
| * SADR02 uses only LSB 4Bit.                                                                                                |                  |        |      |                                                                                            |        |         |        |     |          |        |        |
| STH                                                                                                                         | 93               | 8      | WR   | Horizontal counter test register (Used in test)                                            |        |         |        |     |          |        |        |
| STV                                                                                                                         | 94               | 8      | WR   | Vertical counter test register (Used in test)                                              |        |         |        |     |          |        |        |
| SSYN                                                                                                                        | 95               | 8      | WR   | Title horizontal position adjusting value<br>(After reset, 1 is set and 0 is not allowed.) |        |         |        |     |          |        |        |
| SVRT                                                                                                                        | 96               | 8      | WR   | Title vertical position adjusting value<br>(After reset, 1 is set and 0 is not allowed.)   |        |         |        |     |          |        |        |

KS7301B

DIGITAL CAMERA PROCESSOR

PACKAGE DIMENSION

Unit : mm

