International
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Data Sheet No. PD60225

IRMCK203

High Performance Sensorless Motion Control IC

Features

- **Complete Sensorless control IC for Permanent Magnet AC motors**
- **No voltage feedback sensing required**
- **Sinusoidal current waveform with Synchronously Rotating Frame closed loop current control**
- **High starting torque and smooth speed ramping**
- **Direct interface to IR2175 current sensing high voltage IC**
- **Auto Retry at startup with presettable torque**
- **Versatile loss minimization Space Vector PWM**
- **Configurable architecture**
- **Serial communication interface (RS232C, RS422, SPI)**
- **I^2C serial interface to 1k bit serial EEPROM for parameter storage for stand alone operation**
- **Phase loss/Overcurrent/Overvoltage protection**
- **7-bit discrete I/O for sequencing and status monitor**
- **Integrated brake IGBT control**
- **ServoDesigner™ tool for easy operation**
- **Parallel interface for microcontroller expansion**

Product Summary

Max Clock input	33.3 MHz
Sensorless control computation time	11 usec max
Speed operating range (typical)	< 5% to 100%
Speed control resolution	15 bit full range
Adjustable current limit at start-up	
Programmable retry on start-up trials	max 16
Over current, speed, phase loss, dc bus fault protection	
PWM carrier frequency	16 bit/33MHz
IR2175 Current feedback data resolution	10bit
Optional low side 3-leg current sensing	
Max R3232C speed	56 Kbps
Optional RS422 communication	1 Mbps
Package: QFP80	

Description

IRMCK203 is a high performance digital motion control IC for Sensorless AC permanent magnet motor application. Control is based on closed loop vector control with sinusoidal Back EMF. With IRMCK203, the users can readily build a high performance Sensorless drive system without any programming effort and minimum start-up time. Built-in unique start-up and ramping algorithm enables wide application. This IC is versatile enough that the users can configure and optimize system performance according to the needs of each application. With International Rectifier iMOTION product including high voltage ICs such as IR2175 current sensing IC and IRAM series of Intelligent IGBT module in combination with IRMCK203, the end result is a fully optimized system with reduced electronics component counts. This simplifies the design for low cost Sensorless drive modules. IRMCK203 can be easily adapted to various permanent magnet motors through ServoDesigner™ tool, which is the fully configurable graphic user interface tool.

Overview

IRMCK203 is a new International Rectifier integrated circuit device designed for one-chip solution for complete closed loop current control and velocity control for a high performance servo drive system. Unlike a traditional microcontroller or DSP, IRMCK203 does not require any programming to complete complex AC servo algorithm development. Combined with International Rectifier's high voltage gate drive and current sensing IC, the user can implement a complete AC servo control with minimum component count and virtually no design effort. Although IRMCK203 contains dedicated logic to perform closed loop control of AC current and velocity, it has wide range of application coverage through flexible configuration ability. The drive can be easily configured induction machine closed loop vector control or permanent magnet motor servo drive. Rich motion peripherals, analog and digital I/O can also be configured. Host communication logic contains Asynchronous Communication Interface for RS232C or RS422 or RS485 communication interface, a fast slave SPI interface and an 8 bit wide Host Parallel Interface. All communication ports have same access capability to the host register set. The user can write to, and read from the predefined registers to configure and monitor the drive through these communication ports.

IRMCK203 Main functions

IRMCK203 contains the following functions for AC servo motor control applications:

- Complete closed loop current control based on Synchronously Rotating Frame Field Orientation.
- Configurable update rate with PWM carrier frequency.
- Configurable parameters (all PI controller gains, PI output limit range, current feedback scaling, encoder feedback scaling)
- Built-in sensorless logic for start-up, ramping, and running conditions
- Closed loop velocity control based on estimated speed
- Selectable reference input for torque and speed input
- Auto Retry (programmable) with presettable torque
- Analog reference input
- RS232C/RS422 reference input
- Dynamic braking control for excess DC bus voltage
- Cycle-by-cycle on/off Control for Brake IGBT
- DC bus voltage feedback
- Loss minimization Space Vector PWM with deadtime insertion
- IR2175 current sensing IC interface
- Phase loss, overcurrent (GATEKILL input), overvoltage, undervoltage protection
- Low cost serial 12bit A/D interface with multiplexer and sample/hold circuit
- Optional 3-leg current sensing in lieu of IR2175 IC.
- 4 channel analog output by PWM
  0-5 V output, 16kHz cut-off frequency with 2-pole butter-worth filter
  One channel analog output for Resolver reference (10kHz sinusoidal)
- Local EEPROM for startup initialization of internal data/parameters through host register interface
  AT24C01A, 128X8
- Versatile host communication interface
  RS232C or RS422 host interface
  Fast SPI slave host interface with multi-drop capability
  Parallel Host interface (total 12 pins)
- Multiplexed data/address bus

Address Enable
RD/WR

- Discrete I/O
  Start/Stop (Input)
  E-Stop (Input)
  FWD/REV (Input)
  Fault Clear (Input)
  Fault (Output)
  SYNC (Output)
  PWM Enable (Output)
- LED
  Two bit bi-color

IRMCK203 Block Diagrams

Basic Block Diagram

Error! Reference source not found. shows the basic block diagram of the IRMCK203 surrounded by International Rectifiers' ICs. Host communications are provided over SPI, RS-232C or Host parallel ports. Two current sensing ICs (IR2175) and a three phase high voltage gate drive typically implement the high voltage / current interface between the IRMCK203 IC and motor.

The IRMCK203 can operate in a "stand-alone" mode without the host controller. A serial EEPROM would be utilized to load motor-specific parameters into the IC.

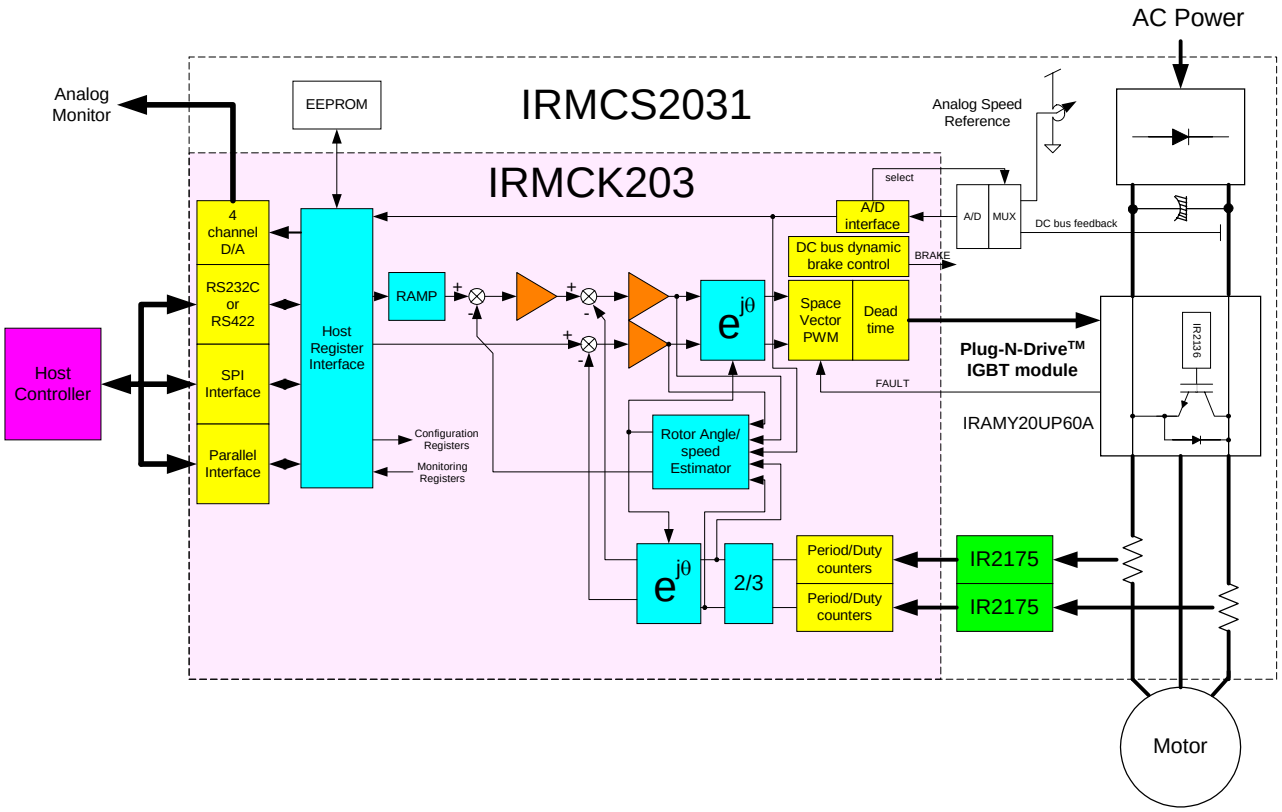

Figure 1. IRMCS2031 Simplified Blocks

Configurable parameters are provided to tailor design to various applications (motor and load). These configurable parameters can be modified via the host register interface through the communication interface. In the IRMCK203 product, a design spread sheet is provided to aid the user for ease of drive start-up, the spread sheet will input high level application data such as motor name plate information, max speed, current limit, speed and current regulator bandwidth, base on this information the program will generate the required configurable parameters. Detail on Drive commissioning is described in the IRMCS2031 Application Development Guide.

Detailed Block Diagram

Figure 2: Detailed Block Diagram of IRMCK203 shows the detailed block diagram or the IRMCK203. All logic and algorithms are pre-programmed, and the user does not need to make any effort to develop code, alleviating the tedious design process. If needed, the user can configure the drive to tailor the control per specific needs to meet the required specification. This configuration can be easily done by accessing the host register interface through the communication interface.

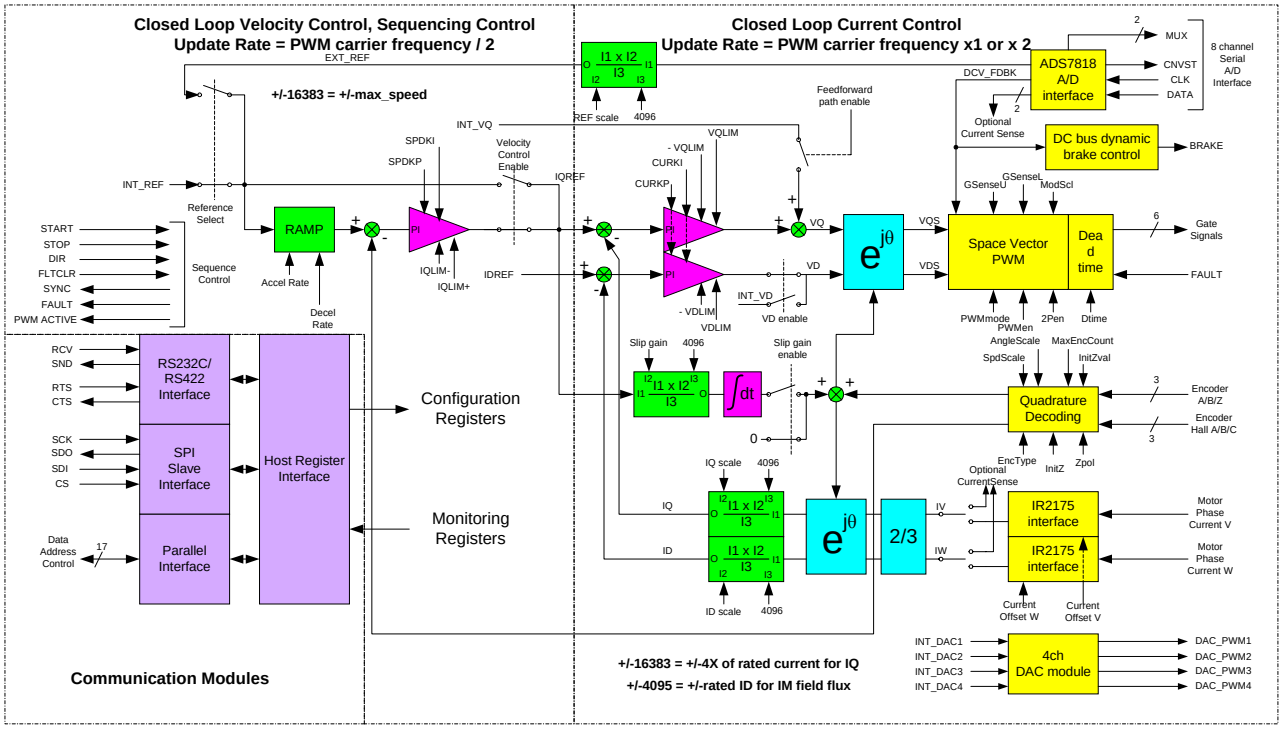

Figure 2: Detailed Block Diagram of IRMCK203

Input/Output of IRMCK203

The I/O signals are shown in Fig. 3. The interface signals are divided into sub-groups. All I/O pins are 3.3V logic interface. For detailed pin assignment, please refer to appendix (Pin definition).

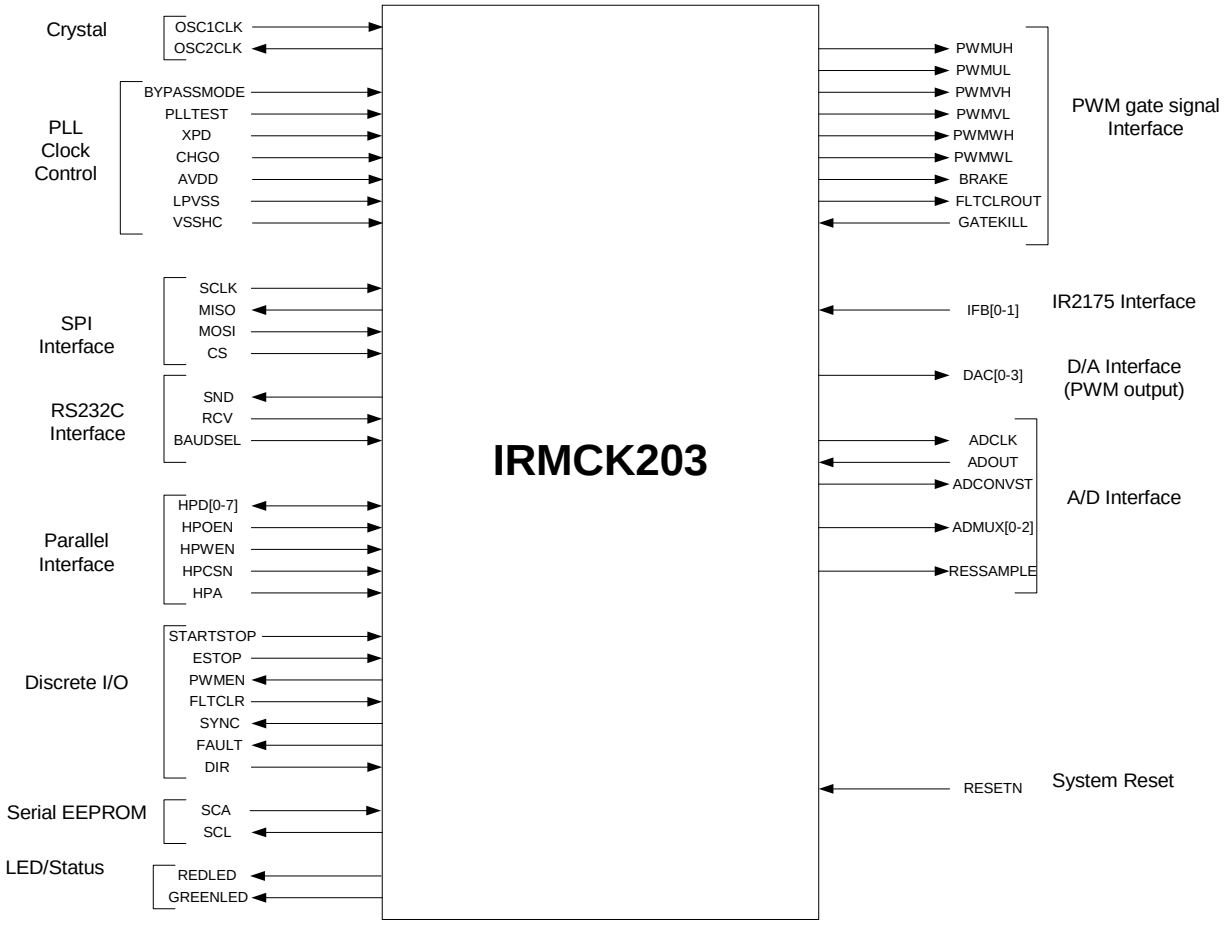

Figure 3 Input/Output of IRMCK203

Communication Group

SPI Interface

- SCLK - Input, SPI clock
- MISO - Output, Master Input and Slave Output, Data output from IRMCK203
- MOSI - Input, Master Output and Slave Input, Data input from the host
- CS - Input, Chip Select

I^2C Interface for EEPROM

- SCA - Bi-directional data, Serial EEROM interface
- SCL - Clock, Serial EEROM interface

Asynchronous Communication (RS232C, RS422, RS485) Interface

- SND - Output, Send data from IRMCK203
- RCV - Input, Receive data to IRMCK203
- BAUDSEL - Baud rate select (57.6k/1M)

Motion Peripheral Group

PWM

- PWMUH - Output, PWM phase U high side gate signal
- PWMUL - Output, PWM phase U low side gate signal
- PWMVH - Output, PWM phase V high side gate signal
- PWMVL - Output, PWM phase V low side gate signal
- PWMWH - Output, PWM phase W high side gate signal
- PWMWL - Output, PWM phase W low side gate signal
- BRAKE - Output, Brake IGBT gate signal

IR2175

- IFB0 - Input, IR2175 channel 0 input (Phase V)
- IFB1 - Input, IR2175 channel 1 input (Phase W)

Fault

- GATEKILL - Input, upon assertion, this negates all six PWM signals
- FLTCLROUT - Output, Fault clear output

Analog interface Group

- ADCLK - Output, clock signal to ADS7818 Channel 0 A/D converter
- ADOUT - Input, serial data from ADS7818 Channel 0 A/D converter
- ADCONVST - Output, conversion start to ADS7818 Channel 0 A/D converter
- ADMUX0 - Output, multiplexer steering address
- ADMUX1 - Output, multiplexer, steering address
- RESSAMPLE - Output, sample/hold control signal channel 0 A/D converter
- DAC[0-3] - Output, 4 channel Analog Output (PWM output)

Discrete I/O Group

- START - Input, Start/Stop command, level sensitive
- ESTOP - Input, Stop, state sensitive
- FAULTCLR - Input, Fault clear, edge sensitive
- PWMEN - Output, PWM enable/disable state output
- SYNC - Output, SYNC pulse output
- FAULT - Output, Fault state output

Parallel Interface Group

- HPD[0-7] - Input/Output, 8bit data/address multiplexed bus for parallel port interface
- HPOEN - Input, Output enable strobe for read access
- HPWEN - Input, Write enable strobe for write access
- HPCSN - Input, Chip Select strobe
- HPA - Input, Address enable

CLOCK/PLL management Group

- BYPASSMODE - Input, must be tied to ground
- CHGO - Output, connected to RC filter circuit
- OSC1CLK - Input, connected to Crystal
- OSC2CLK - Output, connected to Crystal
- PLLTEST - Input must be tied to ground
- XPD - PLL reset, must be asserted while RESETN is active
- VSSHC - Power, must be tied to ground
- MVDD - Power, must be tied to VDD (3.3V)
- AVDD - Power, must be tied to VDD (3.3V)
- LPVSS - Power, must be tied to ground

Miscellaneous Group

- REDLED - Output, LED0 drive signal
- GREENLED - Output, LED1 drive signal

These SPI interface signals are configured for Slave mode. Therefore the host SPI interface determines SPI clock speed.

Application Connections

Typical application connection is shown in Figure . In order to complete a Sensorless drive control, all necessary components are shown in connection to IRMCK203.

Although this is a typical hardware configuration, users can customize the design without changing code by restless programming effort.

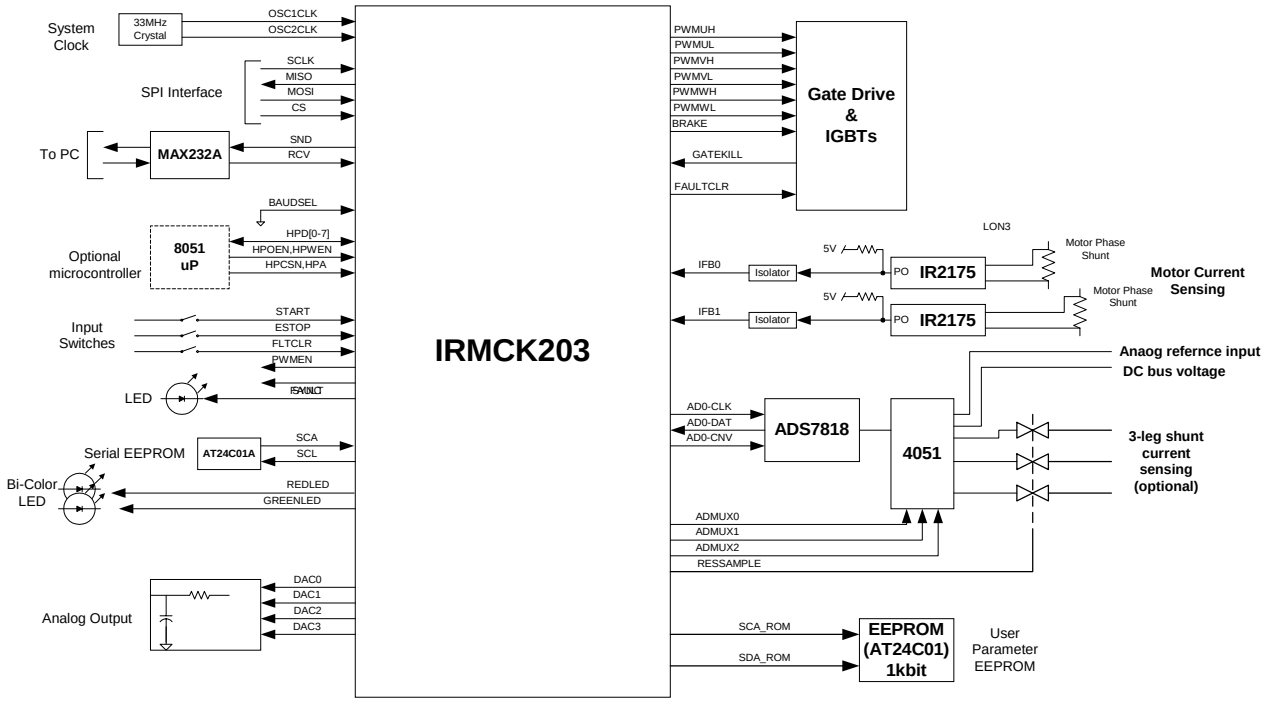

Figure 4. Application Connection of IRMCK203

IC Crystal Clock Circuitry

The clock input to the IC is a 33.33 MHz crystal oscillator. Two shunt capacitors and a possibly a series resistor is required to terminate the crystal to the IC.

The values of the R/C will vary based on actual PCB attributes, and some empirical analysis may be required to get the PLL to start oscillating. Once oscillating, verify that the signal waveform at the OSC1CLK and OSC2CLK pins are sinusoidal rather than trapezoidal. Refer to Table 1: Common Values for the Clock Circuit for suggested R/C values. Most low-cost crystals can be used in this application. An example is a Citizen Part number CM309B33.333MABJT available from Digi-Key under part number 300-4160-1-ND.

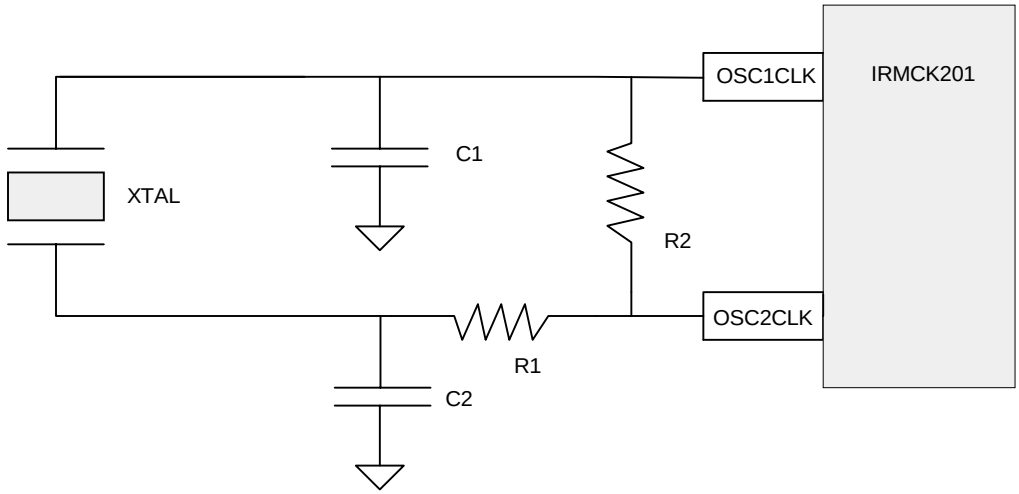

Figure 5: Oscillator Circuit

COMPONENT	VALUE	UNITS
XTAL	33.33	MHz
C1	5	pf
C2	5	pf
R1	0	OHM
R2	3.9K	OHM

Table 1: Common Values for the Clock Circuit

PLL Clock Circuitry

The IRACK201 contains a PLL that creates a 2X and 4X clock from the input 33.33 MHz input clock pin. There are a number of pins on the IC allocated for factory testing purposes, and need to be left unconnected. Table 2: PLL Test Pin Assignments shows required PCB signal connections for these pins.

PIN NUMBER	PCB CONNECTION
1	VSS
2	VSS
7	VSS
15	N/C
16	N/C
17	N/C
18	N/C
23	N/C
24	N/C
25	N/C
41	N/C
45	N/C
56	N/C
89	N/C

Table 2: PLL Test Pin Assignments

Low Pass Filter

The low pass filter for this PLL resides between the CHGO and LPVSS pins. Three passive components are required to implement this filter: Cp, Rp and Cs. Figure 6: PLL Low Pass Filter Shielding shows how to place these components around the IC.

A shield should be placed below Rp, Cp and Cs made out of copper etch.

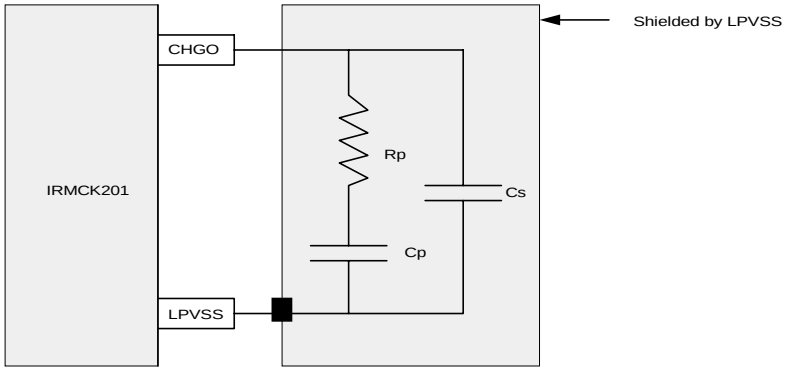

Figure 6: PLL Low Pass Filter Shielding

Implementing the Low Pass Filter Shield

Make all connections between CHGO, Rp, Cp, Cs and LPVSS as short as possible. Create the underlining shield by "copper filling" a larger area in the signal plane of the PCB. Connect this shield to the LPVSS pin of the IC. Do not connect this shield to signal ground (VSS).

Cp Rp and Cs Component Values

For a typical FR4 PCB, the values of the passive components are shown in Figure 7: PLL Low Pass Filter Values.

COMPONENT	VALUE	UNITS
Rp	3.9K	OHM
Cp	1000	pf
Cs	Not Installed	-

Figure 7: PLL Low Pass Filter Values

PLL Reset

There are two reset pins on the IC, XPD and RESETN both low true. XPD holds the PLL circuitry in reset when low. Upon XPD going high, the PLL circuitry begins to lock onto the 33.33 MHz clock input. The PLL circuit may take up to 1 ms to become stable. RESETN asserted low holds the internal DSP logic in reset. Upon RESETN going high, the IC digital logic becomes active.

RESET should be held low during and at least 1 ms after XPD goes high false to hold the internal logic in reset while the PLL becomes stable.

DC Electrical Characteristics and Operating Conditions

Absolute Maximum Ratings

Note: VSS = 0 Volt

PARAMETER	SYMBOL	LIMITS	UNITS	NOTE
Power Supply Voltage	VDD	VSS-0.3 to 4.0	V	
Input Voltage	VI	VSS-0.3 to VDD+0.5	V	Non 5 Volt Tolerant Pins (Note 1)
Input Voltage	VI	VSS-0.3 to 7	V	Only on 5 Volt Tolerant Pins (Note 1)
Output Voltage	VO	VSS-0.3 to VDD+0.5	V	
Output Current per Pin	IOUT	+/- 30	mA	
Storage Temperature	Tstg	-65 to 150	°C	

Table 3: Absolute Maximum Ratings

Recommended Operating Conditions

Note: VSS = 0 Volt

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTE
Power Supply Voltage	VDD	3.0	3.3	3.6	V	
Input Voltage	VI	VSS	-	VDD	V	Non 5 Volt Tolerant Pins (Note 1)
Input Voltage	VI	VSS	-	5.5	V	Only on 5 Volt Tolerant Pins (Note 1)
Ambient Temperature	Ta	-40	-	85	°C	Note 2

Table 4: Recommended Operating Conditions

Notes:
2. The ambient temperature range is recommended for Tj= -40 to 125 °C

DC Characteristics

Common Quiescent and Leakage Current

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Current	IDDS	VI=VDD or VSS VDD=MAX IOH=IOL=0 Ta=Tj=85°C	-	-	.35	uA
Input Leakage Current	ILI	VDD=MAX VIH=VDD VIL=VSS	-1	-	1	uA

Table 5: DC Characteristics

Input Characteristics – Non Schmitt Inputs

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High Level Input Voltage	VIH1	VDD=MAX	2.0	-	-	V
Low Level Input Voltage	VIL1	VDD=MIN	-	-	0.8	V

Table 6: Non Schmitt Input Characteristics

Input Characteristics – Schmitt Inputs

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High Level Input Voltage	VT1+	VDD=MAX	1.1	-	2.4	V
Low Level Input Voltage	VT1-	VDD=MIN	0.6	-	1.8	V
Hysteresis Voltage	VH1	VDD=MIN	0.1	-	-	V

Table 7: Schmitt Input Characteristics

Output Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High Level Output Voltage	VOH3	VDD=MIN IOH=-12mA	VDD - 0.4	-	-	V
Low Level Output Voltage	VOL3	VDD=MIN IOH = 12mA	-	-	VSS + 0.4	V

Table 8: Output Characteristics

Pin and I/O Characteristic Table

Pin Number	Pin Name	INTERNAL IC RESISTOR TERMINATION	Pin Type	5.50 VOLT TOLERANT INPUT	INPUT DC CHARACTERISTIC TABLE	OUTPUT DC CHARACTERISTIC TABLE
1	BYPASSMODE	40K-240K Pull Down	I	-	Table 7: Schmitt Input Characteristics	-
2	FLTCLROUT		O	-		-
3	OSC1CLK		I	-		
4	LVDD		P	-	-	-
5	OSC2CLK		O	-		
6	VSS		P	-	-	-
7	PLLTEST	20K-120K Pull Down	I	-	Table 6: Non Schmitt Input Characteristics	-
8	XPD		I	-	Table 6: Non Schmitt Input Characteristics	-
9	VSSHC		P	-	-	-
10	MVDD		P	-	-	-
11	VSSHC		P	-	-	-
12	AVDD		P	-	-	-
13	CHGO		O	-	-	-
14	LPVSS		P	-	-	-
15	DIR	20K – 120K Pull Down	I			
16	RESETN	20K -120K Pull Up	I	-	Table 7: Schmitt Input Characteristics	-
17	SPICSN		I	YES	Table 7: Schmitt Input Characteristics	-
18	REDLED		O	-	-	Table 8: Output Characteristics
19	GREENLED		O	-	-	Table 8: Output Characteristics
20	VSS		P	-	-	-
21	PWMWL		O	-	-	Table 8: Output Characteristics
22	PWMWH		O	-	-	Table 8: Output Characteristics
23	PWMVL		O	-	-	Table 8: Output Characteristics
24	LVDD		P	-	-	-
25	PWMVH		O	-	-	Table 8: Output Characteristics
26	PWMUL		O	-	-	Table 8: Output Characteristics
27	VSS		P	-	-	-
28	PWMUH		O	-		Table 8: Output Characteristics
29	BRAKE		O	-	-	Table 8: Output Characteristics
30	BAUDSEL0	20K – 120K Pull Down	I	-	-	

Pin Number	Pin Name	INTERNAL IC RESISTOR TERMINATION	Pin Type	5.50 VOLT TOLERANT INPUT	INPUT DC CHARACTERISTIC TABLE	OUTPUT DC CHARACTERISTIC TABLE
31	GATEKILL	20K -120K Pull Up	I	-	Table 7: Schmitt Input Characteristics	-
32	IFB1		I	YES	Table 7: Schmitt Input Characteristics	-
33	IFB2		I	YES	Table 7: Schmitt Input Characteristics	-
34	LVDD		P	-	-	-
35	CLK1XOUT		O	-	-	Table 8: Output Characteristics
36	VSS		P	-		
37	SPIMOSI		I	YES	Table 7: Schmitt Input Characteristics	
38	SPIMISO		O	-	-	Table 8: Output Characteristics
39	SPICLK		I	YES	Table 7: Schmitt Input Characteristics	-
40	TX		O	-	-	Table 8: Output Characteristics
41	RX		I	YES	Table 7: Schmitt Input Characteristics	-
42	BAUDSEL1	20K -120K Pull Down	I	YES	Table 6: Non Schmitt Input Characteristics	-
43	LVDD		P	-	-	-
44	ADMUX0		O	-	-	Table 8: Output Characteristics
45	VSS		P	-	-	-
46	ADMUX1		O	-	-	Table 8: Output Characteristics
47	ADMUX2		O	-	-	Table 8: Output Characteristics
48	RESSAMPLE		O	-	-	Table 8: Output Characteristics
49	ADCONVST		O	-	-	Table 8: Output Characteristics
50	ADCLK		O	-	-	Table 8: Output Characteristics
51	ADOUT		I	YES	Table 7: Schmitt Input Characteristics	-
52	SYNC		O	-	-	Table 8: Output Characteristics
53	FAULT		O	-	-	Table 8: Output Characteristics
54	START/STOP	20K -120K Pull Down	I	YES	Table 7: Schmitt Input Characteristics	-
55	ESTOP	20K -120K Pull Down	I	YES	Table 7: Schmitt Input Characteristics	-
56	FLTCLR	20K -120K Pull Down	I	YES	Table 7: Schmitt Input Characteristics	-
57	LVDD		P	-	-	-

Pin Number	Pin Name	INTERNAL IC RESISTOR TERMINATION	Pin Type	5.50 VOLT TOLERANT INPUT	INPUT DC CHARACTERISTIC TABLE	OUTPUT DC CHARACTERISTIC TABLE
58	PWMEN		O	-	-	Table 8: Output Characteristics
59	DAC3		O	-	-	Table 8: Output Characteristics
60	VSS		P	-	-	-
61	DAC2		O	-	-	Table 8: Output Characteristics
62	DAC1		O	-	-	Table 8: Output Characteristics
63	DAC0		O	-	-	Table 8: Output Characteristics
64	HPD0	20K -120K Pull Down	B	-	Table 6: Non Schmitt Input Characteristics	Table 8: Output Characteristics
65	HPD1	20K -120K Pull Down	B	-	Table 6: Non Schmitt Input Characteristics	Table 8: Output Characteristics
66	HPD2	20K -120K Pull Down	B	-	Table 6: Non Schmitt Input Characteristics	Table 8: Output Characteristics
67	VDD		P	-	-	-
68	HPD3	20K -120K Pull Down	B	-	Table 6: Non Schmitt Input Characteristics	Table 8: Output Characteristics
69	HPD4	20K -120K Pull Down	B	-	Table 6: Non Schmitt Input Characteristics	Table 8: Output Characteristics
70	VSS		P	-	-	-
71	HPD5	20K -120K Pull Down	B	-	Table 6: Non Schmitt Input Characteristics	Table 8: Output Characteristics
72	HPD6	20K -120K Pull Down	B	-	Table 6: Non Schmitt Input Characteristics	Table 8: Output Characteristics
73	HPD7	20K -120K Pull Down	B	-	Table 6: Non Schmitt Input Characteristics	Table 8: Output Characteristics
74	HPOEN		I	YES	Table 7: Schmitt Input Characteristics	-
75	HPWEN		I	YES	Table 7: Schmitt Input Characteristics	
76	HPA		I	YES	Table 7: Schmitt Input Characteristics	-
77	HPCSN		I	YES	Table 7: Schmitt Input Characteristics	-
78	VSS		P	-	-	
79	SCL		O	-	-	Table 8: Output Characteristics
80	SDA	20K -120K Pull Up	B	-	Table 6: Non Schmitt Input Characteristics	Table 8: Output Characteristics

Table 9: Pin and I/O Characteristics

AC Electrical Characteristics and Operating Conditions

System Level AC Characteristics

Sync Pulse to Sync Pulse Timing

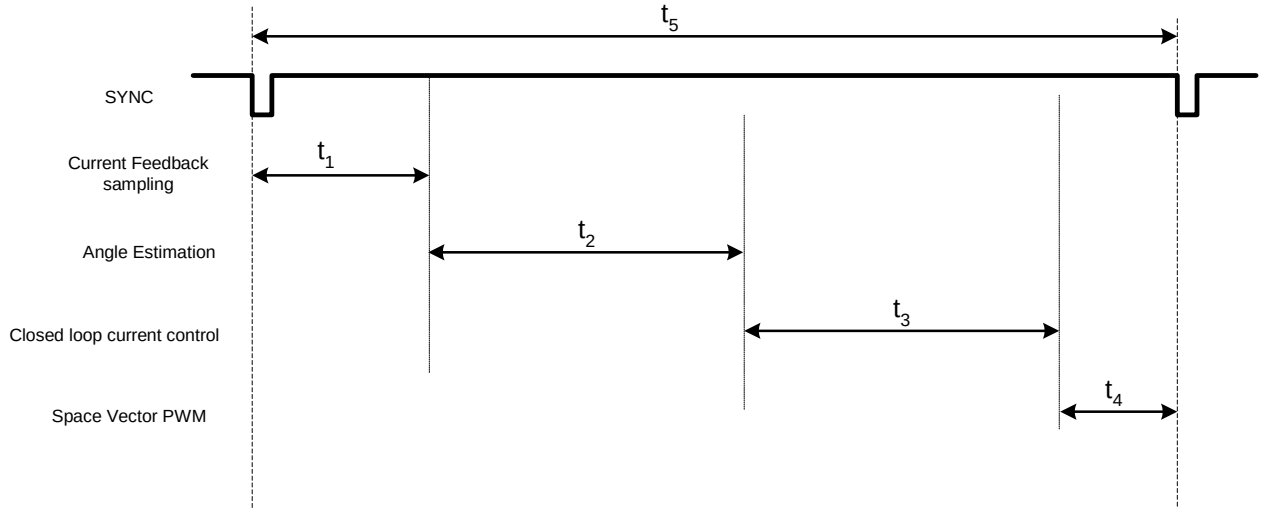

Figure 8: System Level SYNC To SYNC Timing

SYMBOL	DESCRIPTION	TIME	UNITS
t_1	Current Feedback Sample Delay from SYNC Pulse Falling Edge	4.3	us
t_2	Angle Estimation Time	4.9	us
t_3	Closed Loop Computation Time (current and velocity control)	3.1	us
t_4	Space Vector PWM calculation time	2.3	us
t_5	Total SYNC to SYNC minimum time	14.6	us

Table 10: System Level SYNC to SYNC Timing

FAULT and REDLED Response to GATEKILL

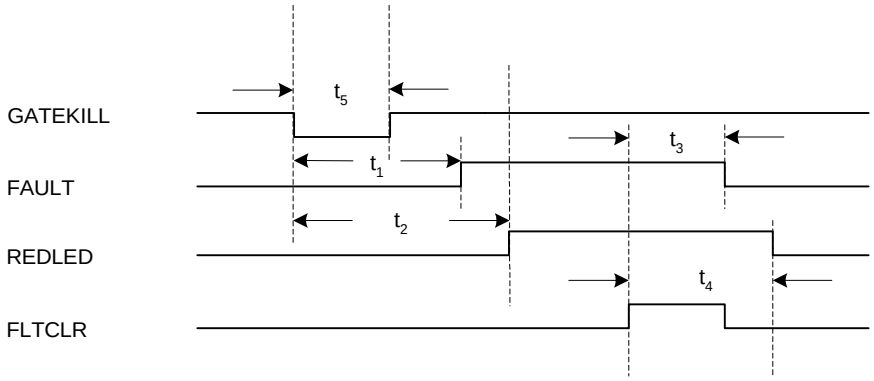

Figure 9: FAULT and REDLED Response to GATEKILL

SYMBOL	DESCRIPTION	MIN	TYP	UNITS
t_1	FAULT Response to GATEKILL		685	ns
t_2	REDLED Response to GATEKILL		715	ns
t_3	FAULT Response to FLTCLR		145	ns
t_4	REDLED Response to FLTCLR		175	ns
t_5	GATEKILL Pulse Width	490		ns

Table 11: FAULT and REDLED Response to GATEKILL

Host Interface AC Characteristics

SPI Timing

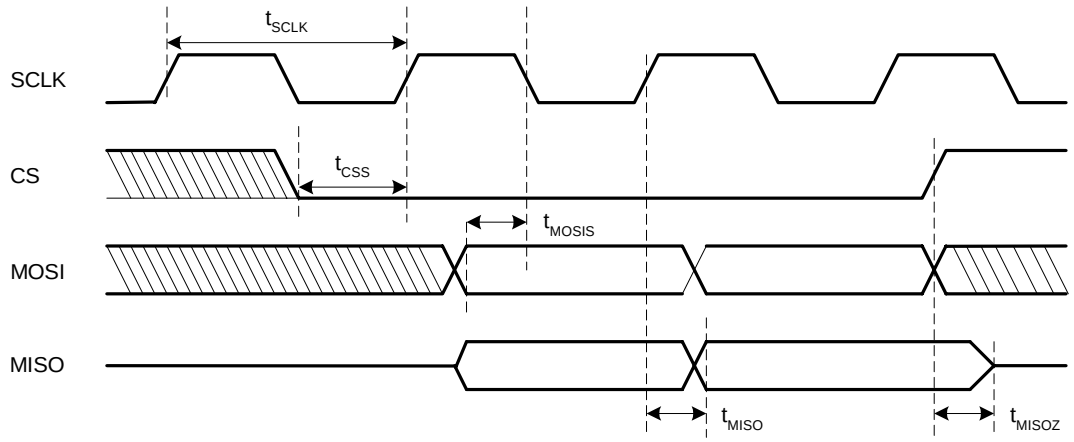

Figure 10 SPI Timing

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
f_{SCLK}	SPI Clock Frequency		8	MHz
t_{SCLK}	SPI Clock Period	125		ns
t_{CSS}	CS to SCLK high Setup	20		ns
t_{MOSIS}	MOSI to SCLK low Setup	20		ns
t_{MISO}	SCLK to MISO Valid	30		ns
t_{MIOZ}	CS to MOSI High Impedance	15	35	ns

Table 12: SPI Timing

Host Parallel Timing

Host Parallel Read Cycle

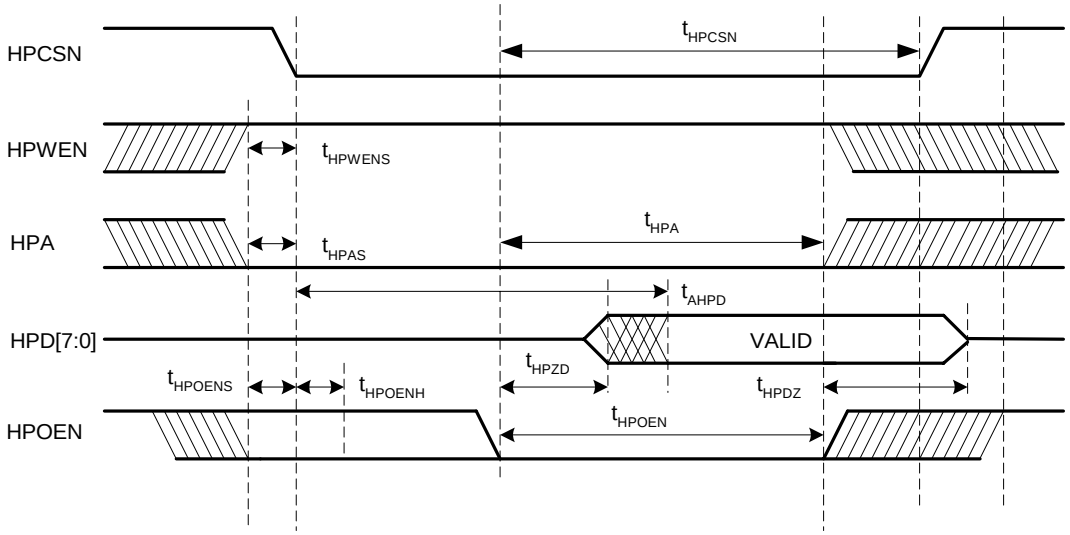

Figure 11: Host Parallel Read Cycle

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTE
t_{HPCSN}	HPCSN Period	70		ns	
t_{HPWENS}	HPWENS Setup	10		ns	
t_{HPAS}	HPA Setup	10		ns	
t_{AHPD}	HPD[7:0] Access	60	105	ns	
T_{HPZD}	HPD[7:0] Active	0	9	ns	
t_{HPDZ}	HPD[7:0] High Impedance	0	6	ns	
t_{HPOENH}	HPOEN Hold	10		ns	Note 3
t_{HPOENS}	HPOEN Setup	10		ns	Note 3
t_{HPOEN}	HPOEN Period	70		ns	

Table 13: Host Parallel Read Cycle Timing

Note:
3. HPOEN must be stable before and after the high to low transition of HPCNS.

Host Parallel Write Cycle

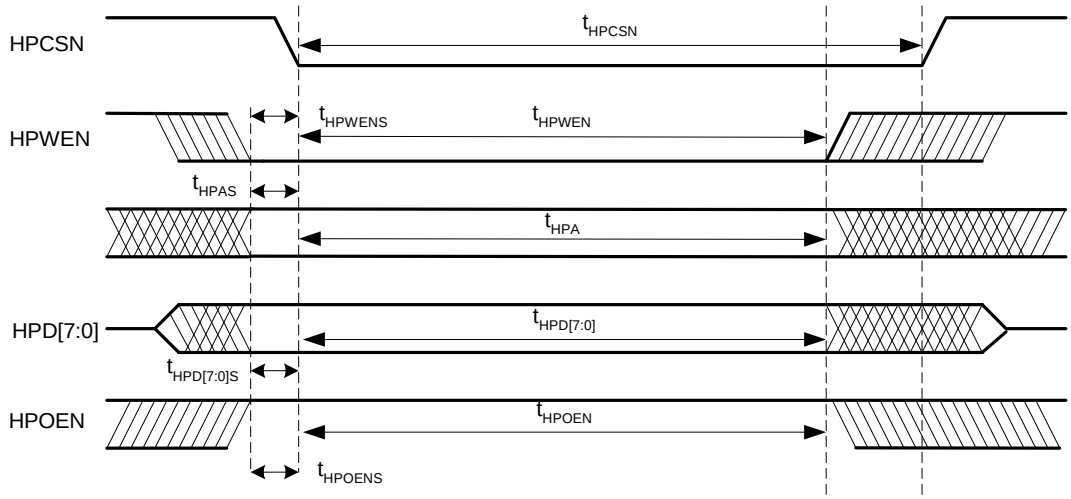

Figure 12: Host Parallel Write Cycle

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTE
t_{HPCSN}	HPCSN Period	70		ns	
t_{HPWENS}	HPWENS Setup	10		ns	
t_{HPWEN}	HPWEN Period	70		ns	
t_{HPAS}	HPA Setup	-10		ns	
t_{HPA}	HPA Period	70		ns	
$t_{HPD[7:0]}$	HPD[7:0] Setup	-10		ns	
t_{HPOENS}	HPOEN Setup	10		ns	
t_{HPOEN}	HPOEN Period	70		ns	Note 4

Table 14: Host Parallel Write Cycle Timing

Note:

4. HPOEN must be asserted high while HPCSN low during a Host Parallel Write Cycle.

Discrete I/O Electrical Characteristics

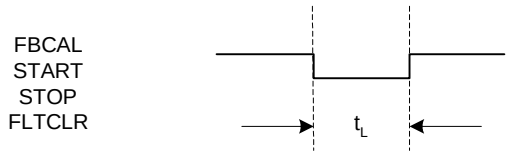

Figure 13: Discrete I/O Timing

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_L	Pulse Width FBCAL	100		ms
	Pulse Width START	100		ns
	Pulse Width STOP	100		ns
	Pulse Width FLTCLR	1		us

Table 15: Discrete I/O Timing

Motion Peripheral Electrical Characteristics

PWM Electrical Characteristics

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Figure 14: PWM Timing

SYMBOL	DESCRIPTION		UNITS
$t_{DEADTIMERESOLUTION}$	Deadtime Insertion Logic Resolution	30	ns

Table 16: PWM Timing

IR2175 Interface

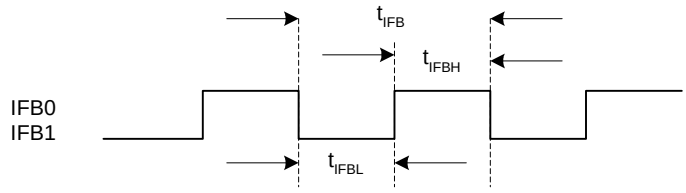


Figure 15: IR2175 Interface

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
f_{IFB}	Current Feedback Input Frequency	95	165	kHz
t_{IFB}	Current Feedback Period	10.52	6.06	us
t_{IBH}	Current Feedback High Pulse Width	500 ns	10 us	
t_{IFBH}	Current Feedback Low Pulse Width	500 ns	10 us	

Table 17: IR2175 Interface

Analog Interface Electrical Characteristics

ADC Timing

System Level Timing

The IRMCK203 contains logic to drive an ADC Converter, Analog MUX and associated Sample and Hold circuits. Figure 16: Top Level ADC Timing shows the system level timing of these elements. Figure 17: ADC Specific Timing shows specific timing parameters associated with the ADC Converter. Refer to the Application Developers Guide for a detailed description of ADC, MUX and Sample and Hold signal system level protocol.

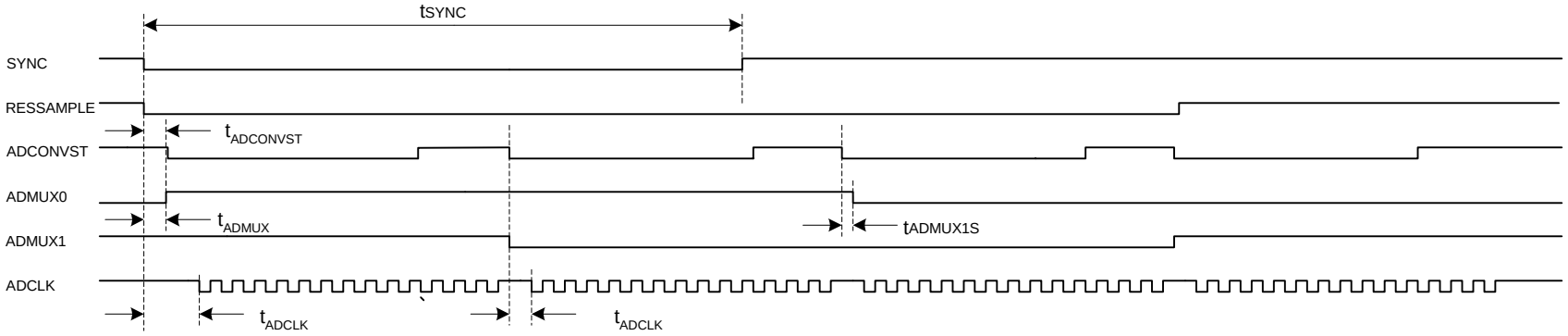


Figure 16: Top Level ADC Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{SYNC}	SYNC Pulse Width		3		us
$t_{RESSAMPLES}$	SYNC Falling Edge to RESSAMPLE Valid	-10		10	ns
$t_{ADMUX0S}$	ADCONVST to ADMUX0 Valid	40		61	ns
$t_{ADMUX1S}$	ADCONVST to ADMUX1 Valid	40		61	ns
$t_{ADCONVSTS}$	ADCONVST to ADCLK	71		91	ns

Table 18: Top Level ADC Timing

Converter Level Timing

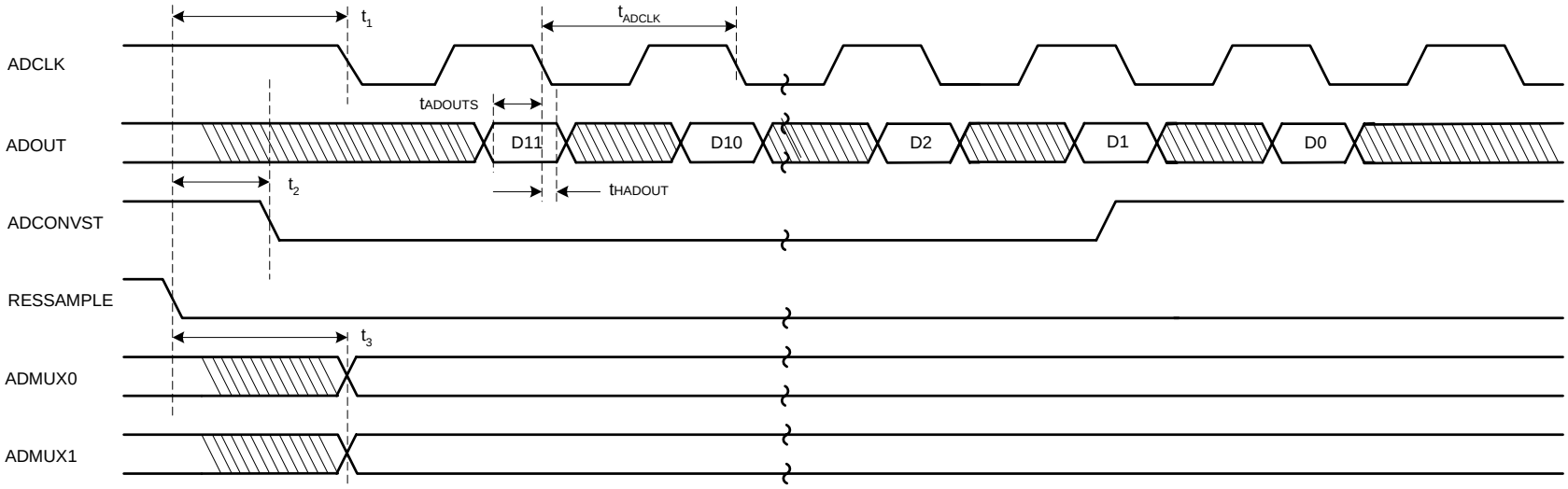


Figure 17: ADC Specific Timing

SYMBOL	DESCRIPTION		MIN	MAX	UNITS
F_{ADCLK}	SPI Clock Frequency	8.33			MHz
t_{ADCLK}	SPI Clock Period	120			ns
t_1	RESSAMPLE to ADCLK			91	ns
t_2	RESSAMPLE to ADCONVST			40	ns
t_3	RESSAMPLE to ADMUX0, ADMUX1			64	ns
t_{HADOUT}	ADOUT to ADCLK Setup		19.7		
t_{ADOUTS}	ADOUT to ADCLK Hold		2		ns

Table 19: ADC Specific Timing

PLL Interface Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Consumption	IDDS	Static	-	-	170	uA
Current Consumption	IDD	Dynamic	-	5	-	MA
Peak jitter	Tpj	-	-	-	1000	ps
Cycle jitter	Tcj	-	-500	-	+500	ps
Lock-up Time	Tlock	-	-	-	1	ms
PLL Reset Period	Trst	Recommended operating condition	10	-	-	ns

Table 20: PLL Electrical Characteristics

Appendix A Host Register Map

Register Access

A host computer controls the IRMCK203 using either its slave-mode Full-Duplex SPI port, or a standard RS-232 port. Both interfaces are always active and can be used interchangeably, although not simultaneously. Control/status registers are mapped into a 128-byte address space.

SPI Register Access

When configured as an SPI device read only and read/write operations are performed using the following transfer format:

Command Byte	Data Byte 0	.....	Data Byte N

Data Transfer Format

Bit Position							
7	6	5	4	3	2	1	0
Read Only	Register Map Starting Address						

Command Byte Format

Data transfers begin at the address specified in the command byte and proceed sequentially until the SPI transfer completes. Note that accesses are read/write unless the “read only” bit is set.

RS-232 Register Access

The IRMCK203 includes an RS-232 interface channel that provides a direct connection to the host PC. The software interface combines a basic "register map" control method with a simple communication protocol to accommodate potential communication errors.

RS-232 Register Write Access

A Register write operation consists of a command/address byte, byte count, register data and checksum. When the IRMCK203 receives the register data, it validates the checksum, writes the register data, and transmits and acknowledgement to the host.

Command / Address Byte	Byte Count	1-6 bytes of register data	Checksum

Register Write Operation

Command Acknowledgement Byte	Checksum

Register Write Acknowledgement

Bit Position

7	6	5	4	3	2	1	0
1=Read/ 0=Write	Register Map Starting Address						

Command/Address Byte Format

Bit Position							
7	6	5	4	3	2	1	0
1=Error/ 0=OK	Register Map Starting Address						

Command Acknowledgement Byte Format

The following example shows a command sequence sent from the host to the IRMCK203 requesting a two-byte register write operation:

0x2F	Write operation beginning at offset 0x2F
0x02	Byte count of register data is 2
0x00	Data byte 1
0x04	Data byte 2
0x35	Checksum (sum of preceding bytes, overflow discarded)

A good reply from the IRMCK203 would appear as follows:

0x2F	Write completed OK at offset 0x2F
0x2F	Checksum

An error reply to the command would have the following format:

0xAF	Write at offset 0x2F completed in error
0xAF	Checksum

RS-232 Register Read Access

A register read operation consists of a command/address byte, byte count and checksum. When the IRMCK203 receives the command, it validates the checksum and transmits the register data to the host.

Command / Address Byte	Byte Count	Checksum

Register Read Operation

Command Acknowledgement Byte	Register Data (Byte Count bytes)	Checksum

Register Read Acknowledgement (transfer OK)

Command Acknowledgement Byte	Checksum

Register Read Acknowledgement (error)

The following example shows a command sequence sent from the host to the IRMCK203 requesting four bytes of read register data:

0xA0	Read operation beginning at offset 0x20 (high-order bit selects read operation)
0x04	Requested data byte count is 4
0xA4	Checksum

A good reply from the IRMCK203 might appear as follows:

0x20	Read completed OK at offset 0x20
0x11	Data byte 1
0x22	Data byte 2
0x33	Data byte 3
0x44	Data byte 4
0xCA	Checksum

An error reply to the command would have the following format:

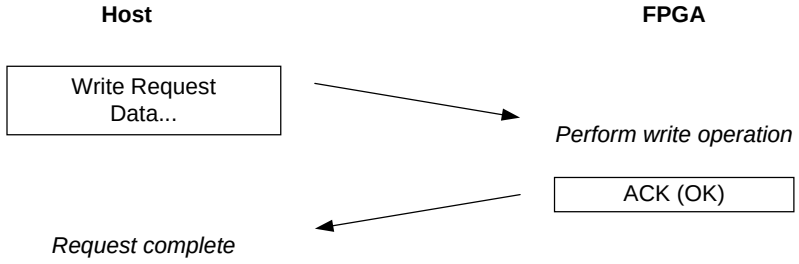
0xA0	Read at offset 0x20 completed in error
0xA0	Checksum

RS-232 Timeout

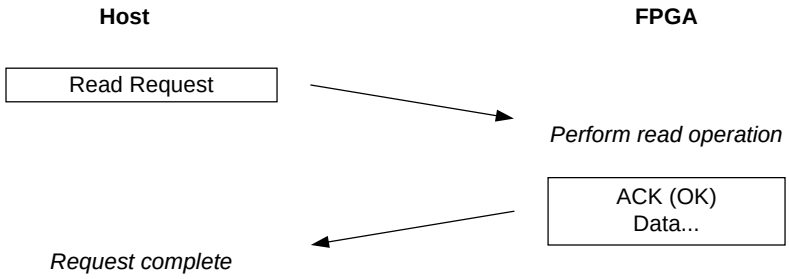
The IRMCK203 receiver includes a timer that automatically terminates transfers from the host to the IRMCK203 after a period of 32 msec.

RS-232 Transfer Examples

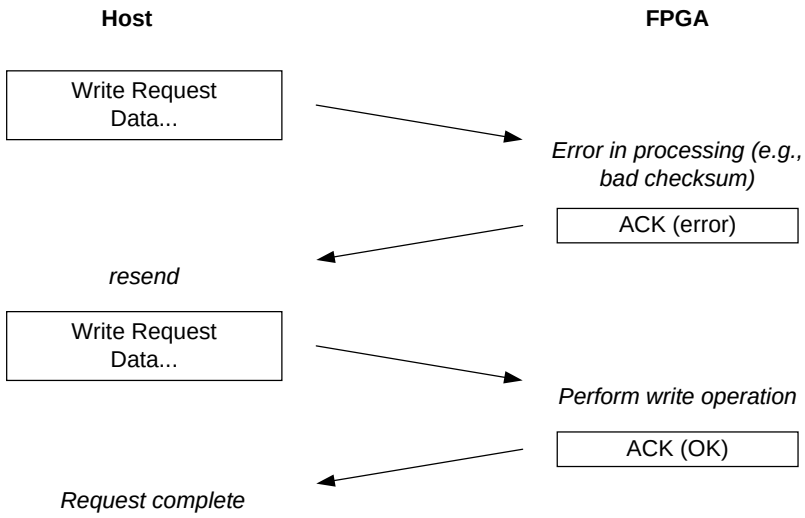
The following example shows a normal exchange executing a register write access.



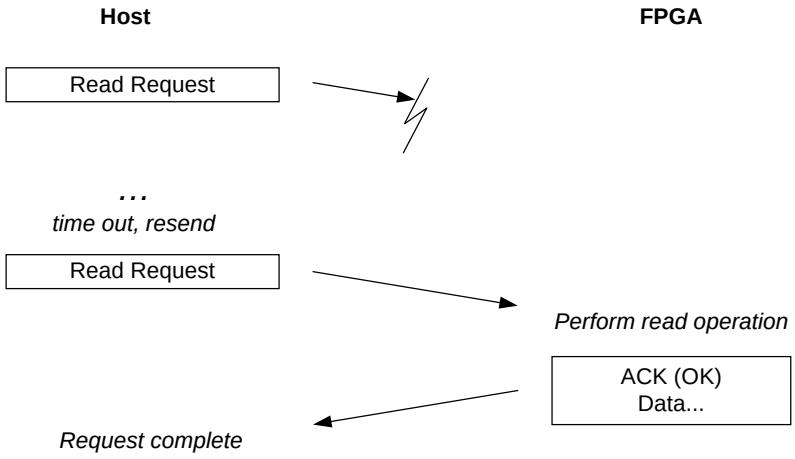
The example below shows a normal register read access exchange.



The following example shows a register write request that is repeated by the host due to a negative acknowledgement from the IRMCK203.



In the final example, the host repeats a register read access request when it receives no response to its first attempt.



Write Register Definitions

PwmConfig Register Group (Write Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0xC	Gatekill Sns (W)	SPARE	Gate SnsL (W)	Gate SnsU (W)	SyncSns	BrakeSns	SPARE	SPARE
0xD	PwmPeriod (LSBs) (W)							
0xE	TwoPhs Pwm (W)	TwoPhs Type (W)	PwmConfig (W)		PwmPeriod (MSBs) (W)			
0xF	PwmDeadTm (W)							
0x44	ModScl (LSBs) (W)							
0x45	ModScl (MSBs) (W)							

PwmConfig Write Register Map

Field Name	Access (R/W)	Field Description
BrakeSns	W	Logic Sense for BRAKE signal output to gate driver IC. 0 = Active low, 1 = active high.
SyncSns	W	Logic Sense for PWM SYNC signal output to microprocessor. 0 = Active low, 1 = active high.
GateSnsU	W	Upper IGBT gate sense. 1 = active high gate control, 0 = active low gate control.
GateSnsL	W	Lower IGBT gate sense. 1 = active high gate control, 0 = active low gate control.
GatekillSns	W	GATEKILL signal sense. 1 = active high GATEKILL, 0 = active low GATEKILL.
PwmPeriod	W	PWM Carrier period. Actual PWM carrier period is 2 * (PwmPeriod + 1) * (System Clock Period).
PwmConfig	W	PWM Configuration. 0 = Asymmetrical center aligned PWM, 1 = Symmetrical Center aligned PWM.
TwoPhsType	W	Used only for two-phase PWM modulation mode: 0 = Type 1 2-phase PWM 1 = Type 2 2-phase PWM
TwoPhsPwm	W	Selects PWM modulation mode: 0 = Enable 3-phase space vector PWM modulation 1 = Enable 2-phase space vector PWM modulation
PwmDeadTm	W	Gate drive dead time in units of system clock cycles (e.g., 30 ns with 33 MHz clock).

Field Name	Access (R/W)	Field Description
ModScl	W	Space vector modulator scale factor. This register, which depends on the PWM carrier frequency, should be set as follows: ModScl = PwmPeriod * sqrt(3) * 4096 / 2355 where PwmPeriod is the value in the PwmConfig write register group's PwmPeriod register.

PwmConfig Write Register Field Definitions

CurrentFeedbackConfig Register Group (Write Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x10	IfbOffsV (LSBs) (W)							
0x11	IfbOffsW (LSBs) (W)				IfbOffsV (MSBs) (W)			
0x12	IfbOffsW (MSBs) (W)							
0x15	IfbkScl (LSB) (W)							
0x16	IfbkScl (MSB) (W)							

CurrentFeedbackConfig Write Register Map

Field Name	Access (R/W)	Field Description
IfbOffsV	W	12-bit signed value for V phase current feedback offset. When the IfbOffsEnb bit in the SystemControl write register group is "0" this value is automatically added to each current measurement in hardware.
IfbOffsW	W	12-bit signed value for W phase current feedback offset. . When the IfbOffsEnb bit in the SystemControl write register group is "0" this value is automatically added to each current measurement in hardware.
IfbkScl	W	Rotating frame Iq component and Id component current feedback scale factor. Constant used to scale current measurements before they are used in the field orientation calculation. This is a 15-bit fixed-point signed number with 10 fractional bits that ranges from –16 to + 16 + 1023 / 1024.

CurrentFeedbackConfig Write Register Field Definitions

SystemControl Register Group (Write Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x17	SPARE	IfbOffs Enb	SPARE			AdcIfb Enb	StartCmd	SPARE

SystemControl Write Register Map

Field Name	Access (R/W)	Field Description
StartCmd	W	Start/Stop bit. Setting this bit to 1 issues a start command. Setting this bit to 0 stops the motor.
AdcIfbEnb	W	A/D Converter IFB Enable. Setting this bit to "1" causes current feedback measurement to be taken from the ADS7818 A/D converter interface.
IfbOffsEnb	W	When IFB PwmEnbW = 1, and FocEnbW = 0, the Current feedback offset is calculated and saved in the CurrentFeedbackOffset read register group. When IfbOffsEnb = 1, the Current feedback offset values in the CurrentFeedbackOffset **Read** registers are applied to each current feedback measurement. When IfbOffsEnb = 0, the Current feedback offset values in the CurrentFeedbackConfig **Write** registers are applied to each current feedback measurement.

SystemControl Write Register Field Definitions

TorqueLoopConfig Register Group (Write Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x1A	KpIreg – Current Loop Proportional Gain (LSBs) (W)							
0x1B	KpIreg – Current Loop Proportional Gain (MSBs) (W)							
0x1C	KxIreg – Current Loop Integral Gain (LSBs) (W)							
0x1D	KxIreg – Current Loop Integral Gain (MSBs) (W)							
0x22	VqLim – Quadrature Current Output Limit (LSBs) (W)							
0x23	VqLim – Quadrature Current Output Limit (MSBs) (W)							
0x26	VdLim – Direct Current Output Limit (LSBs) (W)							

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x27	VdLim – Direct Current Output Limit (MSBs) (W)							

TorqueLoopConfig Write Register Map

Field Name	Access (R/W)	Field Description
KpIreg	W	15-bit signed current loop PI controller proportional gain. Scaled with 14 fractional bits for an effective range of 0 – 1.
KxIreg	W	15-bit signed current loop PI controller integral gain. Scaled with 19 fractional bits for an effective range of 0 - .03125.
VqLim	W	16-bit Quadrature current PI controller voltage output limit.
VdLim	W	16-bit Direct current PI controller voltage output limit.

TorqueLoopConfig Write Register Field Definitions

VelocityControl Register Group (Write Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x32	KpSreg – Velocity loop proportional gain (LSBs) (W)							
0x33	KpSreg – Velocity loop proportional gain (MSBs) (W)							
0x34	KxSreg – Velocity loop integral gain (LSBs) (W)							
0x35	KxSreg – Velocity loop integral gain (MSBs) (W)							
0x36	MotorLim – Velocity loop Output Positive Limit (LSBs) (W)							
0x37	MotorLim – Velocity loop Output Positive Limit (MSBs) (W)							
0x38	RegenLim – – Velocity loop Output Negative Limit (LSBs)							
0x39	RegenLim – – Velocity loop Output Negative Limit (MSBs)							
0x3A	SpdScl – Speed Scale Factor (LSBs)							
0x3B	SpdScl – Speed Scale Factor (MSBs)							
0x3C	TargetSpd – Setpoint/target speed (LSBs)							

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x3D	TargetSpd – Setpoint/target speed (MSBs)							
0x3E	AccelRate							
0x3F	DecelRate							
0x7A	MinSpd							
0x18	StartLim (LSBs)							
0x19	StartLim (MSBs)							

VelocityControl Write Register Map

Field Name	Access (R/W)	Field Description
KpSreg	W	15-bit velocity loop proportional gain, in fixed point with 5 fractional bits. Range = 0 - 512.
KxSreg	W	15-bit velocity loop integral gain, in fixed point with 13 fractional bits. Range = 0 - 2.
MotorLim	W	16-bit speed PI controller output positive limit.
RegenLim	W	16-bit speed PI controller output negative limit (2's complement).
SpdScl	W	Motor Speed Scale factor. Spd value (in the VelocityStatus read register group) is maintained in SPEED units of SpdScl * (Encoder counts / Velocity Loop Execution) or SpdScl * (RATE * Encoder counts / PWM period). The user should set SpdScl = (64 * 16384) * 60 * PWMFREQ / (RATE * Max RPM * Encoder counts/revolution), which will result in a Spd value ranging ±16384 corresponding to ± Max RPM.
TargetSpd	W	Velocity loop speed setpoint in SPEED units, which are determined by the user via the SpdScl register setting.
AccelRate	W	Positive speed rate limit.
DecelRate	W	Negative speed rate limit.
MinSpd	W	Minimum speed protection. This parameter sets the minimum reference speed.
StartLim	W	Drive start-up current limit.

VelocityControl Write Register Field Definitions

FaultControl Register Group (Write Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x42	SPARE						FltClr	DcBusM Enb

FaultControl Write Register Map

Field Name	Access (R/W)	Field Description
DcBusMEnb	W	DC Bus monitor enable. 1 = Monitor DC bus voltage and generate appropriate brake signal control and disable PWM output when voltage fault conditions occur. GatekillFlt and OvrSpdFlt faults cannot be disabled. DC bus voltage thresholds are as follows: Overvoltage – 410V Brake On – 380V Brake Off – 360V Nominal – 310V Undervoltage off – 140V Undervoltage – 120V
FltClr	W	This bit clears all active fault conditions. The user should monitor the FaultStatus read register group to determine fault status and set this bit to "1" to clear any faults that have occurred. A fault condition automatically clears the PwmEnbW and FocEnbW bits in the SystemControl write register group. Note that this bit also directly controls the output 2137 FLTCLR pin. After clearing a fault, the user must explicitly set this bit to "0" to re-enable fault processing.

FaultControl Write Register Field Definitions

SystemConfig Register Group (Write Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x50	ExtCtrl	SpdRef Sel	Ramp Stop	SPARE				

SystemConfig Write Register Map

Field Name	Access (R/W)	Field Description
RampStop	W	Selects the stopping mode: 0 - Configure for Coast stopping 1 - Configure for Ramp stopping

Field Name	Access (R/W)	Field Description
SpdRefSel	W	Selects the source for the Speed PI controller reference input: 0 = Use internal speed reference 1 = Use external speed reference
ExtCtrl	W	Setting this bit to "1" enables direct control of basic motor operation via the external User Interface pins. When this bit is "1", the FocEnbW and PwmEnbW bits in the SystemControl write register group are ignored.

SystemConfig Write Register Field Definitions

EepromControl Registers (Write Registers)

At power up, the write registers can be optionally initialized with values stored in EEPROM. The EepromControl write register group and EepromStatus read register group are used to read and write these EEPROM values. Since the EeAddrW write register (which selects the EEPROM offset to read or write) does not require initialization at power up, the location corresponding to that register in EEPROM (at offset 0x5D) is used to store a register map version code. At power on, the IRMCK203 initializes the write registers from EEPROM only if the version code stored at this offset in EEPROM matches its internal register map version code (which can be read from the RegMapVer field of the EepromStatus read register group).

To enable write register initialization at power up, write the appropriate register map version code to EEPROM at offset 0x5D. To disable write register initialization at power up, write a zero (or any non-matching version code) to offset 0x5D of the EEPROM.

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x5C	SPARE					EeWrite	EeRead	EeRst
0x5D	EeAddrW / RegMapVersCode (W)							
0x5E	EeDataW (W)							

EepromControl Write Register Map

Field Name	Access (R/W)	Field Description
EeRst	W	Self-clearing EEPROM reset. Writing a "1" to this bit resets the I2C EEPROM interface.
EeRead	W	Self-clearing I2c EEPROM Read. Writing a "1" to this bit initiates an EEPROM read from the byte located at EEPROM address EeAddrW. After setting this bit the user should poll the EeBusy bit in the EepromStatus read register group to determine when the read completes and then read the data from EeDataR in the EepromStatus read register group.

Field Name	Access (R/W)	Field Description
EeWrite	W	Self-clearing EEPROM Write. Writing a "1" to this bit initiates an EEPROM write from the data byte in EeDataW to the EEPROM address EeAddrW .
EeAddrW	W	EEPROM Address Register. Contains the address for the next EEPROM read or write operation.
EeDataW	W	EEPROM Data Register. Contains the data for the next EEPROM write operation.

EepromControl Write Register Field Definitions

ClosedLoopAngleEstimator Registers (Write Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x60	IScl (LSBs) (W)							
0x61	IScl (MSBs (W)							
0x62	FlxBInit (LSBs) (W)							
0x63	FlxBInit (MSBs) (W)							
0x6A	PllKp (LSBs) (W)							
0x6B	SPARE		PllKp (MSBs (W)					
0x6C	PllKi (LSBs) (W)							
0x6D	SPARE		PllKi (MSBs (W)					
0x6E	VoltScl (LSBs) (W)							
0x6F	VoltScl (MSBs (W)							
0x70	Rs (LSBs) (W)							
0x71	Rs (MSBs (W)							
0x72	Ld (LSBs) (W)							
0x73	Ld (MSBs (W)							

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x74	AtanTau (LSBs) (W)							
0x75	AtanTau (MSBs (W)							
0x76	FlxTau (LSBs) (W)							
0x77	SPARE			FlxTau (MSBs) (W)				

ClosedLoopAngleEstimator Write Register Map

Field Name	Access (R/W)	Field Description
IScl	W	Current scaler for motor flux calculation.
FlxBInit	W	Initialization value of Beta flux at start.
PllKp	W	Flux phase lock loop proportional gain.
PllKi	W	Flux phase lock loop integral gain.
VoltScl	W	Voltage scaler for motor flux calculation.
Rs	W	Motor per phase resistance including cable (@25C).
Ld	W	Motor per phase inductance.
AtanTau	W	Rotor angle estimator phase compensation gain.
FlxTau	W	Rotor angle estimator flux model time constant.

ClosedLoopAngleEstimator Write Register Field Definitions

OpenLoopAngleEstimator Registers (Write Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x66	KTorque (LSBs) (W)							
0x67	KTorque (MSBs (W)							

OpenLoopAngleEstimator Write Register Map

Field Name	Access (R/W)	Field Description
KTorque	W	Motor mechanical model torque constant.

OpenLoopAngleEstimator Write Register Field Definitions

StartupAngleEstimator Registers (Write Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x64	ParkI (W)							
0x65	DacSel	Zero SpdFlt Disable	Use2xFrq Scale	SPARE	DiagnosticCtrl (W)			
0x68	WeThr (LSBs) (W)							
0x69	WeThr (MSBs (W)							
0x78	ParkTm (W)							

StartupAngleEstimator Write Register Map

Field Name	Access (R/W)	Field Description
ParkI	W	DC current injection level during motor parking (start-up mode).
DiagnosticCtrl	W	1 (0001) – Enable Parking diagnostic 2 (0010) – Enable start-up diagnostic 5 (0101) – Enable current regulator diagnostic 9 (1001) – Enable volts Hertz diagnostic
Use2xFrqScale	W	Selects speed scaling: 0 - Norminal speed scale 1 - Reduce speed feedback scaling by half
ZeroSpdFlt Disable	W	Zero speed fault enable/disable: 0 - Enbale Zero Speed Fault 1 - Disable Zero Speed Fault
DacSel	W	Selects D/A converter diagnostic outputs 0 - 3. A value of 0 selects: Data 0 = Alpha flux Data 1 = Electrical angle Data 2 = Alpha voltage Data 3 = Closed loop/open loop mode (0 = open, 1 = closed) A value of 1 selects: Data 0 = Alpha current Data 1 = Torque current feedback Data 2 = IQ ref Data 3 = Motor speed
WeThr	W	Frequency threshold level (switch over from open-loop to closed-loop mode).
ParkTm	W	Time duration of parking mode.

StartupAngleEstimator Write Register Field Definitions

TraceBufferControl Register Group (Write Registers)

The Trace Buffer Control Register group manages the IRMCK203 diagnostic trace function. The IRMCK203 contains an internal circular trace buffer consisting of 2048 four-byte entries. Each entry consists of two 16-bit items of sampled data: configurable data item "A" and configurable data item "B". Data is read from the trace buffer using the Trace Buffer Status Read Register group.

To use the trace function without the trigger:

1. Write a "1" to the TrcRst bit to reset the trace.
2. Select "A" and "B" data items by writing to the TrcDataASel and TrcDataBSel registers.
3. Specify the number of samples to be collected (1 – 2048) by writing to the PstTrigCnt register.
4. Set TrigEdge to zero.
5. Set the Arm and ForceTrig bits to start collecting data and generate an immediate trigger so collection will stop after PstTrigCnt samples.
6. Read TrcSt (in the TraceBufferStatus read Register group) until its value is 3 (done collecting data).
7. Read TrcDataA and TrcDataB (in the TraceBufferStatus read Register group) 2048 times to retrieve the entire trace buffer. The valid samples are in the last PstTrigCnt buffer entries retrieved. NOTE: To read the data samples properly, you must either read each TrcDataA and TrcDataB together in a single 32-bit operation, or read each TrcDataB first, before reading TrcDataA. This is because the IRMCK203 internal trace buffer pointer increments to the next sample on a read of TrcDataA (LSBs).

To use the trace with trigger:

1. Write a "1" to the TrcRst bit to reset the trace.
2. Select "A" and "B" data items by writing to the TrcDataASel and TrcDataBSel registers. (The trigger is always based on the data "A" item.)
3. Specify the number of samples to be collected after the trigger occurs (1 – 2048) by writing to the PstTrigCnt register.
4. Set TrigLvl to the value of data item "A" at which you want the trigger to occur.
5. Set TrigEdge to 1 or 2 depending on whether you want the trigger to occur on the falling or rising edge of the data item "A" value.
6. Set the Arm bit to start collecting data. (Do not set the ForceTrig bit.)
7. When the trigger occurs, the value of TrcSt (in the TraceBufferStatus Read Register group) changes to 2. Read TrcSt until its value changes to 3 (done collecting data).
8. Read TrcDataA and TrcDataB (in the TraceBufferStatus read Register group) 2048 times to retrieve the entire trace buffer. The oldest samples are retrieved first, so the samples collected after the trigger occurred are in the last PstTrigCnt buffer entries. NOTE: To read the data samples properly, you must either read each TrcDataA and TrcDataB together in a single 32-bit operation, or read each TrcDataB first, before reading TrcDataA. This is because the IRMCK203 internal trace buffer pointer increments to the next sample on a read of TrcDataA (LSBs).

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x2B	SPARE	TrigEdge		SPARE				
0x2C	PstTrigCnt (LSBs)							
0x2D	TrcRst	Arm	ForceTrig	PstTrigCnt (MSBs)				
0x2E	TrcDataBSel				TrcDataASel			
0x2F	TrigLvl (LSBs)							

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x30	TrigLvl (MSBs)							

TraceBufferControl Write Register Map

Field Name	Access (R/W)	Field Description
TrigEdge	W	Trigger edge for threshold level triggering. 0 = Disabled, 1 = Rising edge, 2 = Falling edge.
PstTrigCnt	W	Post Trigger count. Specifies number of samples to collect immediately following a trace trigger occurrence.
ForceTrig	W	Force trace trigger. Setting this self-clearing bit to 1 initiates a trace trigger, which causes data collection to cease immediately after another PstTrigCnt samples.
Arm	W	Trace arm. Setting this self-clearing bit to 1 starts data collection to the circular trace buffer.
TrcRst	W	Trace reset. Setting this self-clearing bit to 1 resets the trace state to Idle.
TrcDataASel, TrcDataBSel	W	Selects data items for display on channels "A" and "B": 1 = DC Bus voltage 2 = V phase current 3 = W phase current 4 = Flx_M 5 = Speed PI reference 6 = Speed PI feedback 7 = Alpha flux 8 = IQ Ref 9 = Q axis voltage Qv 10 = D axis voltage Dv 11 = 12-bit electrical angle 12 = Q axis current Qi 13 = D axis current Di 14 = Alpha current 15 = Beta current
TrigLvl	W	Trigger threshold level. When this field is non-zero, a trace trigger is initiated each time the channel “A” data passes through this value as indicated by the TrigEdge field.

TraceBufferControl Write Register Field Definitions

StartupRetrail Registers (Write Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x79	ParkTmRet							
0x7B	FlxThrL							
0x7C	FlxThrH							
0x7D	RetryTm							
0x7E	NumRetries							
0x7F	ParkIRet							

StartupRetrail Write Register Map

Field Name	Access (R/W)	Field Description
ParkTmRet	W	Start-up failure may be caused by increased shaft friction. After first start-up retry, the parking time can be increased to improve parking performance.
FlxThrL	W	The low flux threshold level for determining a successful startup.
FlxThrH	W	The high flux threshold level for determining start-up failure.
RetryTm	W	This parameter provides the adjustment to the retry sampling instant. The sampling instant starts when Closed_Loop = 1.
NumRetries	W	If start-up fails, the user can program start-up retrial. This parameter determines the number of start-up retries. A value of zero will disable startup retrial. The maximum number of retries is 15.
ParkIRet	W	Start-up failure may be caused by increased shaft friction. After first start-up retry, the parking current can be increased to improve parking performance.

StartupRetrail Write Register Field Definitions

Read Register Definitions

SystemStatus Register Group (Read Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x7	StartStop	FwdRev	SPARE	PwrID		ExtCtrlR	Foc EnbR	Pwm EnbR

SystemStatus Read Register Map

Field Name	Access (R/W)	Field Description
PwmEnbR	R	PWM Enable bit status.
FocEnbR	R	FOC Enable bit status.
ExtCtrlR	R	Reflects the status of the ExtCtrl bit in the System Configuration write register (address 0x50).
PwrID	R	Power ID. 0 = 3 kW, 1 = 2 kW, 2 = 500 W.
FwdRev	R	User Interface “FWD/REV" digital input status. 1 - Forward rotation request 0 - Reverse rotation request
StartStop	R	User Interface “START/STOP" digital input status. 1 - Start 0 - Stop

SystemStatus Read Register Field Definitions

DcBusVoltage Register Group (Read Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0xA	DcBusVolts (LSBs)							
0xB	SPARE			Brake	DcBusVolts (MSBs)			

DcBusVoltage Read Register Map

Field Name	Access (R/W)	Field Description
DcBusVolts	R	DC Bus Voltage. Data range is 0 - 4095, which corresponds to a DC bus voltage between 0 and 500 volts.
Brake	R	Brake signal status. 1 = Brake signal active.

DcBusVoltage Read Register Field Definitions

FocDiagnosticData Register Group (Read Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0xC	IvFbk - V Phase IFB Raw Current (LSBs) (R)							
0xD	IwFbk - W Phase IFB Raw Current (LSBs) (R)				IvFbk - V Phase IFB Raw Current (MSBs) (R)			
0xE	IwFbk - W Phase IFB Raw Current (MSBs) (R)							
0xF	Id – Synchronous Frame Direct Current (LSBs) (R)							
0x10	Id – Synchronous Frame Direct Current (MSBs) (R)							
0x11	Iq – Synchronous Frame Quadrature Current (LSBs) (R)							
0x12	Iq – Synchronous Frame Quadrature Current (MSBs) (R)							
0x13	Ud – Synchronous Frame Direct Voltage (LSBs) (R)							
0x14	Ud – Synchronous Frame Direct Voltage (MSBs) (R)							
0x15	Uq – Synchronous Frame Quadrature Voltage (LSBs) (R)							
0x16	Uq – Synchronous Frame Quadrature Voltage (MSBs) (R)							
0x17	UAlpha – Stationary Frame Alpha Voltage (LSBs) (R)							
0x18	UBeta – Stationary Frame Beta Voltage (LSBs) (R)				UAlpha – Stationary Frame Alpha Voltage (MSBs) (R)			
0x19	UBeta – Stationary Frame Beta Voltage (MSBs) (R)							

FocDiagnosticData Read Register Map

Field Name	Access (R/W)	Field Description
IvFbk, IwFbk	R	Offset-corrected V and W phase raw current from the IR2175 current sensor. Values range from 0 - 4096, where 2048 corresponds to 0 current. The current feedback scale factors IdScl and IqScl in the CurrentFeedbackConfig write register group and the current sense resistor value determine the full scale current value.
Id, Iq	R	Synchronous or rotating frame direct and quadrature current values in 2's complement representation. The full scale current values range from –16384 to 16383.
Ud, Uq	R	Synchronous or rotating frame direct and quadrature voltage values in 2's complement representation. Data ranges are ± VdLim for Ud and ± VqLim for Uq as specified in the TorqueLoopConfig write register group.
UAlpha, UBeta	R	Stationary frame Alpha and Beta voltage output component values. Data range is ± VdLim or ± VqLim (as specified in the TorqueLoopConfig write register group), whichever is larger.

FocDiagnosticData Read Register Field Definitions

FaultStatus Register Group (Read Registers)

The Fault Status register records fault conditions that occur during drive operation. When any of these fault conditions occur, the PWM output is automatically disabled. The user should monitor this register continuously for fault conditions. A fault condition can be cleared by writing a "1" to the FaultClr bit in the FaultControl write register group. (This does not automatically re-enable PWM output.)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x1E	SPARE	RetryFlt	ZeroSpd Flt	ExecTm Flt	OvrSpdFlt	OvFlt	LvFlt	GatekillFlt

FaultStatus Read Register Map

Field Name	Access (R/W)	Field Description
GatekillFlt	R	Filtered and latched version of IR213x FAULT output.
LvFlt	R	DC bus low voltage fault. This fault occurs if the DC bus drops below 120V.
OvFlt	R	DC bus overvoltage fault. This fault occurs if the DC bus voltage exceeds 410V.
OvrSpdFlt	R	Over speed fault. This fault occurs whenever the motor reaches the positive or negative limits. The user should use the scale factor in the SpdScl field of the VelocityControl write register group to scale the motor speed so that it falls between -16384 and +16383 with these limits as the over speed condition.
ExecTmFlt	R	Execution time fault.

Field Name	Access (R/W)	Field Description
ZeroSpdFlt	R	Zero Speed fault. When speed is less than MinSpd/2 (half minimum speed) for a continous period of 2 seconds, the zero speed fault will be set.
RetryFlt	R	Start-up retry fault. After a certain number (determined by parameter NumRetries) of start-up failures, this fault will be set.

FaultStatus Read Register Field Definitions

VelocityStatus Register Group (Read Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x26	Spd (LSBs)							
0x27	Spd (MSBs)							

VelocityStatus Read Register Map

Field Name	Access (R/W)	Field Description
Spd	R	Current motor speed in SPEED units. (See the description of SpdScl in the VelocityControl write register group.)

VelocityStatus Read Register Field Definitions

CurrentFeedbackOffset Register Group (Read Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x30	IfbVOffs (LSBs) (R)							
0x31	IfbWOffs (LSBs) (R)				IfbVOffs (MSBs) (R)			
0x32	IfbWOffs (MSBs) (R)							

CurrentFeedbackOffset Read Register Map

Field Name	Access (R/W)	Field Description
IfbVOffs, IfbWOffs	R	Current feedback offset values from the last IFB Offset calculation. These values are automatically applied to each current feedback measurement value whenever the IfbOffsEnb bit in the SystemControl write register group is set.

CurrentFeedbackOffset Read Register Field Definitions

EepromStatus Registers (Read Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x38	SPARE							EeBusy
0x39	EdDataR (R)							
0x3A	EeAddrR (R)							

EepromStatus Read Register Map

Field Name	Access (R/W)	Field Description
EeBusy	R	I2C EEPROM Interface busy bit. The user should wait for this bit to clear before initiating EEPROM read or write operations.
EeDataR	R	EEPROM Data Register. Contains the data from the last EEPROM read operation. Note that writing to the EeRst field in the EepromControl write register group invalidates this register.
EeAddrR	R	EEPROM Address read register shows the value stored in EEPROM at the offset of the EeAddrW write register (0x5D). Since this address in the EEPROM contains the IRMCK203 register map version, the user can read this field to determine whether or not the write registers were initialized at power on.

EepromStatus Read Register Field Definitions

FOCDiagnosticDataSupplement Register Group (Read Registers)

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x3C	ElecAngR (LSBs) (R)							
0x3D	SPARE				ElecAngR (MSBs) (R)			
0x3E	SpdRef (LSBs) (R)							
0x3F	SpdRef (MSBs) (R)							
0x40	SpdErr (LSBs) (R)							
0x41	SpdErr (MSBs) (R)							
0x42	IqRefR (LSBs) (R)							
0x43	IqRefR (MSBs) (R)							

FOCDiagnosticDataSupplement Read Register Map

Field Name	Access (R/W)	Field Description
ElecAngR	R	Electrical angle.
SpdRef	R	Speed PI controller reference input.
SpdErr	R	Speed PI controller error.
IqRefR	R	Speed PI controller output.

FOCDiagnosticDataSupplement Read Register Field Definitions

TraceBufferStatus Register Group (Read Registers)

The data registers in the TraceBufferStatus Register group access a single entry in the trace buffer. A read of the TrcDataA (LSBs) register causes the internal trace buffer pointer to increment to the next entry. To retrieve all data items for a single trace buffer entry, read the TrcDataA and TrcDataB registers as a single 32-bit access, or read the TrcDataA (LSBs) register last.

See the description of the TraceBufferControl write register group for more information about using the trace function.

Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x1F	SPARE	TrcSt		SPARE				
0x20	TrcDataA (LSBs) (R)							
0x21	TrcDataA (MSBs) (R)							
0x22	TrcDataB (LSBs) (R)							
0x23	TrcDataB (MSBs) (R)							

TraceBufferStatus Read Register Map

Field Name	Access (R/W)	Field Description
TrcSt	R	Trace data collection state. 0 = Idle, 1 = Armed/Collecting, 2 = Triggered, 3 = Done Collecting Data.
TrcDataA	R	Data “A” item from current trace buffer location.
TrcDataB	R	Data “B” item from current trace buffer location.

TraceBufferStatus Read Register Field Definitions

ProductIdentification Registers (Read Registers)

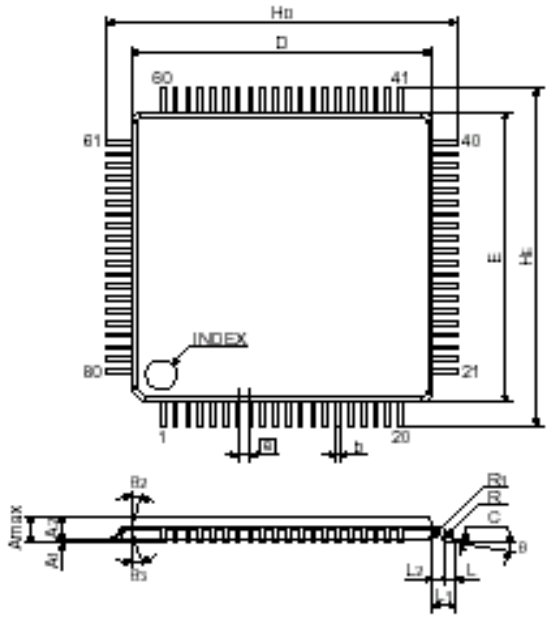
Byte Offset	Bit Position							
	7	6	5	4	3	2	1	0
0x7C	ProductID (R)							
0x7D	RegMapVerID (R)							
0x7E	RevCodeID (LSBs) (R)							
0x7F	RevCodeID (MSBs) (R)							

ProductIdentification Read Register Map

Field Name	Access (R/W)	Field Description
ProductID	R	Product identification code.
RegMapVerID	R	Current register map version code.
RevCodeID	R	IRMCK203 Revision Code. Revision code format is “XX.XX”, where each “X” is a 4-bit hexadecimal number.

ProductIdentification Read Register Field Definitions

Appendix B Package



Lead type STD (TQFP14-80pin STD)

Symbol	Dimension in Millimeters			Dimension in Inches *		
	Min.	Nom.	Max.	Min.	Nom.	Max.
E	11.9	12	12.1	(0.469)	(0.472)	(0.476)
D	11.9	12	12.1	(0.469)	(0.472)	(0.476)
A			1.2			(0.047)
A1		0.1			(0.004)	
A2	0.9	1	1.1	(0.036)	(0.039)	(0.043)
B		0.5			(0.020)	
b	0.11	0.16	0.26	(0.005)	(0.006)	(0.010)
C	0.1	0.125	0.175	(0.004)	(0.005)	(0.006)
θ	0°		8°	(0°)		(8°)
L	0.3	0.5	0.7	(0.012)	(0.020)	(0.027)
L1		1			(0.039)	
L2		0.5			(0.020)	
HE	13.6	14	14.4	(0.536)	(0.551)	(0.566)
HD	13.6	14	14.4	(0.536)	(0.551)	(0.566)
θ2						
θ3						
R						
R1						

* for reference

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