PD - 90639A

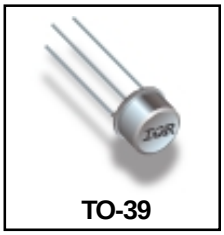
International
IOR Rectifier

REPETITIVE AVALANCHE AND dv/dt RATED
HEXFET® TRANSISTORS THRU-HOLE (TO-39)

IRLF120
100V, N-CHANNEL

Product Summary

Part Number	BVDSS	RDS(on)	ID
IRLF120	100V	0.35Ω	5.3A



TO-39

The Logic Level 'L' series of power MOSFETs are designed to be operated with level logic gate-to-source voltage of 5V. In addition to the well established characterstics of HEXFETs®, they have the added advantage of providing low drive requirements to interface power loads to logic level IC's and microprocessors.

Fields of applications include: high speed power applications such as switching regulators, switching converters, motor drivers, solenoid and relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gatedrive voltage.

The HEXFET technology is the key to International Rectifier's advanced line of logic level power MOSFET transistors. The efficient geometry and unique processing of the HEXFET achieve very low on-state resistance combined with high transconductance and great device ruggedness.

Features:
- Repetitive Avalanche Ratings
- Dynamic dv/dt Rating
- Low Drive Requirements
- Execellent Temperature Stability
- Fast Switching Speeds
- Ease of Paralleling
- Hermetically Sealed
- Light Weight

Absolute Maximum Ratings

	Parameter		Units
I_D @ V_{GS} = 5.0V, T_C = 25°C	Continuous Drain Current	5.3	A
I_D @ V_{GS} = 5.0V, T_C = 100°C	Continuous Drain Current	3.4	
I_{DM}	Pulsed Drain Current ①	21	
P_D @ T_C = 25°C	Max. Power Dissipation	20	W
	Linear Derating Factor	0.16	W/°C
V_{GS}	Gate-to-Source Voltage	±10	V
E_{AS}	Single Pulse Avalanche Energy ②	120	mJ
I_{AR}	Avalanche Current ①	5.3	A
E_{AR}	Repetitive Avalanche Energy ①	2.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.5	V/ns
T_J	Operating Junction	-55 to 150	°C
T_{STG}	Storage Temperature Range		
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)	
	Weight	0.98(typical)	g

For footnotes refer to the last page

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	0.13	—	V/°C	Reference to 25°C, I_D = 250µA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.35	Ω	V_{GS} = 5.0V, I_D = 3.2A ④
		—	—	0.42		V_{GS} = 4.0V, I_D = 2.7A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	3.1	—	—	S (℧)	V_{DS} = 50V, I_{DS} = 3.2A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	µA	V_{DS}= 100V, V_{GS}=0V
		—	—	1000		V_{DS} = 80V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 10V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -10V
Q_g	Total Gate Charge	—	—	13	nC	V_{GS} =5.0V, ID = 5.3A, V_{DS}= 80V
Q_{gs}	Gate-to-Source Charge	—	—	2.4		
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	7.1		
$t_{d(on)}$	Turn-On Delay Time	—	—	13	ns	V_{DD} = 50V, I_D = 5.3A, V_{GS} =5.0V, R_G = 18Ω
t_r	Rise Time	—	—	53		
$t_{d(off)}$	Turn-Off Delay Time	—	—	30		
t_f	Fall Time	—	—	27		
$L_S + L_D$	Total Inductance	—	7.0	—	nH	Measured from drain lead (6mm/ 0.25in. from package) to source lead (6mm/0.25in. from package)
C_{iss}	Input Capacitance	—	480		pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz
C_{oss}	Output Capacitance	—	150	—		
C_{rss}	Reverse Transfer Capacitance	—	30	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	5.3	A	
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	21		
V_{SD}	Diode Forward Voltage	—	—	2.5	V	T_j = 25°C, I_S = 5.3A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	220	nS	T_j = 25°C, I_F = 5.3A, di/dt ≤ 100A/µs
Q_{RR}	Reverse Recovery Charge	—	—	1.1	µC	V_{DD} ≤ 50V ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJC}	Junction-to-Case	—	—	6.25	°C/W	
R_{thJA}	Junction-to-Ambient	—	—	175		Typical socket mount.

Note: Corresponding Spice and Saber models are available on the G&S Website.
For footnotes refer to the last page

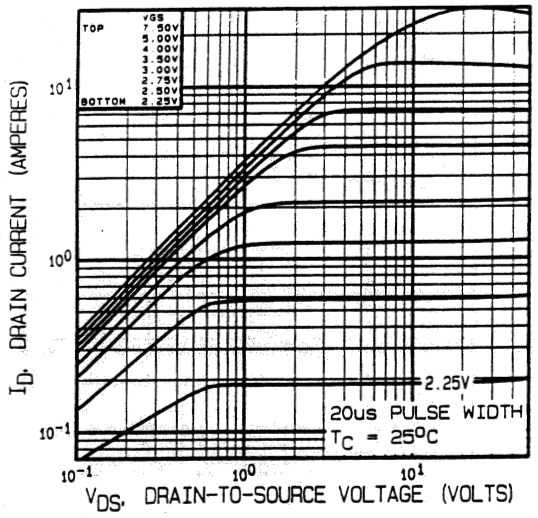


Fig 1. Typical Output Characteristics

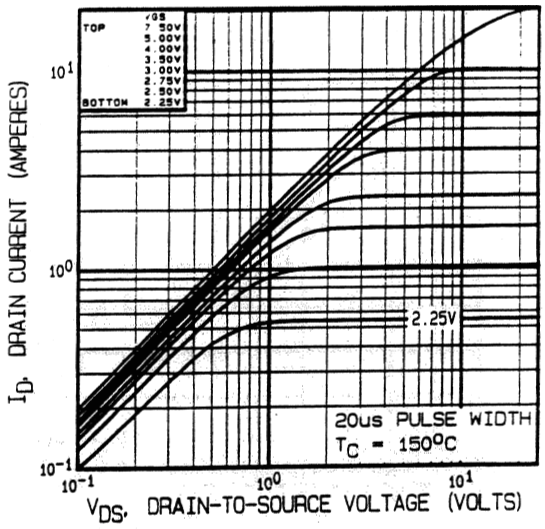


Fig 2. Typical Output Characteristics

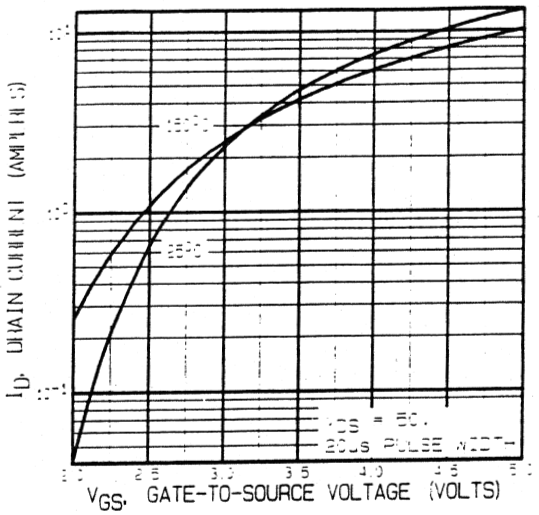


Fig 3. Typical Transfer Characteristics

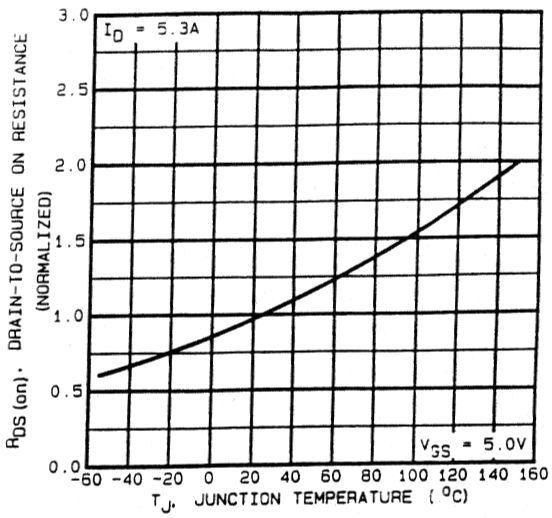


Fig 4. Normalized On-Resistance Vs. Temperature

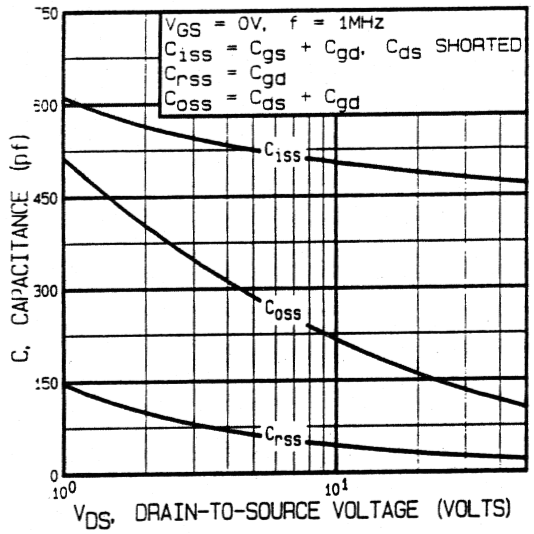


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

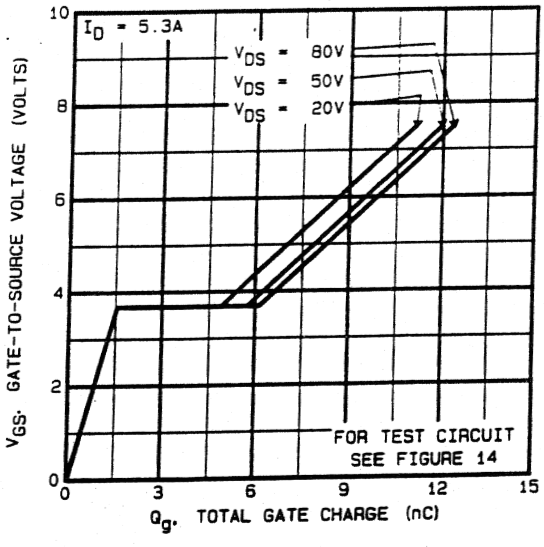


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

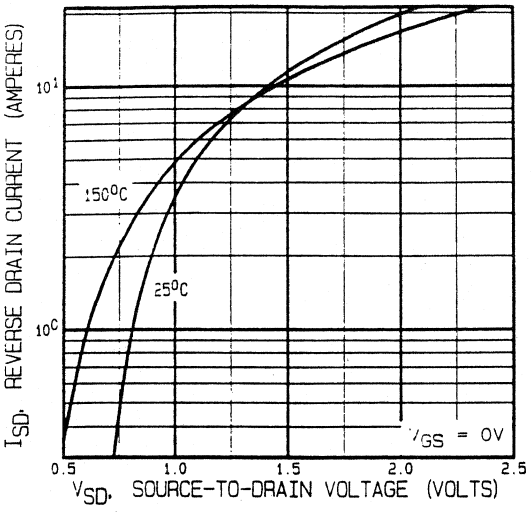


Fig 7. Typical Source-Drain Diode Forward Voltage

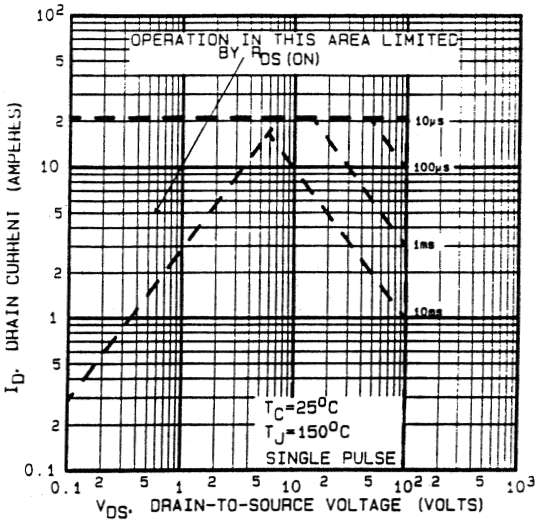


Fig 8. Maximum Safe Operating Area

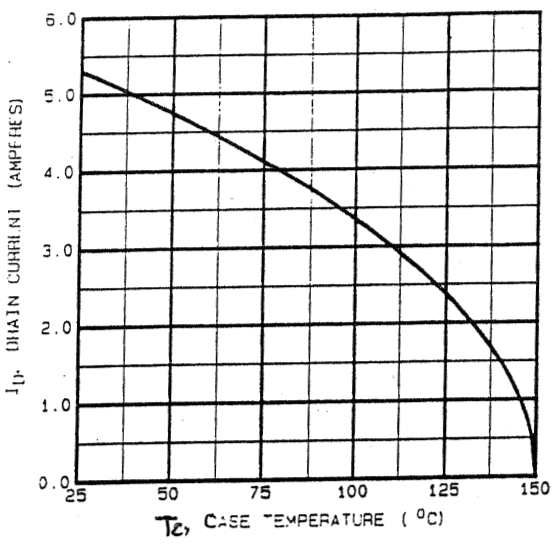


Fig 9. Maximum Drain Current Vs. Case Temperature

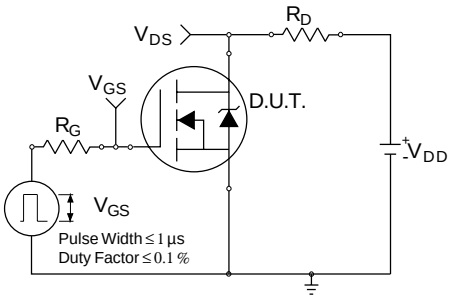


Fig 10a. Switching Time Test Circuit

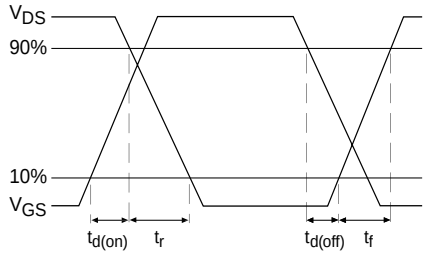


Fig 10b. Switching Time Waveforms

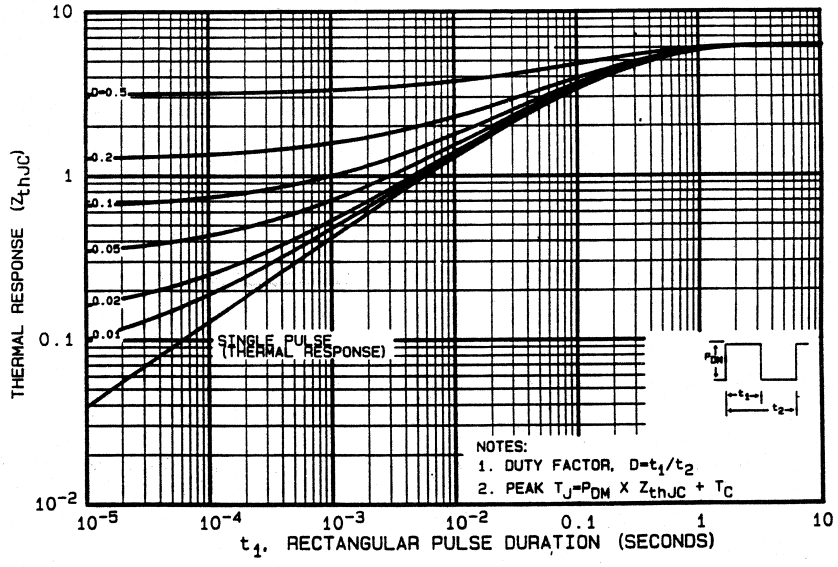


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

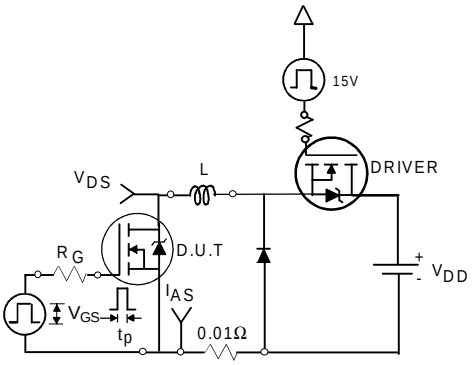


Fig 12a. Unclamped Inductive Test Circuit

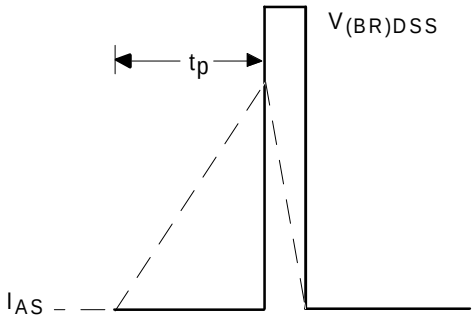


Fig 12b. Unclamped Inductive Waveforms

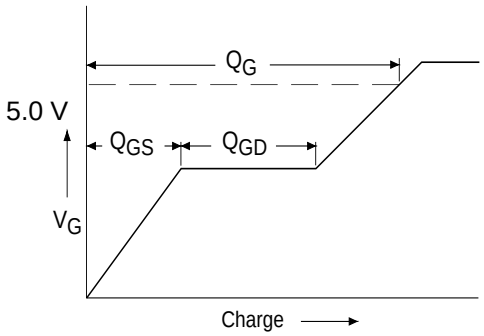


Fig 13a. Basic Gate Charge Waveform

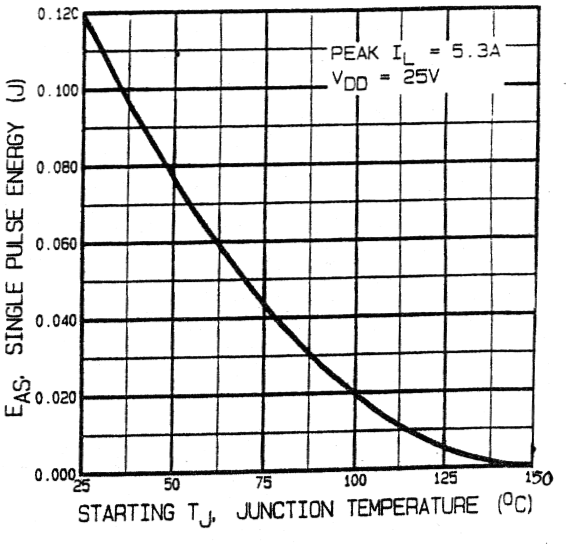


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

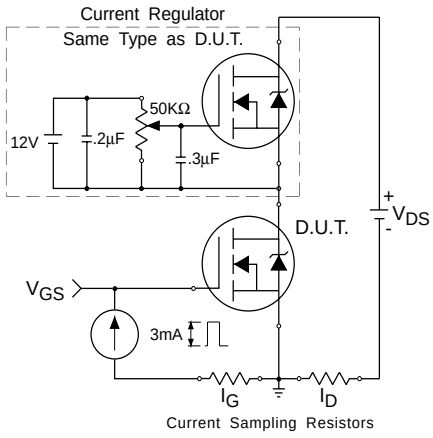


Fig 13b. Gate Charge Test Circuit

Foot Notes:

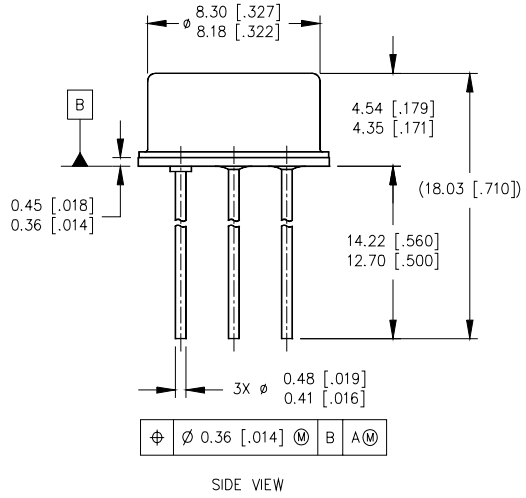
① Repetitive Rating; Pulse width limited by maximum junction temperature.

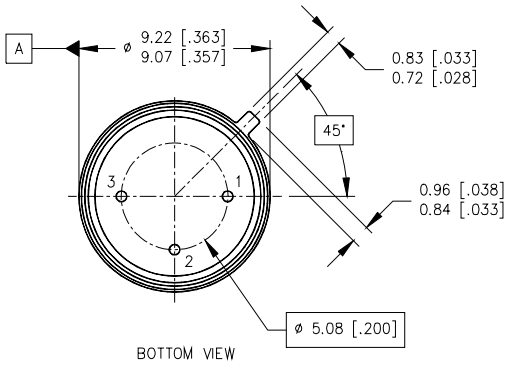
② V_{DD} = 25 V, Starting T_J = 25°C, L= 6.1mH Peak I_{AS} = 5.3A, V_{GS} =5.0V, R_G= 25Ω

③ I_{SD} ≤ 5.3A, di/dt ≤ 110A/μs, V_{DD}≤ 100V, T_J ≤ 150°C Suggested RG =18 Ω

④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

Case Outline and Dimensions —TO-205AF (TO-39)





NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME 14.5M–1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO–205AF (TO–39).

LEGEND

1- SOURCE
2- GATE
3- DRAIN

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