PD - 94052A

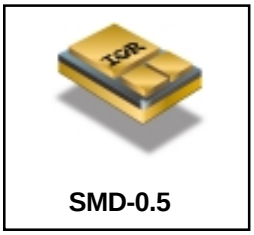
International
IOR Rectifier

# LOGIC LEVEL HEXFET® POWER MOSFET SURFACE MOUNT (SMD-0.5)

# IRL5NJ7404
## 20V, P-CHANNEL

### Product Summary

| Part Number | $BV_{DSS}$ | $R_{DS(on)}$ | $I_D$ |
|---|---|---|---|
| IRL5NJ7404 | -20V | 0.04Ω | -11A |



SMD-0.5

Fifth Generation HEXFET® power MOSFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon unit area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

These devices are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high-energy pulse circuits.

### Features:

- Logic Level Gate Drive
- Low $R_{DS(on)}$
- Avalanche Energy Ratings
- Dynamic dv/dt Rating
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Surface Mount
- Light Weight

## Absolute Maximum Ratings

| | Parameter | | Units |
|---|---|---|---|
| $I_D$ @ $V_{GS}$ = -10V, $T_C$ = 25°C | Continuous Drain Current | -11 | A |
| $I_D$ @ $V_{GS}$ = -10V, $T_C$ = 100°C | Continuous Drain Current | -7.0 | |
| $I_{DM}$ | Pulsed Drain Current ① | -44 | |
| $P_D$ @ $T_C$ = 25°C | Max. Power Dissipation | 50 | W |
| | Linear Derating Factor | 0.4 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ±12 | V |
| $E_{AS}$ | Single Pulse Avalanche Energy ② | 157 | mJ |
| $I_{AR}$ | Avalanche Current ① | -11 | A |
| $E_{AR}$ | Repetitive Avalanche Energy ① | 5.0 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | 0.7 | V/ns |
| $T_J$ | Operating Junction | -55 to 150 | °C |
| $T_{STG}$ | Storage Temperature Range | | |
| | Package Mounting Surface Temperature | 300 (for 5 s) | |
| | Weight | 1.0 (Typical) | g |

For footnotes refer to the last page

## Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

| | Parameter | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-to-Source Breakdown Voltage | -20 | — | — | V | $V_{GS}$ = 0V, $I_D$ = -250µA |
| $\Delta BV_{DSS}/\Delta T_J$ | Temperature Coefficient of Breakdown Voltage | — | 0.14 | — | V/°C | Reference to 25°C, $I_D$ = -1.0mA |
| $R_{DS(on)}$ | Static Drain-to-Source On-State Resistance | — | — | 0.04 | Ω | $V_{GS}$ = -4.5V, $I_D$ = -11A ④ |
| | | — | — | 0.07 | | $V_{GS}$ = -2.7V, $I_D$ = -7.0A |
| $V_{GS(th)}$ | Gate Threshold Voltage | -0.7 | — | — | V | $V_{DS}$ = $V_{GS}$, $I_D$ = -250µA |
| $g_{fs}$ | Forward Transconductance | 9.0 | — | — | S (℧) | $V_{DS}$ = -15V, $I_{DS}$ = -3.2A ④ |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | — | — | -1.0 | µA | $V_{DS}$ = -16V ,$V_{GS}$=0V |
| | | — | — | -25 | | $V_{DS}$ = -16V, $V_{GS}$ = 0V, $T_J$ =125°C |
| $I_{GSS}$ | Gate-to-Source Leakage Forward | — | — | -100 | nA | $V_{GS}$ = -12V |
| $I_{GSS}$ | Gate-to-Source Leakage Reverse | — | — | 100 | | $V_{GS}$ = 12V |
| $Q_g$ | Total Gate Charge | — | — | 50 | nC | $V_{GS}$ =-4.5V, $I_D$ = -3.2A |
| $Q_{gs}$ | Gate-to-Source Charge | — | — | 5.5 | | $V_{DS}$ = -16V |
| $Q_{gd}$ | Gate-to-Drain ('Miller') Charge | — | — | 21 | | |
| $t_{d(on)}$ | Turn-On Delay Time | — | — | 20 | ns | $V_{DD}$ = -10V, $I_D$ = -3.2A, $V_{GS}$ =-4.5V, $R_G$ = 6.0Ω |
| $t_r$ | Rise Time | — | — | 150 | | |
| $t_{d(off)}$ | Turn-Off Delay Time | — | — | 65 | | |
| $t_f$ | Fall Time | — | — | 90 | | |
| $L_S + L_D$ | Total Inductance | — | 4.0 | — | nH | Measured from the center of drain pad to center of source pad |
| $C_{iss}$ | Input Capacitance | — | 1450 | — | pF | $V_{GS}$ = 0V, $V_{DS}$ = -15V f = 1.0MHz |
| $C_{oss}$ | Output Capacitance | — | 830 | — | | |
| $C_{rss}$ | Reverse Transfer Capacitance | — | 430 | — | | |

## Source-Drain Diode Ratings and Characteristics

| | Parameter | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | — | — | -11 | A | |
| $I_{SM}$ | Pulse Source Current (Body Diode) ① | — | — | -44 | | |
| $V_{SD}$ | Diode Forward Voltage | — | — | -1.0 | V | $T_j$ = 25°C, $I_S$ = -3.2A, $V_{GS}$ = 0V ④ |
| $t_{rr}$ | Reverse Recovery Time | — | — | 80 | ns | $T_j$ = 25°C, $I_F$ = -3.2A, di/dt ≤ 100A/µs |
| $Q_{RR}$ | Reverse Recovery Charge | — | — | 100 | nC | $V_{DD}$ ≤ -20V ④ |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S$ + $L_D$. | | | | |

## Thermal Resistance

| | Parameter | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $R_{thJC}$ | Junction-to-Case | — | — | 2.5 | °C/W | |

**Note: Corresponding Spice and Saber models are available on the G&S Website.**

For footnotes refer to the last page

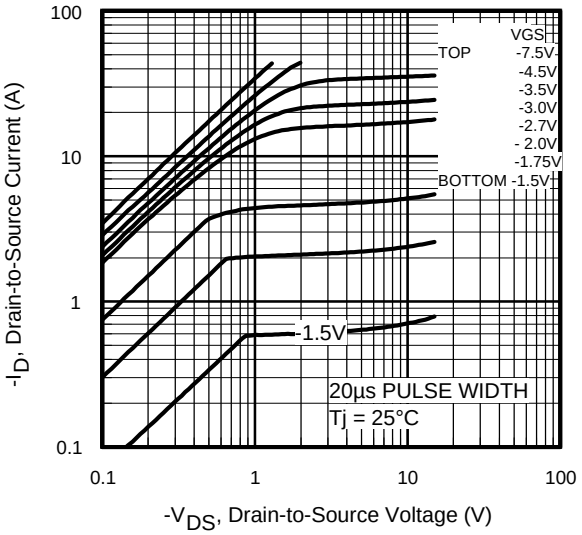



**Fig 1.** Typical Output Characteristics

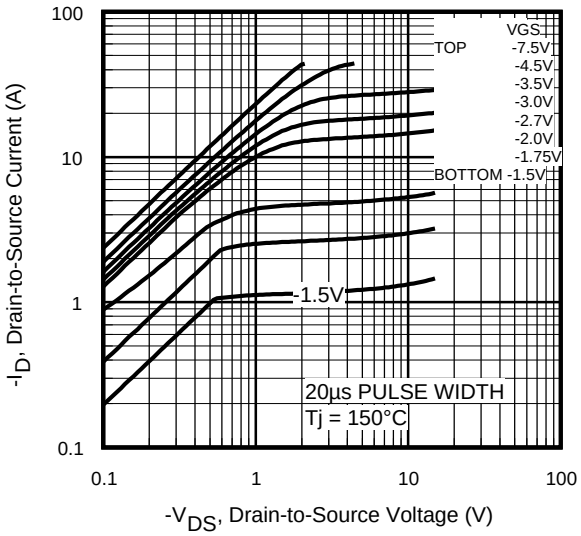



**Fig 2.** Typical Output Characteristics

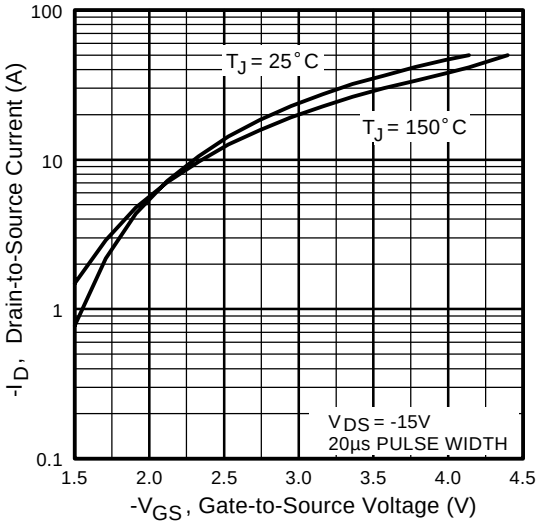



**Fig 3.** Typical Transfer Characteristics

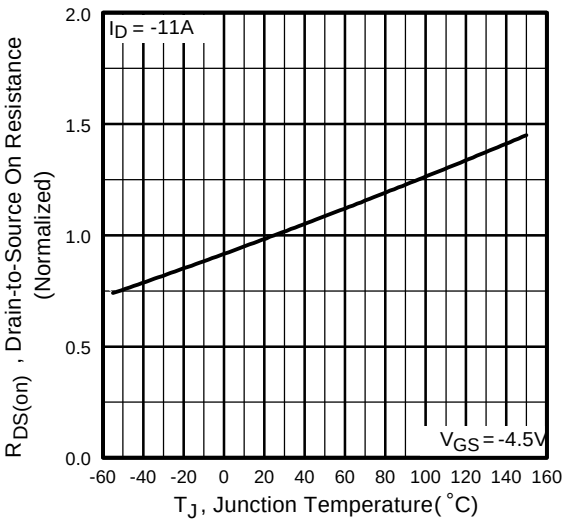



**Fig 4.** Normalized On-Resistance Vs. Temperature

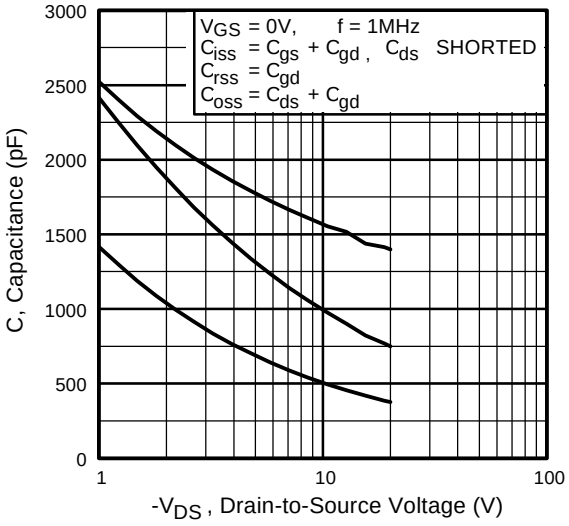



**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

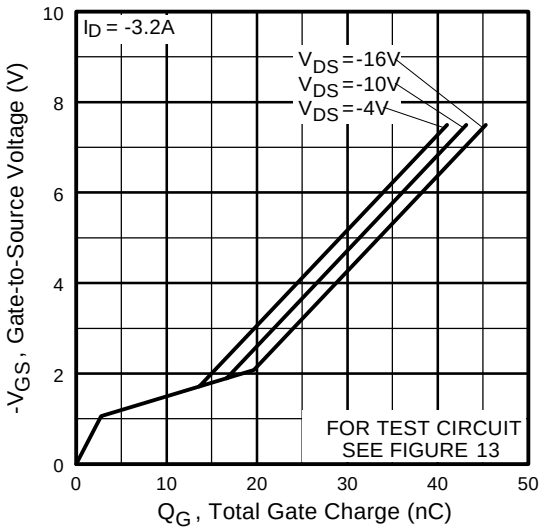



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

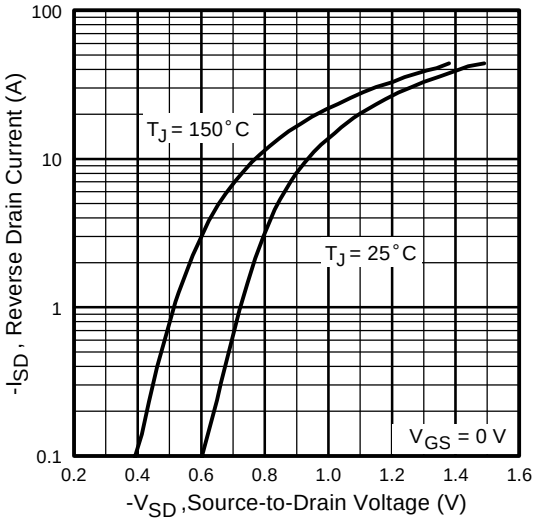



**Fig 7.** Typical Source-Drain Diode Forward Voltage

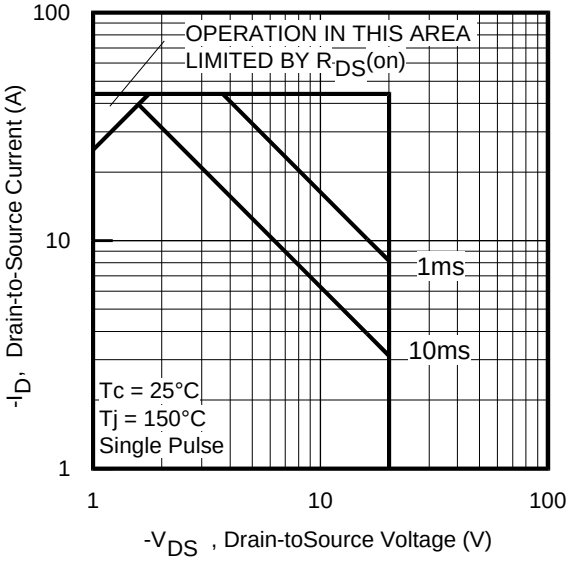



**Fig 8.** Maximum Safe Operating Area

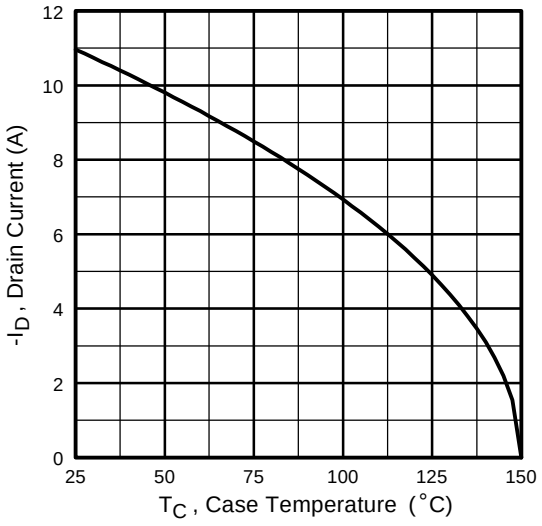



**Fig 9.** Maximum Drain Current Vs. Case Temperature

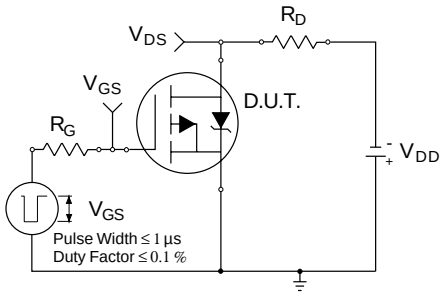



**Fig 10a.** Switching Time Test Circuit

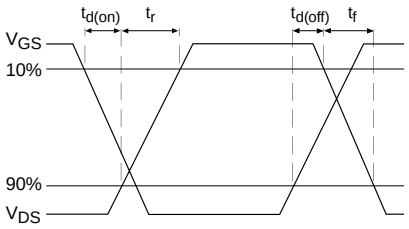



**Fig 10b.** Switching Time Waveforms

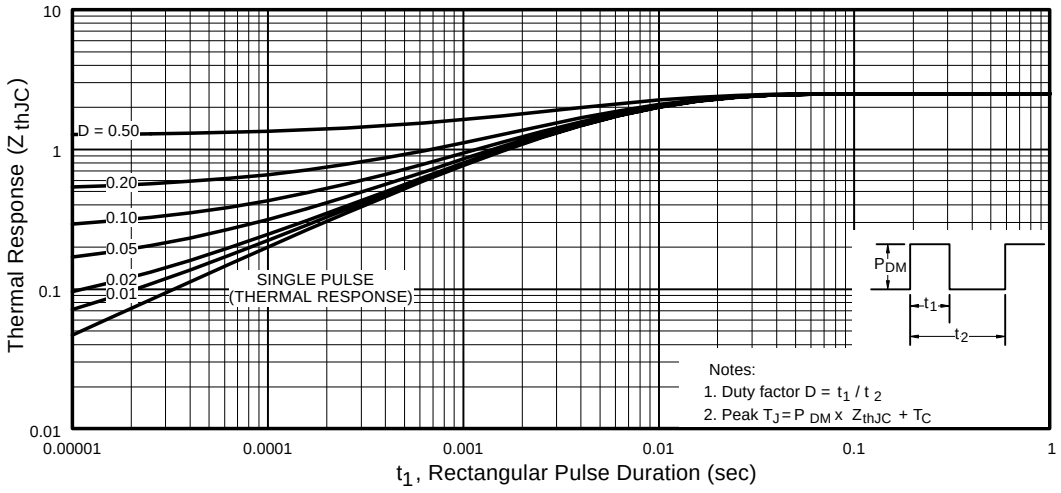



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

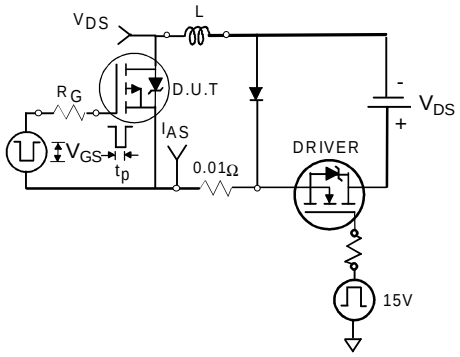



**Fig 12a.** Unclamped Inductive Test Circuit

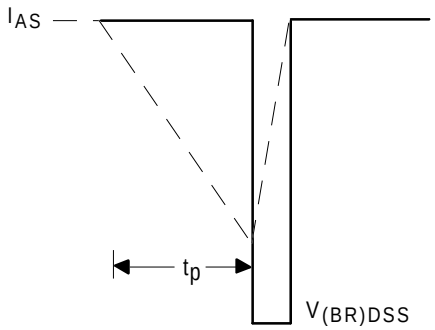



**Fig 12b.** Unclamped Inductive Waveforms

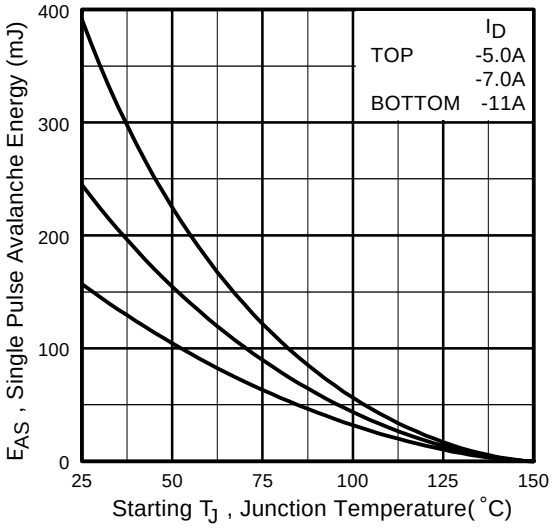



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

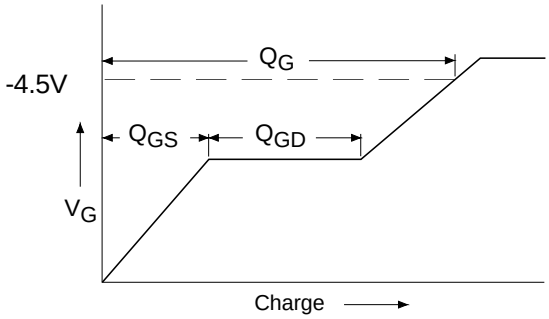



**Fig 13a.** Basic Gate Charge Waveform

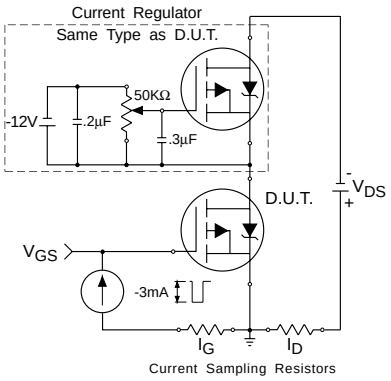
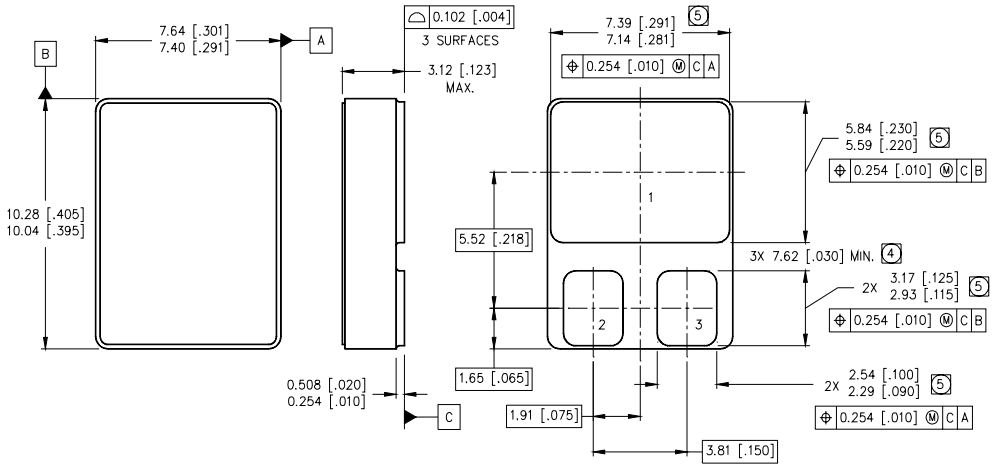



**Fig 13b.** Gate Charge Test Circuit

## Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.
② $V_{DD}$ = -15 V, Starting $T_J$ = 25°C, L= 2.6mH Peak $I_{AS}$ = -11A, $V_{GS}$ =-10V, $R_G$= 25Ω
③ $I_{SD}$ ≤ -11A, di/dt ≤ -84 A/µs, $V_{DD}$ ≤ -20V, $T_J$ ≤ 150°C
④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

## Case Outline and Dimensions — SMD-0.5




NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. DIMENSION INCLUDES METALLIZATION FLASH.
5. DIMENSION DOES NOT INCLUDE METALLIZATION FLASH.

PAD ASSIGNMENTS
1 = DRAIN
2 = GATE
3 = SOURCE

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