International
IOR Rectifier

PD - 91781A

IRHQ6110

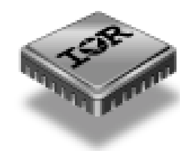
RADIATION HARDENED POWER MOSFET SURFACE MOUNT (LCC-28)

100V, Combination 2N-2P-CHANNEL

RAD-Hard™ HEXFET®
MOSFET TECHNOLOGY

Product Summary

Part Number	Radiation Level	$R_{DS(on)}$	I_D	CHANNEL
IRHQ6110	100K Rads (Si)	0.6Ω	3.0A	N
IRHQ63110	300K Rads (Si)	0.6Ω	3.0A	N
IRHQ6110	100K Rads (Si)	1.1Ω	-2.3A	P
IRHQ63110	300K Rads (Si)	1.1Ω	-2.3A	P



LCC-28

International Rectifier's RAD-Hard™ HEXFET® MOSFET Technology provides high performance power MOSFETs for space applications. This technology has over a decade of proven performance and reliability in satellite applications. These devices have been characterized for both Total Dose and Single Event Effects (SEE). The combination of low $R_{DS(on)}$ and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features:

- Single Event Effect (SEE) Hardened
- Low $R_{DS(on)}$
- Low Total Gate Charge
- Proton Tolerant
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Ceramic Package
- Surface Mount
- Light Weight

Absolute Maximum Ratings

Pre-Irradiation

	Parameter	N-Channel	P-Channel	Units
I_D @ V_{GS} = 12V, T_C = 25°C	Continuous Drain Current	3.0	-2.3	A
I_D @ V_{GS} = 12V, T_C = 100°C	Continuous Drain Current	1.9	-1.5	
I_{DM}	Pulsed Drain Current ①	12	-9.2	
P_D @ T_C = 25°C	Max. Power Dissipation	12	12	W
	Linear Derating Factor	0.1	0.1	W/°C
V_{GS}	Gate-to-Source Voltage	±20	±20	V
E_{AS}	Single Pulse Avalanche Energy	85 ②	75 ⑦	mJ
I_{AR}	Avalanche Current ①	3.0	-2.3	A
E_{AR}	Repetitive Avalanche Energy ①	1.2	1.2	mJ
dv/dt	Peak Diode Recovery dv/dt	3.0 ③	9.0 ⑧	V/ns
T_J T_{STG}	Operating Junction Storage Temperature Range	-55 to 150		°C
	Pckg. Mounting Surface Temp.	300 (for 5s)		
	Weight	0.89 (Typical)		g

For footnotes refer to the last page

7/24/01

Electrical Characteristics For Each N-Channel Device @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	0.11	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.62	Ω	V_{GS} = 12V, I_D = 3.0A ④
		—	—	0.60		V_{GS} = 12V, I_D = 1.9A
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 1.0mA
g_{fs}	Forward Transconductance	1.4	—	—	S (℧)	V_{DS} > 15V, I_{DS} = 1.9A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	25	µA	V_{DS}= 80V, V_{GS}=0V
		—	—	250		V_{DS} = 80V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	17	nC	V_{GS} = 12V, I_D = 3.0A V_{DS} = 50V
Q_{gs}	Gate-to-Source Charge	—	—	4.0		
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	5.5		
$t_{d(on)}$	Turn-On Delay Time	—	—	13	ns	V_{DD} = 50V, I_D = 3.0A, V_{GS} = 12V, R_G = 7.5Ω
t_r	Rise Time	—	—	16		
$t_{d(off)}$	Turn-Off Delay Time	—	—	23		
t_f	Fall Time	—	—	15		
$L_S + L_D$	Total Inductance	—	6.1	—	nH	Measured from the center of drain pad to center of source pad
C_{iss}	Input Capacitance	—	270	—	pF	V_{GS} = 0V, V_{DS} = 25V f = 1.0MHz
C_{oss}	Output Capacitance	—	110	—		
C_{rss}	Reverse Transfer Capacitance	—	23	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	3.0	A	
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	12		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_j = 25°C, I_S = 3.0A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	173	nS	T_j = 25°C, I_F = 3.0A, di/dt ≤ 100A/µs V_{DD} ≤ 25V ④
Q_{RR}	Reverse Recovery Charge	—	—	863	nC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJC}	Junction-to-Case	—	—	10.4	°C/W	

Note: Corresponding Spice and Saber models are available on the G&S Website.
For footnotes refer to the last page

Electrical Characteristics For Each P-Channel Device @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-100	—	—	V	V_{GS} = 0V, I_D = -1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	-0.10	—	V/°C	Reference to 25°C, I_D = -1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	1.1	Ω	V_{GS} = -12V, I_D = -1.5A ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} = V_{GS}$, I_D = -1.0mA
g_{fs}	Forward Transconductance	1.2	—	—	S (℧)	V_{DS} > -15V, I_{DS} = -1.5A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-25	μA	V_{DS}= -80V, V_{GS}=0V
		—	—	-250		V_{DS} = -80V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V_{GS} = -20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	100		V_{GS} = 20V
Q_g	Total Gate Charge	—	—	16	nC	V_{GS} = -12V, I_D = -2.3A
Q_{gs}	Gate-to-Source Charge	—	—	4.3		V_{DS} = -50V
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	3.3		
$t_{d(on)}$	Turn-On Delay Time	—	—	21	ns	V_{DD} = -50V, I_D = -2.3A,
t_r	Rise Time	—	—	17		V_{GS} = -12V, R_G = 7.5Ω
$t_{d(off)}$	Turn-Off Delay Time	—	—	32		
t_f	Fall Time	—	—	32		
$L_S + L_D$	Total Inductance	—	6.1	—	nH	Measured from the center of drain pad to center of source pad
C_{iss}	Input Capacitance	—	285	—	pF	V_{GS} = 0V, V_{DS} = -25V
C_{oss}	Output Capacitance	—	90	—		f = 1.0MHz
C_{rss}	Reverse Transfer Capacitance	—	13	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-2.3	A	
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	-9.2		
V_{SD}	Diode Forward Voltage	—	—	-2.5	V	T_j = 25°C, I_S = -2.3A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	138	nS	T_j = 25°C, I_F = -2.3A, di/dt ≤ 100A/μs
Q_{RR}	Reverse Recovery Charge	—	—	555	nC	V_{DD} ≤ -25V ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJC}	Junction-to-Case	—	—	10.4	°C/W	

For footnotes refer to the last page

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics For Each N-Channel Device @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	100K Rads(Si)[1]		300K to 1000K Rads (Si)[2]		Units	Test Conditions
		Min	Max	Min	Max		
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	100	—	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.0	1.25	4.5		V_{GS} = V_{DS}, I_D = 1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	—	100	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	-100	—	-100		V_{GS} = -20 V
I_{DSS}	Zero Gate Voltage Drain Current	—	25	—	25	µA	V_{DS}= 80V, V_{GS} =0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-39)	—	0.556	—	0.706	Ω	V_{GS} = 12V, I_D = 1.9A
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (LCC-28)	—	0.60	—	0.75	Ω	V_{GS} = 12V, I_D = 1.9A
V_{SD}	Diode Forward Voltage ④	—	1.2	—	1.2	V	V_{GS} = 0V, I_S = 3.0A

1. Part number IRHQ6110
2. Part number IRHQ63110

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Single Event Effect Safe Operating Area

Ion	LET MeV/(mg/cm²))	Energy (MeV)	Range (µm)	V_{DS} (V)				
				@V_{GS}=0V	@V_{GS}=-5V	@V_{GS}=-10V	@V_{GS}=-15V	@V_{GS}=-20V
Cu	28.0	285	43.0	100	100	100	100	70
Br	36.8	305	39.0	100	80	70	50	—
I	59.8	343	32.6	50	40	35	—	—

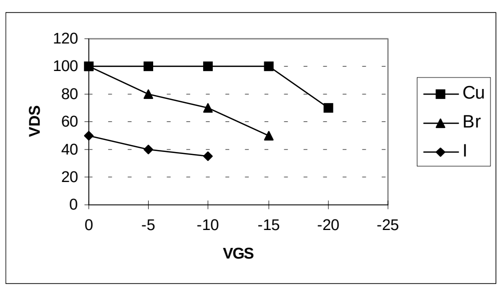


Fig a. Single Event Effect, Safe Operating Area

For footnotes refer to the last page

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics For Each P-Channel Device @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	100K Rads(Si)[1]		300K to 1000K Rads (Si)[2]		Units	Test Conditions
		Min	Max	Min	Max		
BV_{DSS}	Drain-to-Source Breakdown Voltage	-100	—	-100	—	V	V_{GS} = 0V, I_D = -1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	- 2.0	-4.0	- 2.0	-5.0		$V_{GS} = V_{DS}$, I_D = -1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	—	-100	—	-100	nA	V_{GS} = -20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	100	—	100		V_{GS} = 20 V
I_{DSS}	Zero Gate Voltage Drain Current	—	-25	—	25	µA	V_{DS}= -80V, V_{GS} =0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-39)	—	1.056	—	1.056	Ω	V_{GS} = -12V, I_D = -1.5A
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (LCC-28)	—	1.1	—	1.1	Ω	V_{GS} = -12V, I_D = -1.5A
V_{SD}	Diode Forward Voltage ④	—	-2.5	—	-2.5	V	V_{GS} = 0V, I_S = -2.3A

1. Part numbers IRHQ6110
2. Part number IRHQ63110

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Single Event Effect Safe Operating Area

Ion	LET MeV/(mg/cm²))	Energy (MeV)	Range (µm)	V_{DS} (V) @V_{GS}=0V	@V_{GS}=5V	@V_{GS}=10V	@V_{GS}=15V	@V_{GS}=20V
Cu	28.0	285	43.0	-100	-100	-100	-70	-60
Br	36.8	305	39.0	-100	-100	-70	- 50	-40
I	59.8	343	32.6	-60	—	—	—	—

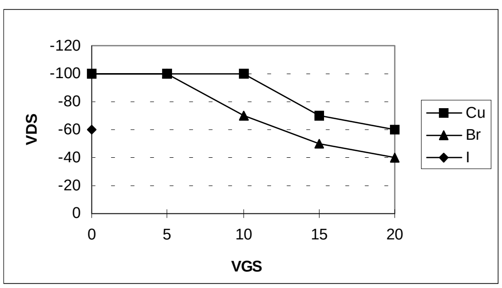


Fig a. Single Event Effect, Safe Operating Area

For footnotes refer to the last page

N-Channel
Q1,Q4

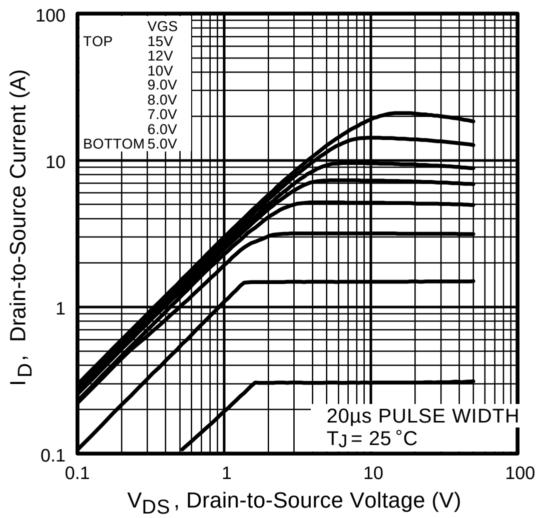


Fig 1. Typical Output Characteristics

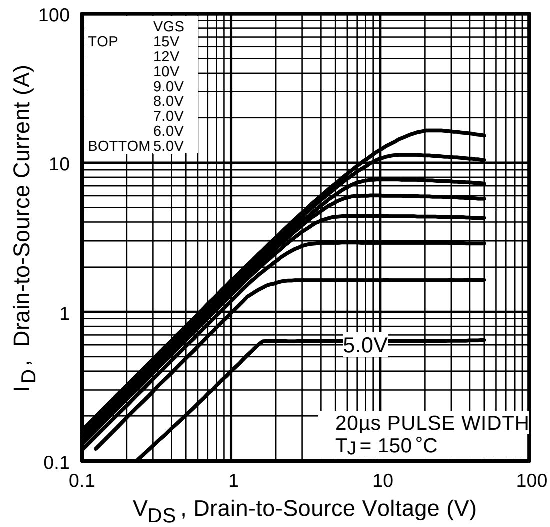


Fig 2. Typical Output Characteristics

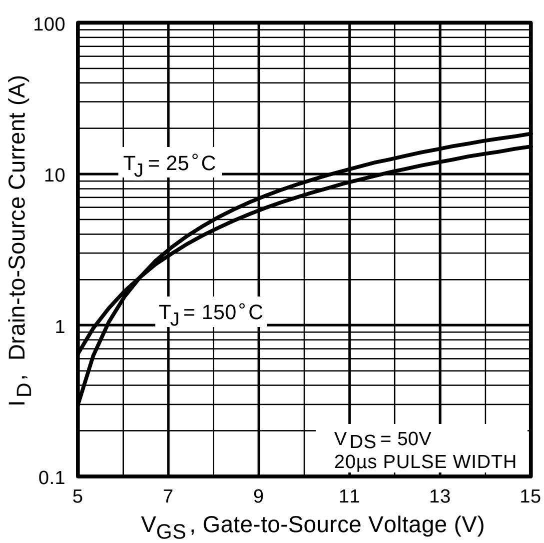


Fig 3. Typical Transfer Characteristics

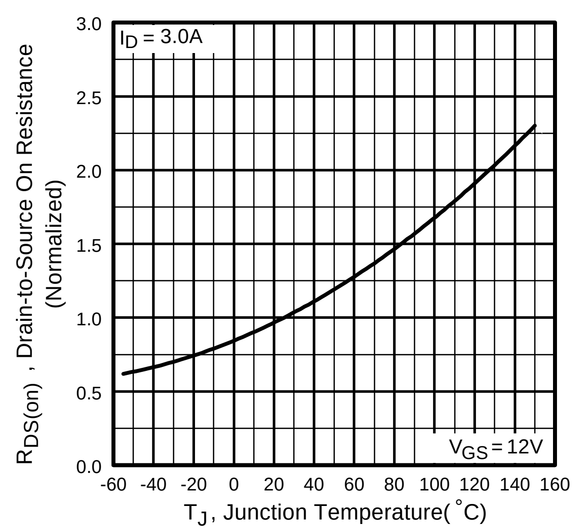


Fig 4. Normalized On-Resistance Vs. Temperature

N-Channel
Q1,Q4

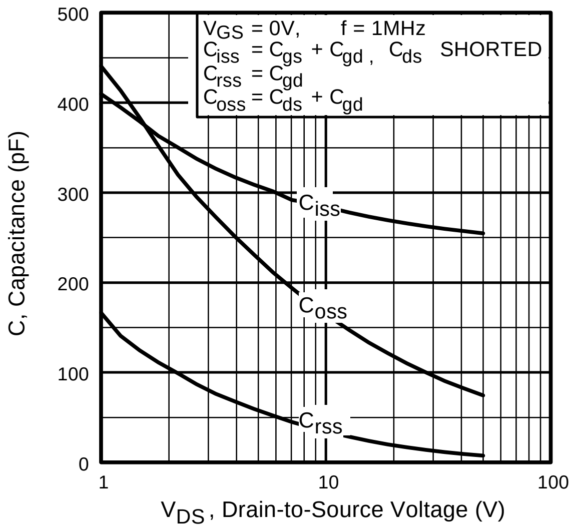


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

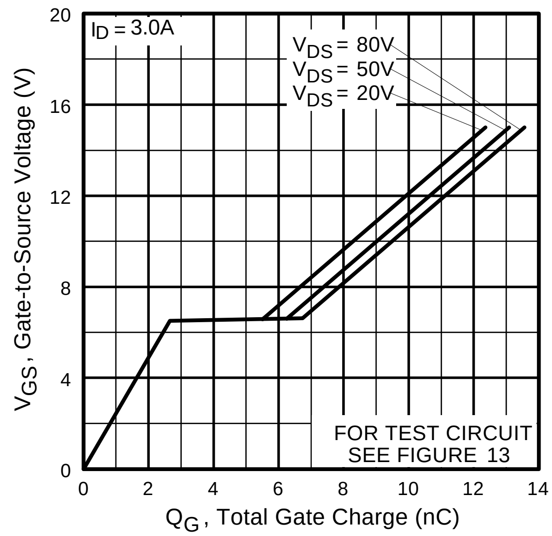


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

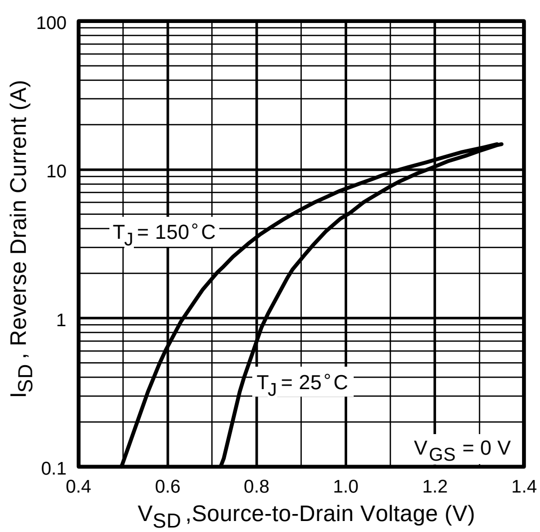


Fig 7. Typical Source-Drain Diode Forward Voltage

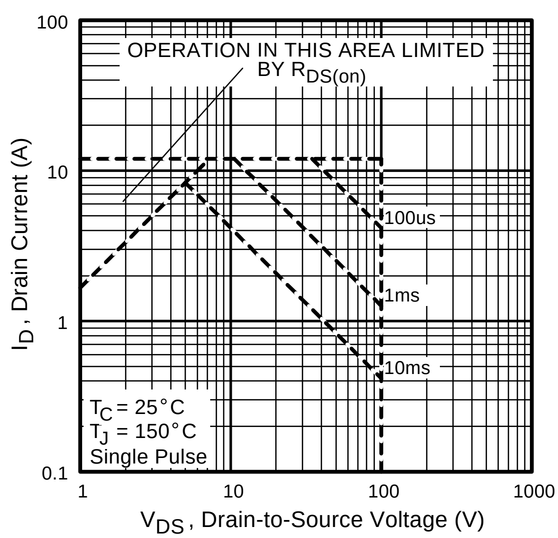


Fig 8. Maximum Safe Operating Area

N-Channel
Q1,Q4

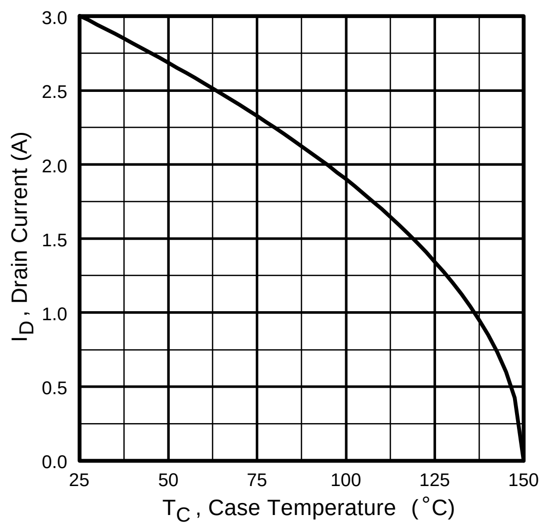


Fig 9. Maximum Drain Current Vs. Case Temperature

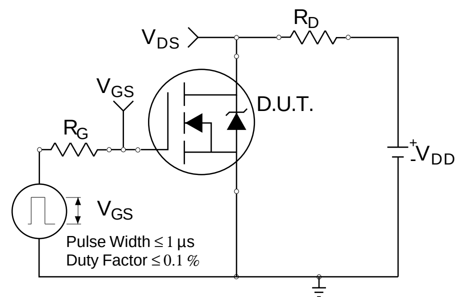


Fig 10a. Switching Time Test Circuit

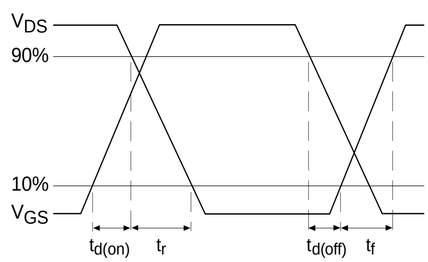


Fig 10b. Switching Time Waveforms

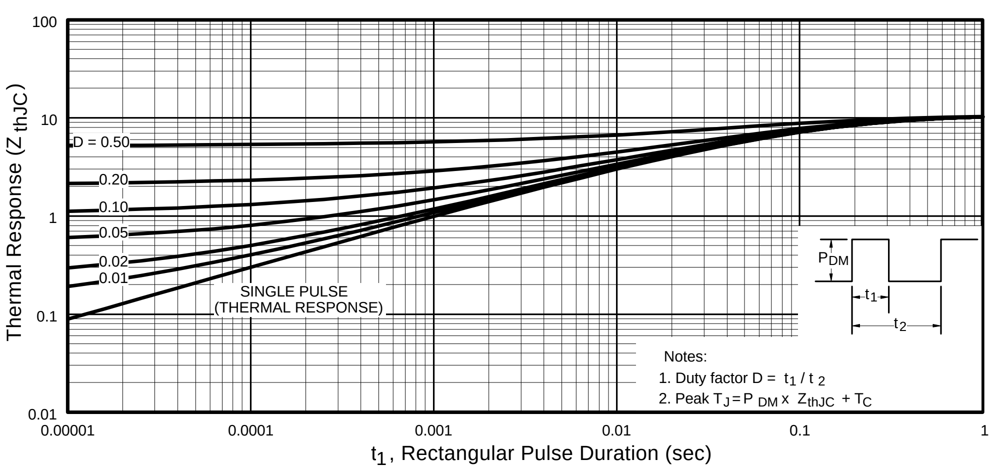


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

N-Channel
Q1,Q4

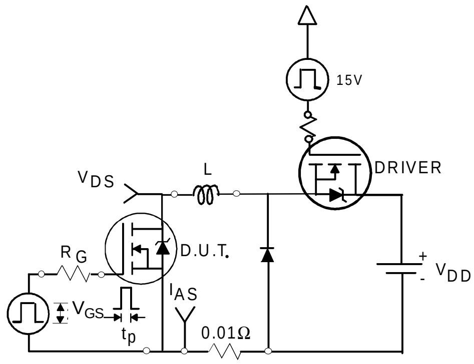


Fig 12a. Unclamped Inductive Test Circuit

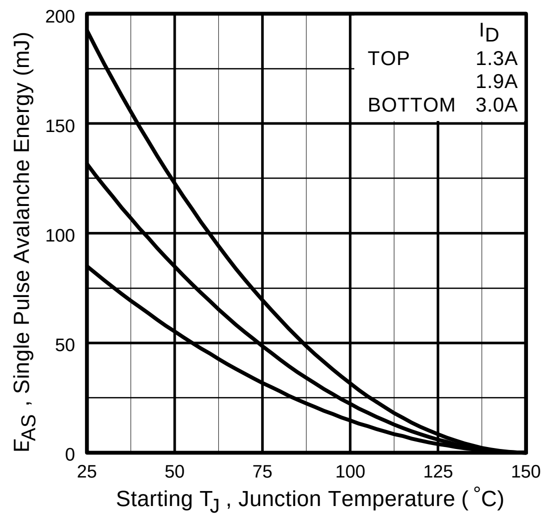


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

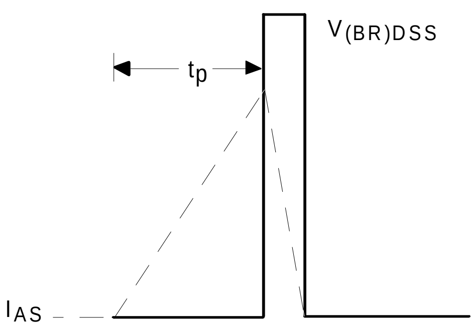


Fig 12b. Unclamped Inductive Waveforms

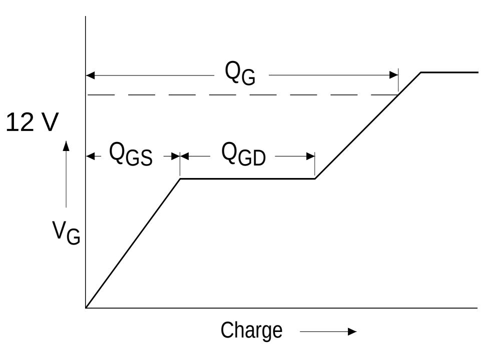


Fig 13a. Basic Gate Charge Waveform

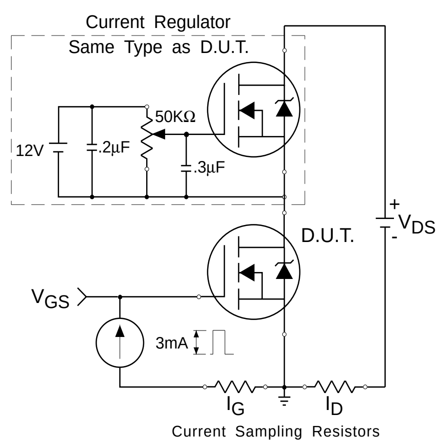


Fig 13b. Gate Charge Test Circuit

P-Channel
Q2,Q3

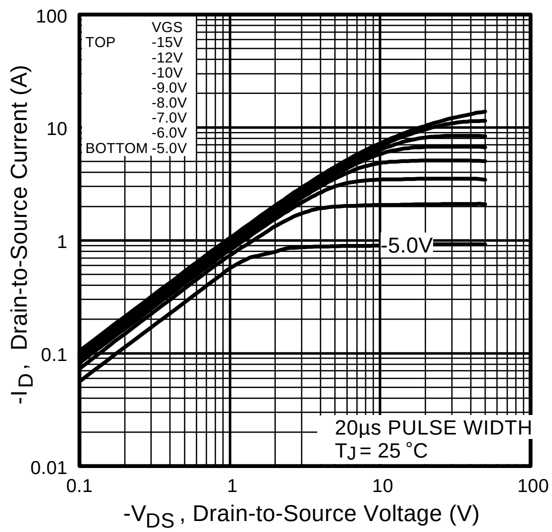


Fig 1. Typical Output Characteristics

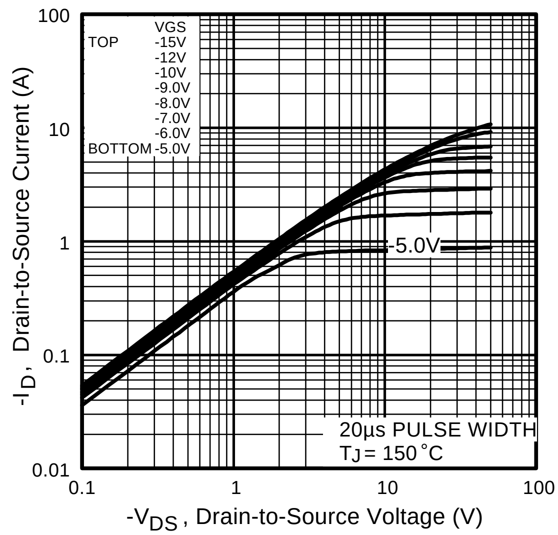


Fig 2. Typical Output Characteristics

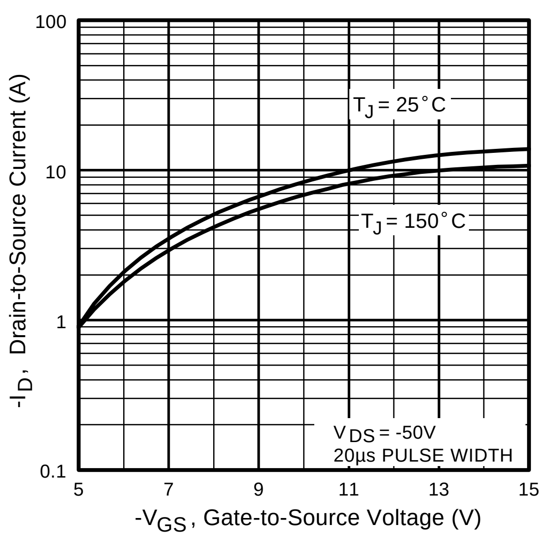


Fig 3. Typical Transfer Characteristics

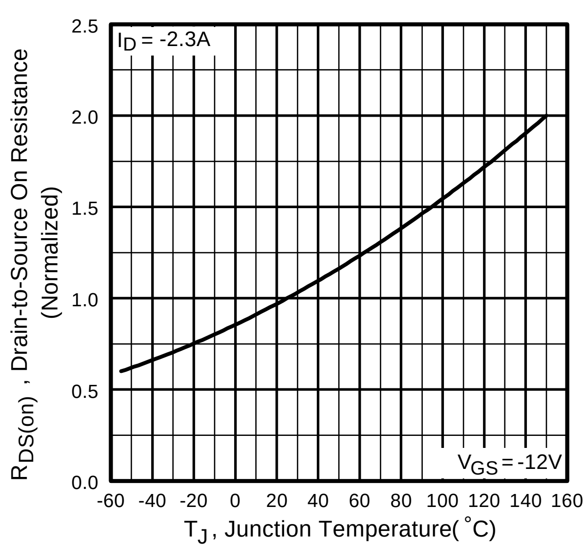


Fig 4. Normalized On-Resistance Vs. Temperature

P-Channel
Q2,Q3

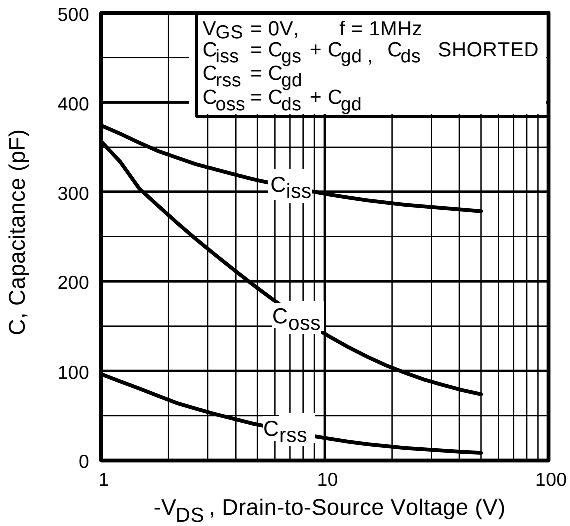


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

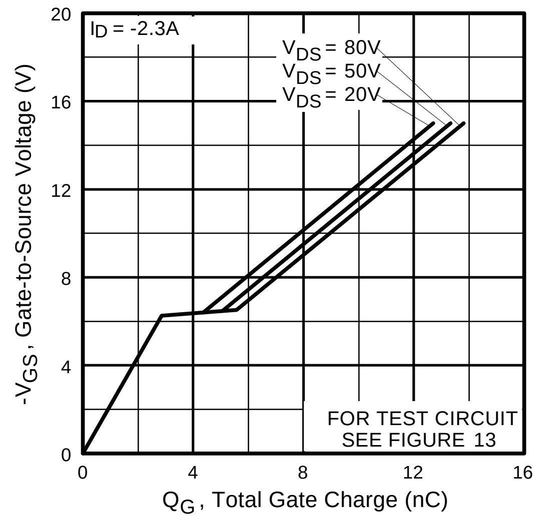


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

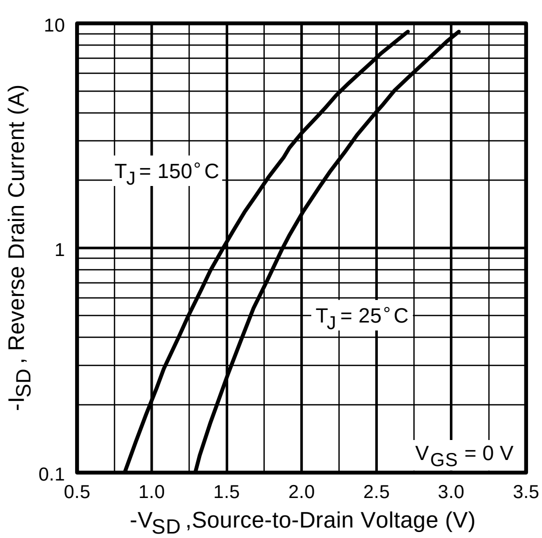


Fig 7. Typical Source-Drain Diode Forward Voltage

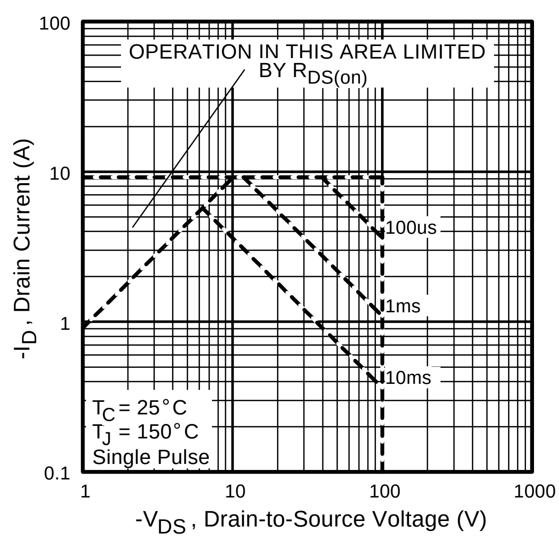


Fig 8. Maximum Safe Operating Area

P-Channel
Q2,Q3

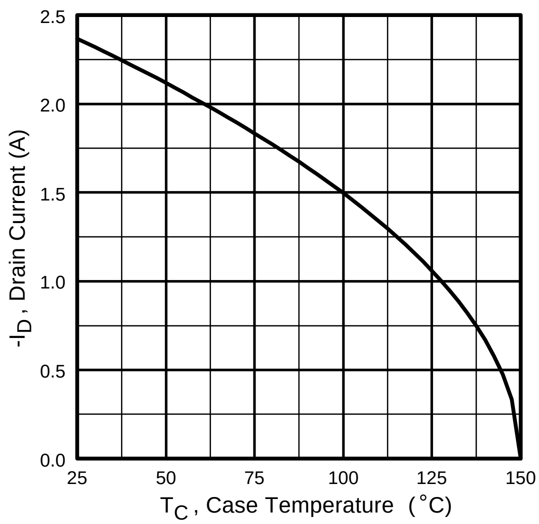


Fig 9. Maximum Drain Current Vs. Case Temperature

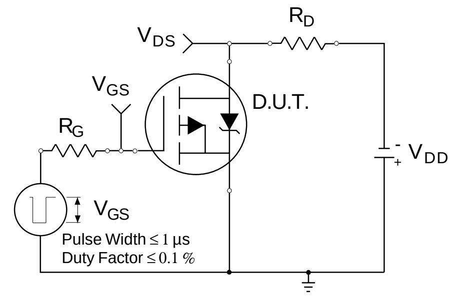


Fig 10a. Switching Time Test Circuit

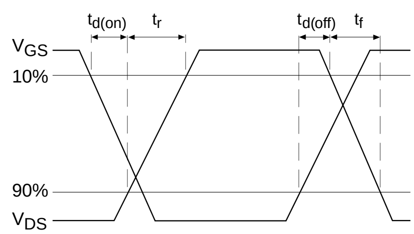


Fig 10b. Switching Time Waveforms

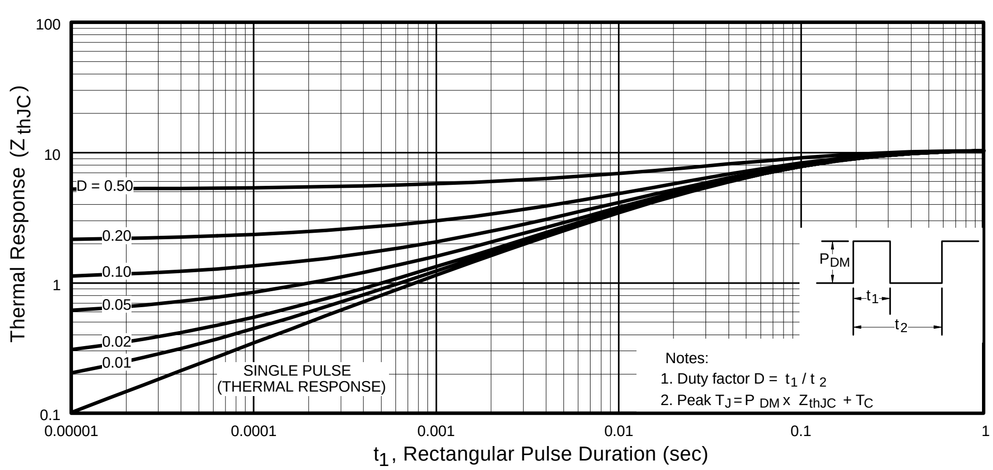


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

P-Channel
Q2,Q3

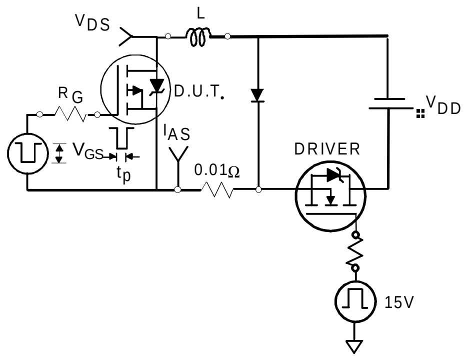


Fig 12a. Unclamped Inductive Test Circuit

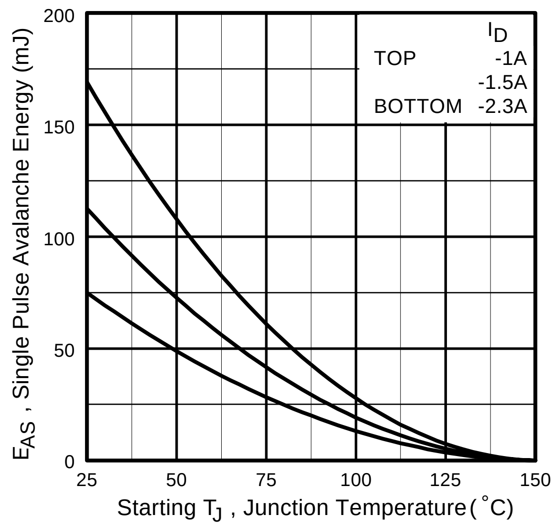


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

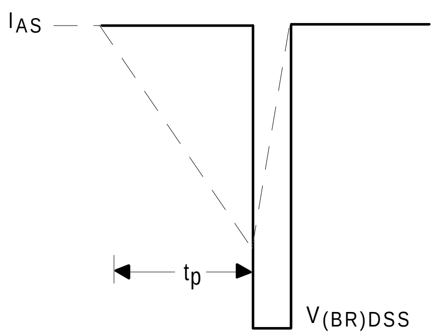


Fig 12b. Unclamped Inductive Waveforms

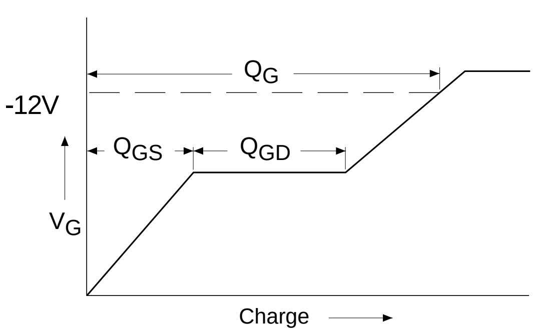


Fig 13a. Basic Gate Charge Waveform

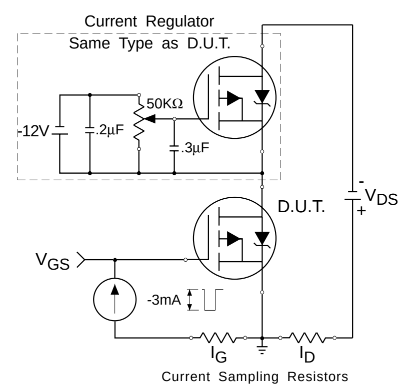


Fig 13b. Gate Charge Test Circuit

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = 25V, starting T_J = 25°C, L= 18.7mH, Peak I_L = 3.0A, V_{GS} = 12V

③ $I_{SD} \leq$ 3.0A, di/dt $\leq$ 165A/µs, $V_{DD} \leq$ 100V, $T_J \leq$ 150°C

④ Pulse width $\leq$ 300 µs; Duty Cycle $\leq$ 2%

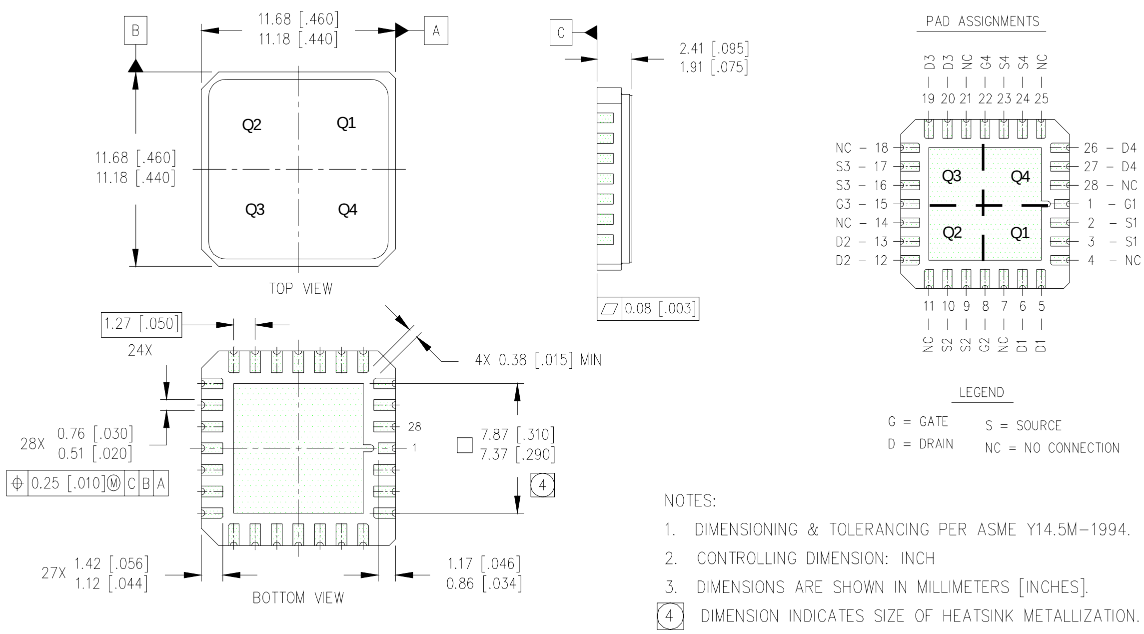
⑤ **Total Dose Irradiation with V_{GS} Bias.** 12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, method 1019, condition A

⑥ **Total Dose Irradiation with V_{DS} Bias.** 80 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, method 1019, condition A

⑦ V_{DD} = - 25V, starting T_J = 25°C, L= 28.4mH, Peak I_L = - 2.3A, V_{GS} = -12V

⑧ $I_{SD} \leq$ - 2.3A, di/dt $\leq$ - 244A/µs, $V_{DD} \leq$ -100V, $T_J \leq$ 150°C

Case Outline and Dimensions — LCC-28



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