

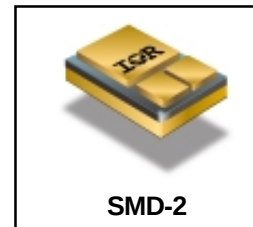
**RADIATION HARDENED
POWER MOSFET
SURFACE MOUNT (SMD-2)**

IRHNA57264SE
250V, N-CHANNEL
R₅ TECHNOLOGY

Product Summary

Part Number	Radiation Level	R _{DS(on)}	I _D
IRHNA57264SE	100K Rads (Si)	0.06Ω	49A

International Rectifier's R₅TM technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80 (MeV/(mg/cm²)). The combination of low R_{DS(on)} and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.



SMD-2

Features:

- Single Event Effect (SEE) Hardened
- Ultra Low R_{DS(on)}
- Low Total Gate Charge
- Proton Tolerant
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Surface Mount
- Ceramic Package
- Light Weight

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
I _D @ V _{GS} = 12V, T _C = 25°C	Continuous Drain Current	49	A
I _D @ V _{GS} = 12V, T _C = 100°C	Continuous Drain Current	31	
I _{DM}	Pulsed Drain Current ①	196	
P _D @ T _C = 25°C	Max. Power Dissipation	300	W
	Linear Derating Factor	2.4	W/°C
V _{GS}	Gate-to-Source Voltage	±20	V
E _{AS}	Single Pulse Avalanche Energy ②	222	mJ
I _{AR}	Avalanche Current ①	49	A
E _{AR}	Repetitive Avalanche Energy ①	30	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T _J	Operating Junction	-55 to 150	°C
T _{STG}	Storage Temperature Range		
	Pckg. Mounting Surface Temp.	300 (for 5s)	
	Weight	3.3 (Typical)	g

For footnotes refer to the last page

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	250	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔBV _{DSS} /ΔT _J	Temperature Coefficient of Breakdown Voltage	—	0.28	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	0.06	Ω	V _{GS} = 12V, I _D = 31A ④
V _{GS(th)}	Gate Threshold Voltage	2.5	—	4.5	V	V _{DS} = V _{GS} , I _D = 1.0mA
g _{fs}	Forward Transconductance	27	—	—	S (r)	V _{DS} > 15V, I _{DS} = 31A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	10	μA	V _{DS} = 200V, V _{GS} = 0V
		—	—	25		V _{DS} = 200V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Q _g	Total Gate Charge	—	—	165	nC	V _{GS} = 12V, I _D = 49A V _{DS} = 125V
Q _{gs}	Gate-to-Source Charge	—	—	45		
Q _{gd}	Gate-to-Drain ('Miller') Charge	—	—	75		
t _{d(on)}	Turn-On Delay Time	—	—	40	ns	V _{DD} = 125V, I _D = 49A, R _G = 2.35Ω
t _r	Rise Time	—	—	125		
t _{d(off)}	Turn-Off Delay Time	—	—	80		
t _f	Fall Time	—	—	65		
L _S + L _D	Total Inductance	—	4.0	—	nH	Measured from the center of drain pad to center of source pad
C _{iss}	Input Capacitance	—	5045	—	pF	V _{GS} = 0V, V _{DS} = 25V f = 1.0MHz
C _{oss}	Output Capacitance	—	781	—		
C _{rss}	Reverse Transfer Capacitance	—	70	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	49	A	
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	196		
V _{SD}	Diode Forward Voltage	—	—	1.2	V	T _J = 25°C, I _S = 49A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	560	nS	T _J = 25°C, I _F = 49A, di/dt ≤ 100A/μs V _{DD} ≤ 25V ④
Q _{RR}	Reverse Recovery Charge	—	—	8.6	μC	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction-to-Case	—	—	0.42	°C/W	
R _{thJ-PCB}	Junction-to-PC board	—	1.6	—		soldered to a 2" square copper-clad board

Note: Corresponding Spice and Saber models are available on the G&S Website.

For footnotes refer to the last page

Radiation Characteristics

IRHNA57264SE

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	100K Rads (Si)		Units	Test Conditions ③
		Min	Max		
BV _{DSS}	Drain-to-Source Breakdown Voltage	250	—	V	V _{GS} = 0V, I _D = 1.0mA
V _{GS(th)}	Gate Threshold Voltage	2.0	4.5		V _{GS} = V _{DSS} , I _D = 1.0mA
I _{GSS}	Gate-to-Source Leakage Forward	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	-100		V _{GS} = -20V
I _{DSS}	Zero Gate Voltage Drain Current	—	10	μA	V _{DSS} =160V, V _{GS} =0V
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	0.061	Ω	V _{GS} = 12V, I _D = 31A
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (SMD-2)	—	0.060	Ω	V _{GS} = 12V, I _D = 31A
V _{SD}	Diode Forward Voltage ④	—	1.2	V	V _{GS} = 0V, I _D = 49A

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Single Event Effect Safe Operating Area

Ion	LET MeV/(mg/cm ²)	Energy (MeV)	Range (μm)	V _{DS} (V)				
				@V _{GS} =0V	@V _{GS} =-5V	@V _{GS} =-10V	@V _{GS} =-15V	@V _{GS} =-20V
Br	36.7	309	39.5	250	250	250	250	250
I	59.8	341	32.5	250	250	250	250	240
Au	82.3	350	28.4	250	250	225	175	50

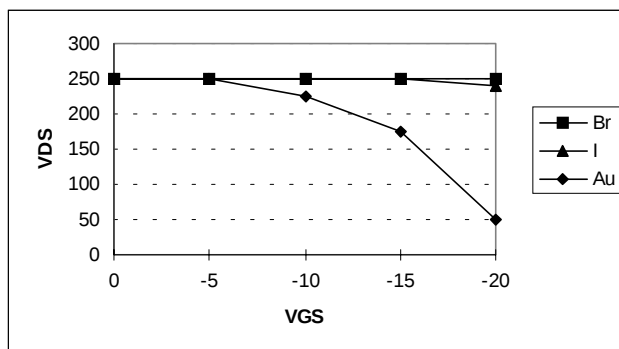


Fig a. Single Event Effect, Safe Operating Area

For footnotes refer to the last page

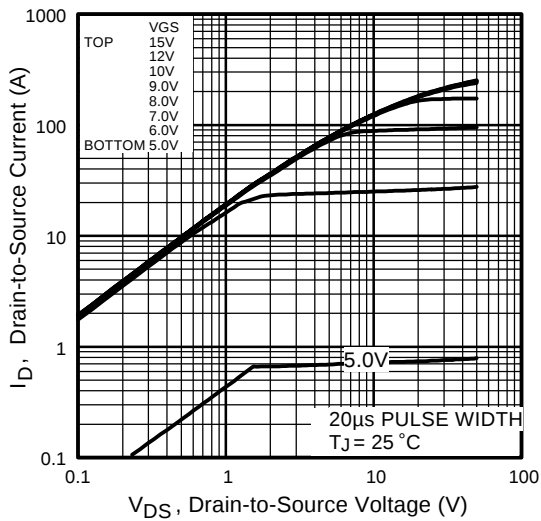


Fig 1. Typical Output Characteristics

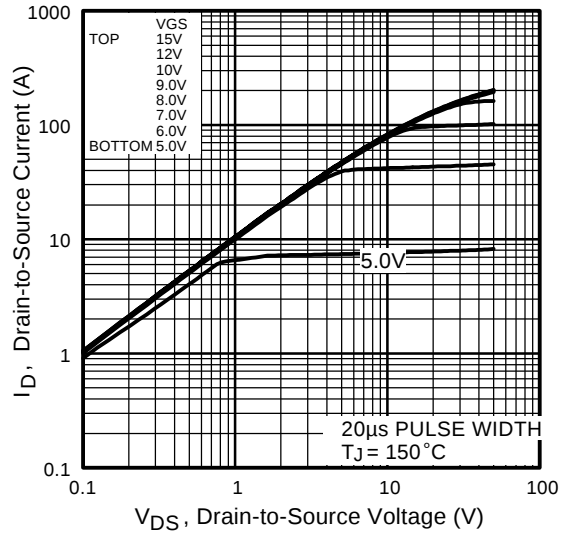


Fig 2. Typical Output Characteristics

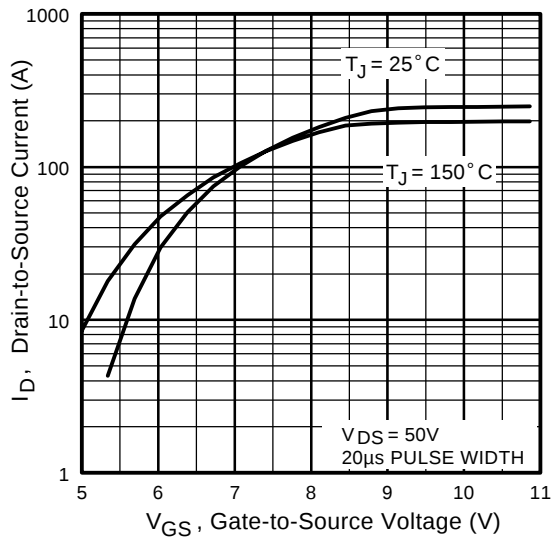


Fig 3. Typical Transfer Characteristics

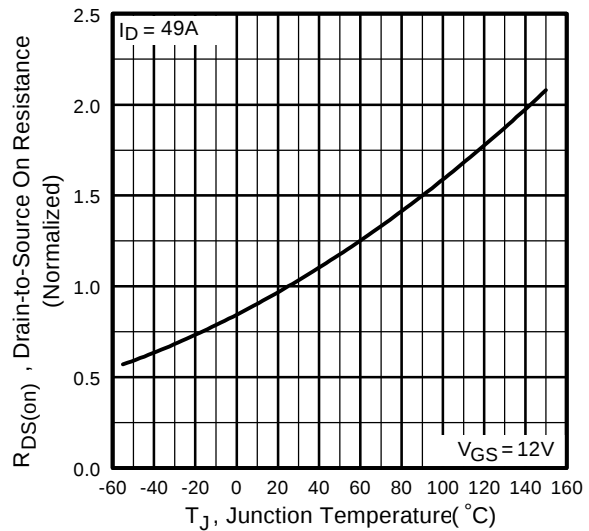


Fig 4. Normalized On-Resistance Vs. Temperature

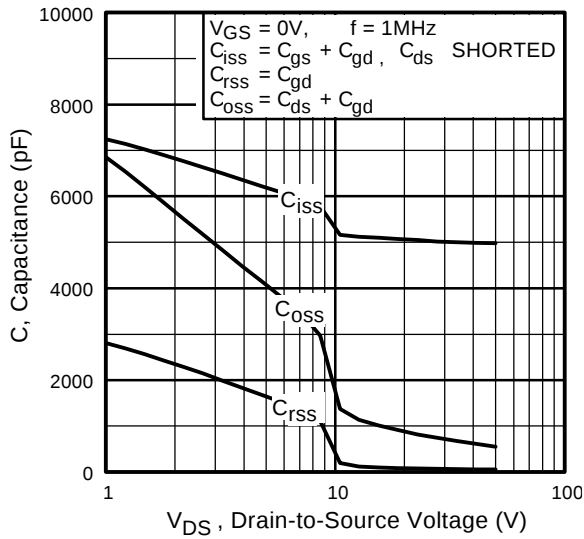


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

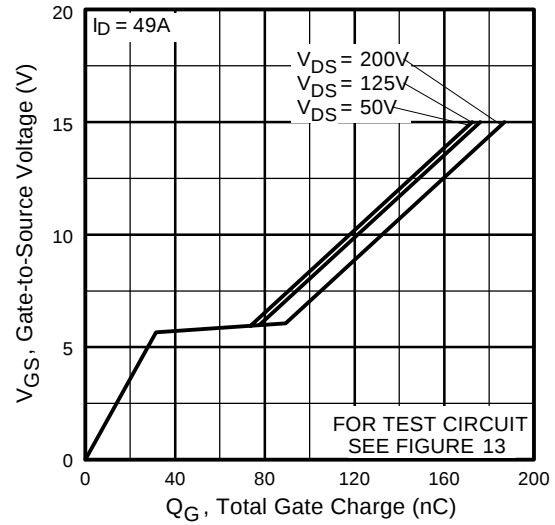


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

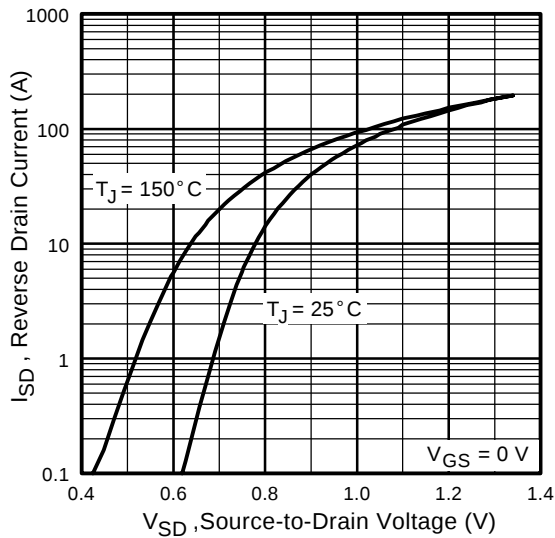


Fig 7. Typical Source-Drain Diode Forward Voltage

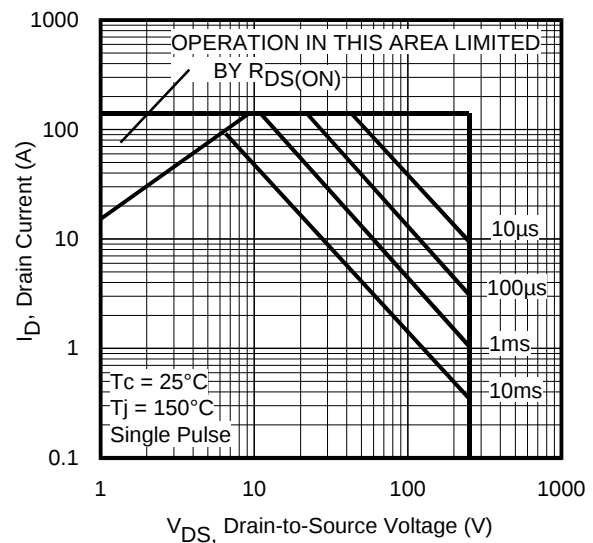


Fig 8. Maximum Safe Operating Area

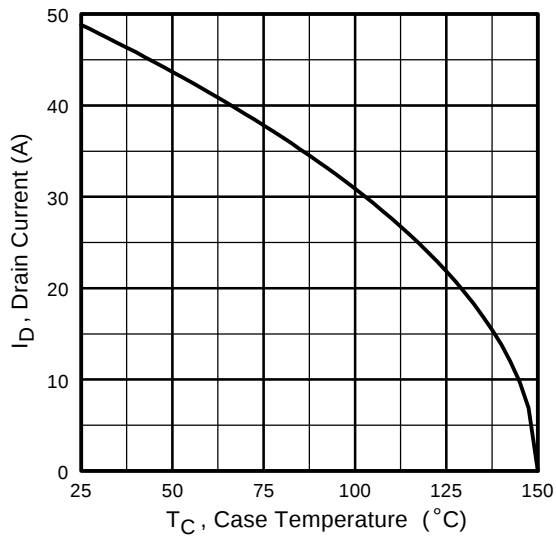


Fig 9. Maximum Drain Current Vs. Case Temperature

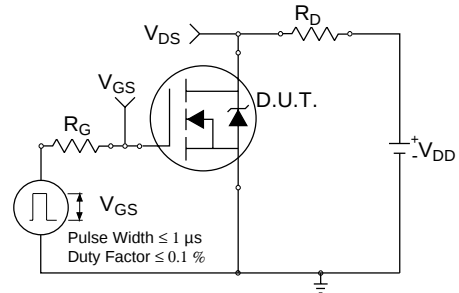


Fig 10a. Switching Time Test Circuit

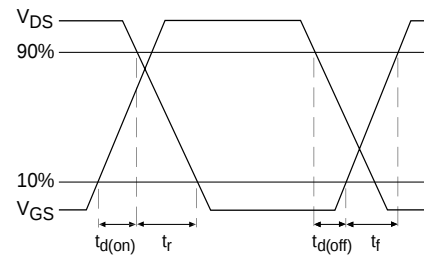


Fig 10b. Switching Time Waveforms

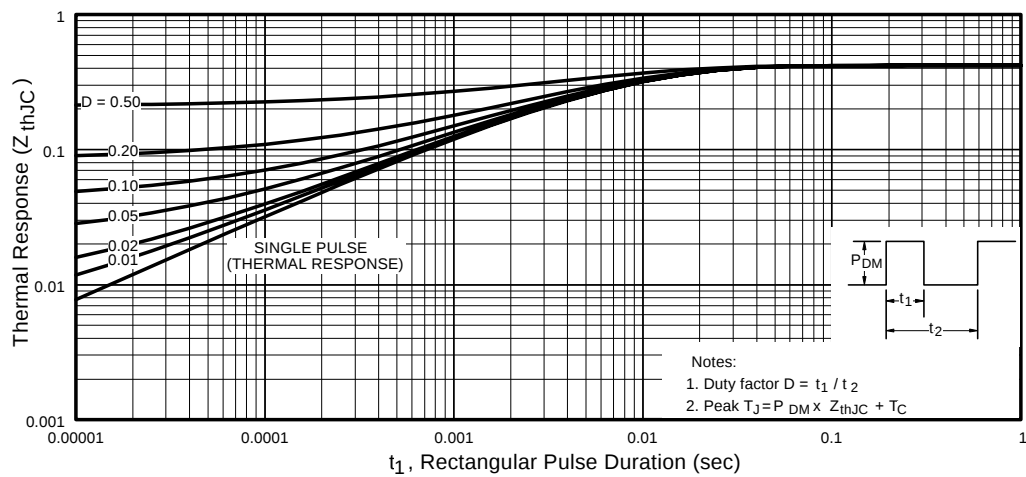


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

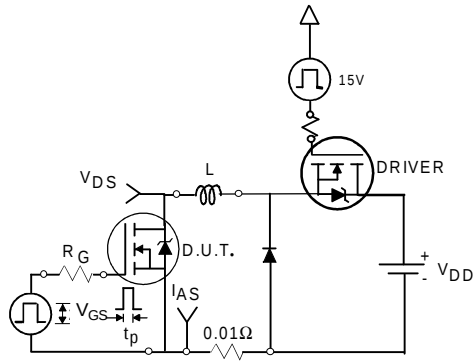


Fig 12a. Unclamped Inductive Test Circuit

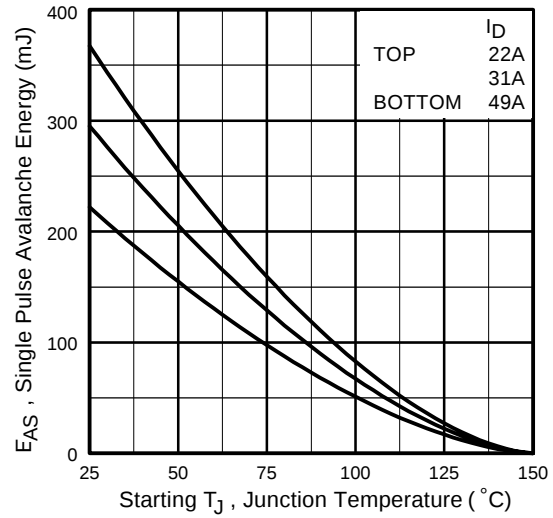


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

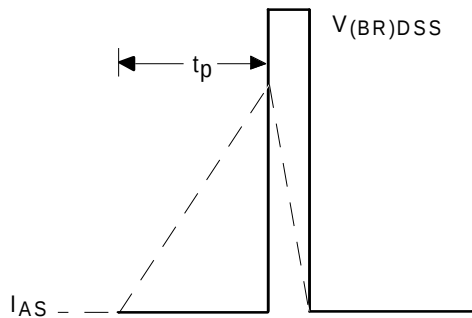


Fig 12b. Unclamped Inductive Waveforms

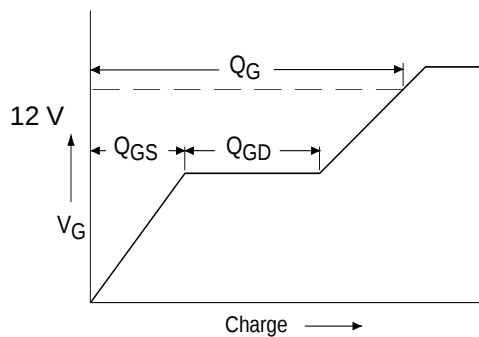


Fig 13a. Basic Gate Charge Waveform

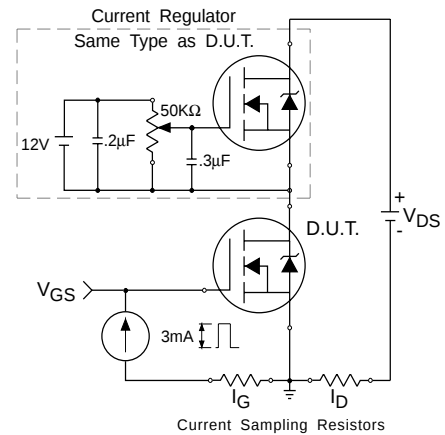
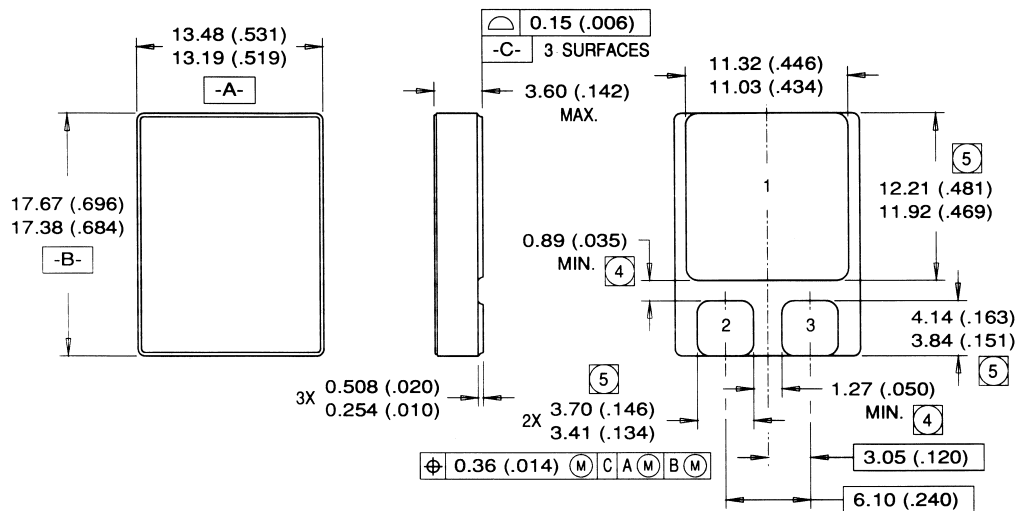


Fig 13b. Gate Charge Test Circuit

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
 ② $V_{DD} = 50V$, starting $T_J = 25^\circ C$, $L = 0.19\text{ mH}$
 Peak $I_L = 49A$, $V_{GS} = 12V$
 ③ $I_{SD} \leq 49A$, $di/dt \leq 274A/\mu s$,
 $V_{DD} \leq 250V$, $T_J \leq 150^\circ C$
 ④ Pulse width $\leq 300\text{ }\mu s$; Duty Cycle $\leq 2\%$
 ⑤ **Total Dose Irradiation with V_{GS} Bias.**
 12 volt V_{GS} applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.
 ⑥ **Total Dose Irradiation with V_{DS} Bias.**
 200 volt V_{DS} applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.

Case Outline and Dimensions — SMD-2**NOTES:**

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
- ④ DIMENSION INCLUDES METALLIZATION FLASH.
- ⑤ DIMENSION DOES NOT INCLUDE METALLIZATION FLASH.

PAD ASSIGNMENTS

- 1 = DRAIN
 2 = GATE
 3 = SOURCE

International
IR Rectifier

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