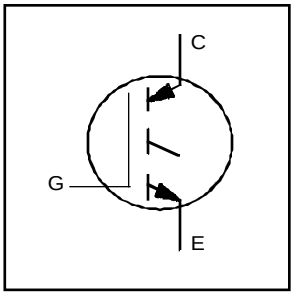
International
IOR Rectifier

TARGET

IRGCH50SE

IRGCH50SE IGBT Die in Wafer Form



1200 V
Size 5
Standard Speed
5" Wafer

Electrical Characteristics (Wafer Form)

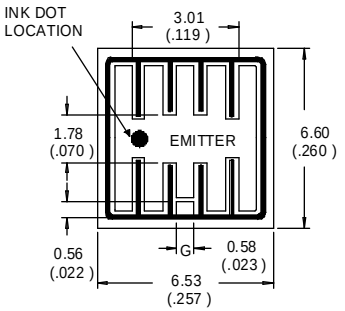
Parameter	Description	Guaranteed (Min/Max)	Test Conditions
$V_{CE\ (on)}$	Collector-to-Emitter Saturation Voltage	3.3V Max.	I_C = 20A, T_J = 25°C, V_{GE} = 15V
$V_{(BR)CES}$	Colletor-to-Emitter Breakdown Voltage	1200V Min.	T_J = 25°C, I_{CES} = 250µA, V_{GE} = 0V
$V_{GE(th)}$	Gate Threshold Voltage	3.0V Min., 5.5V Max.	V_{GE} = V_{CE} , T_J =25°C, I_C =250µA
I_{CES}	Zero Gate Voltage Collector Current	250 µA Max.	T_J = 25°C, V_{CE} = 1200V
I_{GES}	Gate-to-Emitter Leakage Current	± 500 nA Max.	T_J = 25°C, V_{GE} = +/- 20V

Mechanical Data

Norminal Backmetal Composition, Thickness:	Cr-Ni-Ag (1kA-4kA-6kA)
Norminal Front Metal Composition, Thickness:	99% Al, 1% Si (3 microns)
Dimensions:	0.257" x 0.260"
Wafer Diameter:	125mm, with std. < 100 > flat
Wafer thickness:	.015" + / -.003"
Relevant Die Mechanical Dwg. Number	01-5104
Minimum Street Width	100 Microns
Reject Ink Dot Size	0.25mm Diameter Minimum
Ink Dot Location	See Die Outline drawing below
Recommended Storage Environment:	Store in original container, in dessicated nitrogen, with no contamination

Reference Standard IR packaged part (for design) : IRGPH50S

Die Outline



NOTES :
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
2. CONTROLLING DIMENSION : (INCH)
3. LETTER DESIGNATION :
   S = SOURCE
   G = GATE
4. DIMENSIONAL TOLERANCES
   BONDING PADS : < 0.635 TOLERANCE = +/- 0.013
   WIDTH < (.0250) TOLERANCE =+/- (.0005)
   & > 0.635 TOLERANCE = +/- 0.025
   LENGTH > (.0250) TOLERANCE = +/- (.0010)
   OVERALL DIE < 1.270 TOLERANCE = +/- 0.102
   WIDTH < (.050) TOLERANCE = +/- (.004)
   & > 0.635 TOLERANCE = +/- 0.203
   LENGTH > (.050) TOLERANCE = +/- (.008)
5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III