International
IOR Rectifier

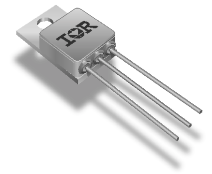
IRFY9240C,IRFY9240CM

POWER MOSFET
THRU-HOLE (TO-257AA)

200V, P-CHANNEL
HEXFET® MOSFET TECHNOLOGY

Product Summary

Part Number	Rds(on)	Id	Eyelets
IRFY9240C	0.51 Ω	-9.4A	Ceramic
IRFY9240CM	0.51 Ω	-9.4A	Ceramic


TO-257AA

HEXFET® MOSFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry design achieves very low on-state resistance combined with high transconductance. HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and electrical parameter temperature stability. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, high energy pulse circuits, and virtually any application where high reliability is required. The HEXFET transistor's totally isolated package eliminates the need for additional isolating material between the device and the heatsink. This improves thermal efficiency and reduces drain capacitance.

Features:

- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Electrically Isolated
- Ceramic Eyelets
- Ideally Suited For Space Level Applications

Absolute Maximum Ratings

	Parameter		Units
I_D @ V_{GS} = -10V, T_C = 25°C	Continuous Drain Current	-9.4	A
I_D @ V_{GS} = -10V, T_C = 100°C	Continuous Drain Current	-6.0	
I_{DM}	Pulsed Drain Current ①	-36	
P_D @ T_C = 25°C	Max. Power Dissipation	100	W
	Linear Derating Factor	0.8	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	700	mJ
I_{AR}	Avalanche Current ①	-9.4	A
E_{AR}	Repetitive Avalanche Energy ①	10	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.5	V/ns
T_J T_{STG}	Operating Junction Storage Temperature Range	-55 to 150	°C
	Lead Temperature	300(0.063in.(1.6mm)from case for 10 sec)	
	Weight	4.3 (Typical)	g

For footnotes refer to the last page

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-200	—	—	V	V_{GS} = 0V, I_D = -1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	-0.2	—	V/°C	Reference to 25°C, I_D = -1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.51	Ω	V_{GS} = -10V, I_D = -6.0A ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} = V_{GS}$, I_D = -250μA
g_{fs}	Forward Transconductance	4.0	—	—	S (℧)	V_{DS} > -15V, I_{DS} = -6.0A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-25	μA	V_{DS}= -160V ,V_{GS}=0V
		—	—	-250		V_{DS} = -160V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V_{GS} = -20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	100		V_{GS} = 20V
Q_g	Total Gate Charge	—	—	60	nC	V_{GS} = -10V, I_D = -9.4A
Q_{gs}	Gate-to-Source Charge	—	—	15		V_{DS} = -100V
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	38		
$t_{d(on)}$	Turn-On Delay Time	—	—	35	ns	V_{DD} = -100V, I_D = -9.4A,
t_r	Rise Time	—	—	85		R_G = 9.1Ω
$t_{d(off)}$	Turn-Off Delay Time	—	—	85		
t_f	Fall Time	—	—	65		
$L_S + L_D$	Total Inductance	—	6.8	—	nH	Measured from drain lead (6mm/0.25in. from package) to source lead (6mm/0.25in. from package)
C_{iss}	Input Capacitance	—	1200	—	pF	V_{GS} = 0V, V_{DS} = -25V
C_{oss}	Output Capacitance	—	570	—		f = 1.0MHz
C_{rss}	Reverse Transfer Capacitance	—	81	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-9.4	A	
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	-36		
V_{SD}	Diode Forward Voltage	—	—	-4.6	V	T_j = 25°C, I_S = -9.4A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	440	nS	T_j = 25°C, I_F = -9.4A, di/dt ≤ -100A/μs
Q_{RR}	Reverse Recovery Charge	—	—	7.2	μC	V_{DD} ≤ -50V ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJC}	Junction-to-Case	—	—	1.25	°C/W	
R_{thCS}	Case-to-sink	—	0.21	—		
R_{thJA}	Junction-to-Ambient	—	—	80		Typical socket mount

Note: Corresponding Spice and Saber models are available on the G&S Website.

For footnotes refer to the last page

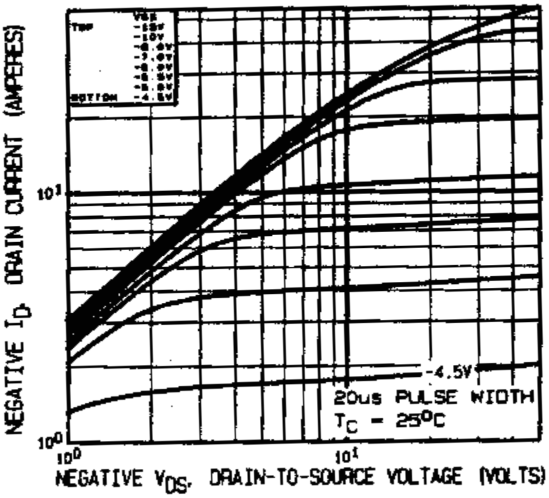


Fig 1. Typical Output Characteristics

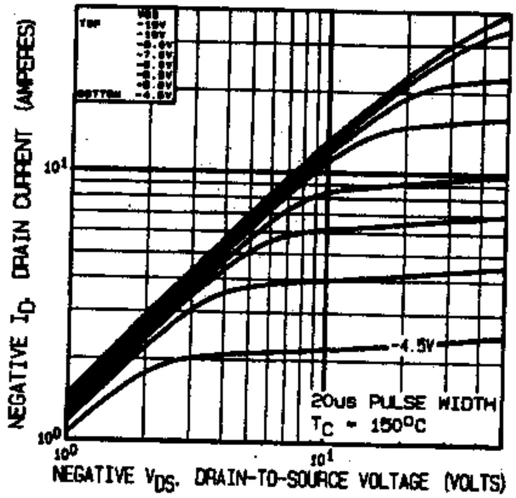


Fig 2. Typical Output Characteristics

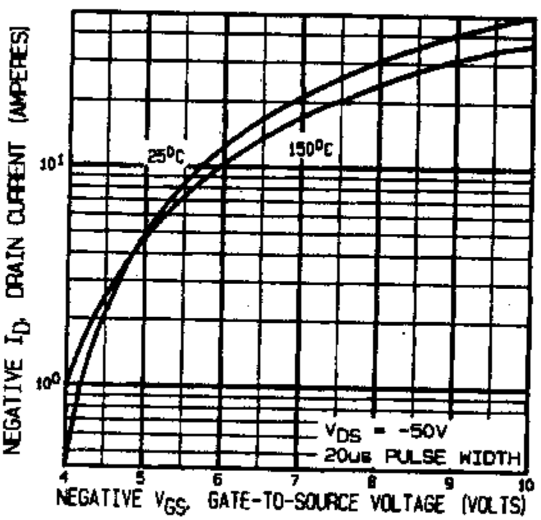


Fig 3. Typical Transfer Characteristics

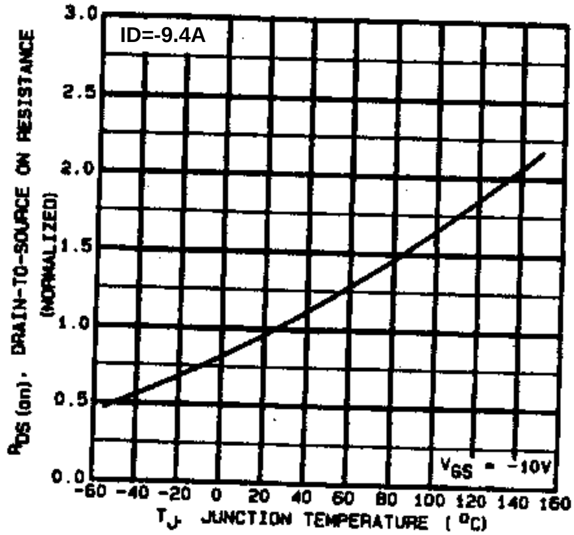


Fig 4. Normalized On-Resistance Vs. Temperature

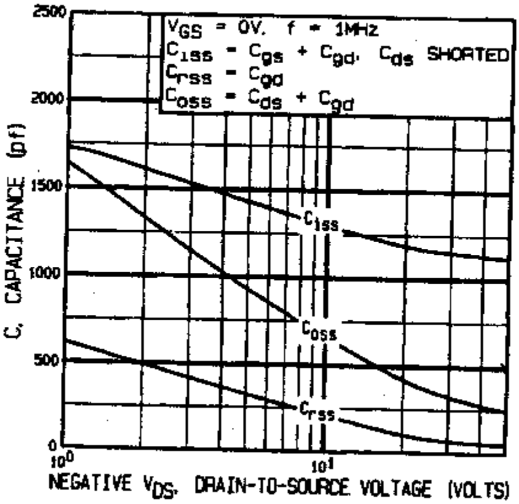


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

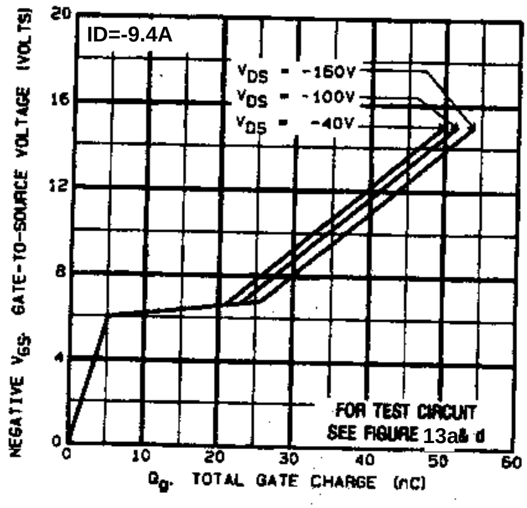


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

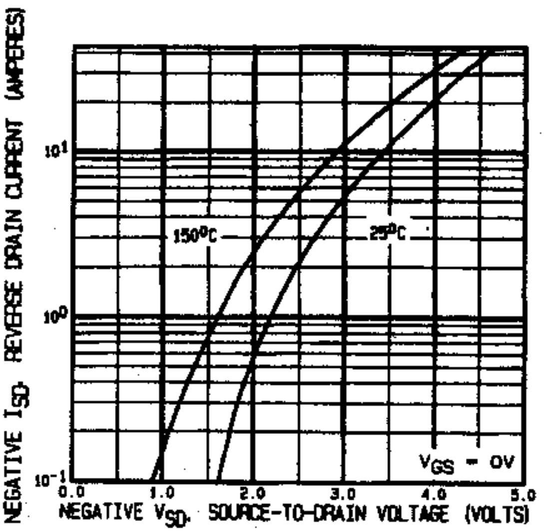


Fig 7. Typical Source-Drain Diode Forward Voltage

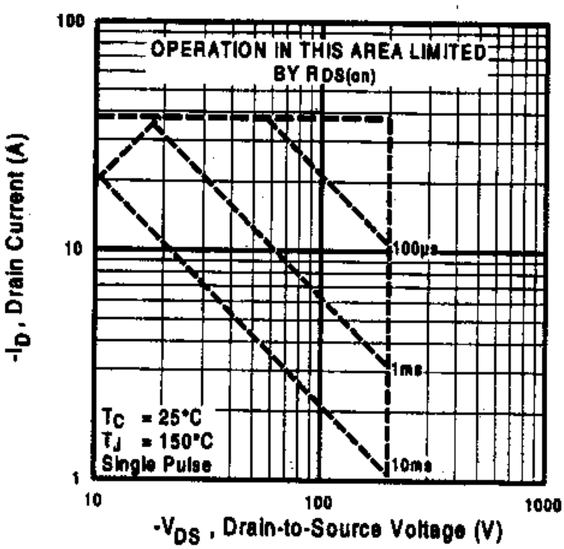


Fig 8. Maximum Safe Operating Area

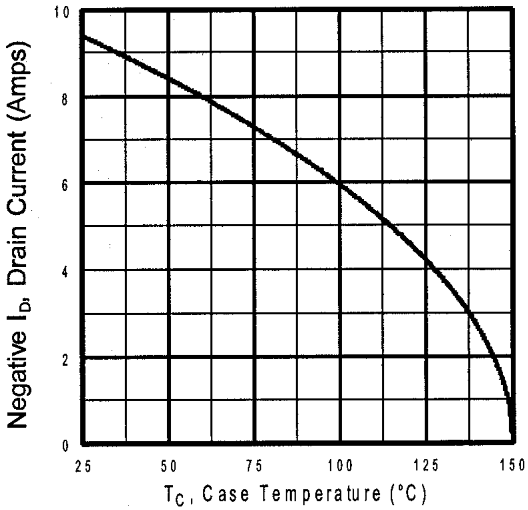


Fig 9. Maximum Drain Current Vs. Case Temperature

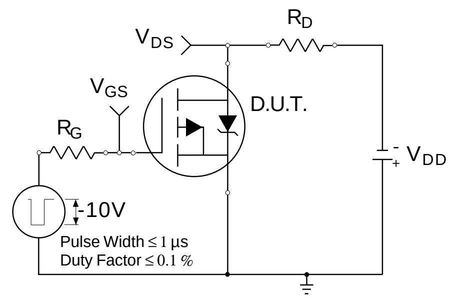


Fig 10a. Switching Time Test Circuit

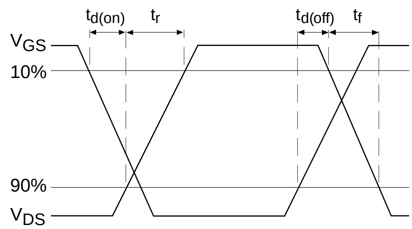


Fig 10b. Switching Time Waveforms

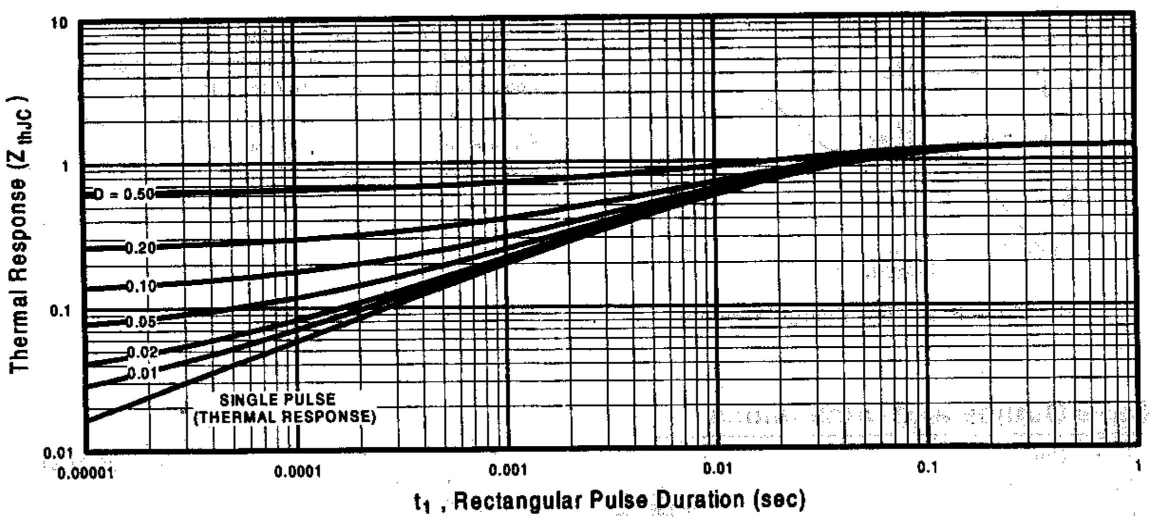


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

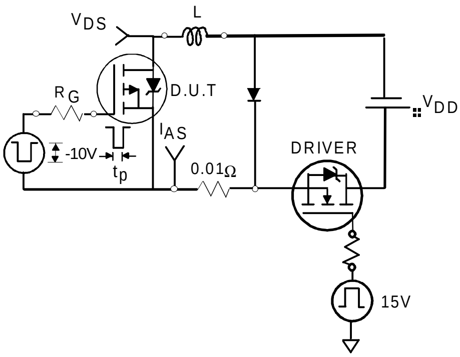


Fig 12a. Unclamped Inductive Test Circuit

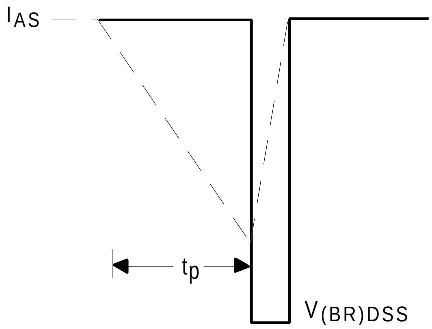


Fig 12b. Unclamped Inductive Waveforms

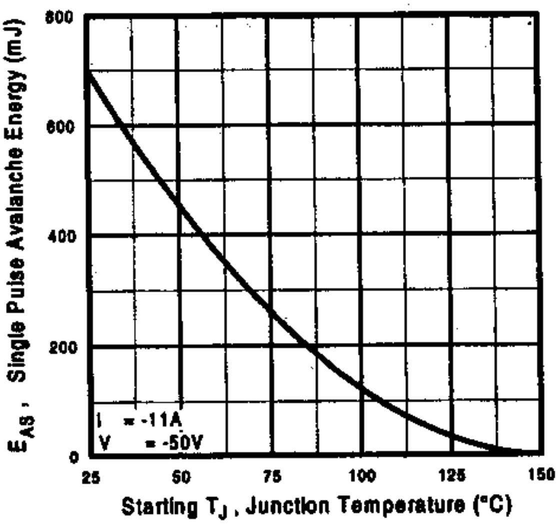


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

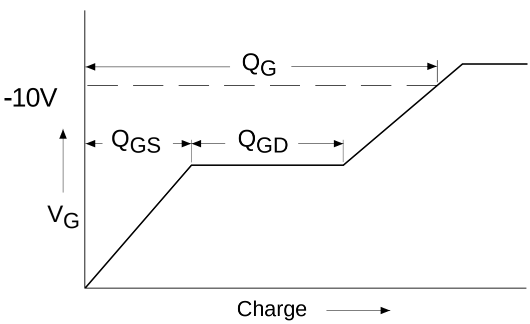


Fig 13a. Basic Gate Charge Waveform

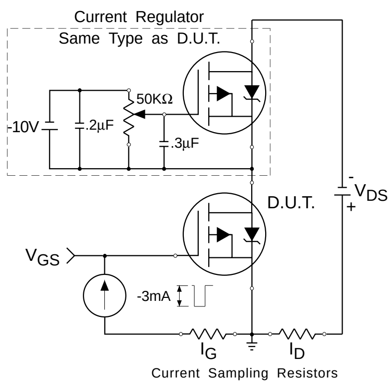


Fig 13b. Gate Charge Test Circuit

Foot Notes:

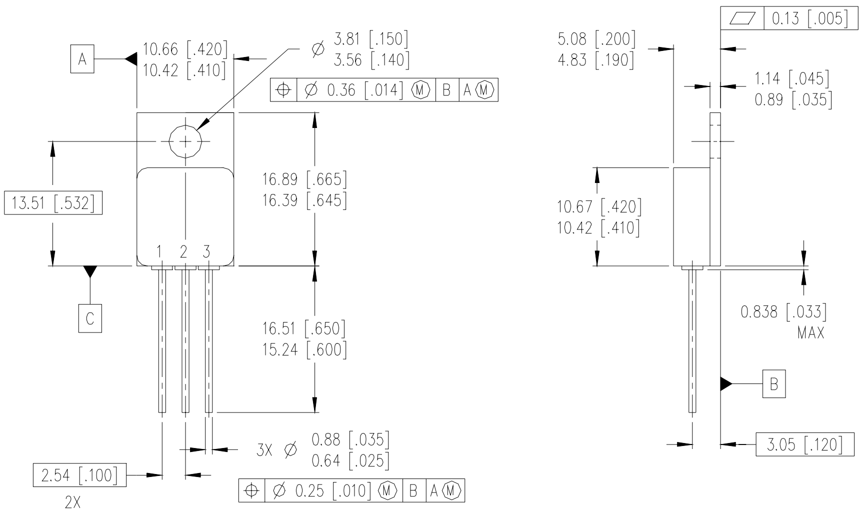
① Repetitive Rating; Pulse width limited by maximum junction temperature.

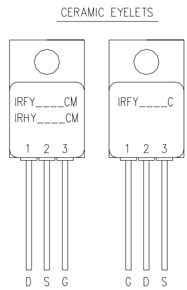
② V_{DD} = -50V, starting T_J = 25°C, L= 15mH Peak I_L = -9.4A, V_{GS} = -10V

③ I_{SD} ≤ -9.4A, di/dt ≤ -150A/µs, V_{DD} ≤ -200V, T_J ≤ 150°C

④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

Case Outline and Dimensions — TO-257AA





NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-257AA.

LEGEND

D - DRAIN
S - SOURCE
G - GATE

International
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Data and specifications subject to change without notice. 04/01