PD- 94227

International
IOR Rectifier

IRFPS35N50L

SMPS MOSFET

HEXFET® Power MOSFET

Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- ZVS and High Frequency Circuit
- PWM Inverters

V_{DSS}	$R_{DS(on)}$ typ.	I_D
500V	0.125Ω	34A

Benefits

- Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Low Trr and Soft Diode Recovery
- High Performance Optimised Anti-parallel Diode

Super-247™

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	34	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	22	
I_{DM}	Pulsed Drain Current ①	140	
P_D @T_C = 25°C	Power Dissipation	450	W
	Linear Derating Factor	3.6	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
	dv/dtPeak Diode Recovery dv/dt ③	11	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	34	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	140		
V_{SD}	Diode Forward Voltage	——	——	1.5	V	T_J = 25°C, I_S = 34A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	170	250	ns	T_J = 25°C I_F = 34A
		——	220	330		T_J = 125°C di/dt = 100A/µs ④
Q_{rr}	Reverse Recovery Charge	——	670	1010	nC	T_J = 25°C
		——	1.5	2.2	µC	T_J = 125°C
I_{RRM}	Reverse Recovery Current	——	8.5	——	A	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Typical SMPS Topologies

- Bridge Converters
- All Zero Voltage Switching

Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.12	—	V/°C	Reference to 25°C, I_D = 1mA⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.125	0.145	Ω	V_{GS} = 10V, I_D = 20A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	—	—	50	µA	V_{DS} = 500V, V_{GS} = 0V
		—	—	2.0	mA	V_{DS} = 400V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	18	—	—	S	V_{DS} = 50V, I_D = 20A
Q_g	Total Gate Charge	—	—	230	nC	I_D = 34A
Q_{gs}	Gate-to-Source Charge	—	—	65		V_{DS} = 400V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	110		V_{GS} = 10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	24	—	ns	V_{DD} = 250V
t_r	Rise Time	—	100	—		I_D = 34A
$t_{d(off)}$	Turn-Off Delay Time	—	42	—		R_G = 1.2Ω
t_f	Fall Time	—	42	—		V_{GS} = 10V,See Fig. 10 ④
C_{iss}	Input Capacitance	—	5580	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	590	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	58	—		f = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	—	7290	—		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	160	—		V_{GS} = 0V, V_{DS} = 400V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	—	320	—		V_{GS} = 0V, V_{DS} = 0V to 400V ⑤

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	560	mJ
I_{AR}	Avalanche Current①	—	34	A
E_{AR}	Repetitive Avalanche Energy①	—	45	mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.28	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)

② Starting T_J = 25°C, L = 0.97mH, R_G = 25Ω, I_{AS} = 34A (See Figure 12a)

③ I_{SD} ≤ 34A, di/dt ≤ 510A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 150°C.

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

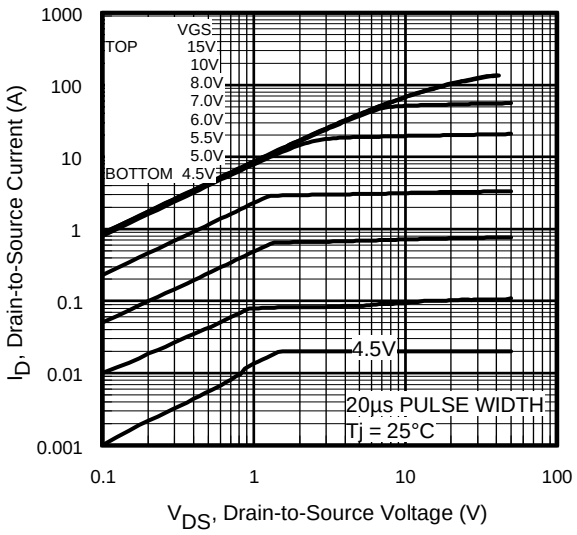


Fig 1. Typical Output Characteristics

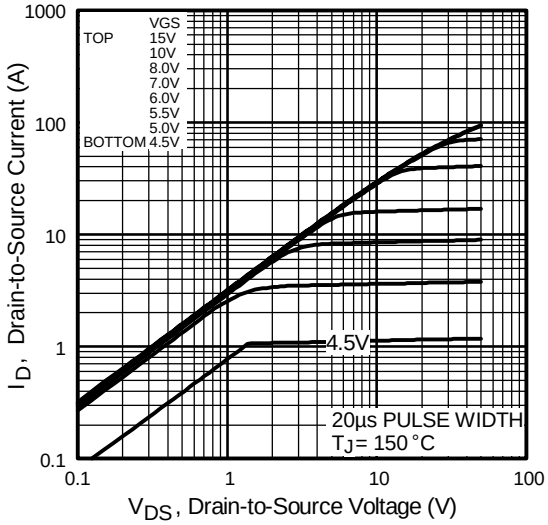


Fig 2. Typical Output Characteristics

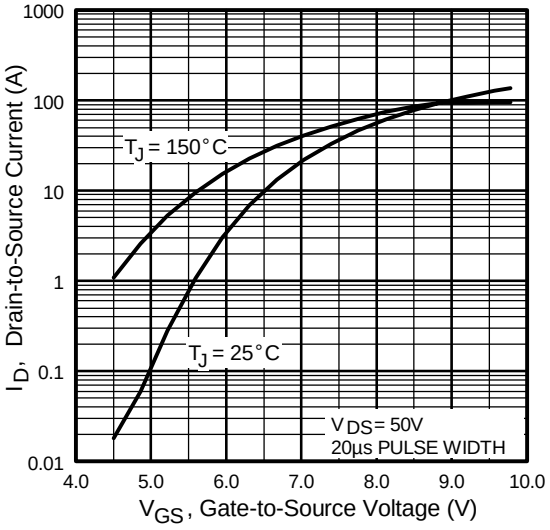


Fig 3. Typical Transfer Characteristics

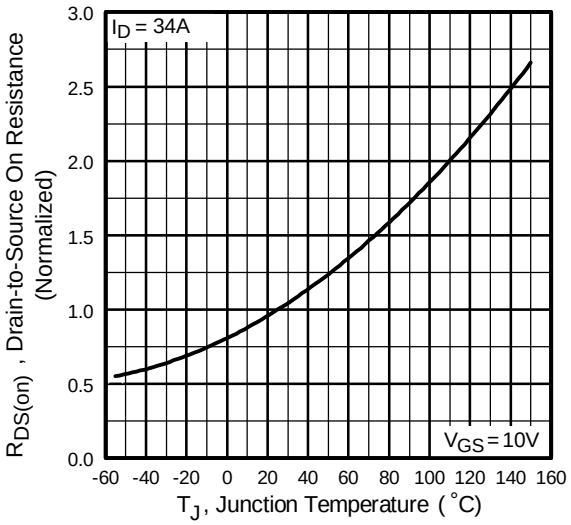


Fig 4. Normalized On-Resistance Vs. Temperature

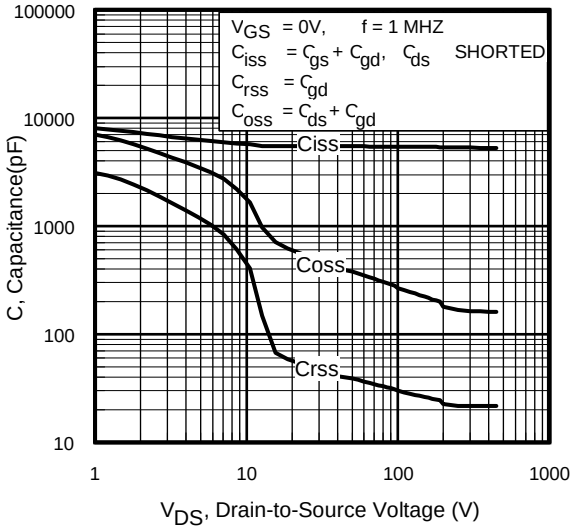


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

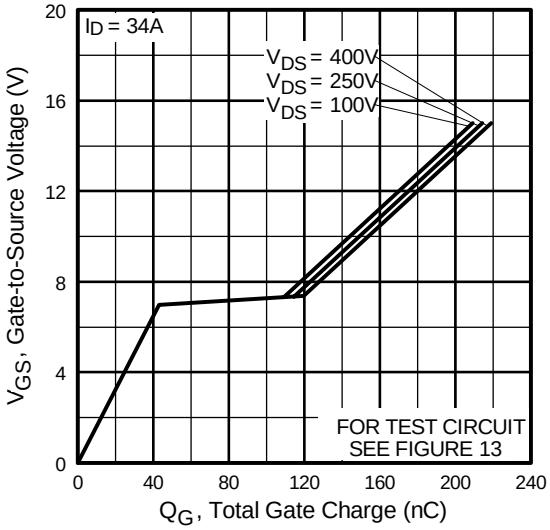


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

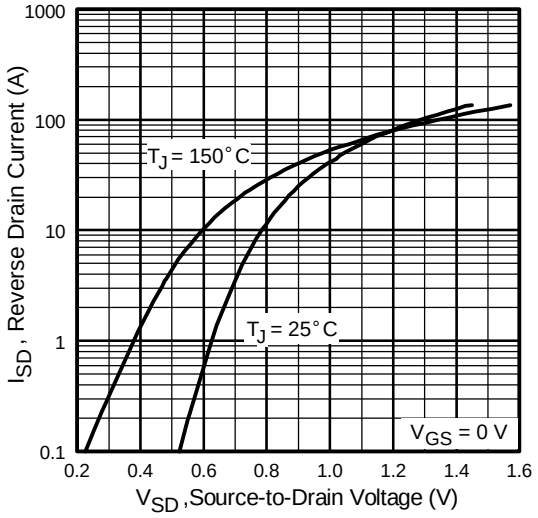


Fig 7. Typical Source-Drain Diode Forward Voltage

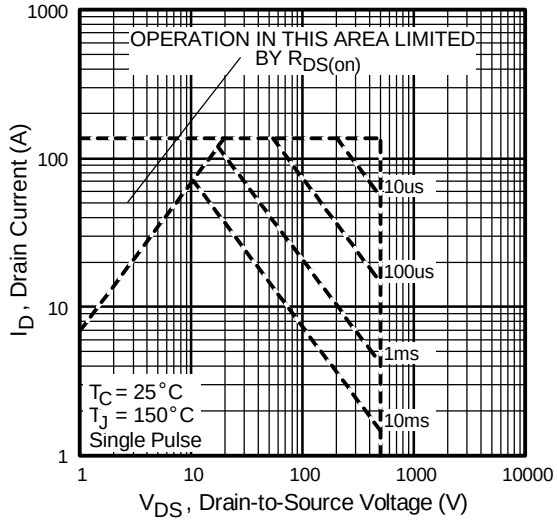


Fig 8. Maximum Safe Operating Area

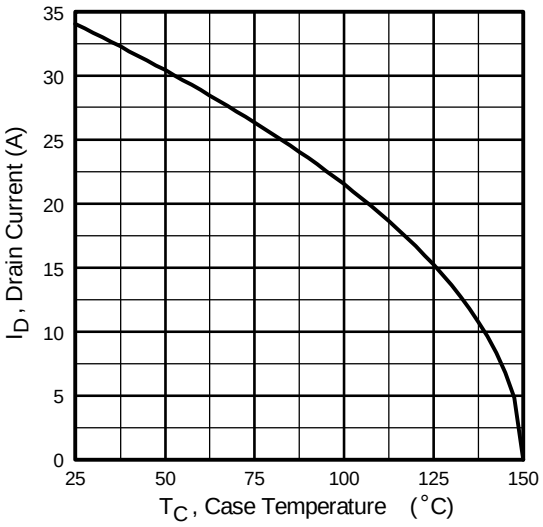


Fig 9. Maximum Drain Current Vs. Case Temperature

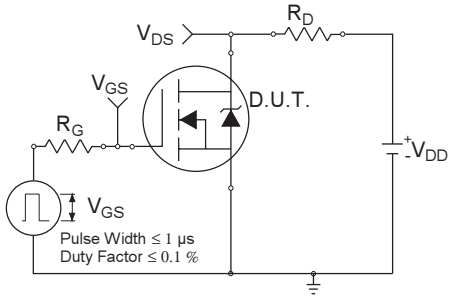


Fig 10a. Switching Time Test Circuit

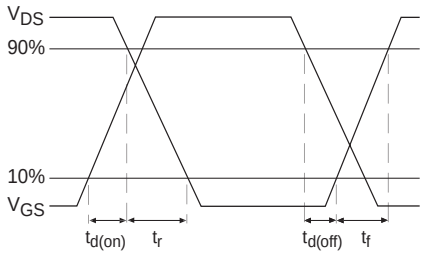


Fig 10b. Switching Time Waveforms

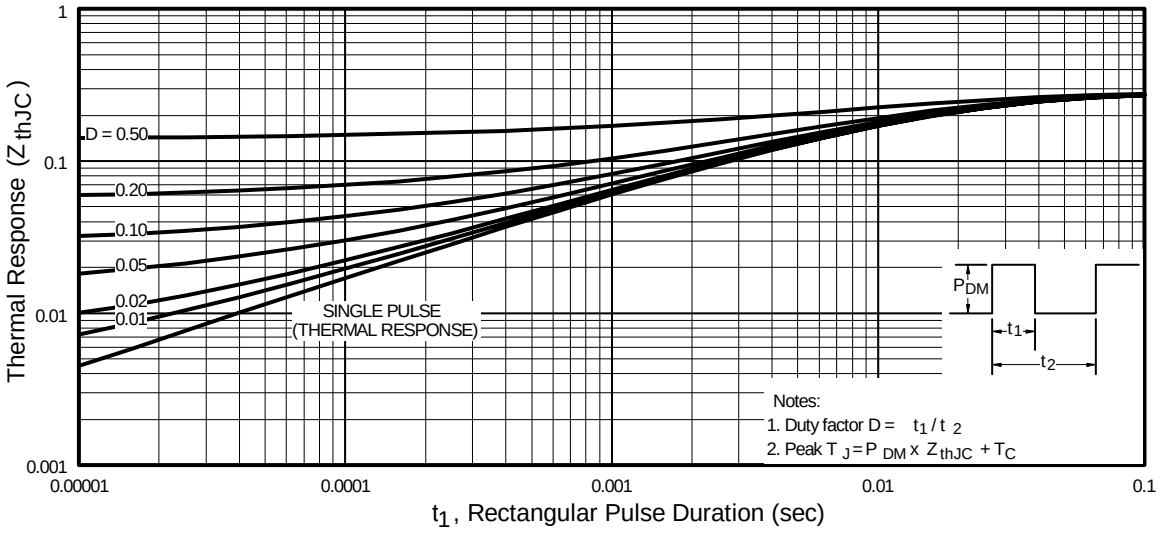


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

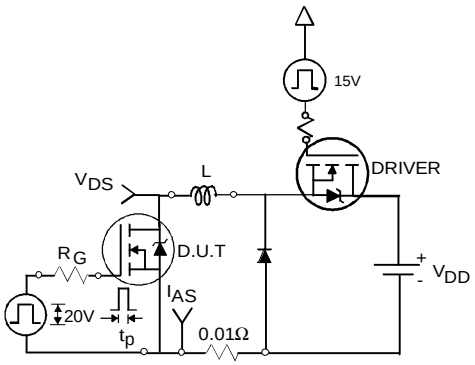


Fig 12a. Unclamped Inductive Test Circuit

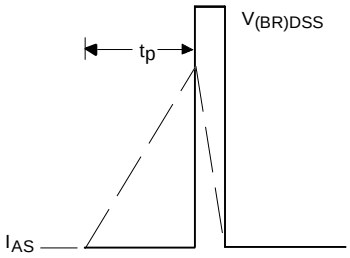


Fig 12b. Unclamped Inductive Waveforms

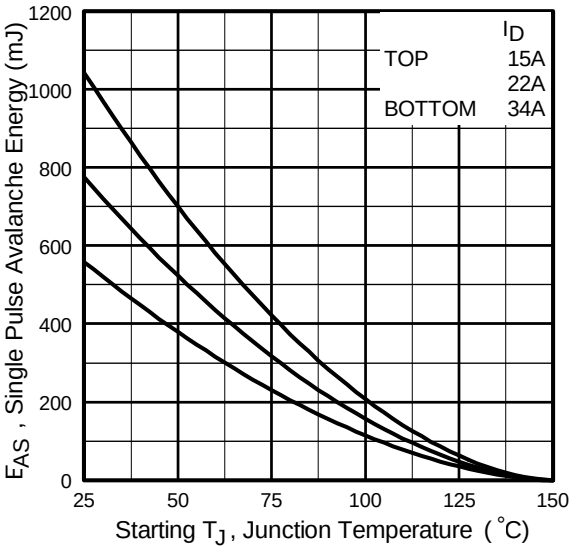


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

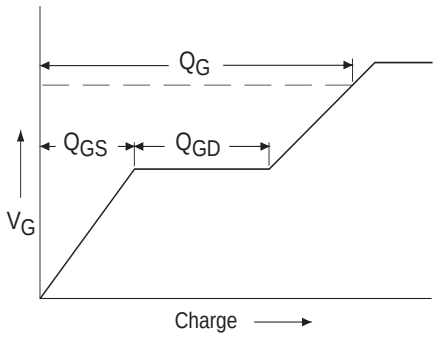


Fig 13a. Basic Gate Charge Waveform

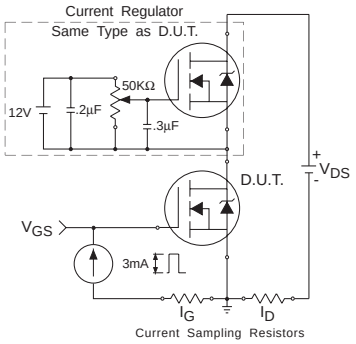


Fig 13b. Gate Charge Test Circuit

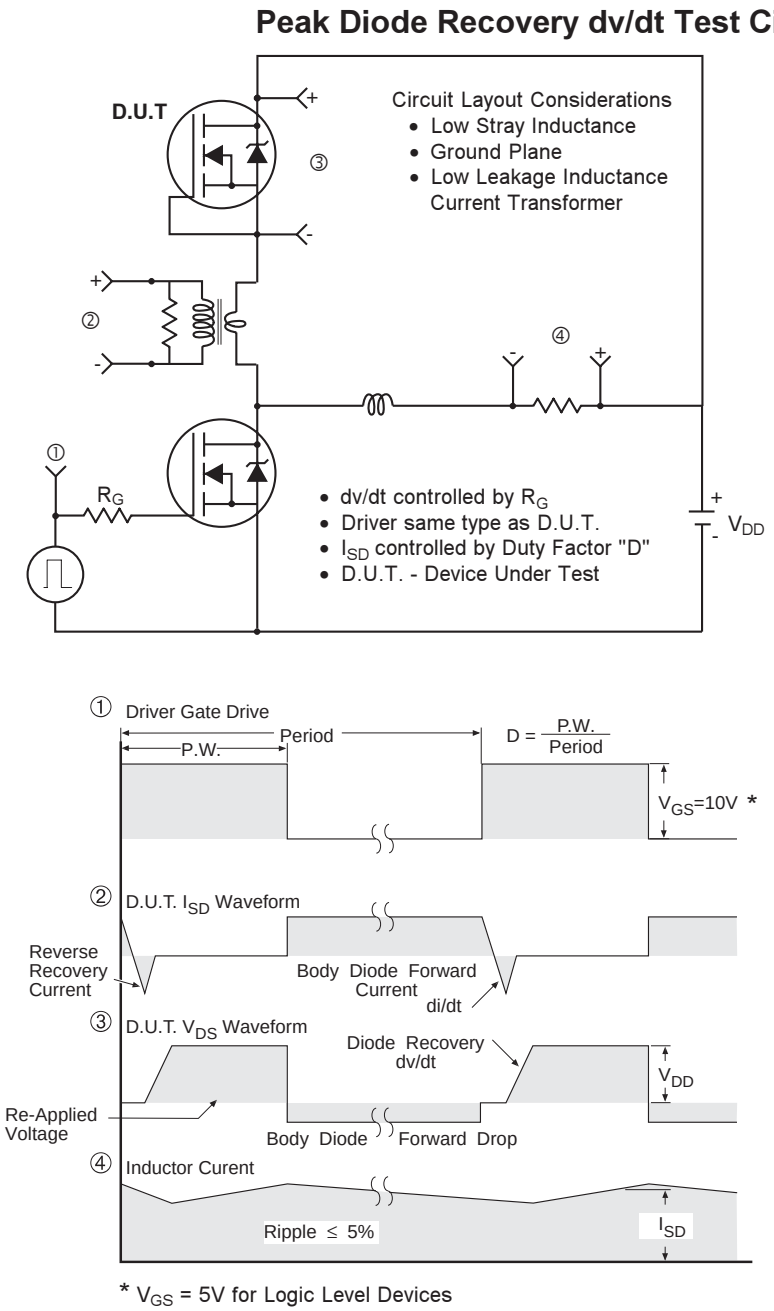
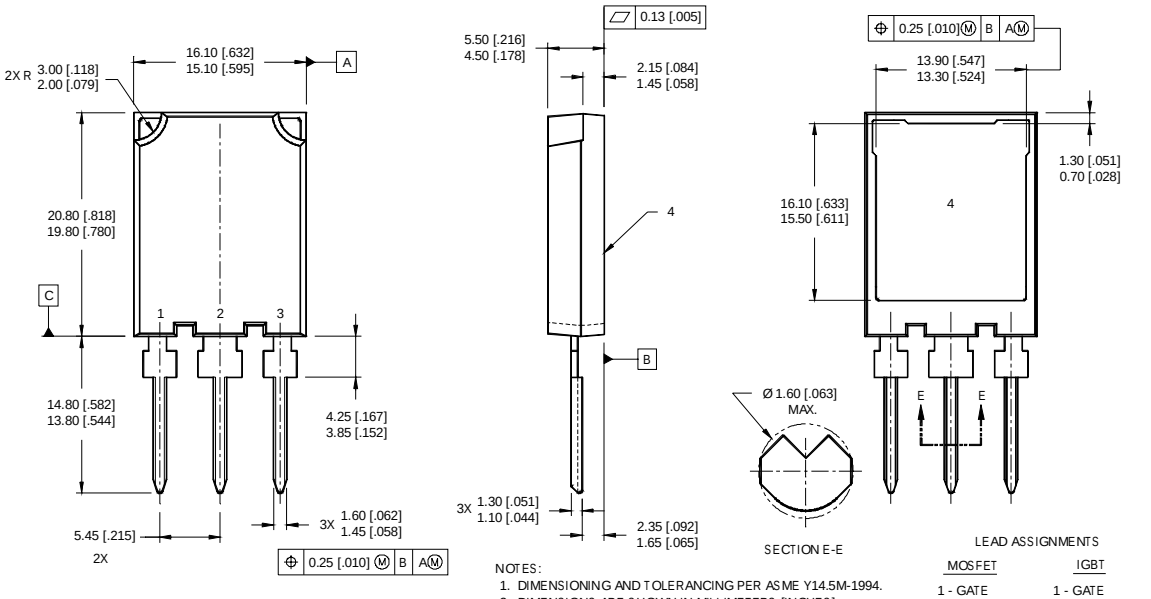


Fig 14. For N-Channel HEXFET® Power MOSFETs

Super-247™ Package Outline



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
3. CONTROLLING DIMENSION: MILLIMETER
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-274AA

LEAD ASSIGNMENTS

MOSFET	IGBT
1 - GATE	1 - GATE
2 - DRAIN	2 - COLLECTOR
3 - SOURCE	3 - EMITTER
4 - DRAIN	4 - COLLECTOR

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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