PD-94098

International
IOR Rectifier

SMPS MOSFET

IRFP460N

HEXFET® Power MOSFET

Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptable Power Supply
- High speed power switching

V_{DSS}	Rds(on) max	I_D
500V	**0.24Ω**	**20A**

Benefits

- Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective Coss specified (See AN1001)

TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	20	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	13	
I_{DM}	Pulsed Drain Current ①	80	
P_D @T_C = 25°C	Power Dissipation	280	W
	Linear Derating Factor	2.2	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torqe, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Typical SMPS Topologies:

- Full Bridge
- PFC Boost

Notes ① through ⑤ are on page 8

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Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	–––	–––	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	0.58	–––	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	–––	0.24	Ω	V_{GS} = 10V, I_D = 12A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	–––	5.0	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	25	µA	V_{DS} = 500V, V_{GS} = 0V
		–––	–––	250		V_{DS} = 400V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	–––	–––	-100		V_{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	10	–––	–––	S	V_{DS} = 50V, I_D = 12A
Q_g	Total Gate Charge	–––	–––	124	nC	I_D = 20A
Q_{gs}	Gate-to-Source Charge	–––	–––	40		V_{DS} = 400V
Q_{gd}	Gate-to-Drain ("Miller") Charge	–––	–––	57		V_{GS} = 10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	–––	23	–––	ns	V_{DD} = 250V
t_r	Rise Time	–––	87	–––		I_D = 20A
$t_{d(off)}$	Turn-Off Delay Time	–––	34	–––		R_G = 4.3Ω
t_f	Fall Time	–––	33	–––		R_D = 13Ω,See Fig. 10 ④
C_{iss}	Input Capacitance	–––	3540	–––	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	–––	350	–––		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	–––	30	–––		ƒ = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	–––	3930	–––		V_{GS} = 0V, V_{DS} = 1.0V, ƒ = 1.0MHz
C_{oss}	Output Capacitance	–––	95	–––		V_{GS} = 0V, V_{DS} = 400V, ƒ = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	–––	200	–––		V_{GS} = 0V, V_{DS} = 0V to 400V ⑤

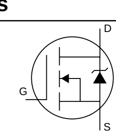
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	–––	340	mJ
I_{AR}	Avalanche Current①	–––	20	A
E_{AR}	Repetitive Avalanche Energy①	–––	28	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	–––	0.45	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	–––	
$R_{\theta JA}$	Junction-to-Ambient	–––	40	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	20	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	–––	–––	80		
V_{SD}	Diode Forward Voltage	–––	–––	1.8	V	T_J = 25°C, I_S = 20A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	–––	550	825	ns	T_J = 25°C, I_F = 20A
Q_{rr}	Reverse RecoveryCharge	–––	7.2	10.8	µC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

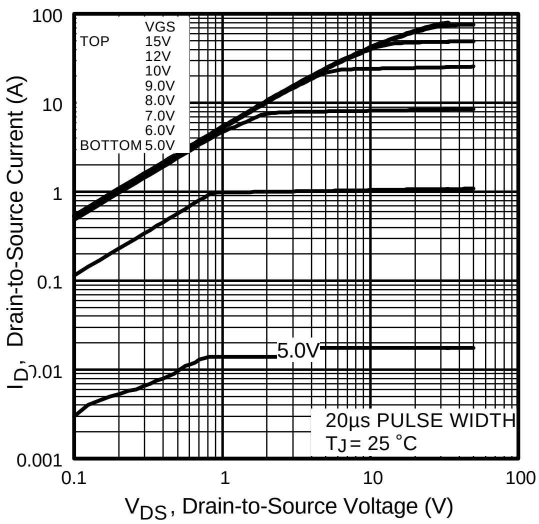


Fig 1. Typical Output Characteristics

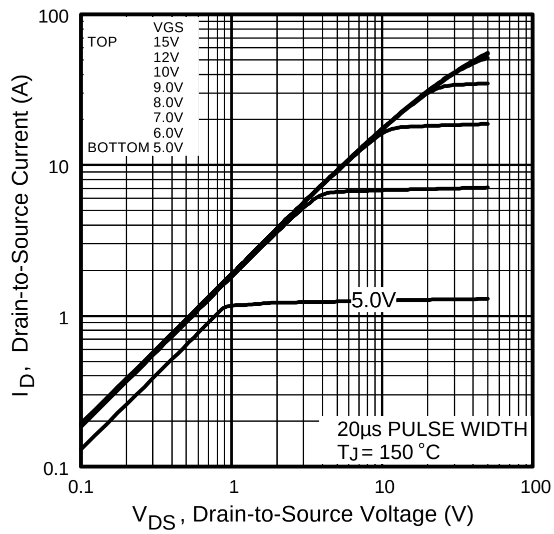


Fig 2. Typical Output Characteristics

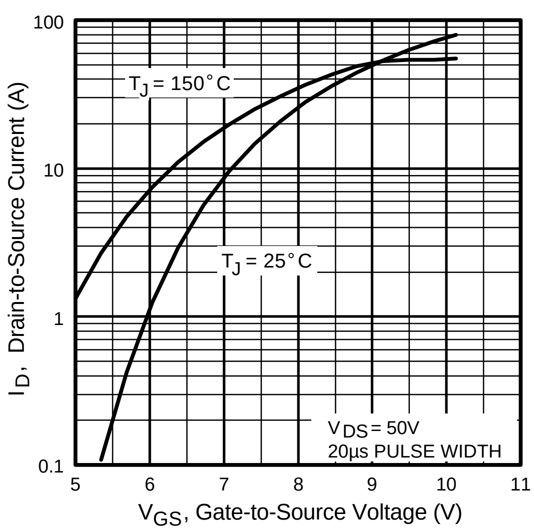


Fig 3. Typical Transfer Characteristics

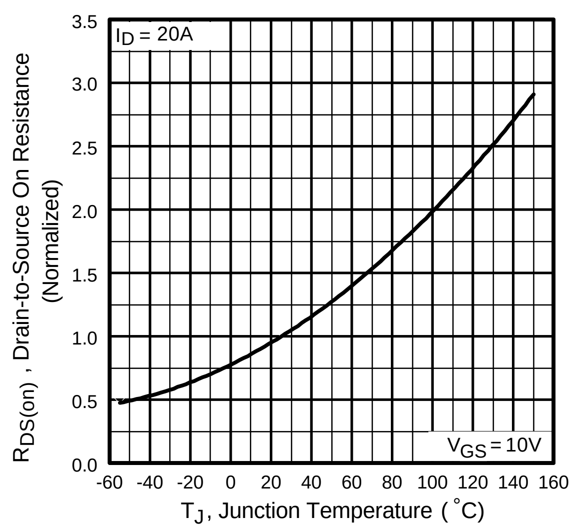


Fig 4. Normalized On-Resistance
Vs. Temperature

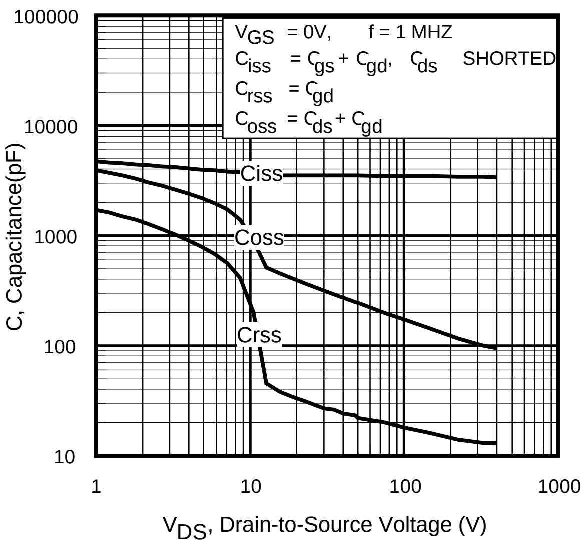


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

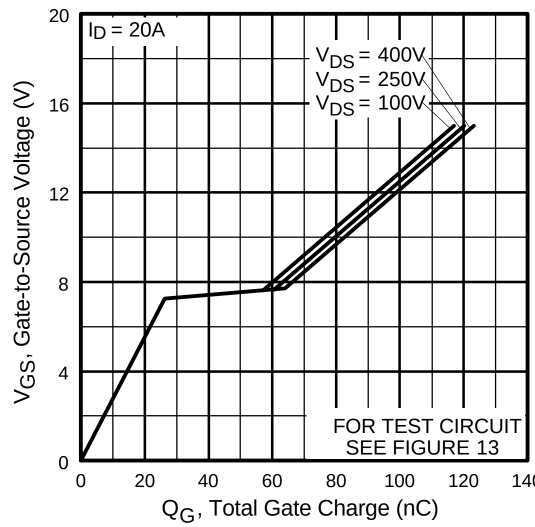


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

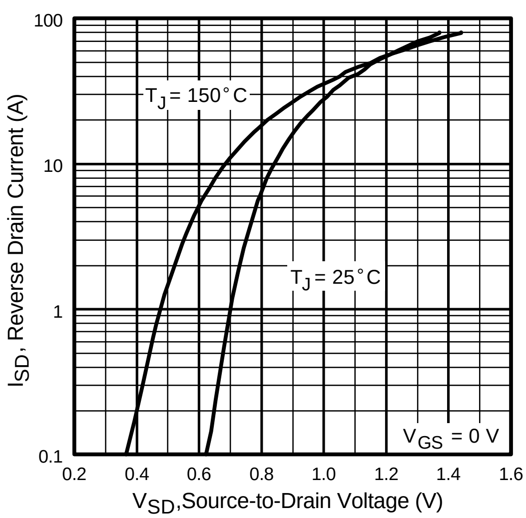


Fig 7. Typical Source-Drain Diode Forward Voltage

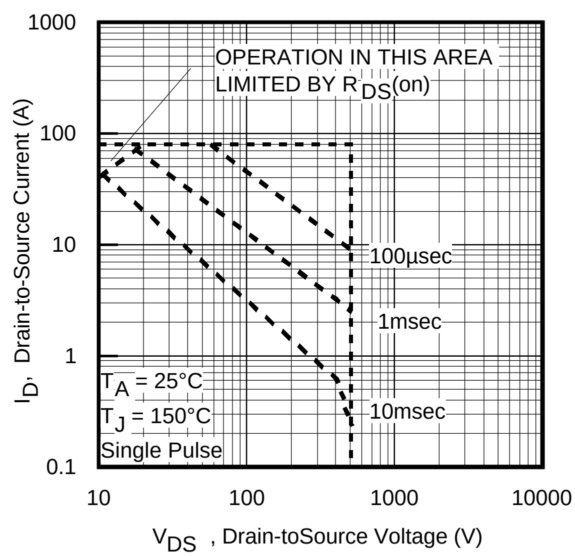


Fig 8. Maximum Safe Operating Area

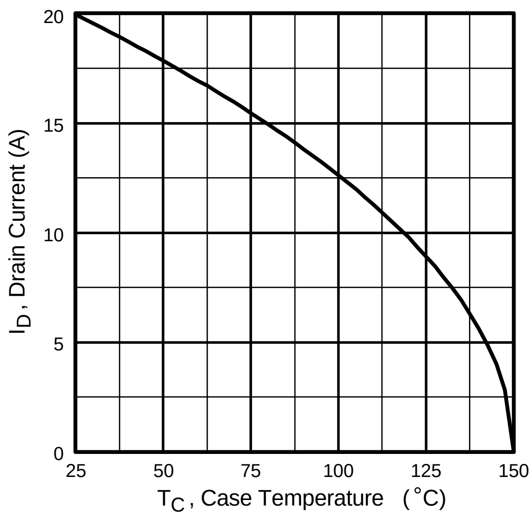


Fig 9. Maximum Drain Current Vs. Case Temperature

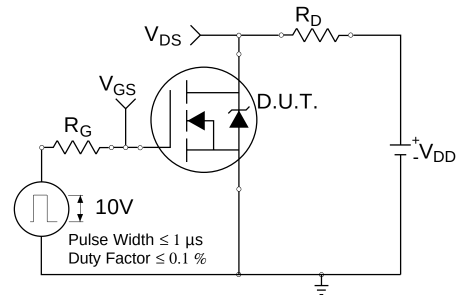


Fig 10a. Switching Time Test Circuit

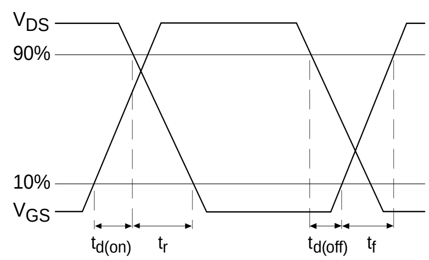


Fig 10b. Switching Time Waveforms

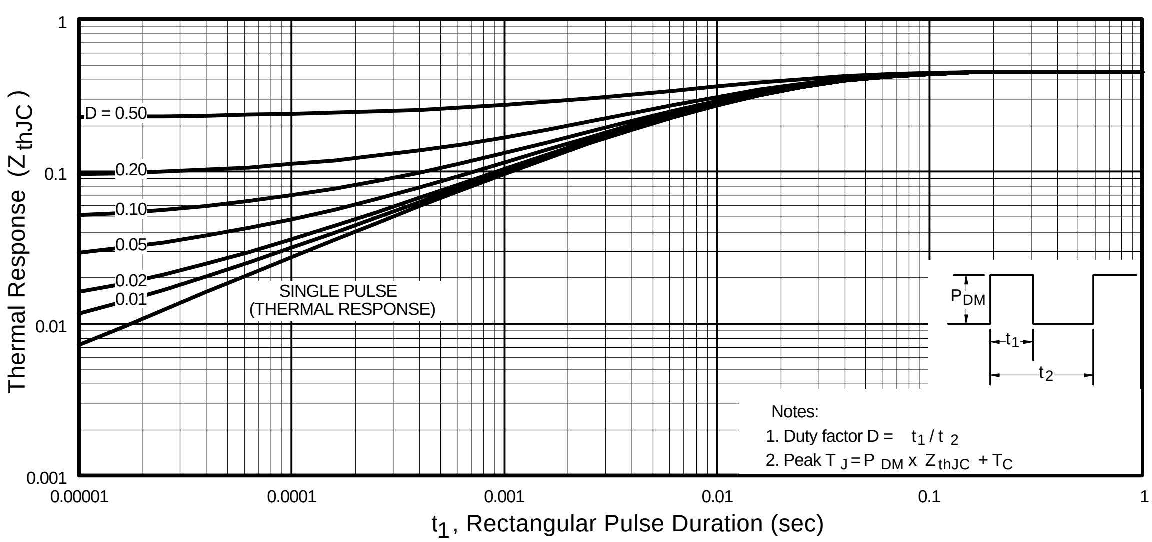


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

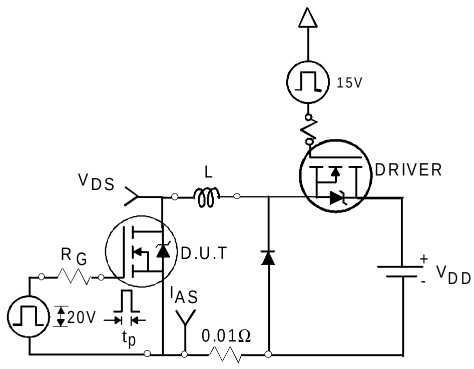


Fig 12a. Unclamped Inductive Test Circuit

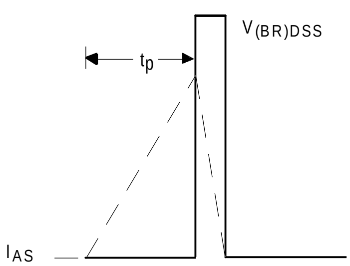


Fig 12b. Unclamped Inductive Waveforms

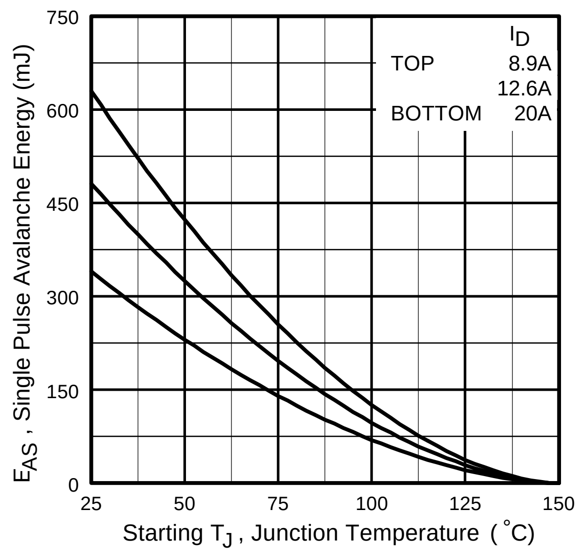


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

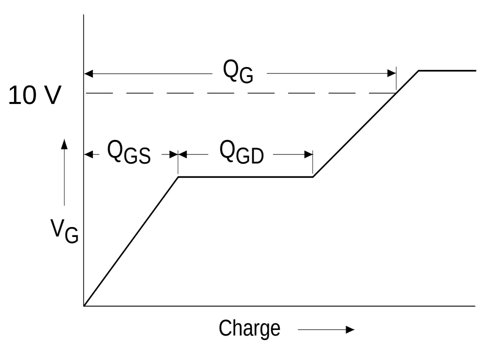


Fig 13a. Basic Gate Charge Waveform

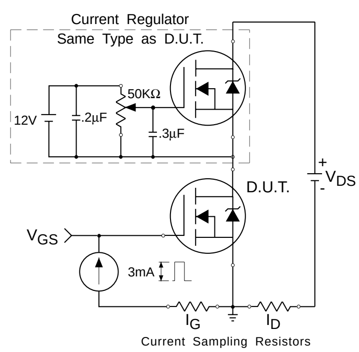
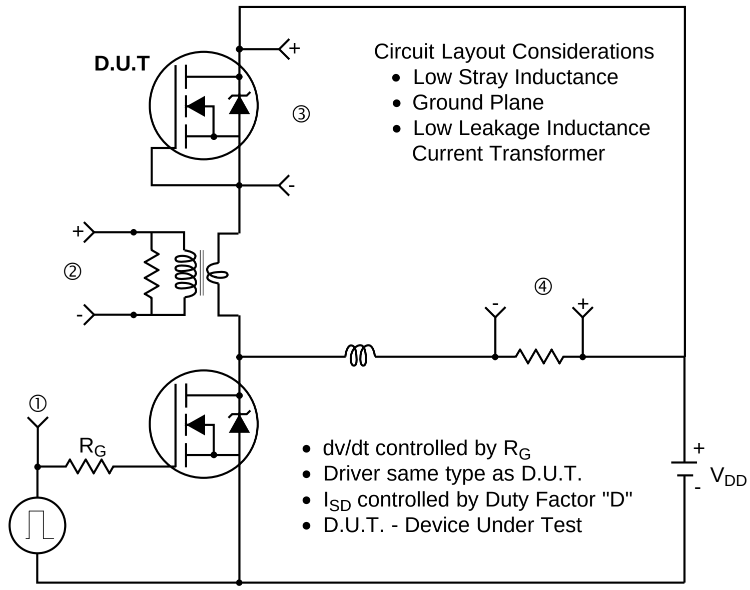
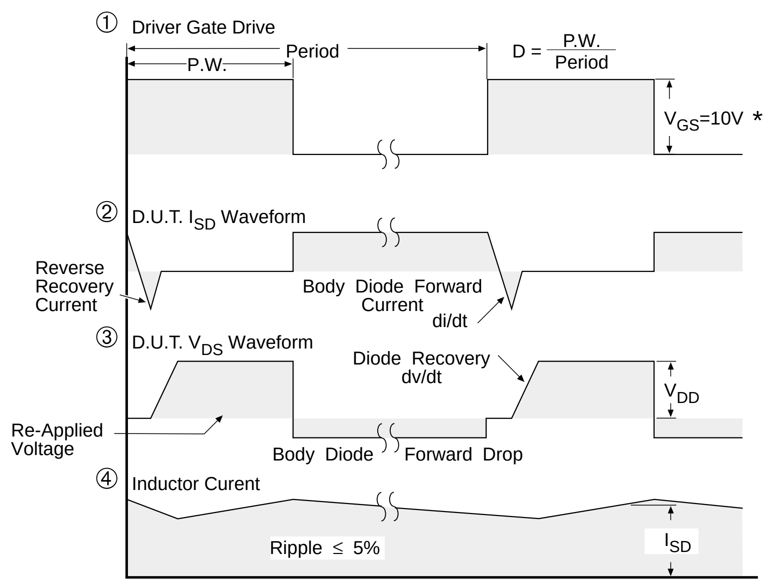


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit





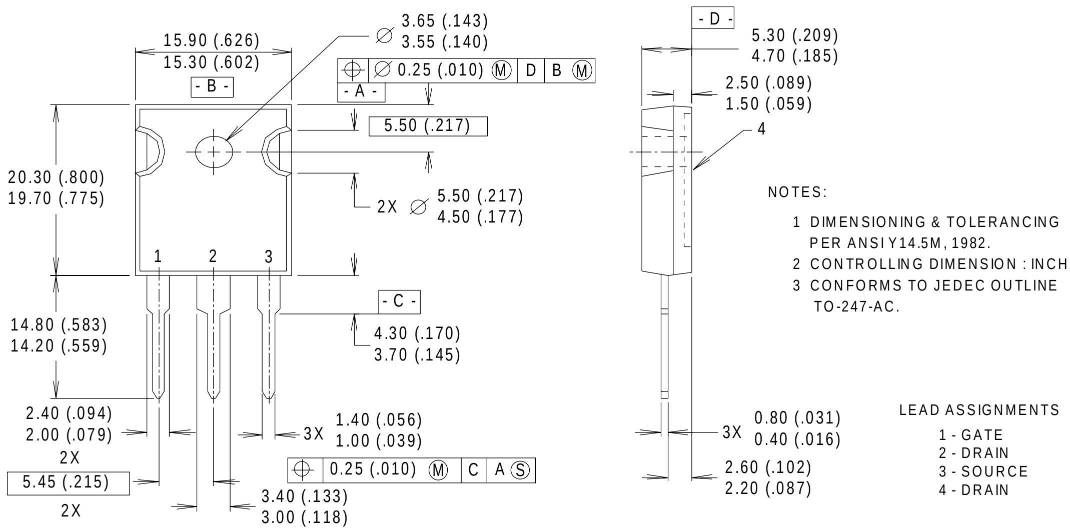
* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

Package Outline

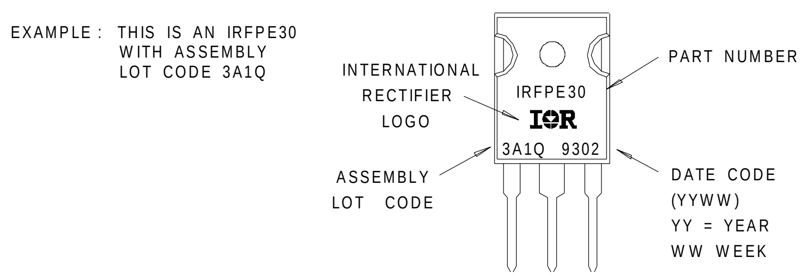
TO-247AC

Dimensions are shown in millimeters (inches)



Part Marking Information

TO-247AC



Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting $T_J = 25°C$, L = 1.8mH $R_G = 25\Omega$, $I_{AS} = 20A$. (See Figure 12)

③ $I_{SD} \le 20A$, di/dt $\le$ 140A/µs, $V_{DD} \le V_{(BR)DSS}$, $T_J \le 150°C$

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web site.

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.

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