

REPETITIVE AVALANCHE AND dv/dt RATED HEXFET[®] TRANSISTORS THRU-HOLE (TO-204AA/AE)

IRFAG50 1000V, N-CHANNEL

Product Summary

Part Number	BVDSS	RDS(on)	Id
IRFAG50	1000V	2.0 Ω	5.6A

The HEXFET[®] technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dv/dt capability.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high energy pulse circuits.



TO-3

Features:

- Repetitive Avalanche Ratings
- Dynamic dv/dt Rating
- Hermetically Sealed
- Simple Drive Requirements
- Ease of Paralleling

Absolute Maximum Ratings

	Parameter		Units
I_D @ $V_{GS} = 0V$, $T_C = 25^\circ C$	Continuous Drain Current	5.6	A
I_D @ $V_{GS} = 0V$, $T_C = 100^\circ C$	Continuous Drain Current	3.5	
I_{DM}	Pulsed Drain Current ①	22	
P_D @ $T_C = 25^\circ C$	Max. Power Dissipation	150	W
	Linear Derating Factor	1.2	W/ $^\circ C$
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	860	mJ
I_{AR}	Avalanche Current ①	5.6	A
E_{AR}	Repetitive Avalanche Energy ①	15	mJ
dv/dt	Peak Diode Recovery dv/dt ③	1.0	V/ns
T_J	Operating Junction	-55 to 150	$^\circ C$
T_{STG}	Storage Temperature Range		
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)	
	Weight	11.5(typical)	g

For footnotes refer to the last page

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	1000	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔBV _{DSS} /ΔT _j	Temperature Coefficient of Breakdown Voltage	—	1.4	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	2.0	Ω	V _{GS} = 10V, I _D = 3.5A④
		—	—	2.3		V _{GS} = 10V, I _D = 5.6A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250mA
g _{fs}	Forward Transconductance	5.2	—	—	S (Ω)	V _{DS} > 15V, I _{DS} = 3.5A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	25	μA	V _{DS} = 800V, V _{GS} = 0V
		—	—	250		V _{DS} = 800V V _{GS} = 0V, T _j = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Q _g	Total Gate Charge	88	—	200	nC	V _{GS} = 10V, I _D = 5.6A V _{DS} = 500V
Q _{gs}	Gate-to-Source Charge	8.8	—	20		
Q _{gd}	Gate-to-Drain ('Miller') Charge	48	—	110		
t _{d(on)}	Turn-On Delay Time	—	—	30	ns	V _{DD} = 400V*, I _D = 5.6A, R _G = 2.35Ω
t _r	Rise Time	—	—	44		
t _{d(off)}	Turn-Off Delay Time	—	—	210		
t _f	Fall Time	—	—	60		
L _S + L _D	Total Inductance	—	6.1	—	nH	Measured from drain lead (6mm/0.25in. from package) to source lead (6mm/0.25in. from package)
C _{iss}	Input Capacitance	—	2400	—	pF	V _{GS} = 0V, V _{DS} = 25V f = 1.0MHz
C _{oss}	Output Capacitance	—	240	—		
C _{rss}	Reverse Transfer Capacitance	—	80	—		

*Equipment Limitation

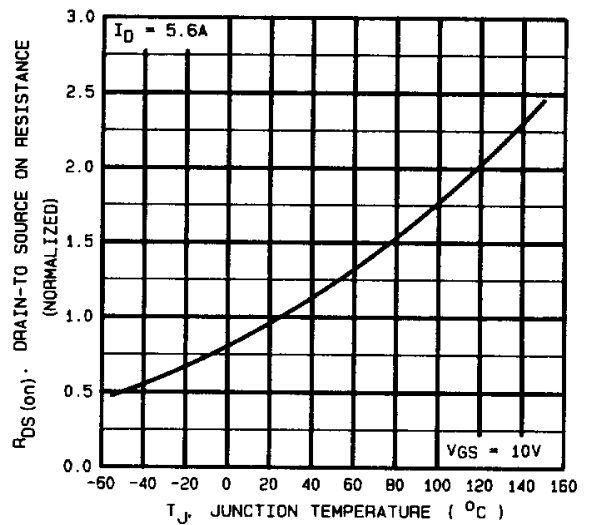
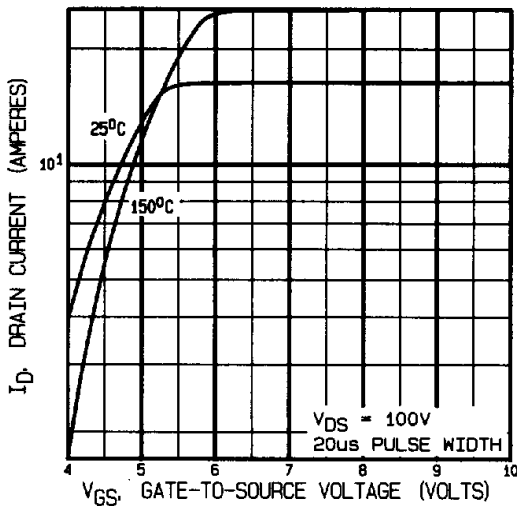
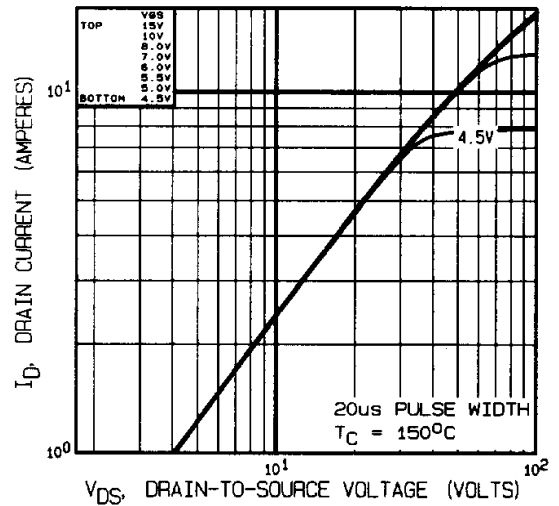
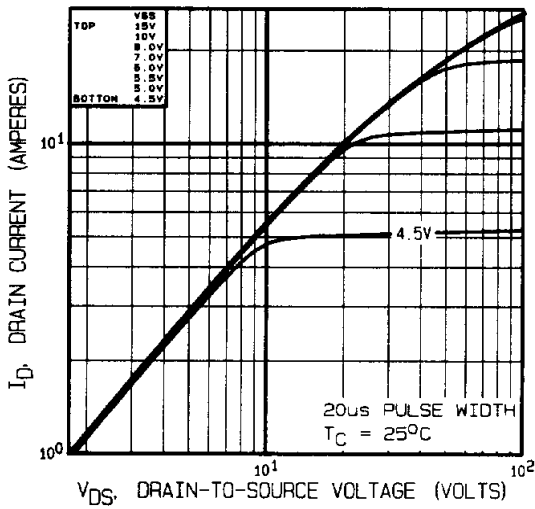
Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	5.6	A	
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	22		
V _{SD}	Diode Forward Voltage	—	—	1.8	V	T _j = 25°C, I _S =5.6A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	1200	nS	T _j = 25°C, I _F =5.6A, di/dt ≤ 100A/μs V _{DD} ≤ 50V ④
Q _{RR}	Reverse Recovery Charge	—	—	8.4	μC	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction to Case	—	—	0.83	°C/W	
R _{thJA}	Junction to Ambient	—	—	30		Typical socket mount

For footnotes refer to the last page



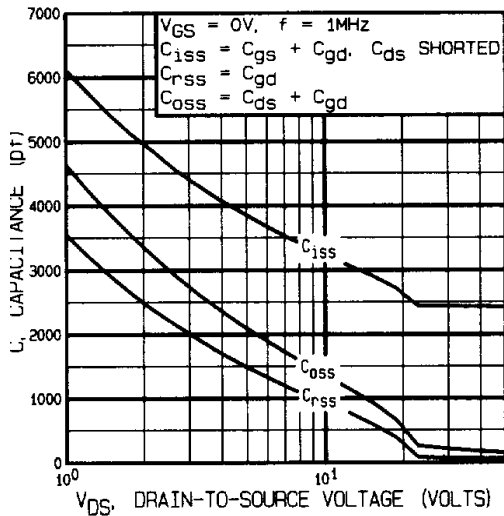


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

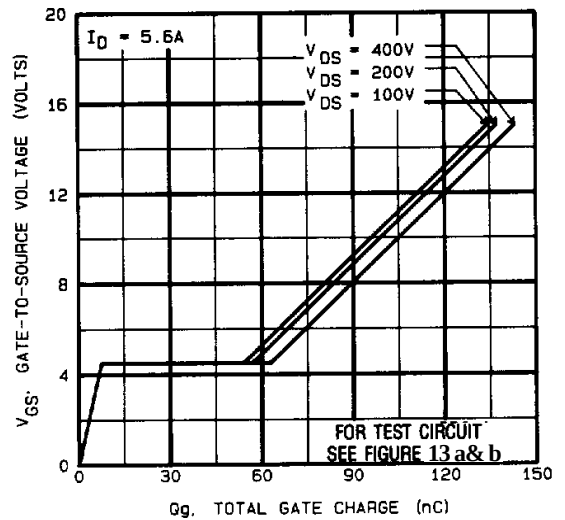


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

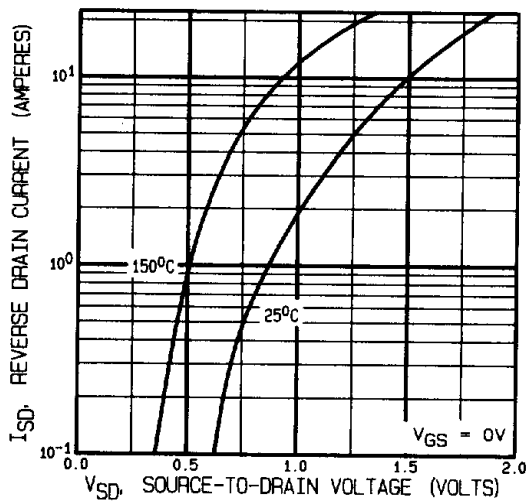


Fig 7. Typical Source-Drain Diode Forward Voltage

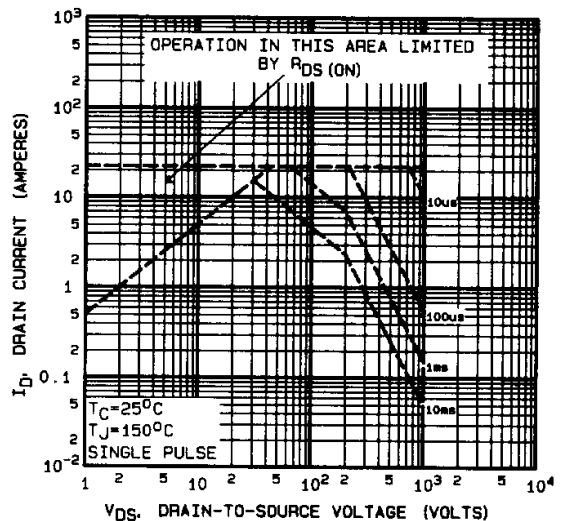


Fig 8. Maximum Safe Operating Area

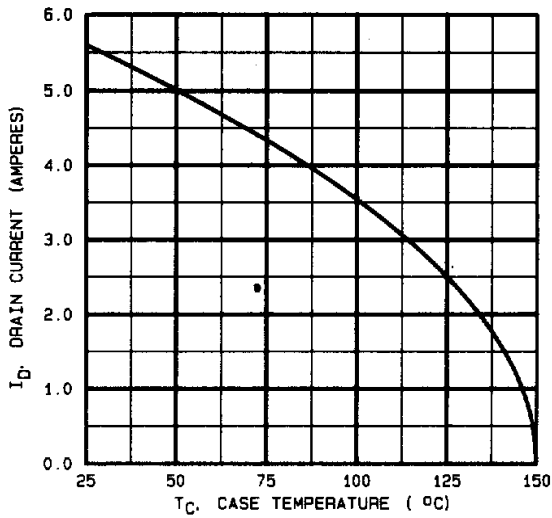


Fig 9. Maximum Drain Current Vs. Case Temperature

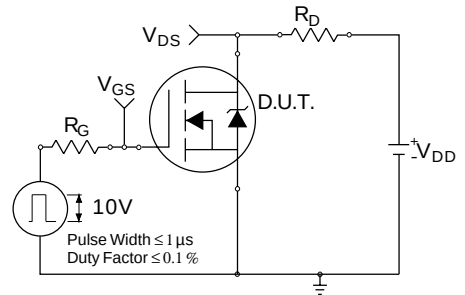


Fig 10a. Switching Time Test Circuit

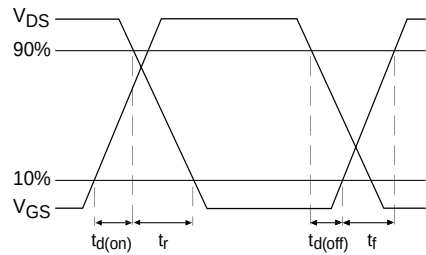


Fig 10b. Switching Time Waveforms

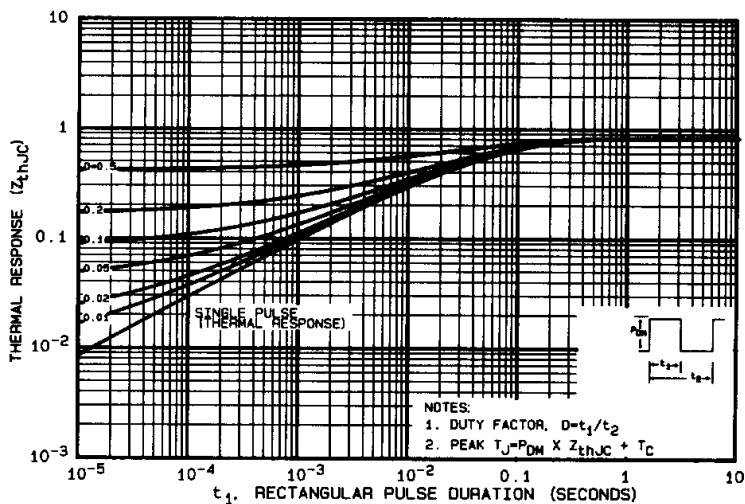


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

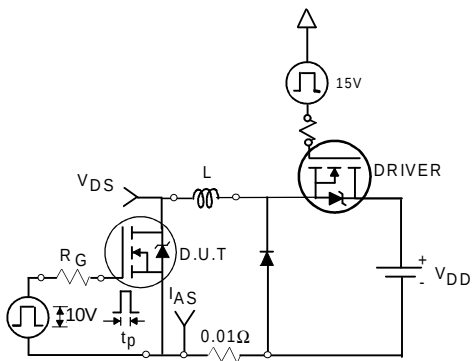


Fig 12a. Unclamped Inductive Test Circuit

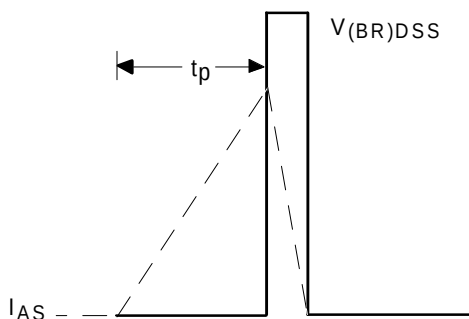


Fig 12b. Unclamped Inductive Waveforms

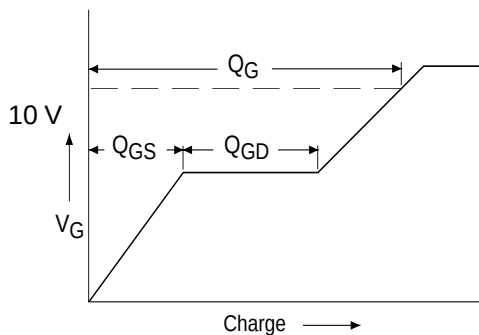


Fig 13a. Basic Gate Charge Waveform

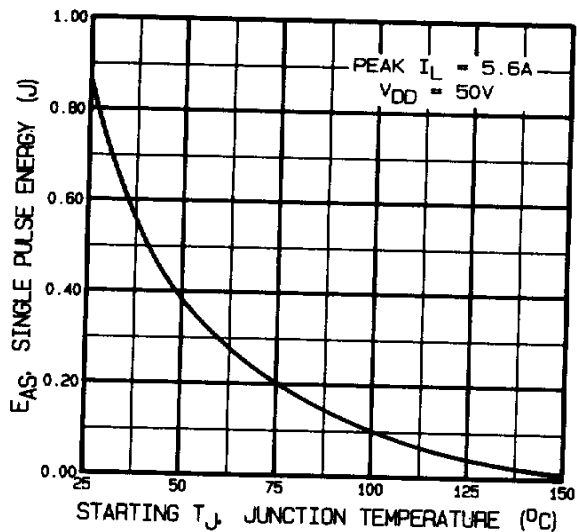
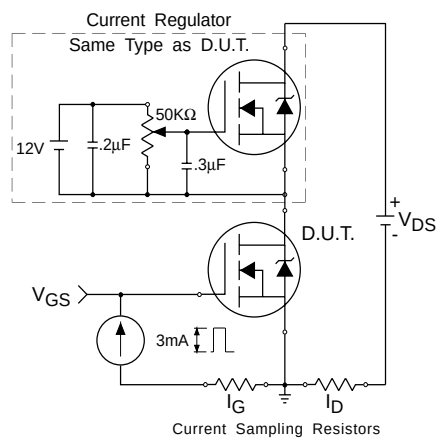
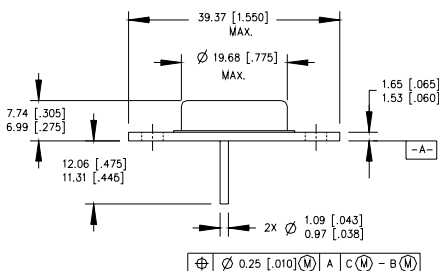
Fig 12c. Maximum Avalanche Energy
Vs. Drain Current

Fig 13b. Gate Charge Test Circuit

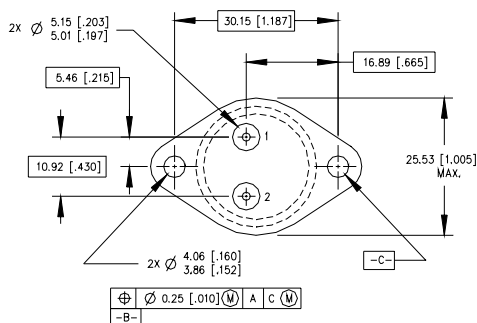
Foot Notes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = 50V$, starting $T_J = 25^{\circ}C$, Peak $I_L = 5.6A$,
- ③ $I_{SD} \leq 5.6A$, $di/dt \leq 120A/\mu s$, $V_{DD} \leq 1000V$, $T_J \leq 150^{\circ}C$
Suggested $R_G = 2.35 \Omega$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$

Case Outline and Dimensions —TO-204AA (Modified TO-3)



PIN ASSIGNMENTS		
HEXFET	SCHOTTKY	IGBT
1 - SOURCE	1 - ANODE 1	1 - GATE
2 - GATE	2 - ANODE 2	2 - EMITTER
3 - DRAIN (CASE)	3 - COMMON CATHODE (CASE)	3 - COLLECTOR (CASE)



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION : INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-204-AA.

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Data and specifications subject to change without notice. 1/01