International IOR Rectifier

AUTOMOTIVE MOSFET

IRF540Z
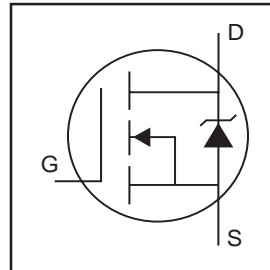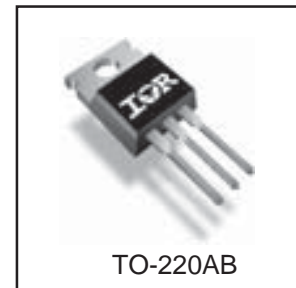
HEXFET® Power MOSFET

Features
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax

$V_{DSS} = 100V$

$R_{DS(on)} = 29.5m\Omega$

$I_D = 34A$

Description
Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating . These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	34	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (See Fig. 9)	24	
I_{DM}	Pulsed Drain Current ①	140	
P_D @T_C = 25°C	Maximum Power Dissipation	91	W
	Linear Derating Factor	0.61	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②	96	mJ
E_{AS} (tested)	Single Pulse Avalanche Energy Tested Value ⑦	120	
I_{AR}	Avalanche Current ①	See Fig.12a,12b,15,16	A
E_{AR}	Repetitive Avalanche Energy ⑥		mJ
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

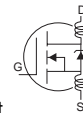|	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	1.64	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient	——	62	

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Static @ T$_J$ = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V$_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	——	——	V	V$_{GS}$ = 0V, I$_D$ = 250µA
ΔBV$_{DSS}$/ΔT$_J$	Breakdown Voltage Temp. Coefficient	——	0.088	——	V/°C	Reference to 25°C, I$_D$ = 1mA
R$_{DS(on)}$	Static Drain-to-Source On-Resistance	——	23.5	29.5	mΩ	V$_{GS}$ = 10V, I$_D$ = 20A ④
V$_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V$_{DS}$ = V$_{GS}$, I$_D$ = 250µA
gfs	Forward Transconductance	52	——	——	S	V$_{DS}$ = 25V, I$_D$ = 20A
I$_{DSS}$	Drain-to-Source Leakage Current	——	——	20	µA	V$_{DS}$ = 100V, V$_{GS}$ = 0V
		——	——	250		V$_{DS}$ = 100V, V$_{GS}$ = 0V, T$_J$ = 125°C
I$_{GSS}$	Gate-to-Source Forward Leakage	——	——	200	nA	V$_{GS}$ = 20V
	Gate-to-Source Reverse Leakage	——	——	-200		V$_{GS}$ = -20V
Q$_g$	Total Gate Charge	——	40	61	nC	I$_D$ = 20A
Q$_{gs}$	Gate-to-Source Charge	——	9.6	14		V$_{DS}$ = 80V
Q$_{gd}$	Gate-to-Drain ("Miller") Charge	——	15	23		V$_{GS}$ = 10V ④
t$_{d(on)}$	Turn-On Delay Time	——	15	——	ns	V$_{DD}$ = 50V
t$_r$	Rise Time	——	53	——		I$_D$ = 20A
t$_{d(off)}$	Turn-Off Delay Time	——	45	——		R$_G$ = 12Ω
t$_f$	Fall Time	——	47	——		V$_{GS}$ = 10V ④
L$_D$	Internal Drain Inductance	——	4.5	——	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L$_S$	Internal Source Inductance	——	7.5	——		
C$_{iss}$	Input Capacitance	——	1800	——	pF	V$_{GS}$ = 0V
C$_{oss}$	Output Capacitance	——	170	——		V$_{DS}$ = 25V
C$_{rss}$	Reverse Transfer Capacitance	——	94	——		f = 1.0MHz, See Fig. 5
C$_{oss}$	Output Capacitance	——	710	——		V$_{GS}$ = 0V, V$_{DS}$ = 1.0V, f = 1.0MHz
C$_{oss}$	Output Capacitance	——	110	——		V$_{GS}$ = 0V, V$_{DS}$ = 80V, f = 1.0MHz
C$_{oss}$ eff.	Effective Output Capacitance	——	180	——		V$_{GS}$ = 0V, V$_{DS}$ = 0V to 80V

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I$_S$	Continuous Source Current (Body Diode)	——	——	34	A	MOSFET symbol showing the integral reverse p-n junction diode.
I$_{SM}$	Pulsed Source Current (Body Diode) ①	——	——	140		
V$_{SD}$	Diode Forward Voltage	——	——	1.3	V	T$_J$ = 25°C, I$_S$ = 20A, V$_{GS}$ = 0V ④
t$_{rr}$	Reverse Recovery Time	——	42	63	ns	T$_J$ = 25°C, I$_F$ = 20A, V$_{DD}$ = 50V
Q$_{rr}$	Reverse Recovery Charge	——	82	120	nC	di/dt = 100A/µs ④
t$_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Limited by T$_{Jmax}$, starting T$_J$ = 25°C, L = 0.46mH, R$_G$ = 25Ω, I$_{AS}$ = 20A, V$_{GS}$ =10V. Part not recommended for use above this value.

③ I$_{SD}$ ≤ 20A, di/dt ≤ 400A/µs, V$_{DD}$ ≤ V$_{(BR)DSS}$, T$_J$ ≤ 175°C.

④ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.

⑤ C$_{oss}$ eff. is a fixed capacitance that gives the same charging time as C$_{oss}$ while V$_{DS}$ is rising from 0 to 80% V$_{DSS}$.

⑥ Limited by T$_{Jmax}$, see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

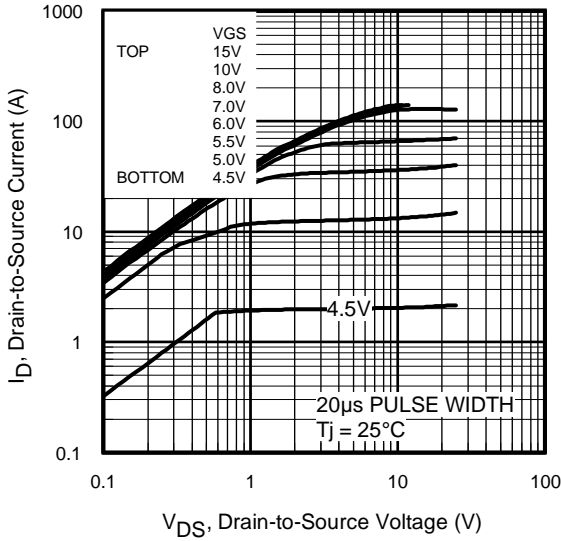⑦ This value determined from sample failure population. 100% tested to this value in production.
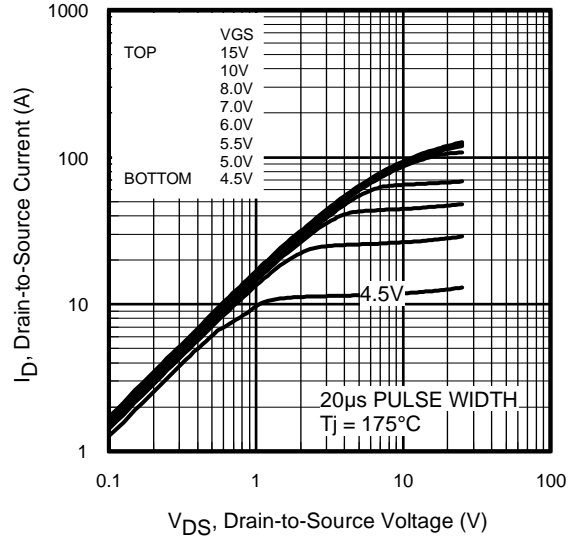
Fig 1. Typical Output Characteristics
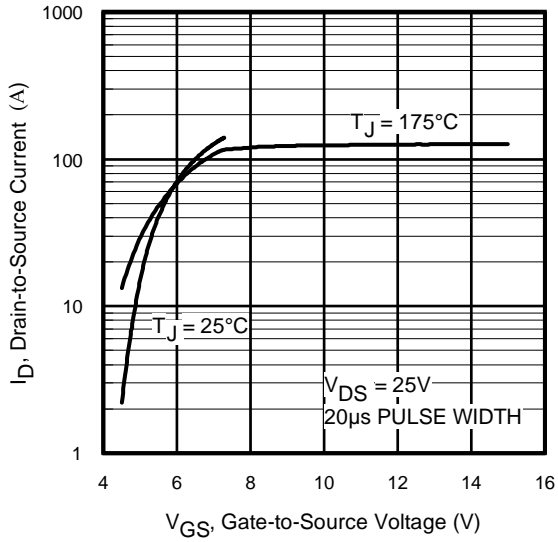

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics
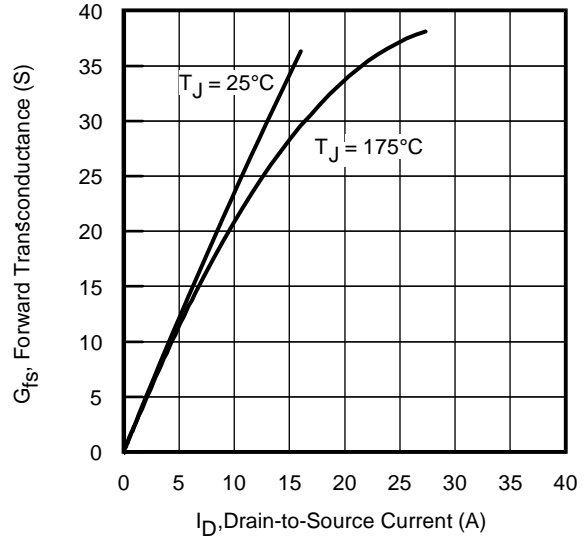

Fig 4. Typical Forward Transconductance vs. Drain Current
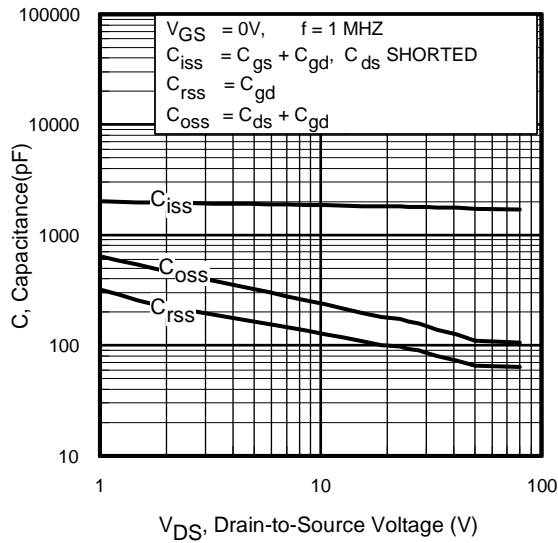
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Fig 5. Typical Capacitance vs.
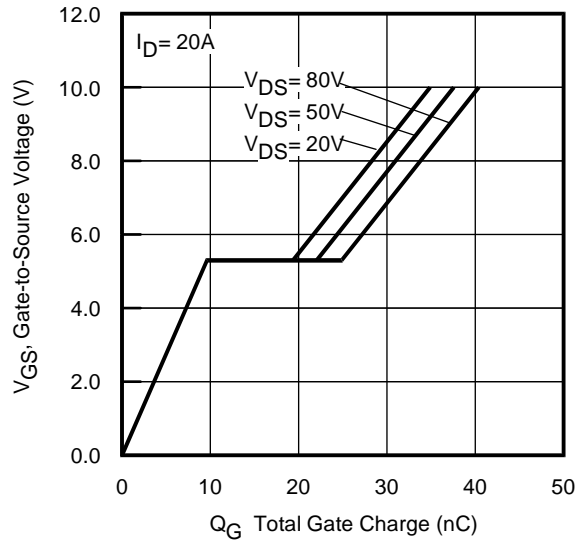Drain-to-Source Voltage
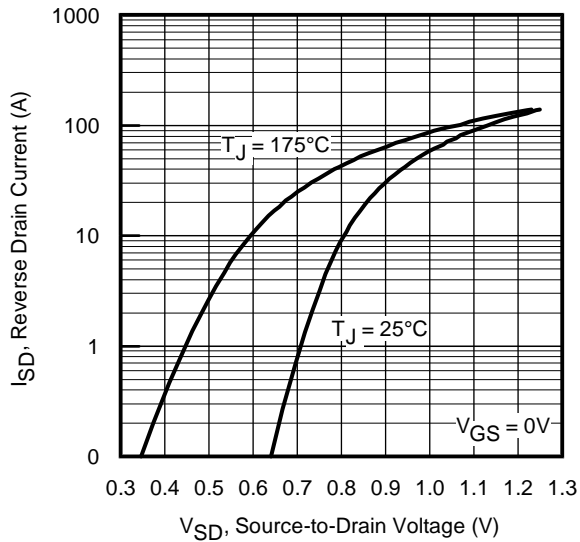

Fig 6. Typical Gate Charge vs.
Gate-to-Source Voltage
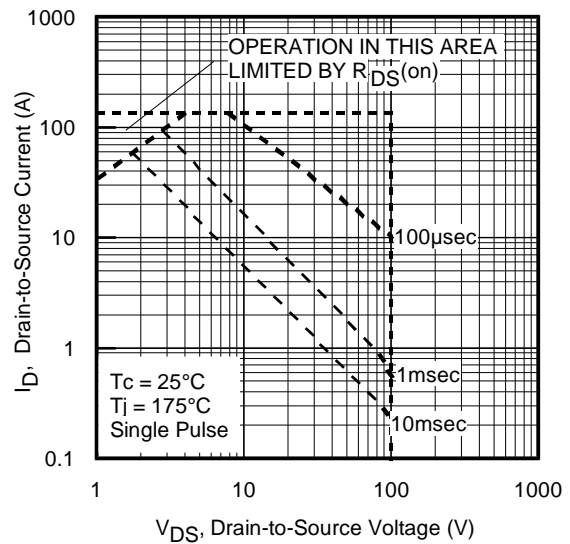

Fig 7. Typical Source-Drain Diode
Forward Voltage

Fig 8. Maximum Safe Operating Area
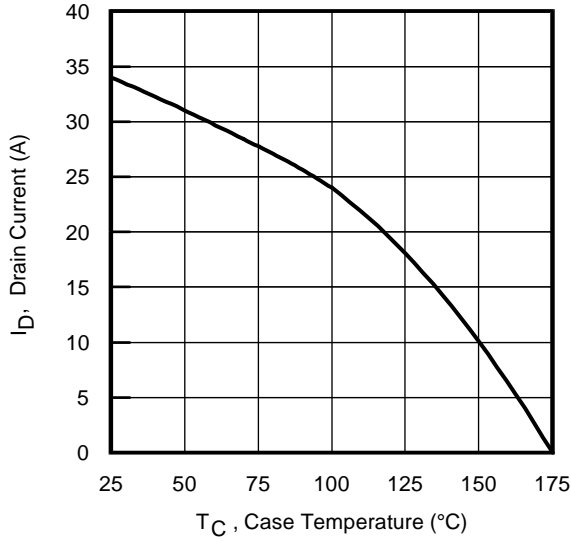
4

Fig 9. Maximum Drain Current vs. Case Temperature
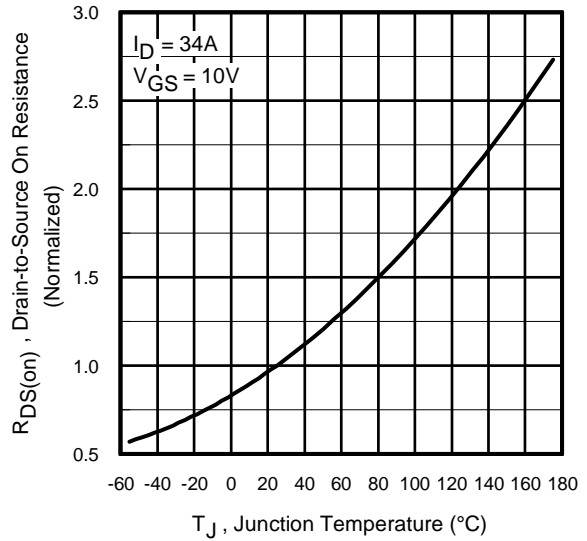

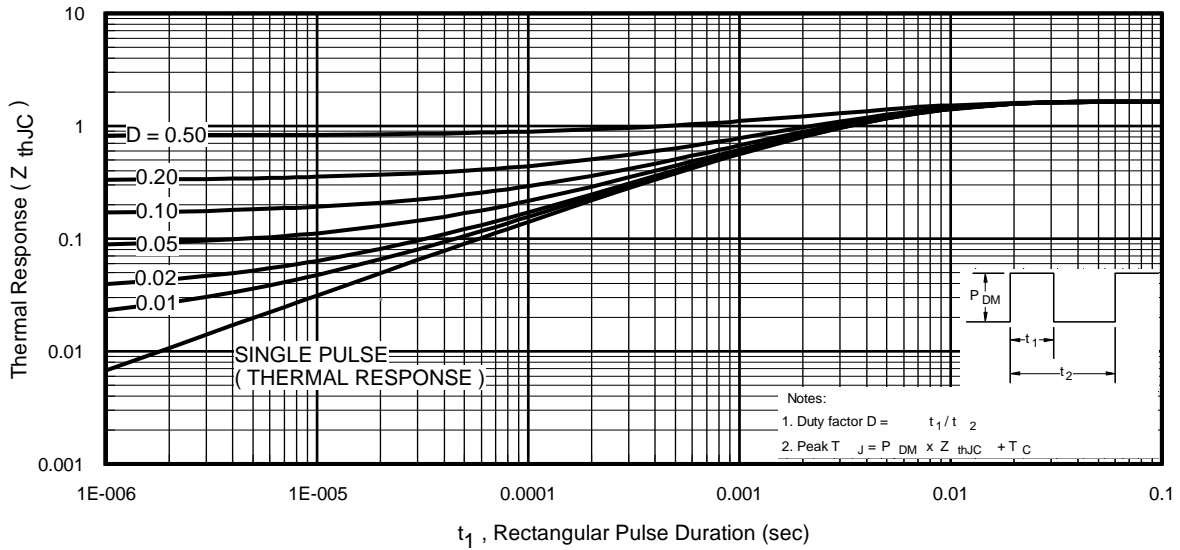**Fig 10.** Normalized On-Resistance vs. Temperature

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case
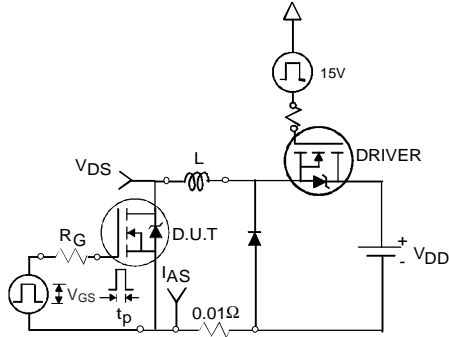
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Fig 12a. Unclamped Inductive Test Circuit

Fig 12b. Unclamped Inductive Waveforms

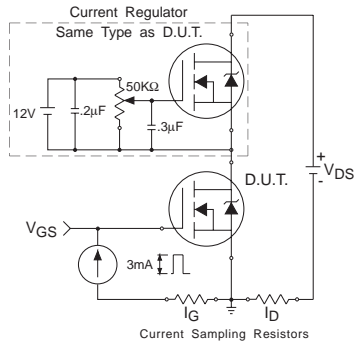**Fig 13a.** Basic Gate Charge Waveform
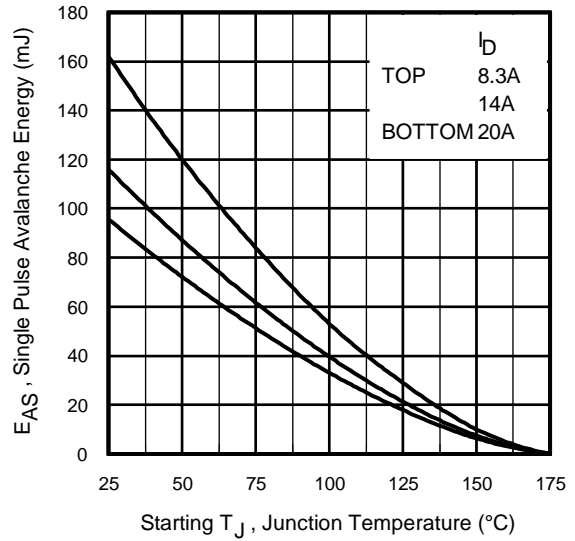

Fig 13b. Gate Charge Test Circuit

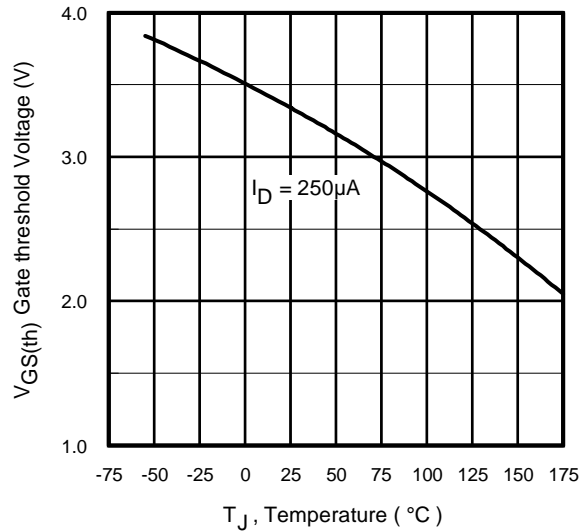**Fig 12c.** Maximum Avalanche Energy
vs. Drain Current

Fig 14. Threshold Voltage vs. Temperature

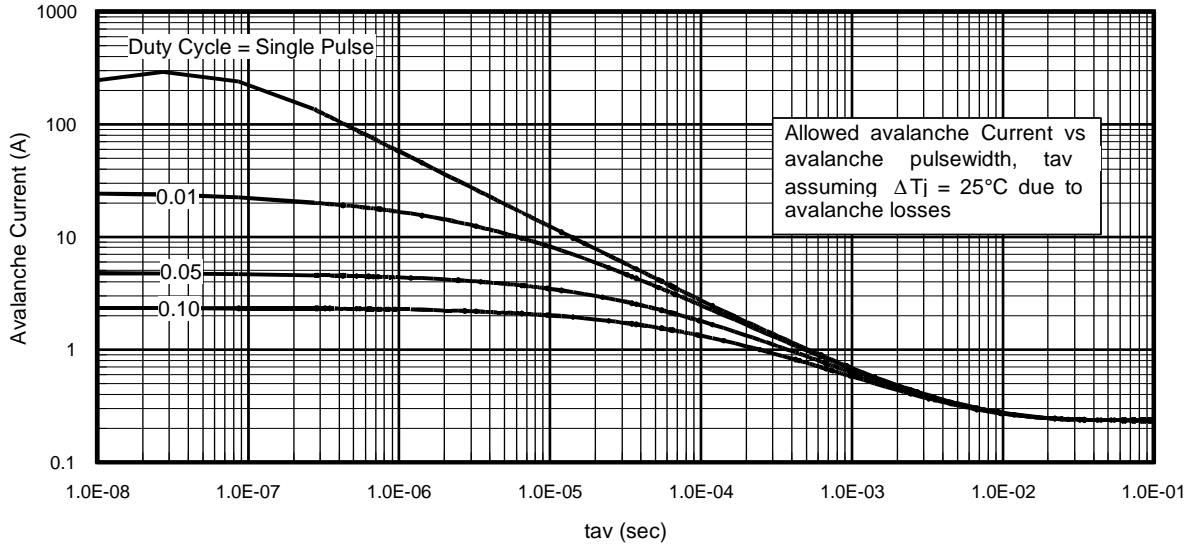Avalanche Current (A) vs tav (sec)

Duty Cycle = Single Pulse

0.01
0.05
0.10

Allowed avalanche Current vs avalanche pulsewidth, tav assuming ∆Tj = 25°C due to avalanche losses

Fig 15. Typical Avalanche Current vs.Pulsewidth

E_{AR}, Avalanche Energy (mJ) vs Starting T_J, Junction Temperature (°C)

TOP   Single Pulse
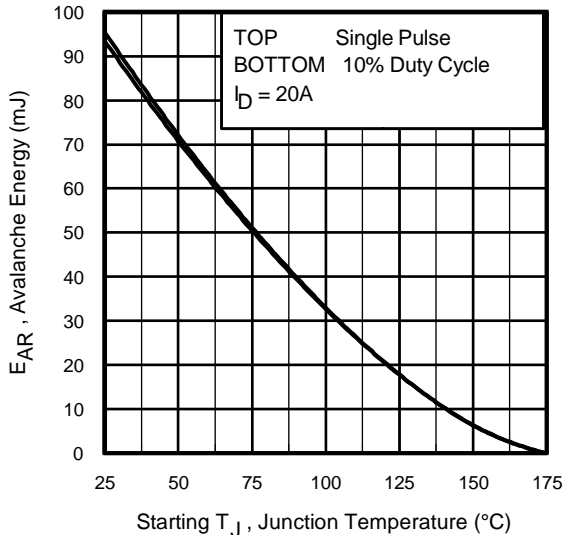BOTTOM   10% Duty Cycle
I_D = 20A

Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T/\ Z_{thJC}$$
$$I_{av} = 2\Delta T/\ [1.3 \cdot BV \cdot Z_{th}]$$
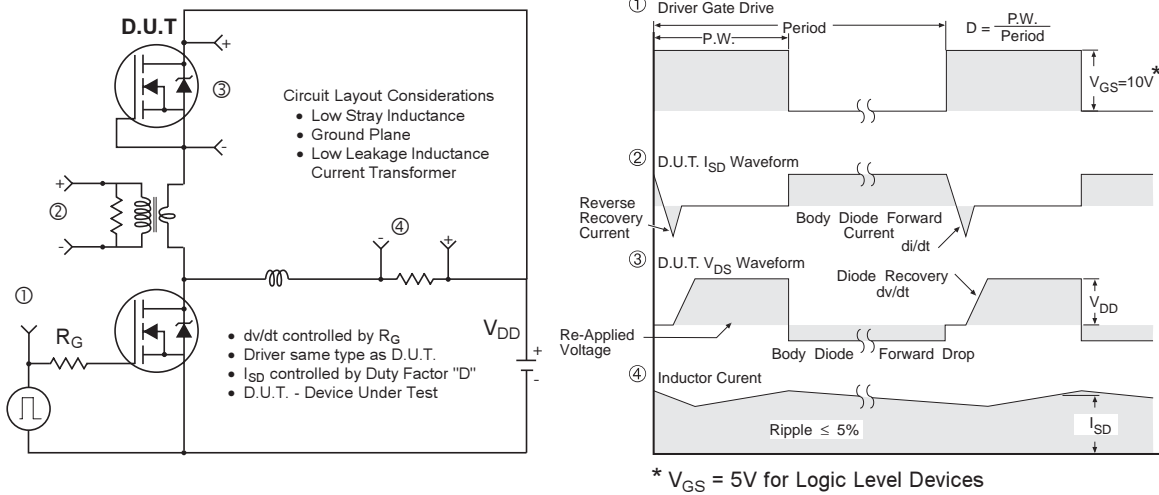$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

Circuit Layout Considerations
• Low Stray Inductance
• Ground Plane
• Low Leakage Inductance
  Current Transformer

• dv/dt controlled by R_G
• Driver same type as D.U.T.
• I_{SD} controlled by Duty Factor "D"
• D.U.T. - Device Under Test

① Driver Gate Drive

$D = \dfrac{P.W.}{Period}$

$V_{GS}=10V$*

② D.U.T. I_{SD} Waveform

Reverse Recovery Current
Body Diode Forward Current
di/dt

③ D.U.T. V_{DS} Waveform

Diode Recovery dv/dt

V_{DD}

Re-Applied Voltage
Body Diode Forward Drop

④ Inductor Curent

Ripple ≤ 5%
I_{SD}

* V_{GS} = 5V for Logic Level Devices

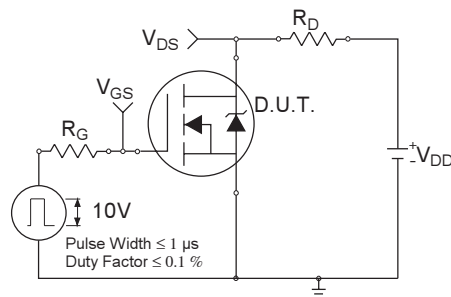**Fig 17.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

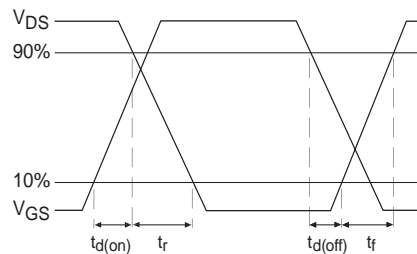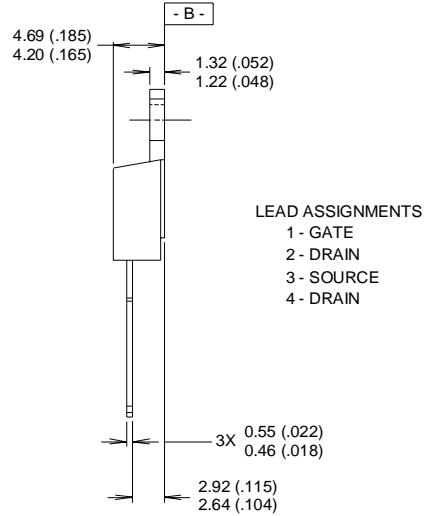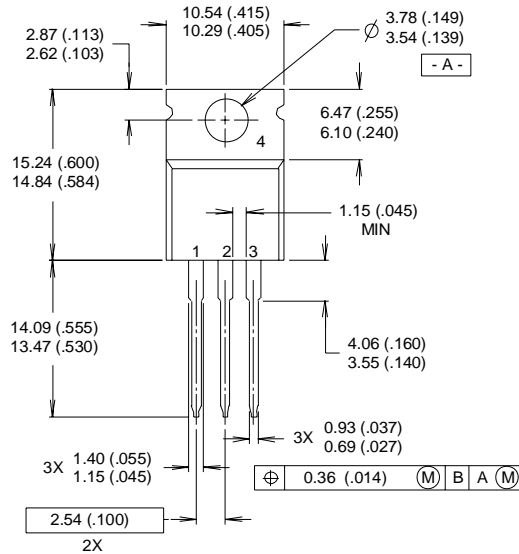**Fig 18a.** Switching Time Test Circuit

Fig 18b. Switching Time Waveforms

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN
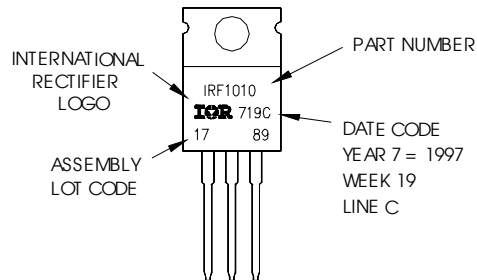
NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

ASSEMBLY LOT CODE

DATE CODE
YEAR 7 = 1997
WEEK 19
LINE C

TO-220AB package is not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Automotive [Q101] market.
Qualification Standards can be found on IR's Web site.

International **I꒝R** Rectifier