International IⓇR Rectifier

**AUTOMOTIVE MOSFET**

IRF2805

HEXFET® Power MOSFET

Typical Applications
- Climate Control, ABS, Electronic Braking, Windshield Wipers

Features
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
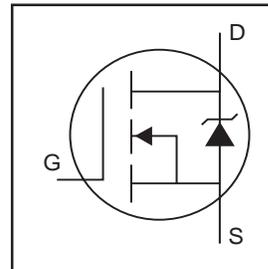
$V_{DSS} = 55V$

$R_{DS(on)} = 4.7m\Omega$

$I_D = 75A$

TO-220AB

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.
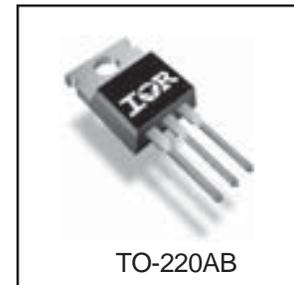
Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon limited)	175	
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (See Fig.9)	120	A
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Package limited)	75	
I_{DM}	Pulsed Drain Current ①	700	
P_D @T_C = 25°C	Power Dissipation	330	W
	Linear Derating Factor	2.2	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	450	mJ
E_{AS} (6 sigma)	Single Pulse Avalanche Energy Tested Value⑦	1220	
I_{AR}	Avalanche Current①	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy⑥		mJ
T_J	Operating Junction and	-55 to + 175	
T_{STG}	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	1.1 (10)	N•m (lbf•in)

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.45	
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	——	°C/W
$R_{\theta JA}$	Junction-to-Ambient	——	62	

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions	
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	——	——	V	V_{GS} = 0V, I_D = 250μA	
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.06	——	V/°C	Reference to 25°C, I_D = 1mA	
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	3.9	4.7	mΩ	V_{GS} = 10V, I_D = 104A ④	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = 10V, I_D = 250μA	
g_{fs}	Forward Transconductance	91	——	——	S	V_{DS} = 25V, I_D = 104A	
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	μA	V_{DS} = 55V, V_{GS} = 0V	
		——	——	250		V_{DS} = 55V, V_{GS} = 0V, T_J = 125°C	
I_{GSS}	Gate-to-Source Forward Leakage	——	——	200	nA	V_{GS} = 20V	
	Gate-to-Source Reverse Leakage	——	——	-200		V_{GS} = -20V	
Q_g	Total Gate Charge	——	150	230		I_D = 104A	
Q_{gs}	Gate-to-Source Charge	——	38	57	nC	V_{DS} = 44V	
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	52	78		V_{GS} = 10V④	
$t_{d(on)}$	Turn-On Delay Time	——	14	——		V_{DD} = 28V	
t_r	Rise Time	——	120	——	ns	I_D = 104A	
$t_{d(off)}$	Turn-Off Delay Time	——	68	——		R_G = 2.5Ω	
t_f	Fall Time	——	110	——		V_{GS} = 10V ④	
L_D	Internal Drain Inductance	——	4.5	——	nH	Between lead, 6mm (0.25in.) from package and center of die contact	
L_S	Internal Source Inductance	——	7.5	——			
C_{iss}	Input Capacitance	——	5110	——		V_{GS} = 0V	
C_{oss}	Output Capacitance	——	1190	——	pF	V_{DS} = 25V	
C_{rss}	Reverse Transfer Capacitance	——	210	——		f = 1.0MHz, See Fig. 5	
C_{oss}	Output Capacitance	——	6470	——		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz	
C_{oss}	Output Capacitance	——	860	——		V_{GS} = 0V, V_{DS} = 44V, f = 1.0MHz	
C_{oss} eff.	Effective Output Capacitance ⑤	——	1600	——		V_{GS} = 0V, V_{DS} = 0V to 44V	
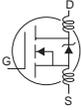
Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions	
I_S	Continuous Source Current (Body Diode)	——	——	175	A	MOSFET symbol showing the integral reverse p-n junction diode.	
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	700			
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 104A, V_{GS} = 0V ④	
t_{rr}	Reverse Recovery Time	——	80	120	ns	T_J = 25°C, I_F = 104A	
Q_{rr}	Reverse Recovery Charge	——	290	430	nC	di/dt = 100A/μs ④	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)					

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Starting T_J = 25°C, L = 0.08mH
  R_G = 25Ω, I_{AS} = 104A. (See Figure 12).

③ I_{SD} ≤ 104A, di/dt ≤ 240A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 400μs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑥ Limited by T_{Jmax}, see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

⑦ This value determined from sample failure population. 100% tested to this value in production.

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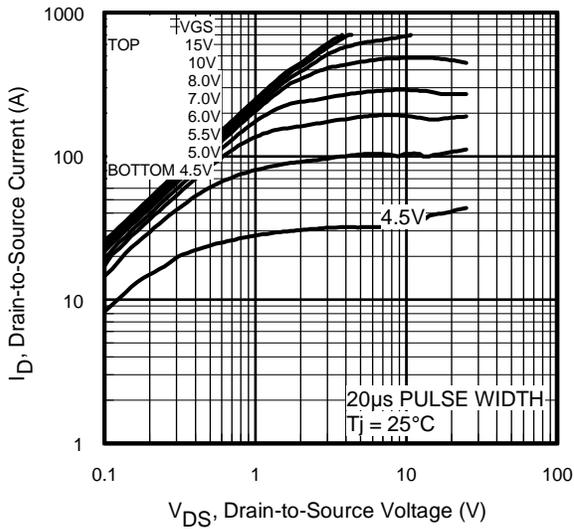
Fig 1. Typical Output Characteristics
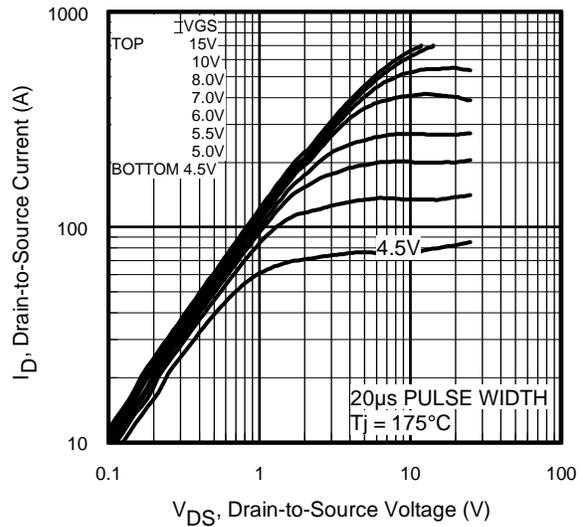

Fig 2. Typical Output Characteristics
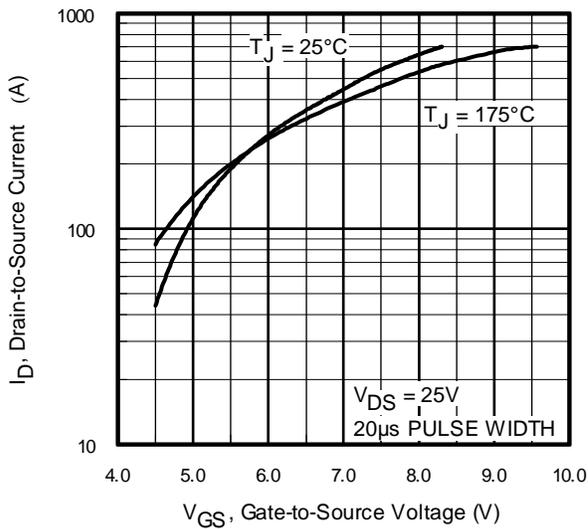
Fig 3. Typical Transfer Characteristics
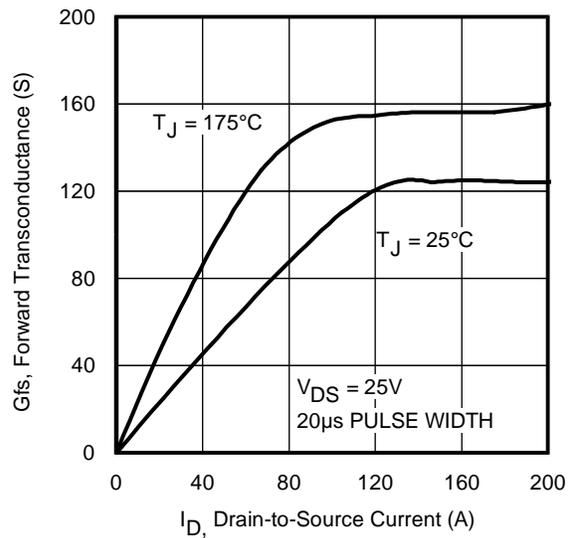
**Fig 4.** Typical Forward Transconductance Vs. Drain Current

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V_{GS} = 0V,   f = 1 MHZ
C_{iss} = C $_{gs}$ + C $_{gd}$, C $_{ds}$ SHORTED
C_{rss} = C_{gd}
C_{oss} = C_{ds} + C_{gd}

Ciss

Coss

Crss

C, Capacitance (pF)

V_{DS}, Drain-to-Source Voltage (V)
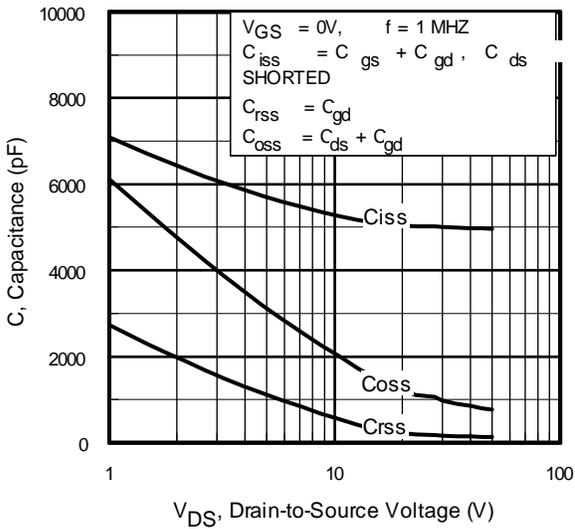
Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

I_D= 104A V_{DS}= 44V
VDS= 28V

V_{GS}, Gate-to-Source Voltage (V)

Q_G Total Gate Charge (nC)
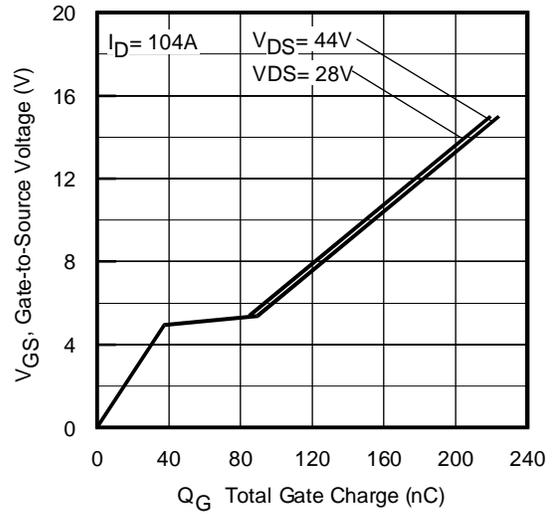
Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

T_J = 175°C

T_J = 25°C

V_{GS} = 0V

I_{SD}, Reverse Drain Current (A)

V_{SD}, Source-toDrain Voltage (V)
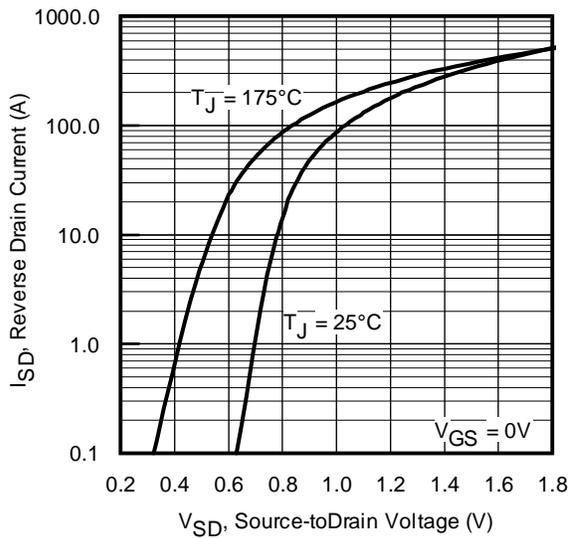
Fig 7. Typical Source-Drain Diode Forward Voltage

OPERATION IN THIS AREA LIMITED BY R_{DS}(on)

100μsec

1msec

Tc = 25°C
Tj = 175°C
Single Pulse

10msec

I_D, Drain-to-Source Current (A)

V_{DS} , Drain-toSource Voltage (V)
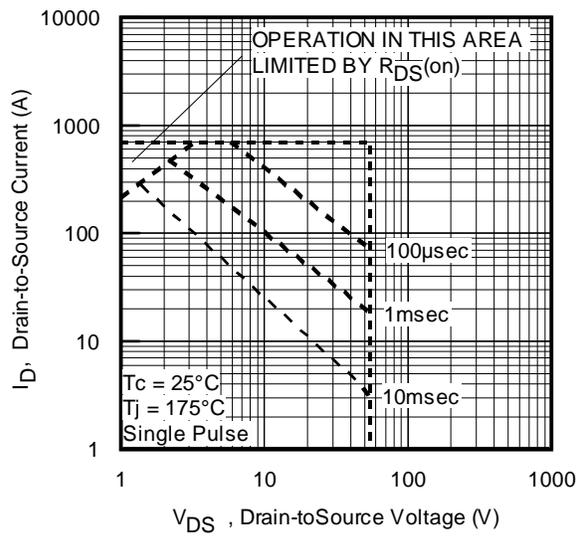
Fig 8. Maximum Safe Operating Area

4
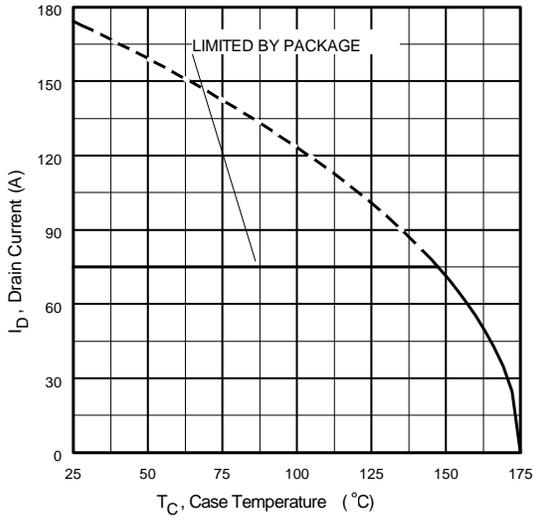
Fig 9. Maximum Drain Current Vs.
Case Temperature
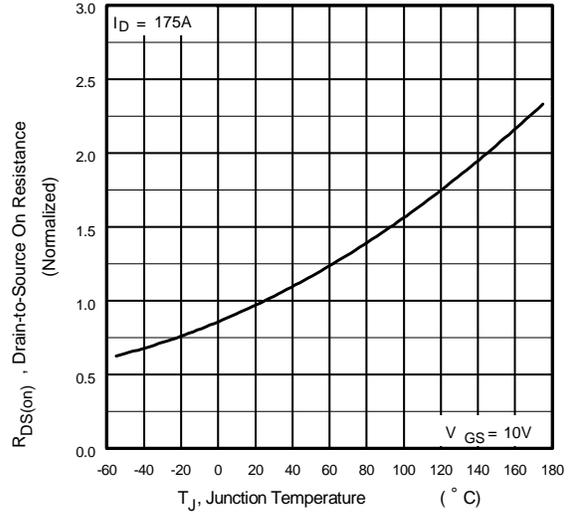
Fig 10. Normalized On-Resistance
Vs. Temperature
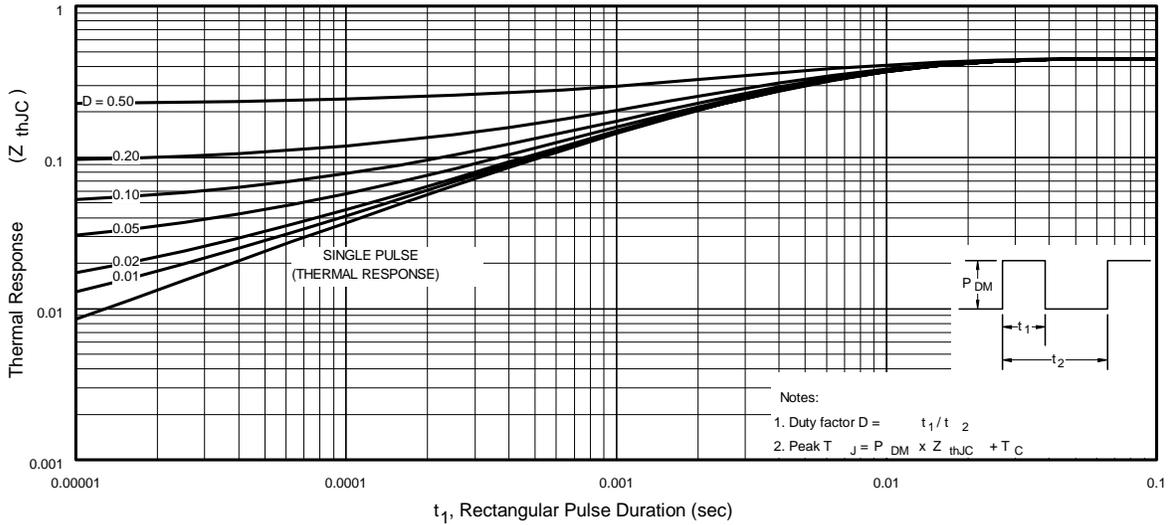
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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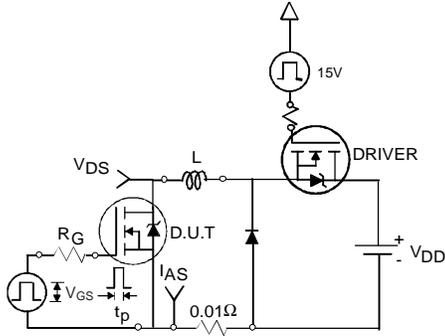
Fig 12a. Unclamped Inductive Test Circuit
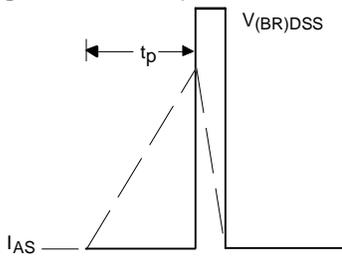
Fig 12b. Unclamped Inductive Waveforms
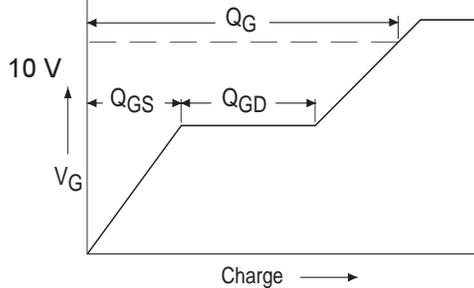
**Fig 13a.** Basic Gate Charge Waveform
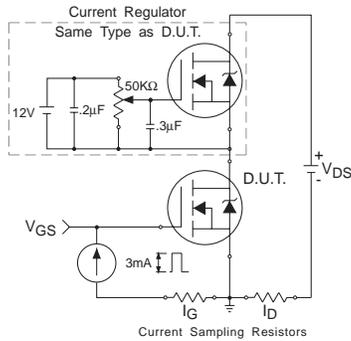

Fig 13b. Gate Charge Test Circuit

6
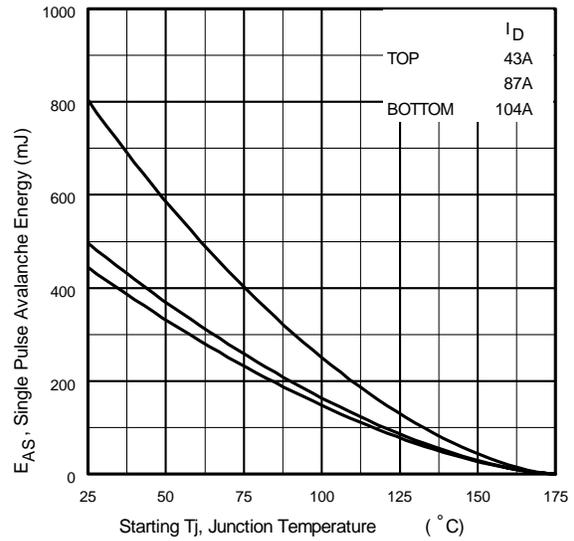
**Fig 12c.** Maximum Avalanche Energy
Vs. Drain Current
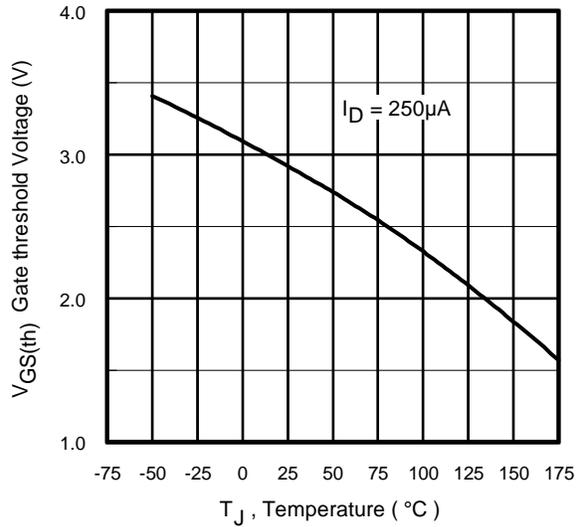
Fig 14. Threshold Voltage Vs. Temperature

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Duty Cycle = Single Pulse

Allowed avalanche Current vs avalanche pulsewidth, tav assuming ΔTj = 25°C due to avalanche losses. Note: In no case should Tj be allowed to exceed Tjmax
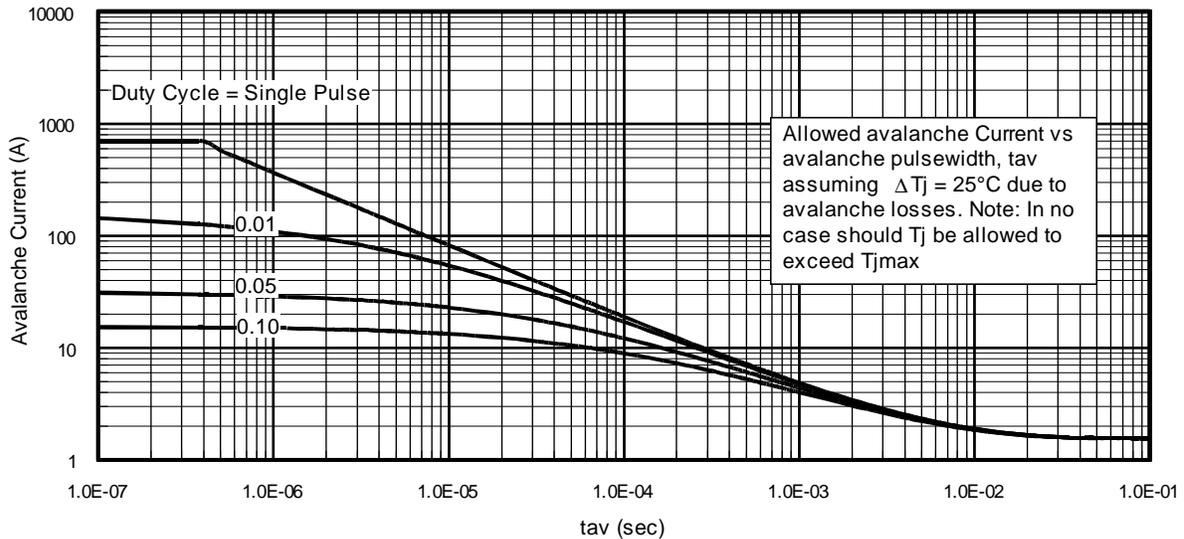
Fig 15. Typical Avalanche Current Vs.Pulsewidth

TOP   Single Pulse
BOTTOM   10% Duty Cycle
I_D = 104A
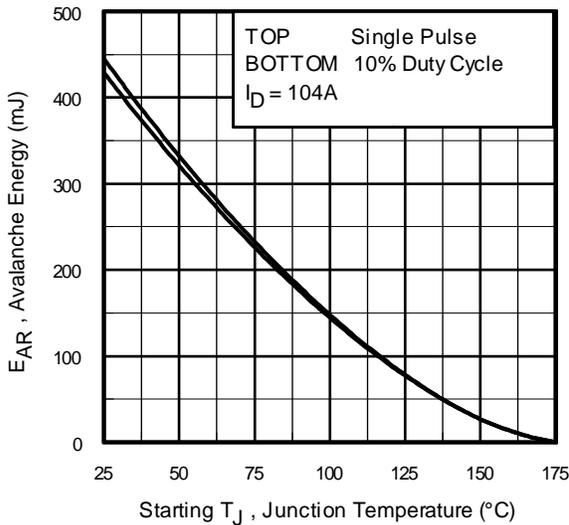
Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)
1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   Z_{thJC}(D, t_{av}) = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T/\ Z_{thJC}$$
$$I_{av} = 2\Delta T/\ [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$
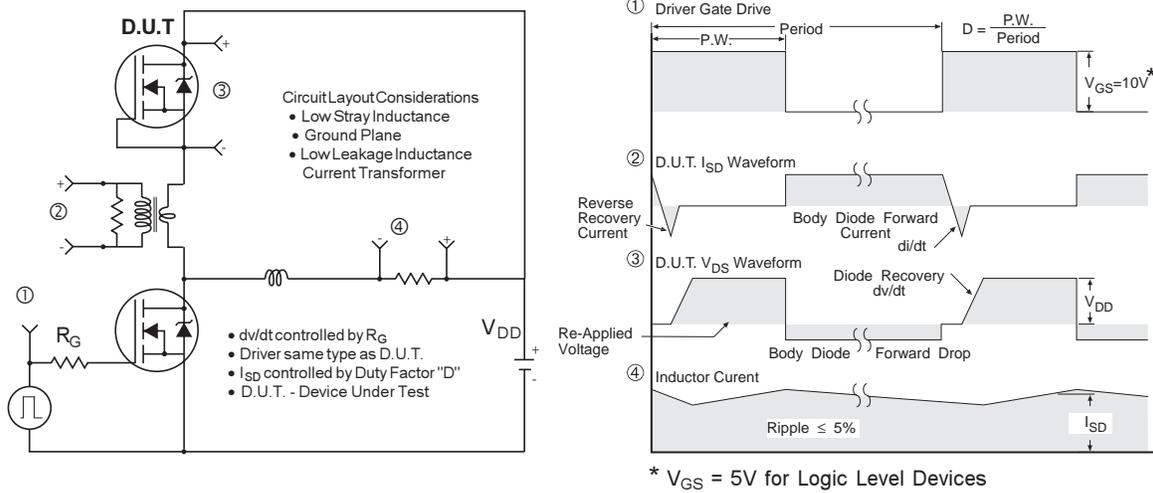
**Fig 17.** Peak Diode Recovery dv/dt Test Circuit for N-Channel
HEXFET® Power MOSFETs
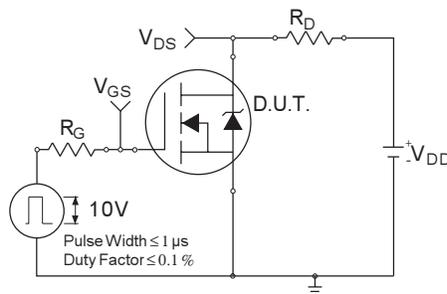

Fig 18a. Switching Time Test Circuit
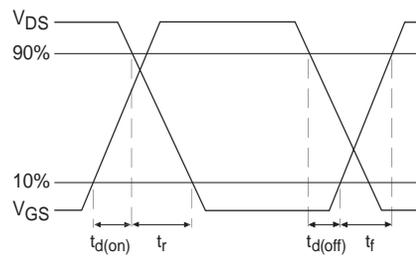
Fig 18b. Switching Time Waveforms

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN
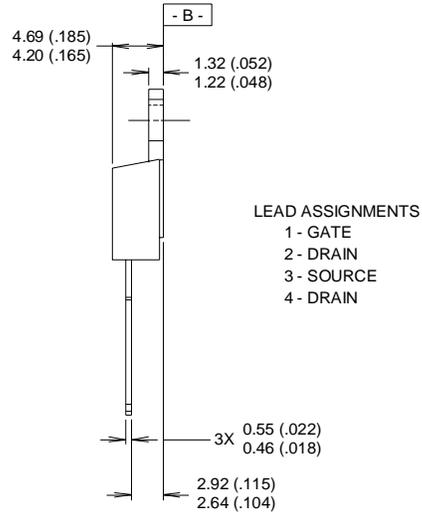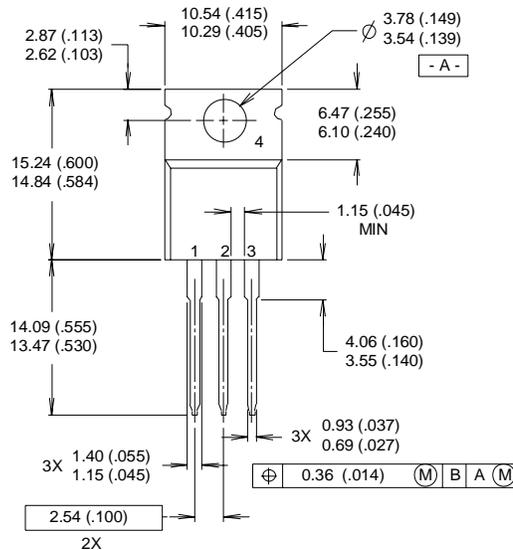
NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.

2 CONTROLLING DIMENSION : INCH

3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.

4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

DATE CODE
YEAR 7 = 1997
WEEK 19
LINE C

ASSEMBLY LOT CODE
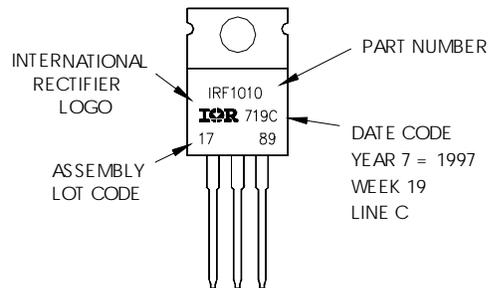
Data and specifications subject to change without notice.
This product has been designed and qualified for the Automotive [Q101] market.
Qualification Standards can be found on IR's Web site.

International **IQR** Rectifier