International
IOR Rectifier

IR2304(S)

HALF-BRIDGE DRIVER

Features

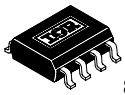
- Floating channel designed for bootstrap operation to +600V. Tolerant to negative transient voltage dV/dt immune
- Gate drive supply range from 10 to 20V
- Under voltage lockout for both channels
- 3.3V, 5V, and 15V input logic input compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Lower di/dt gate driver for better noise immunity
- Internal 100ns dead-time
- Output in phase with input

Product Summary

V_{OFFSET}	600V max.
I_O+/- (min)	60 mA/130 mA
V_{OUT}	10 - 20V
Delay Matching	50 ns
Internal deadtime	100 ns
ton/off (typ.)	220/220 ns

Package


8-Lead PDIP


8 Lead SOIC

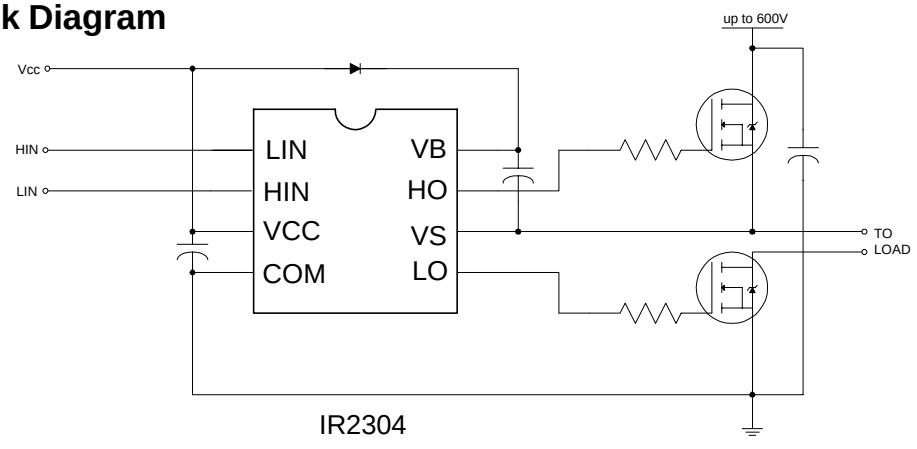
Description

The IR2304(S) are a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output driver features a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

2106/2301/2108/2109/2302/2304 Feature Comparison

Part	Input logic	Cross-conduction prevention logic	Dead-Time	Ground Pins
2106/2301	HIN/LIN	no	none	COM
21064				VSS/COM
2108	HIN/$\overline{\text{LIN}}$	yes	Internal 540ns	COM
21084			Programmable 0.54~5µs	VSS/COM
2109/2302	IN/$\overline{\text{SD}}$	yes	Internal 540ns	COM
21094			Programmable 0.54~5µs	VSS/COM
2304	HIN/LIN	yes	Internal 100ns	COM

Block Diagram



IR2304

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_S	High side offset voltage		V_B - 25	V_B + 0.3	V
V_B	High side floating supply voltage		-0.3	625	
V_{HO}	High side floating output voltage HO		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage LO		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN, LIN)		-0.3	V_{CC} + 0.3	
Com	Logic ground		V_{CC} -25	V_{CC} + 0.3	
dV_S/dt	Allowable offset voltage SLEW RATE		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	8-Lead SOIC	—	0.625	W
		8-Lead PDIP	—	1.0	
Rth_{JA}	Thermal resistance, junction to ambient	8-Lead SOIC	—	200	°C/W
		8-Lead PDIP	—	125	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side (HO) output voltage	V_S	V_B	
V_{LO}	Low side (LO) output voltage	COM	V_{CC}	
V_{IN}	Logic input voltage (HIN, LIN)	COM	V_{CC}	
V_{CC}	Low side supply voltage	10	20	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of COM -5 to COM +600V. Logic state held for V_S of COM -5V to COM -V_{BS}.

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and V_S is applicable to HO and LO.

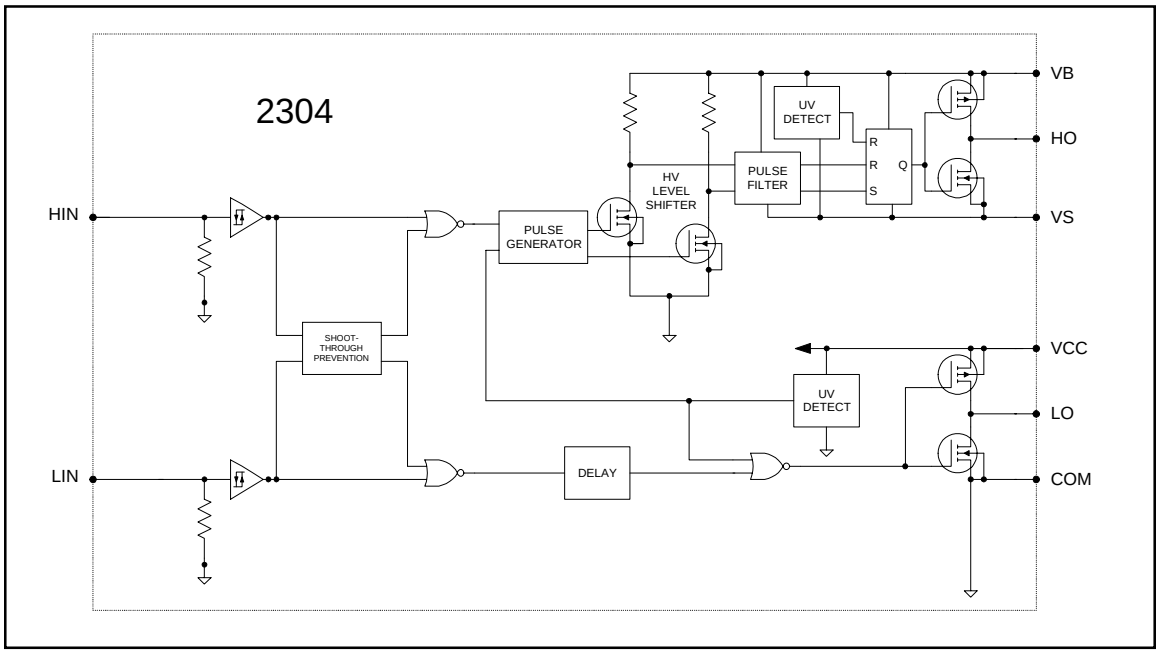
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9		
V_{CCUVH} V_{BSUVH}	V_{CC} supply undervoltage lockout hysteresis	0.3	0.7	—		
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	20	60	150		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	50	120	240		V_{IN} = 0V or 5V
V_{IH}	Logic “1” input voltage	2.3	—	—	V	
V_{IL}	Logic “0” input voltage	—	—	0.8		
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	2.8		I_O = 20mA
V_{OL}	Low level output voltage, V_O	—	—	1.2		
I_{IN+}	Logic “1” input bias current	—	5	40	µA	V_{IN} = 5V
I_{IN-}	Logic “0” input bias current	—	1.0	2.0		V_{IN} = 0V
I_{O+}	Output high short circuit pulse current	60	—	—	mA	V_O = 0V PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	130	—	—		

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_S = COM, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	120	220	320	ns	V_S = 0V
t_{off}	Turn-off propagation delay	130	220	330		V_S = 0V or 600V
t_r	Turn-on rise time	60	200	300		
t_f	Turn-off fall time	20	100	170		
DT	Dead time	80	100	190		
MT	Delay matching, HS & LS turn-on/off	—	—	50		

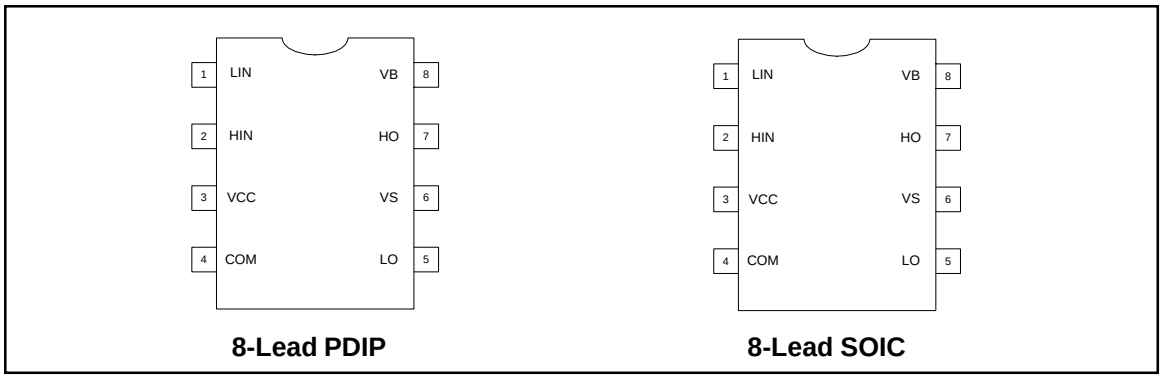
Functional Block Diagram



Lead Definitions

Symbol	Description
V_{CC}	Low side supply voltage
COM	Logic ground and low side driver return
HIN	Logic input for high side gate driver output
LIN	Logic input for low side gate driver output
V_B	High side floating supply
HO	High side driver output
V_S	High voltage floating supply return
LO	Low side driver output

Lead Assignments



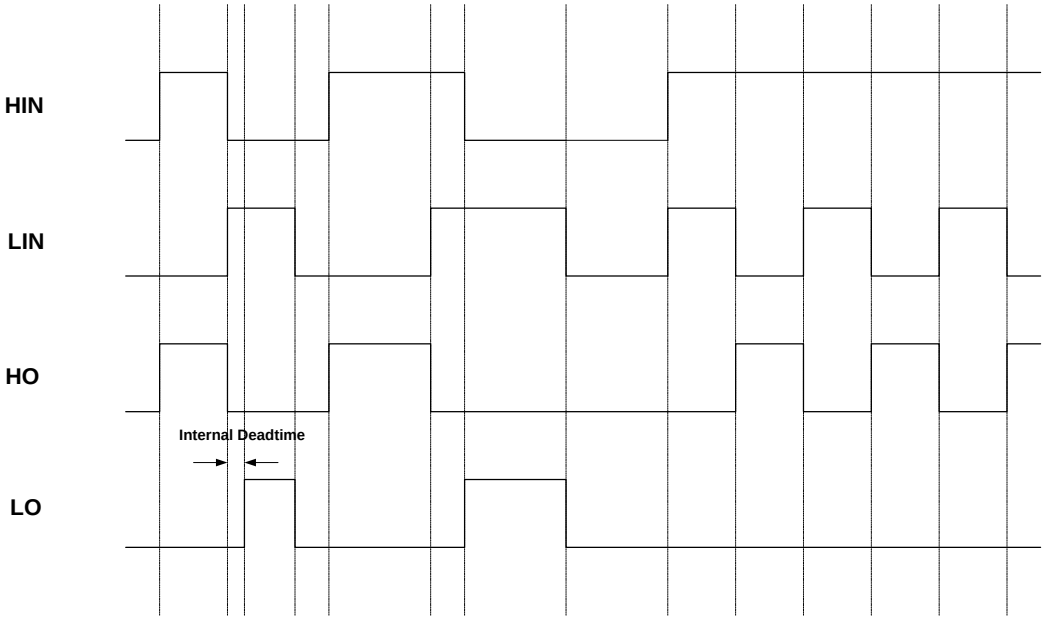


Figure 1. Input/Output Functionality Diagram

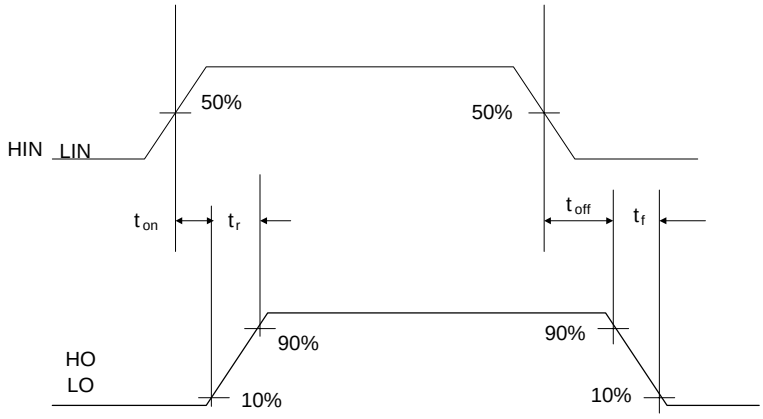


Figure 2. Switching Time Waveforms

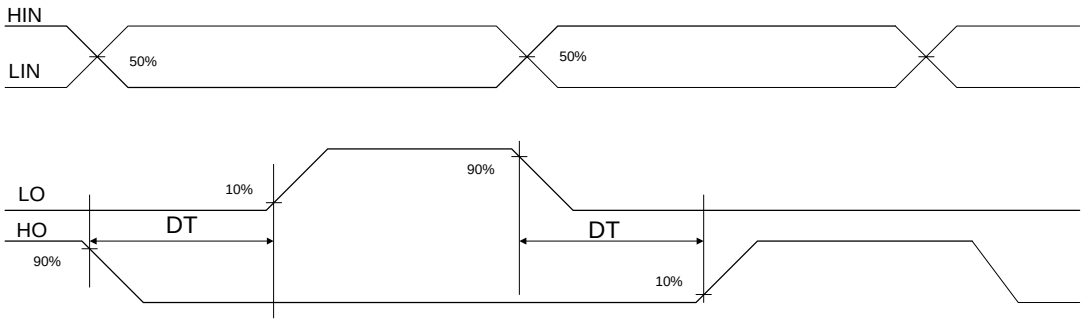
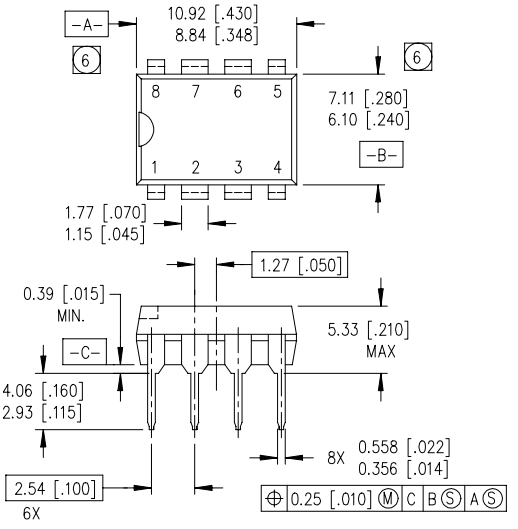
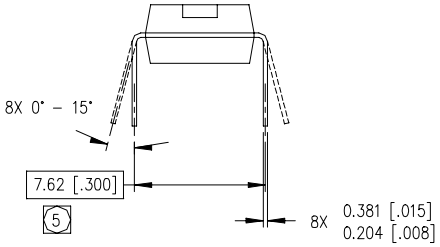


Figure 3. Internal Deadtime Timing

Case outlines

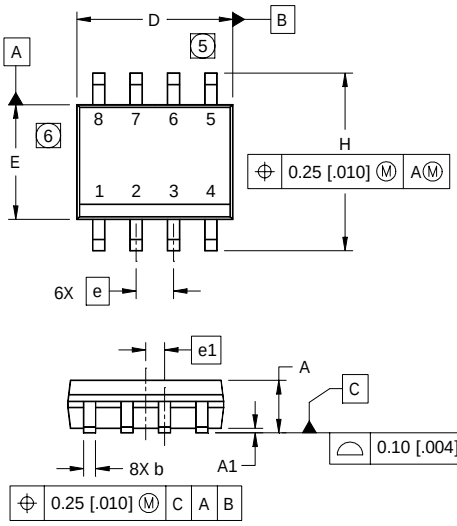


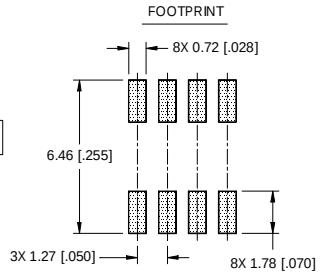
NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



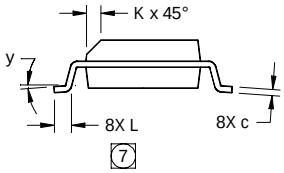
8-Lead PDIP

01-6014
01-3003 01 (MS-001AB)





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8 Lead SOIC

01-6027
01-0021 11 (MS-012AA)