International
IOR Rectifier

ADVANCE INFORMATION **Data Sheet No. PD60184-A**

IR2167(S)

PFC BALLAST CONTROL IC

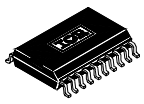
Features

- PFC, Ballast Control and Half Bridge Driver in One IC
- Critical Conduction Mode Boost Type PFC
- No PFC Current Sense Resistor Required
- Programmable Preheat Time & Frequency
- Programmable Ignition Ramp
- Programmable Over-Current
- Lamp Filament Sensing & Protection
- Capacitive Mode Protection
- Brown-Out Protection
- Automatic Restart for Lamp Exchange
- Thermal Overload Protection
- Programmable Deadtime
- Internal 15.6V Zener Clamp Diode on VCC
- Micropower Startup (150µA)
- Latch Immunity and ESD Protection

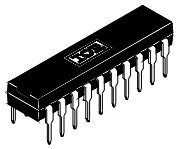
Description

The IR2167 is a fully integrated, fully protected 600V ballast control IC designed to drive virtually all types of rapid start fluorescent lamp ballasts. PFC circuitry provides for high PF, low THD and DC Bus regulation. Externally programmable features such as preheat time & frequency, ignition ramp characteristics, and running mode operating frequency provide a high degree of flexibility for the ballast design engineer. Comprehensive protection features such as protection from failure of a lamp to strike, filament failures, low AC line conditions, thermal overload, or lamp failure during normal operation, as well as an automatic restart function, have been included in the design. The heart of this control IC is a variable frequency oscillator with externally programmmable deadtime. Precise control of a 50% duty cycle is accomplished using a T-flip-flop. The IR2167 is available in both 20 pin DIP and 20 pin wide body SOIC packages.

Packages

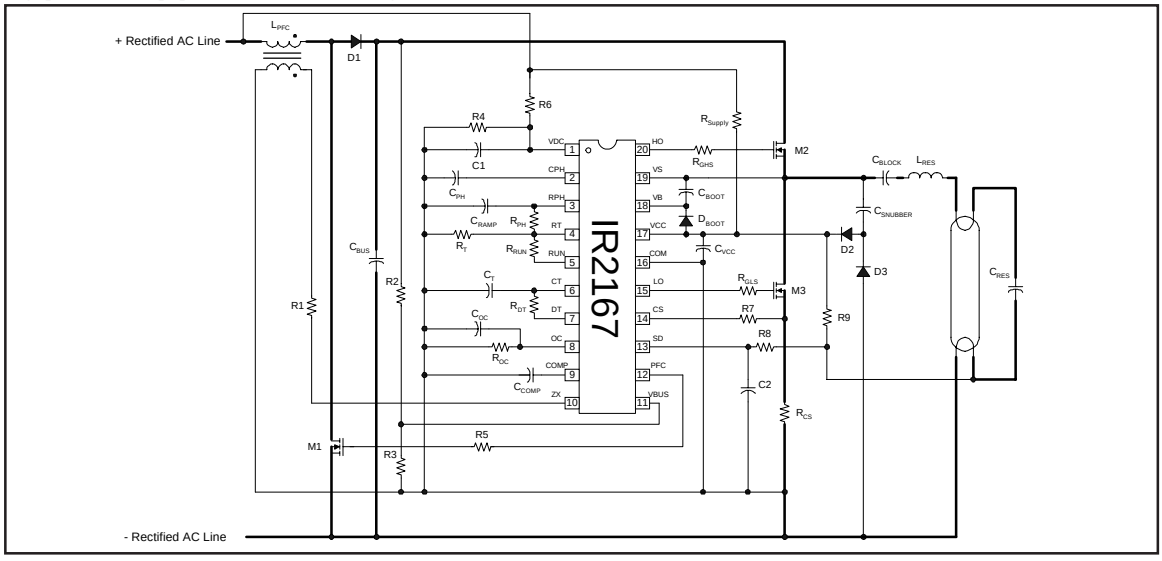


20 Lead SOIC
(wide body)



20 Lead PDIP

Typical Application Diagram



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{PFC}	PFC gate driver output voltage		-0.3	V_{CC} + 0.3	
I_{OMAX}	Max. allowable output current (HO,LO,PFC) due to external power transistor miller effect		-500	500	mA
I_{RT}	R_T pin current		-5	5	
V_{CT}	C_T pin voltage		-0.3	6.5	V
V_{DC}	VDC pin voltage		-0.3	V_{CC} + 0.3	
I_{CPH}	CPH pin current		-5	5	mA
I_{RPH}	RPH pin current		-5	5	
I_{RUN}	RUN pin current		-5	5	
I_{DT}	Deadtime pin current		-5	5	
V_{CS}	Current sense pin voltage		-0.3	6.5	V
I_{CS}	Current sense pin current		-5	5	mA
I_{OC}	Over-current threshold pin current		-5	5	
I_{SD}	Shutdown pin current		-5	5	
V_{BUS}	DC bus sensing input voltage		-0.3	V_{CC}	V
I_{ZX}	PFC inductor current, zero crossing detection input		-5	5	mA
I_{COMP}	PFC error amplifier compensation current		-5	5	
I_{CC}	Supply current (note 1)		-20	20	
dV/dt	Allowable offset supply voltage slew ratet		-50	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(20 lead PDIP)	—	1.50	W
		(20 lead SOIC)	—	1.25	
Rth_{JA}	Thermal resistance, junction to ambient	(20 lead PDIP)	—	85	°C/W
		(20 lead SOIC)	—	90	
T_J	Junction temperature		-55	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead

Symbol	Definition	Min.	Max.	Units
V_{BS}	High side floating supply voltage	V_{CC} - 0.7	V_{CLAMP}	V
V_S	Steady state high side floating supply offset voltage	-3.0	600	
V_{CC}	Supply voltage	V_{CCUV+}	V_{CLAMP}	
I_{CC}	Supply current	Note 2	10	mA
V_{DC}	V_{DC} lead voltage	0	VCC	V
C_T	C_T lead capacitance	220	—	pF
R_{DT}	Deadtime resistance	1.0	—	kΩ
I_{RT}	R_T lead current (Note 3)	-500	-50	uA
I_{RPH}	RPH lead current (Note 3)	0	450	
I_{RUN}	RUN lead current (Note 3)	0	450	
I_{SD}	Shutdown lead current	-1	1	mA
I_{CS}	Current sense lead current	-1	1	
I_{ZX}	Zero crossing detection lead current	-1	1	
T_J	Junction temperature	-40	125	°C

Electrical Characteristics

V_{CC} = V_{BS} = V_{BIAS} = 14V +/- 0.25V, R_T = 40.0kΩ, C_T = 470 pF, RPH and RUN leads no connection, V_{CPH} = 0.0V, R_{DT} = 6.1kΩ, R_{OC} = 20.0kΩ, V_{CS} = 0.5V, V_{SD} = 0.0V, C_L = 1000pF, T_A = 25°C unless otherwise specified.

Supply Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	—	11.4	—		V_{CC} rising from 0V
V_{UVHYS}	V_{CC} supply undervoltage lockout hysteresis	—	1.8	—		
I_{QCCUV}	UVLO mode quiescent current	—	150	—	µA	V_{CC} < V_{CCUV-}
I_{QCCFLT}	Fault-mode quiescent current	—	200	—		SD = 5V, CS = 2V or Tj > T_{SD}
I_{QCC}	Quiescent V_{CC} supply current	—	3.8	—	mA	R_T no connection, C_T connected to COM
I_{QCC50K}	V_{CC} supply current, f = 50kHz	—	4.5	—		R_T =36kΩ, R_{DT} = 5.6kΩ, C_T=220pF
V_{CLAMP}	V_{CC} zener clamp voltage	—	15.6	—	V	ICC = 10mA

Note 2: Sufficient current should be supplied to the VCC pin to keep the internal 15.6V zener clamp diode on this pin regulating its voltage.

Note 3: Due to the fact that the RT pin is a voltage-controlled current source, the total RT pin current is the sum of all of the parallel current sources connected to that pin. For optimum oscillator current mirror performance, this total current should be kept between 50mA and 500mA. During the preheat mode, the total current flowing out of the RT pin consists of the RPH pin current plus the current due to the RT resistor. During the run mode, the total RT pin current consists of the RUN pin current plus the the current due to the RT resistor.

Electrical Characteristics (cont.)

V_{CC} = V_{BS} = V_{BIAS} = 14V +/- 0.25V, R_T = 40.0kΩ, C_T = 470 pF, RPH and RUN leads no connection, V_{CPH} = 0.0V, R_{DT} = 6.1kΩ, R_{OC} = 20.0kΩ, V_{CS} = 0.5V, V_{SD} = 0.0V, C_L = 1000pF, T_A = 25°C unless otherwise specified.

Floating Supply Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
I_{QBS0}	Quiescent V_{BS} supply current	—	0	—	µA	V_{HO} = V_S
I_{QBS1}	Quiescent V_{BS} supply current	—	30	—		V_{HO} = V_B
V_{BSMIN}	Min. req'd V_{BS} voltage for proper HO functionality		—	4	5	V
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V

PFC Error Amplifier Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{BUS}	VBUS sense input threshold	—	0	—		V_{HO} = V_S
I_{VBUS}	VBUS sense input bias current	—	30	—		V_{HO} = V_B
gm	Error amplifier transconductance	—	0	—		V_{HO} = V_S
I_{SOURCE}	Error amplifier output current sourcing		—	30	—	V_{HO} = V_B
I_{SINK}	Error amplifier output current sinking	—	0	—		V_{HO} = V_S
$V_{OH(EA)}$	Error amplifier output voltage swing (Hi state)		—	30	—	V_{HO} = V_B
$V_{0L(EA)}$	Error amplifier output voltage swing (Lo state)		—	0	—	V_{HO} = V_S

PFC Over Voltage Comparator

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{0V}	Over voltage comparator threshold	—	4.3	—	V	

PFC Overvoltage Comparator

V_{ZX}	ZX lead comparator threshold voltage	—	2.0	—	V	
V_{ZXhys}	ZX lead comparator hysterisis	—	120	—	mV	
$V_{ZXclamp+}$	ZX lead clamp voltage (high state)	—	7.5	—	V	I_{ZX} = 2mA

Oscillator I/O Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
f_{osc}	Oscillator frequency	—	30	—	kHz	R_T = 32kΩ, R_{DT} = 6.1kΩ, C_T=470pF
		—	100	—		R_T = 6.1kΩ, R_{DT} = 6.1kΩ, C_T=470pF
df/dV	Oscillator frequency voltage stability	—	0.5	—	%/V	V_{CCUV+} < V_{CC} < 15V
df/dT	Oscillator frequency temperature stability	—	0.02	—	%/C	-40°C < Tj < 125°C
d	Oscillator duty cycle	—	50	—	%	
V_{CT+}	Upper C_T ramp voltage threshold	—	4.0	—	V	
V_{CT-}	Lower C_T ramp voltage threshold	—	2.0	—		
V_{CTFLT}	Fault-mode C_T lead voltage	—	0	—	mV	SD = 5V, CS = 2V, or Tj > TSD
V_{RT}	R_T lead voltage	—	2.0	—	V	
V_{RTFLT}	Fault-mode R_T lead voltage	—	0	—	mV	SD = 5V, CS = 2V, or Tj > TSD
tdlo	LO output deadtime	—	2.0	—	µsec	
tdho	HO output deadtime	—	2.0	—		
dtd/dV	Deadtime voltage stability	—	0.5	—	%/V	V_{CCUV+} < V_{CC} < 15V
dtd/dT	Deadtime temperature stability	—	0.02	—	%/C	-40°C < Tj < 125°C

Electrical Characteristics (cont.)

V_{CC} = V_{BS} = V_{BIAS} = 14V +/- 0.25V, R_T = 40.0kΩ, C_T = 470 pF, RPH and RUN leads no connection, V_{CPH} = 0.0V, R_{DT} = 6.1kΩ, R_{OC} = 20.0kΩ, V_{CS} = 0.5V, V_{SD} = 0.0V, C_L = 1000pF, T_A = 25°C unless otherwise specified.

Preheat Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
I_{CPH}	CPH lead charging current	—	1.0	—	µA	V_{CPH} = 0V
V_{CPHIGN}	CPH lead Ignition mode threshold voltage	—	4.0	—	V	
V_{CPHRUN}	CPH lead run mode threshold voltage	—	5.15	—		
$V_{CPHCLMP}$	CPH lead clamp voltage	—	10	—		I_{CPH} = 1µA
V_{CPHFLT}	Fault-mode CPH lead voltage	—	0	—	mV	SD = 5V, CS = 2V, or Tj > TSD

RPH Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
I_{RPHLK}	Open circuit RPH lead leakage current	—	0.1	—	µA	V_{RPH} =5V,V_{RPH} =6V
V_{RPHFLT}	Fault-mode RPH lead voltage	—	0	—	mV	SD = 5V, CS = 2V, or Tj > TSD

RUN Characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
I_{RUNLK}	Open circuit RUN lead leakage current	—	0.1	—	µA	V_{RUN} = 5V
V_{RUNFLT}	Fault-mode RUN lead voltage	—	0	—	mV	SD = 5V, CS = 2V, or Tj > TSD

Protection Circuitry Characteristics

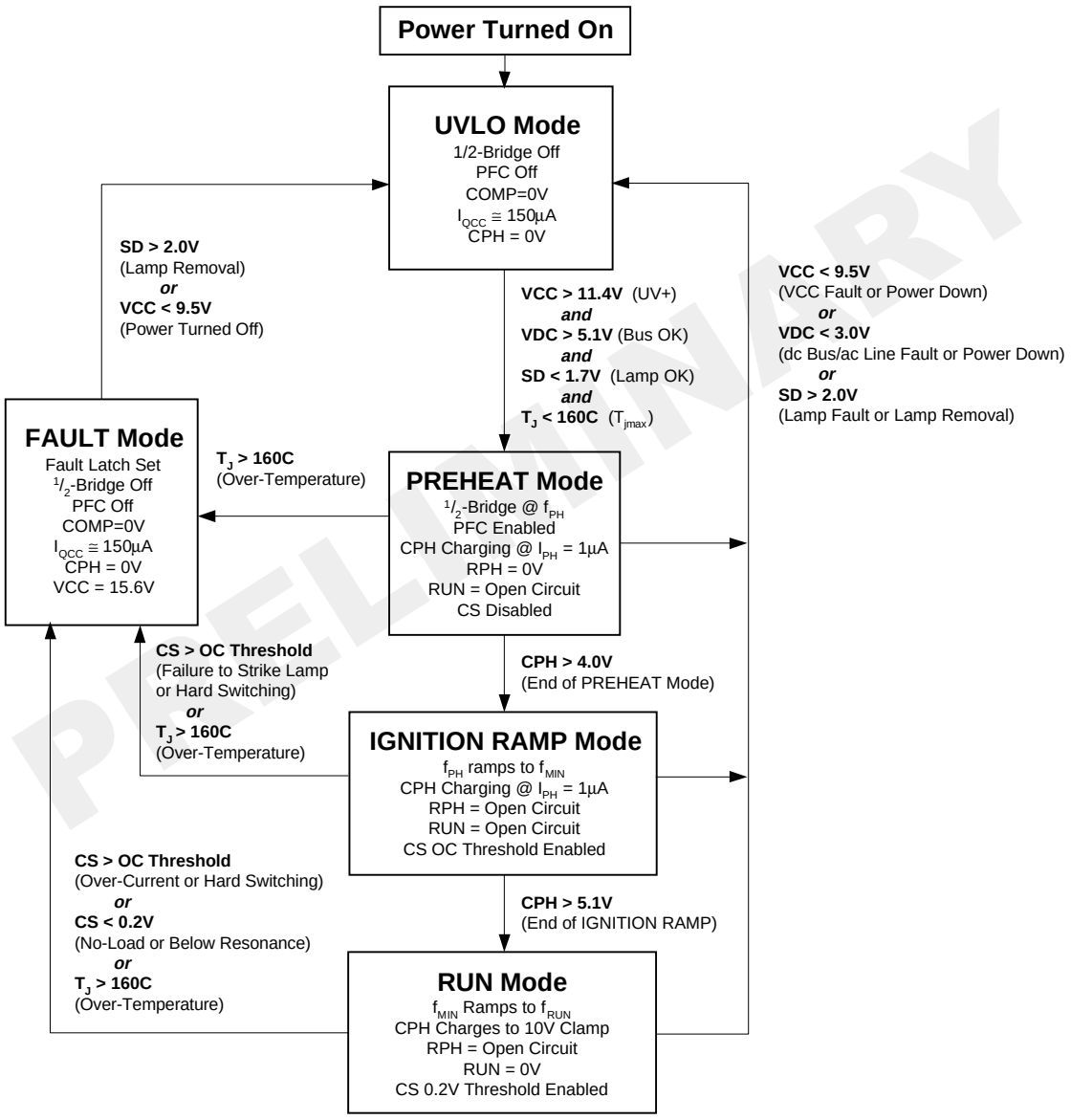
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{SDTH+}	Rising shutdown lead threshold voltage	—	2.0	—	V	
V_{SDHYS}	Shutdown lead threshold hysteresis	—	150	—	mV	
V_{CSTH+}	Over-current sense threshold voltage	—	1.0	—	V	
V_{CSTH-}	Under-current sense threshold voltage	—	0.2	—		
T_{CS}	Over-current sense propogation delay	—	160	—	nsec	Delay from CS to LO
V_{DC+}	Low V_{BUS}/rectified line input upper threshold	—	5.15	—	V	
V_{DC-}	Low V_{BUS}/rectified line input lower threshold	—	3.0	—		
T_{SD}	Thermal shutdown junction temperature	—	160	—	°C	Note 4

Gate Driver Output Characteristics

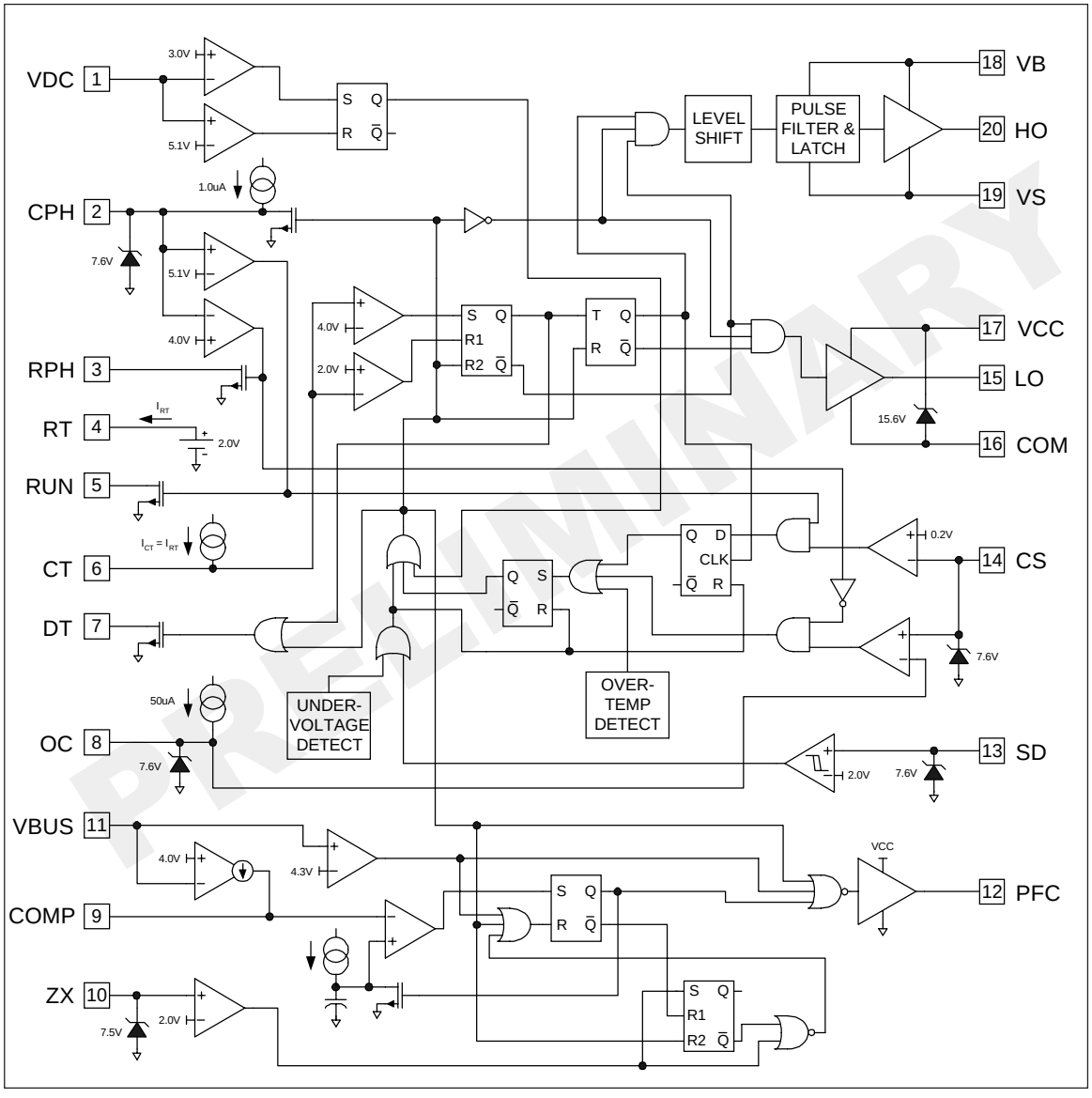
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
VOL	Low level output voltage	—	0	100	mV	I_O = 0
V_{OH}	High level output voltage	—	0	100		V_{BIAS} - V_O, I_O = 0
t_r	Turn-on rise time	—	85	150	nsec	
t_f	Turn-off fall time	—	45	100		

Note 4: When the IC senses an overtemperature condition (Tj > 160ºC), the IC is latched off. In order to reset this Fault Latch, the SD lead must be cycled high and then low, or the V_{CC} supply to the IC must be cycled below the falling undervoltage lockout threshold (V_{CCUV-}).

State Diagram

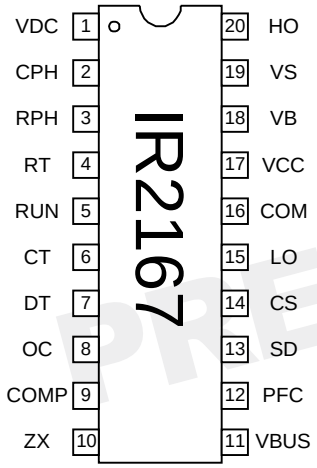


Functional Block Diagram



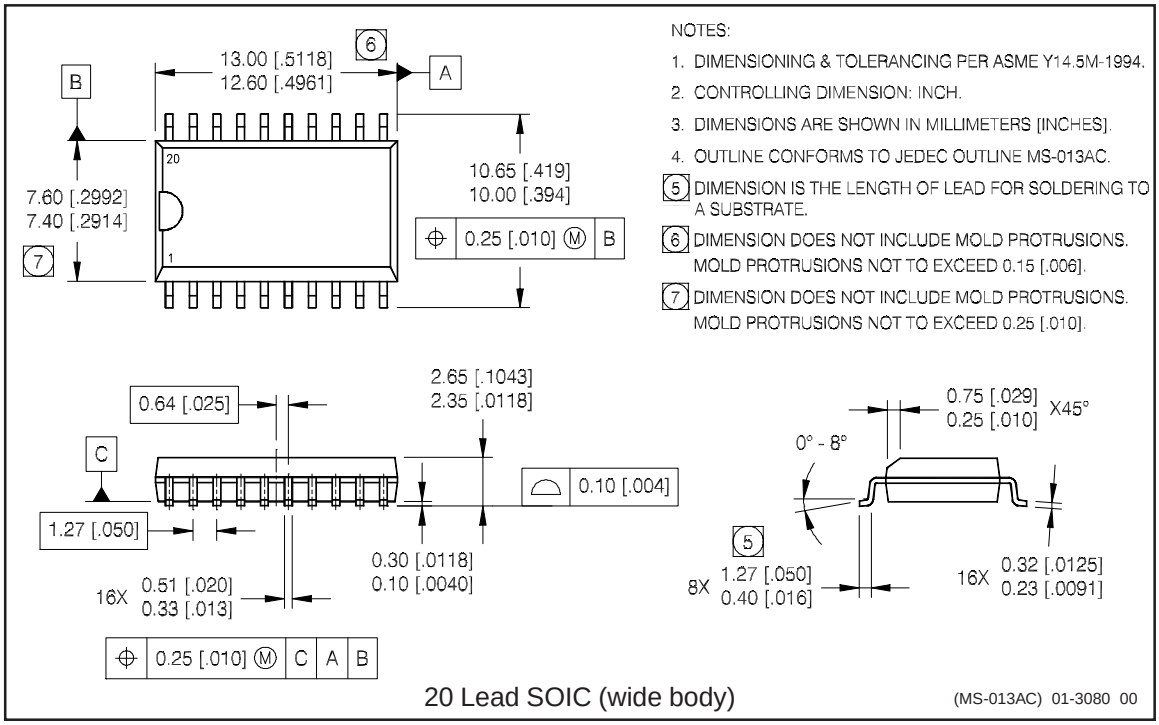
Lead Assignments

Pin Assignments



Pin #	Symbol	Description
1	VDC	DC Bus Sensing Input
2	CPH	Preheat Timing Capacitor
3	RPH	Preheat Frequency Resistor & Ignition Capacitor
4	RT	Oscillator Timing Resistor
5	RUN	Run Frequency Resistor
6	CT	Oscillator Timing Capacitor
7	DT	Deadtime Programming
8	OC	Over-current (CS+) Threshold Programming
9	COMP	Error Amplifier Compensation
10	ZX	Zero-Crossing, PFC Inductor
11	VBUS	Bus Voltage Sense Input
12	PFC	PFC Gate Driver Output
13	SD	Shutdown Input
14	CS	Current Sensing Input
15	LO	Low-Side Gate Driver Output
16	COM	IC Power & Signal Ground
17	VCC	Logic & Low-Side Gate Driver Supply
18	VB	High-Side Gate Driver Floating Supply
19	VS	High Voltage Floating Return
20	HO	High-Side Gate Driver Output

Caseoutline

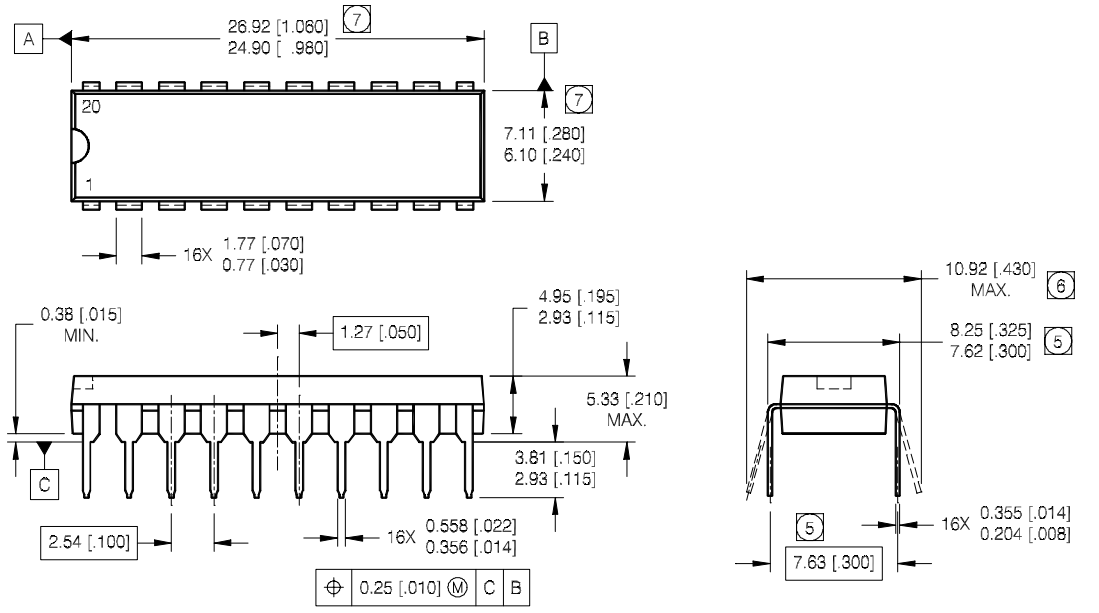


NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-013AC.
5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
7. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

20 Lead SOIC (wide body) (MS-013AC) 01-3080 00

Caseoutline



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2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AD.

5 DIMENSION MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

6 DIMENSION MEASURED AT LEAD TIPS WITH THE LEADS UNCONSTRAINED.

7 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

20 Lead PDIP (MS-001AD) 01-3079 00