Data Sheet No. PD60160-B

International Rectifier

IPS0551T

FULLY PROTECTED POWER MOSFET SWITCH

Features

- Over temperature shutdown
- Over current shutdown
- Active clamp
- Low current & logic level input
- E.S.D protection

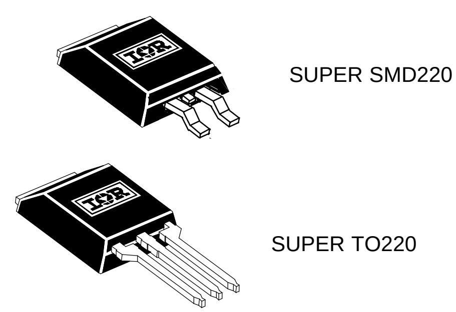
Description

The IPS0551T is a fully protected three terminal SMART POWER MOSFET that features over-current, over-temperature, ESD protection, and drain to source active clamp. This device combines a HEXFET® POWER MOSFET and a gate driver. It offers full protection and high reliability required in harsh environments. The driver allows short switching times and provides efficient protection by turning OFF the power MOSFET when temperature exceeds 165°C or when the drain current reaches 100A. The device restarts once the input is cycled. The avalanche capability is significantly enhanced by the active clamp and covers most inductive load demagnetizations.

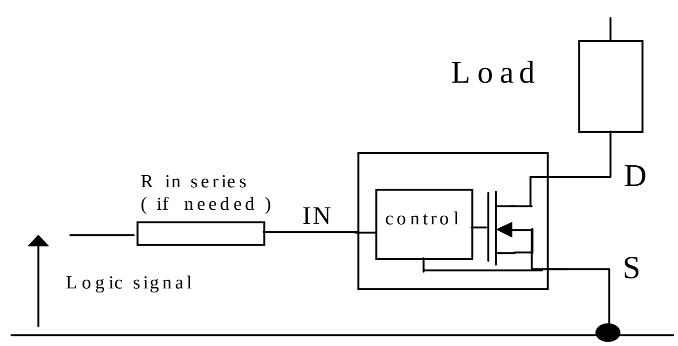
Product Summary

$R_{ds(on)}$	6.0mΩ (max)
V_{clamp}	40V
$I_{shutdown}$	100A
T_{on}/T_{off}	4µs

Package



Typical Connection



(Refer to lead assignment for correct pin configuration)

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are referenced to SOURCE lead. ($T_{Ambient}$ = 25°C unless otherwise specified). PCB mounting uses the standard footprint with 70 µm copper thickness.

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{ds}	Maximum drain to source voltage	—	37	V	
V_{in}	Maximum input voltage	-0.3	7		
$I+_{in}$	Maximum IN current	-10	+10	mA	
$I_{sd\ cont.}$	Diode max. continuous current (1)			A	
	(rth=60°C/W)	—	2.8		
	(rth=5°C/W)	—	35		
$I_{sd\ pulsed}$	Diode max. pulsed current (1)	—	100		
P_d	Maximum power dissipation(1) (rth=60°C/W)	—	2	W	
ESD1	Electrostatic discharge voltage (Human Body)	—	4	kV	C=100pF, R=1500Ω,
ESD2	Electrostatic discharge voltage (Machine Model)	—	0.5		C=200pF, R=0Ω, L=10µH
$T_{stor.}$	Max. storage temperature	-55	150	°C	
T_j max.	Max. junction temperature	-40	+150		
T_{lead}	Lead temperature (soldering, 10 seconds)	—	300		

Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{th} 1	Thermal resistance free air	—	60	—	°C/W	
R_{th} 2	Thermal resistance to PCB min footprint	—	60	—		
R_{th} 3	Thermal resistance to PCB 1" sq. footprint	—	35	—		
R_{th} 4	Thermal resistance junction to case	—	0.7	—		

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
$V_{ds\ (max)}$	Continuous drain to source voltage	—	18	V
V_{IH}	High level input voltage	4	6	
V_{IL}	Low level input voltage	0	0.5	
I_{ds} Tamb=85°C	Continuous drain current			A
	(TAmbient = 85°C, IN = 5V, rth = 80°C/W, Tj = 125°C)	—	8	
	(TAmbient = 85°C, IN = 5V, rth = 5°C/W, Tj = 125°C)	—	35	
R_{in}	Recommended resistor in series with IN pin	0.1	0.5	kΩ
$T_{r\text{-}in\ (max)}$	Max recommended rise time for IN signal (see fig. 2)	—	1	µS
$F_{r\text{-}Isc}$ (2)	Max. frequency in short circuit condition (Vcc = 14V)	0	1	kHz

(1) Limited by junction temperature (pulsed current limited also by internal wiring)
(2) Operation at higher switching frequencies is possible. See Appl. Notes.

Static Electrical Characteristics

(T_j = 25°C and Vcc = 14V unless otherwise specified. Standard footprint 70µm of copper thickness)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{ds(on)}$ @Tj=25°C	ON state resistance T_j = 25°C	—	4.5	6.0	mΩ	V_{in} = 5V, I_{ds} = 10A
$R_{ds(on)}$ @Tj=150°C	ON state resistance T_j = 150°C	—	7.5	8.8	mΩ	V_{in} = 5V, I_{ds} = 10A
Idss @Tj=25°C	Drain to source leakage current	0	0.01	25	µA	Vcc = 14V, Tj = 25°C
V clamp 1	Drain to source clamp voltage 1	37	40	—	V	I_d = 20mA (see Fig.3 & 4)
V clamp 2	Drain to source clamp voltage 2	—	43	48	V	I=35A -t<100us
V_{sd}	Body diode forward voltage	—	0.85	1	V	I_d = 35A, V_{in} = 0V
$V_{in\ clamp}$	IN to source clamp voltage	7	8.0	9.5	V	I_{in} = 1 mA
V_{th}	IN threshold voltage	1.0	1.8	2.2	V	I_d = 50mA, Vds = 14V
$I_{in,\ on}$	Input supply current (normal operation)	25	90	300	µA	V_{in} = 5V
$I_{in,\ off}$	Input supply current (protection mode)	50	130	400	µA	V_{in} = 5V over-current triggered

Switching Electrical Characteristics

V_{cc} = 14V, Resistive Load = 0.4Ω, Rinput = 50Ω, 100µs pulse, T_j = 25°C, (unless otherwise specified).

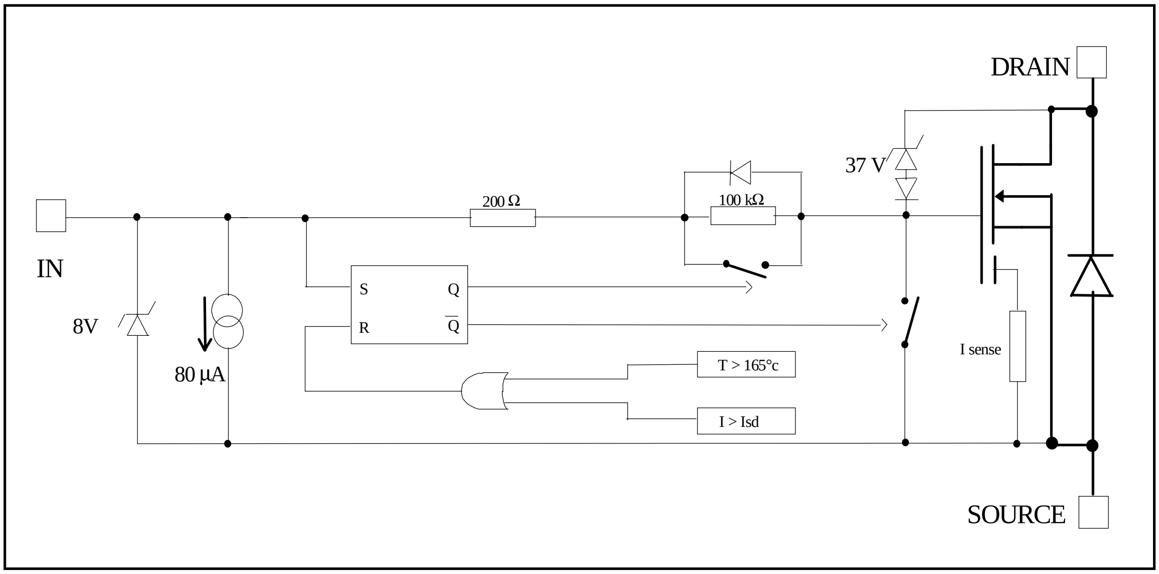
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{on}	Turn-on delay time	0.25	1	4	µs	See figure 2
T_r	Rise time	0.25	1	4	µs	See figure 2
T_{rf}	Time to 130% final $R_{ds(on)}$	—	15	—	µs	
T_{off}	Turn-off delay time	1.5	4	8	µs	See figure 2
T_f	Fall time	0.5	2	5	µs	See figure 2
Q_{in}	Total gate charge	—	200	—	nC	V_{in} = 5V

Protection Characteristics

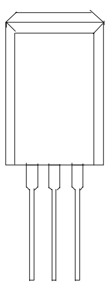
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{sd}	Over temperature threshold	—	165	—	°C	See fig. 1
I_{sd}	Over current threshold	60	100	150	A	See fig. 1
V_{reset}	IN protection reset threshold	1.5	1.9	2.8	V	
T_{reset}	Time to reset protection	2	10	40	µs	V_{in} = 0V, Tj = 25°C
EOI_OT	Short circuit energy (cf application note)	100	400	1200	µJ	V_{cc} = 14V

Functional Block Diagram

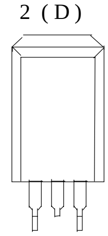
All values are typical



Lead Assignments



SUPER TO220



SUPER SMD220
(Advanced Information)

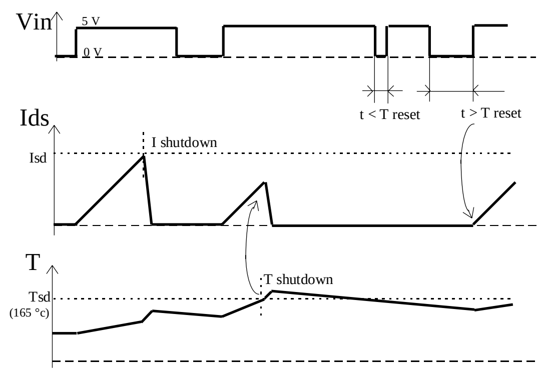


Figure 1 - Timing diagram

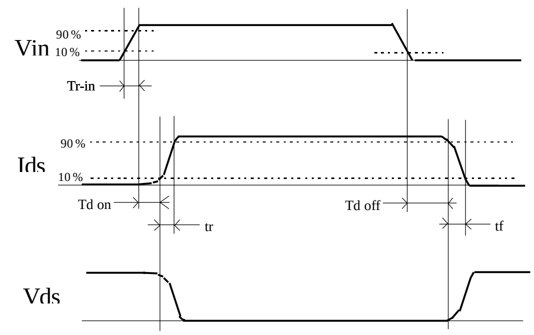


Figure 2 - IN rise time & switching time definitions

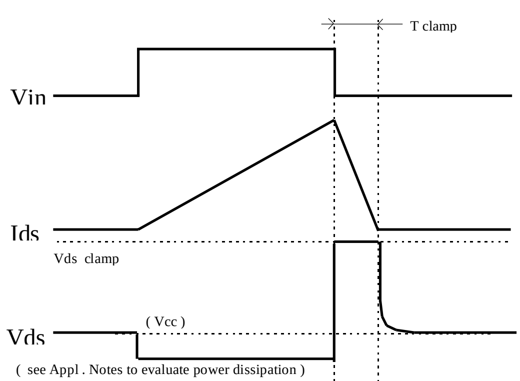


Figure 3 - Active clamp waveforms

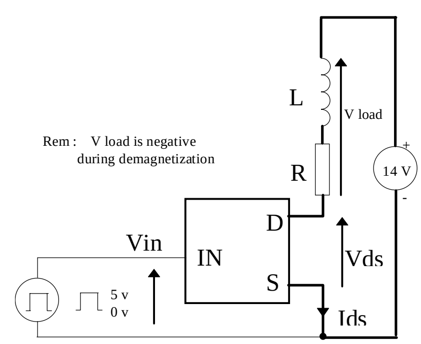


Figure 4 - Active clamp test circuit

All curves are typical values with standard footprint. Operating in the shaded area is not recommended.

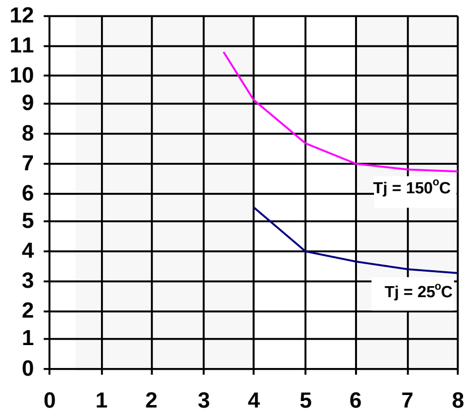


Figure 5 - Rds(on) (mΩ) Vs Input Voltage (V)

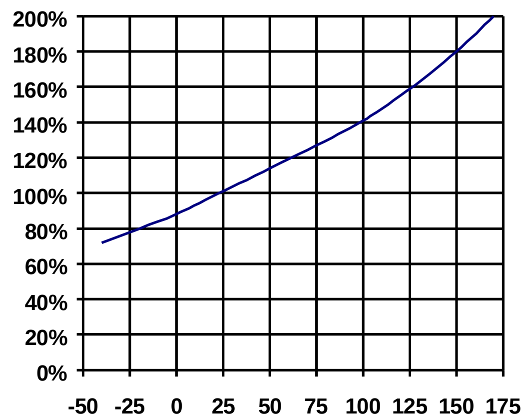


Figure 6 - Normalised Rds(on) (%) Vs T_j (°C)

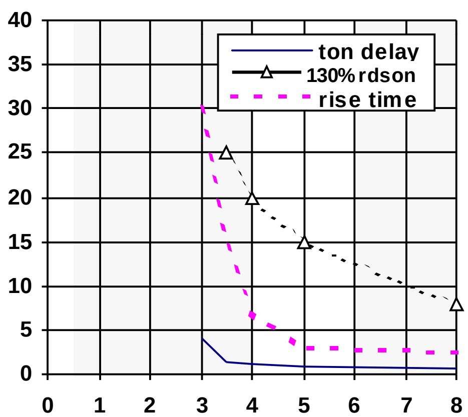


Figure 7 - Turn-ON Delay Time, Rise Time & Time to 130% final Rds(on) (us) Vs Input Voltage (V)

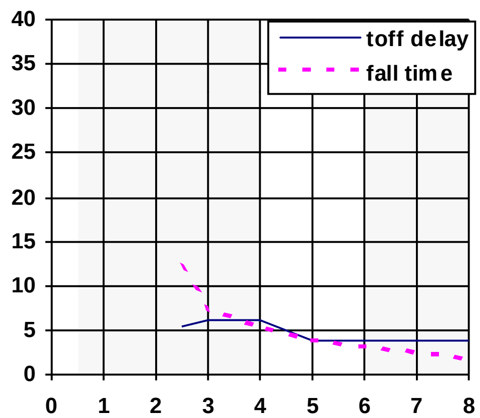


Figure 8 - Turn-OFF Delay Time & Fall Time (us) Vs Input Voltage (V)

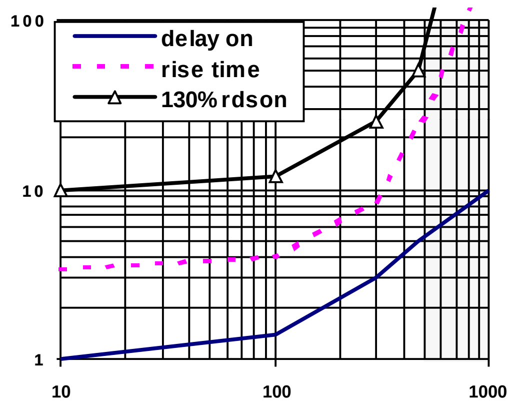


Figure 9 - Turn-ON Delay Time, Rise Time & Time to 130% final Rds(on) (us) Vs IN Resistor (Ω)

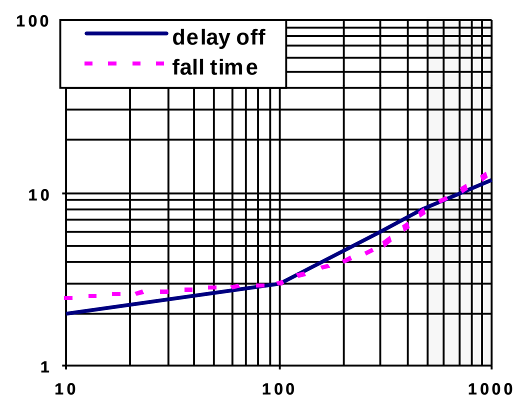


Figure 10 - Turn-OFF Delay Time & Fall Time (us) Vs IN Resistor (Ω)

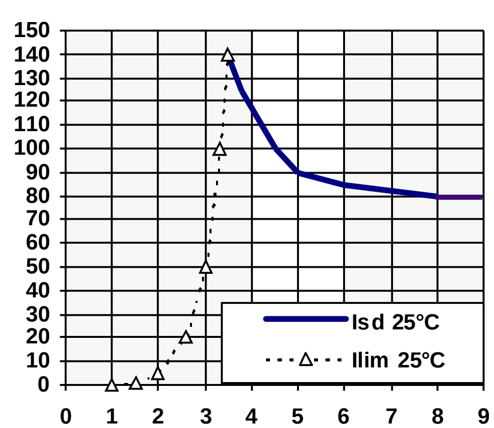


Figure 11 - Current lim. & Ishutdown (A) Vs Vin (V)

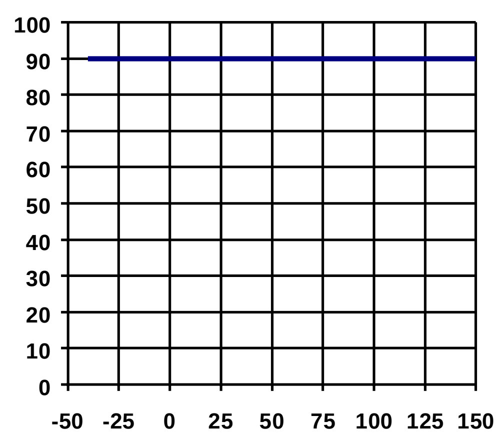


Figure 12 - Over-current (A) Vs Temperature (^{o}C)

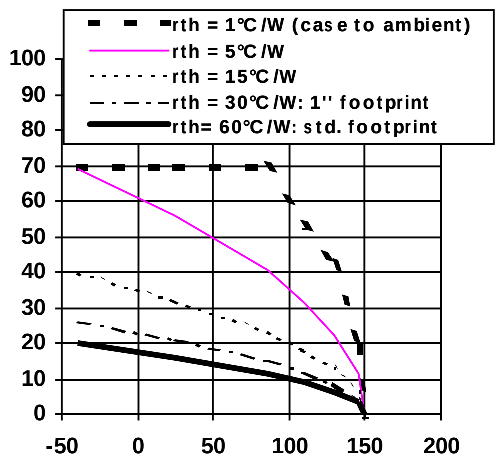


Figure 13 - Max.Cont. Ids (A) Vs
Amb. Temperature (^{o}C)

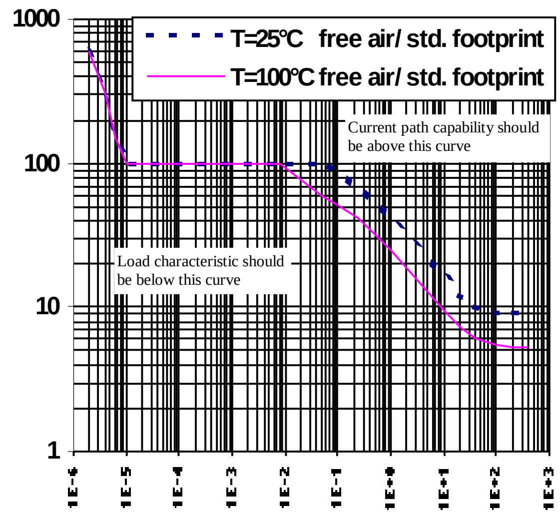


Figure 14 - Ids (A) Vs Protection Resp. Time (s)

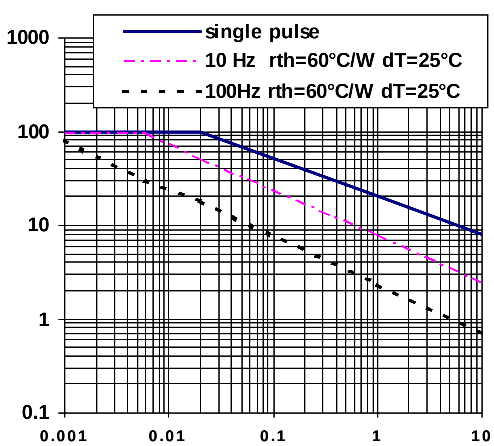


Figure 15 - Iclamp (A) Vs Inductive Load (mH)

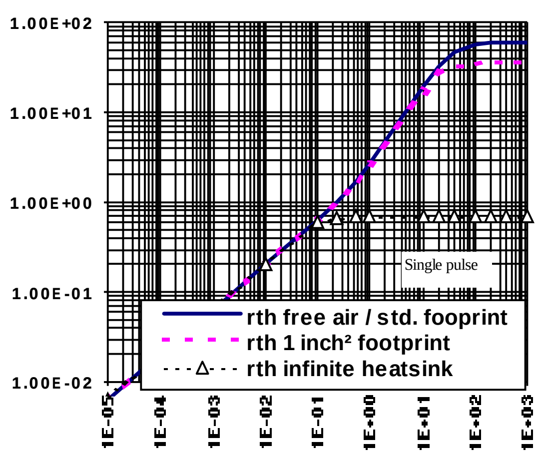


Figure 16 - Transient Thermal Imped. (^{o}C/W)
Vs Time (s)

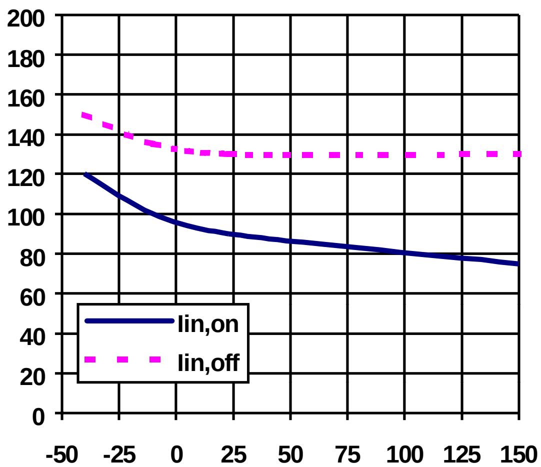


Figure 17 - Inputcurrent (µA) Vs Junction (°C)

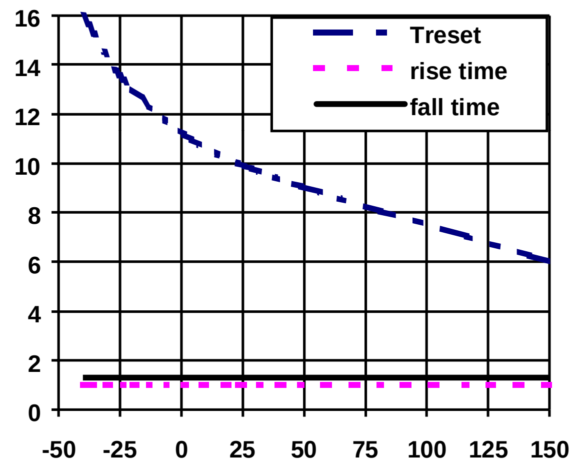


Figure 18 - Turn-on, Turn-off and Treset (µS) Vs Tj (°C)

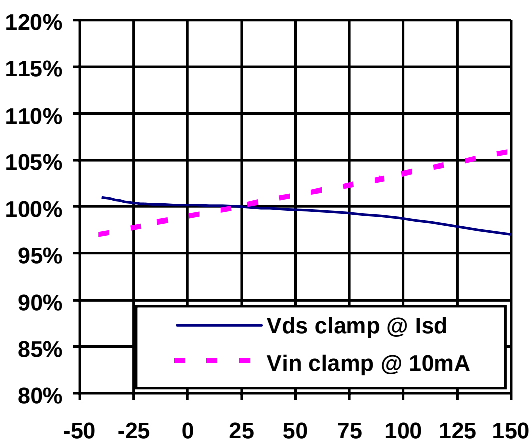
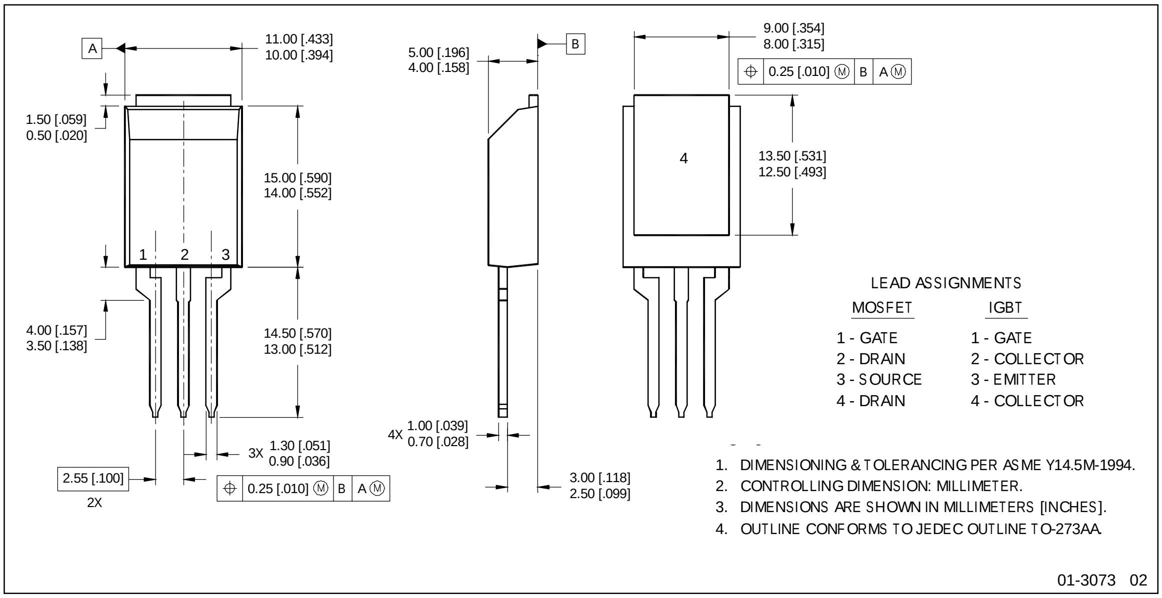


Figure 19 - Vin clamp1 & Vin clamp2 (%) Vs Tj (°C)

Case outline Super TO220



Case outline Super SMD220