Hitachi 16-Bit Single-Chip Microcomputer

H8S/2678 Series

H8S/2677
HD64F2677, HD6432677
H8S/2676
HD64F2676, HD6432676
H8S/2675
HD6432675
H8S/2673
HD6432673
H8S/2670
HD6412670

Reference Manual

HITACHI

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Organization of H8S/2678 Series Reference Manual

The following manuals are available for H8S/2678 Series products.

Table 1 H8S/2678 Series Manuals

Title	Document Code
H8S/2600 Series, H8S/2000 Series Programming Manual	ADE-602-083A
H8S/2678 Series Hardware Manual	ADE-602-193
H8S/2678 Series Reference Manual	ADE-602-192

The H8S/2600 Series, H8S/2000 Series Programming Manual gives a detailed description of the architecture and instruction set of the H8S/2600 CPU incorporated into H8S/2678 Series products.

The H8S/2678 Series Hardware Manual describes the operation of on-chip functions common to H8S/2678 Series products, and gives a detailed description of the related registers.

The H8S/2678 Series Reference Manual mainly covers information specific to H8S/2678 Series products, including pin arrangement, I/O ports, MCU operating modes (memory maps), interrupt vectors, bus control, and electrical characteristics, and also includes a brief description of all I/O registers for the convenience of the user.

The contents of the H8S/2678 Series Hardware Manual and the H8S/2678 Series Reference Manual are summarized in table 2.

Table 2 Contents of Hardware Manual and Reference Manual

No.	Item	Hardware Manual	Reference Manual
1	Overview	○	○ (Including pin arrangement)
2	MCU operating modes (including memory maps)	—	◎
3	Exception handling	○	○
4	Interrupt controller	◎	○
5	Bus controller	◎	◎
6	DMA controller (DMAC)	◎	—
7	Data transfer controller (DTC)	◎	—
8	16-bit timer unit (TPU)	◎	—
9	Programmable pulse generator (PPG)	◎	—
10	8-bit timers	◎	—
11	Watchdog timer	◎	—
12	Serial communication interface (SCI)	◎	—
13	Smart card interface	◎	—
14	A/D converter	◎	—
15	D/A converter	◎	—
16	RAM	◎	—
17	ROM (flash memory)	◎	—
18	Clock pulse generator	◎	—
19	Power-down modes	◎	—
20	I/O ports (including port block diagrams)	—	◎
21	Electrical characteristics	—	○
22	Register reference chart (in address order, with function summary)	—	○
23	Instruction set	○	—
24	Package dimension diagrams	—	○

○: Included

◎: Included (with detailed register descriptions)

—: Not included

The following chart shows where to find various kinds of information for different purposes.

For product evaluation information, or comparative specification information for current users of Hitachi products

For H8S/2678 Series specifications

Overview	1.1 Overview
Pin arrangement diagram	1.3 Pin Arrangement
Block diagrams of function modules	Section 6 Peripheral Block Diagrams
Pin functions	1.5 Pin Functions
Electrical characteristics	Section 7 Electrical Characteristics

For detailed information on functions

For details of operation of H8S/2678 Series modules

I/O port information	Section 5 I/O Ports
Interrupts and exception handling	Section 3 Exception Handling and Interrupt Controller
Information on other modules	H8S/2678 Series Hardware Manual
Pin functions	1.5 Pin Functions

For information on H8S/2678 Series operating modes

List	1.4 Pin Functions in Each Operating Mode
Detailed descriptions	Section 2 MCU Operating Modes

For use as design material

For information on H8S/2678 Series registers

List	Section 8 Registers
To find a register from its address	8.1 List of Registers (Address Order)
To find register information by function	8.2 List of Registers (By Module)
Setting procedure and notes	H8S/2678 Series Hardware Manual

For information on H8S/2678 Series instructions

List	
Operation description and notes	H8S/2600 Series, H8S/2000 Series Programming Manual
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Section 1 Overview

1.1 Overview

The H8S/2678 Series comprises microcomputers (MCUs), built around the H8S/2600 CPU, employing Hitachi's original architecture, and equipped with on-chip supporting functions necessary for system configuration.

The H8S/2600 CPU has an internal 32-bit architecture, is provided with sixteen 16-bit general registers and a concise, optimized instruction set designed for high-speed operation, and can address a 16-Mbyte linear address space. The instruction set is upward-compatible with H8/300 and H8/300H CPU instructions at the object-code level, facilitating migration from the H8/300, H8/300L, or H8/300H Series.

On-chip supporting functions required for system configuration include direct memory access controller (DMAC), EXDMA controller (EXDMAC), and data transfer controller (DTC) bus masters, ROM and RAM memory, a16-bit timer pulse unit (TPU), programmable pulse generator (PPG), 8-bit timer module (TMR), watchdog timer module (WDT), serial communication interfaces (SCI, IrDA), A/D converter, D/A converter, and I/O ports.

A high-functionality bus controller is also provided, enabling fast and easy connection of DRAM and other kinds of memory.

The on-chip ROM is either single-power-supply flash memory (F-ZTAT™*) or mask ROM, enabling users to respond quickly and flexibly to changing application specifications, growing production volumes, and other conditions. The ROM is connected to the CPU via a 16-bit data bus, enabling both byte and word data to be accessed in one state. Instruction fetching is thus speeded up, and processing speed increased.

The features of the H8S/2678 Series are shown in table 1.1.

Note: * F-ZTAT is a trademark of Hitachi, Ltd.

Table 1.1 Overview

Item	Specifications
CPU	• General-register architecture — Sixteen 16-bit general registers (also usable as sixteen 8-bit registers or eight 32-bit registers) • High-speed operation suitable for realtime control — Maximum operating frequency: 33 MHz — High-speed arithmetic operations 8/16/32-bit register-register add/subtract: 30 ns (33 MHz operation) 16 × 16-bit register-register multiply: 90 ns (33 MHz operation) 32 ÷ 16-bit register-register divide: 600 ns (33 MHz operation) • Instruction set suitable for high-speed operation — Sixty-five basic instructions — 8/16/32-bit transfer/arithmetic and logic instructions — Unsigned/signed multiply and divide instructions — Powerful bit-manipulation instructions • CPU operating mode — Advanced mode: 16-Mbyte address space
Bus controller	• Address space divided into 8 areas, with bus specifications settable independently for each area • Chip select output possible for each area • Selection of 8-bit or 16-bit access space for each area • 2-state or 3-state access space can be designated for each area • Number of program wait states can be set for each area • Maximum 8-Mbyte DRAM directly connectable (or use of interval timer possible) • External bus release function
DMA controller (DMAC)	• Selection of short address mode or full address mode • Four channels in short address mode, two channels in full address mode • Transfer possible in repeat mode, block transfer mode, etc. • Single address mode transfer possible • Can be activated by internal interrupt

Item	Specifications
EXDMA controller (EXDMAC)	• Four DMA channels exclusively for external bus use • Selection of dual address mode or single address mode • Transfer possible in burst transfer mode, block transfer mode, etc. • Repeat area setting function • Can operate in parallel with internal bus operations by internal bus master
Data transfer controller (DTC)	• Activated by internal interrupt or software • Multiple transfers or multiple types of transfer possible for one activation source • Transfer possible in repeat mode, block transfer mode, etc. • Request can be sent to CPU for interrupt that activated DTC
16-bit timer-pulse unit (TPU)	• Six-channel 16-bit timer on-chip • Pulse I/O processing capability for up to 16 pins • Automatic 2-phase encoder count capability
Programmable pulse generator (PPG)	• Maximum 16-bit pulse output possible with TPU as time base • Output trigger selectable in 4-bit groups • Non-overlap margin can be set • Direct output or inverse output setting possible
8-bit timer, 2 channels	• 8-bit up-counter (external event count capability) • Two time constant registers • Two-channel connection possible
Watchdog timer	• Watchdog timer or interval timer selectable
Serial communi-cation interface (SCI), 3 channels	• Asynchronous mode or synchronous mode selectable • Multiprocessor communication function • Smart card interface function • One channel (SCI0) functions as SCI with IrDA — Conforms to IrDA specification ver. 1.0 — IrDA format encoding/decoding of TxD and RxD

Item	Specifications
A/D converter	• Resolution: 10 bits • Input: 12 channels • 6.7 µs minimum conversion time (at 20 MHz operation) • Single or scan mode selectable • Sample-and-hold function • A/D conversion can be activated by external trigger or timer trigger
D/A converter	• Resolution: 8 bits • Output: 4 channels
I/O ports	• 103 input/output pins, 12 input pins
Memory	• Flash memory, mask ROM • High-speed static RAM

Product Name	ROM/RAM (Bytes)	F-ZTAT Version	Mask ROM Version	ROMless Version
H8S/2677	384 k/8 k	In planning stage	In planning stage	—
H8S/2676	256 k/8 k	HD64F2676	HD6432676	—
H8S/2675	128 k/8 k	—	In planning stage	—
H8S/2673	64 k/8 k	—	HD6432673	—
H8S/2670	—/8 k	—	—	HD6412670

Interrupt controller	• 17 external interrupt pins (NMI, $\overline{\text{IRQ0}}$ to $\overline{\text{IRQ15}}$) • 56 internal interrupt sources • Eight interrupt priority levels settable
Power-down state	• Clock division mode • Sleep mode • Module stop mode • Software standby mode • Hardware standby mode

Item	Specifications
Operating modes	• Selection of twelve MCU operating modes (F-ZTAT™ version)

MCU Operating Mode	CPU Operating Mode	Description	On-Chip ROM	External Data Bus	
				Initial Value	Maximum Value
0	—	—	—	—	—
1	Advanced	Expanded mode with on-chip ROM disabled	Disabled	16 bits	16 bits
2				8 bits	16 bits
3		—	—	—	—
4		Expanded mode with on-chip ROM enabled	Enabled	8 bits	16 bits
5		External ROM activation expanded mode with on-chip ROM enabled	Enabled	16 bits	16 bits
6				8 bits	16 bits
7		Single-chip activation mode with on-chip ROM enabled	Enabled	—	16 bits
8	—	—	—	—	—
9					
10	Advanced	Boot mode	Enabled	8 bits	16 bits
11				—	—
12	Advanced	User program mode	Enabled	8 bits	16 bits
13				16 bits	16 bits
14	Advanced	User program mode	Enabled	8 bits	16 bits
15				—	16 bits

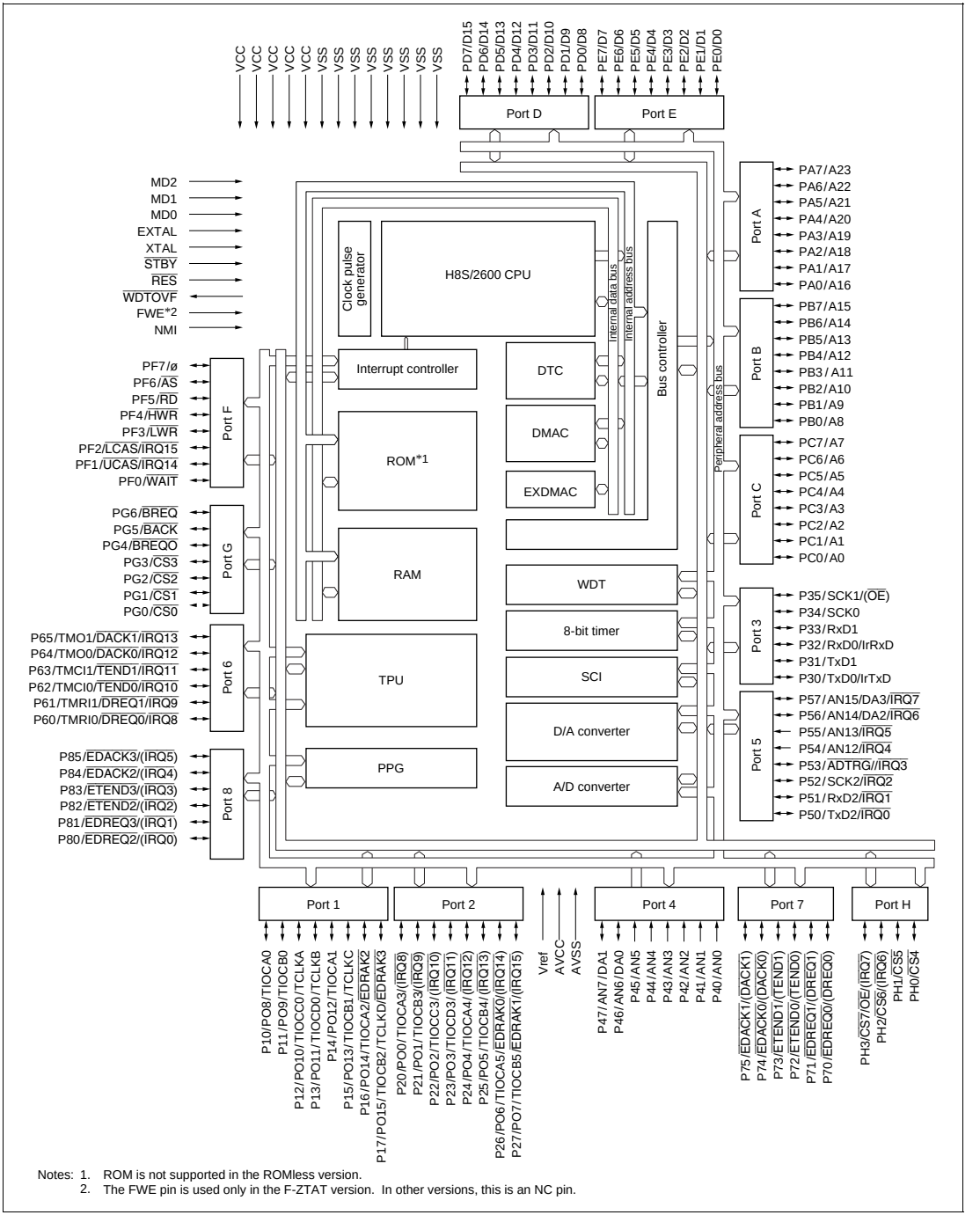
• Selection of six MCU operating modes (mask ROM version, ROMless version)

MCU Operating Mode	CPU Operating Mode	Description	On-Chip ROM	External Data Bus	
				Initial Value	Maximum Value
0	—	—	—	—	—
1*	Advanced	Expanded mode with on-chip ROM disabled	Disabled	16 bits	16 bits
2*				8 bits	16 bits
3	—	—	—	—	—
4	Advanced	Expanded mode with on-chip ROM enabled	Enabled	8 bits	16 bits
5		External ROM activation expanded mode with on-chip ROM enabled	Enabled	16 bits	16 bits
6				8 bits	16 bits
7		Single-chip activation mode with on-chip ROM enabled	Enabled	—	16 bits

Note: * Only modes 1 and 2 are available in the ROMless version.

Clock pulse generator	• Built-in PLL circuits (×1, ×2, ×4) Input clock frequency (2 to 33 MHz)
Packages	• 144-pin plastic QFP (FP-144)

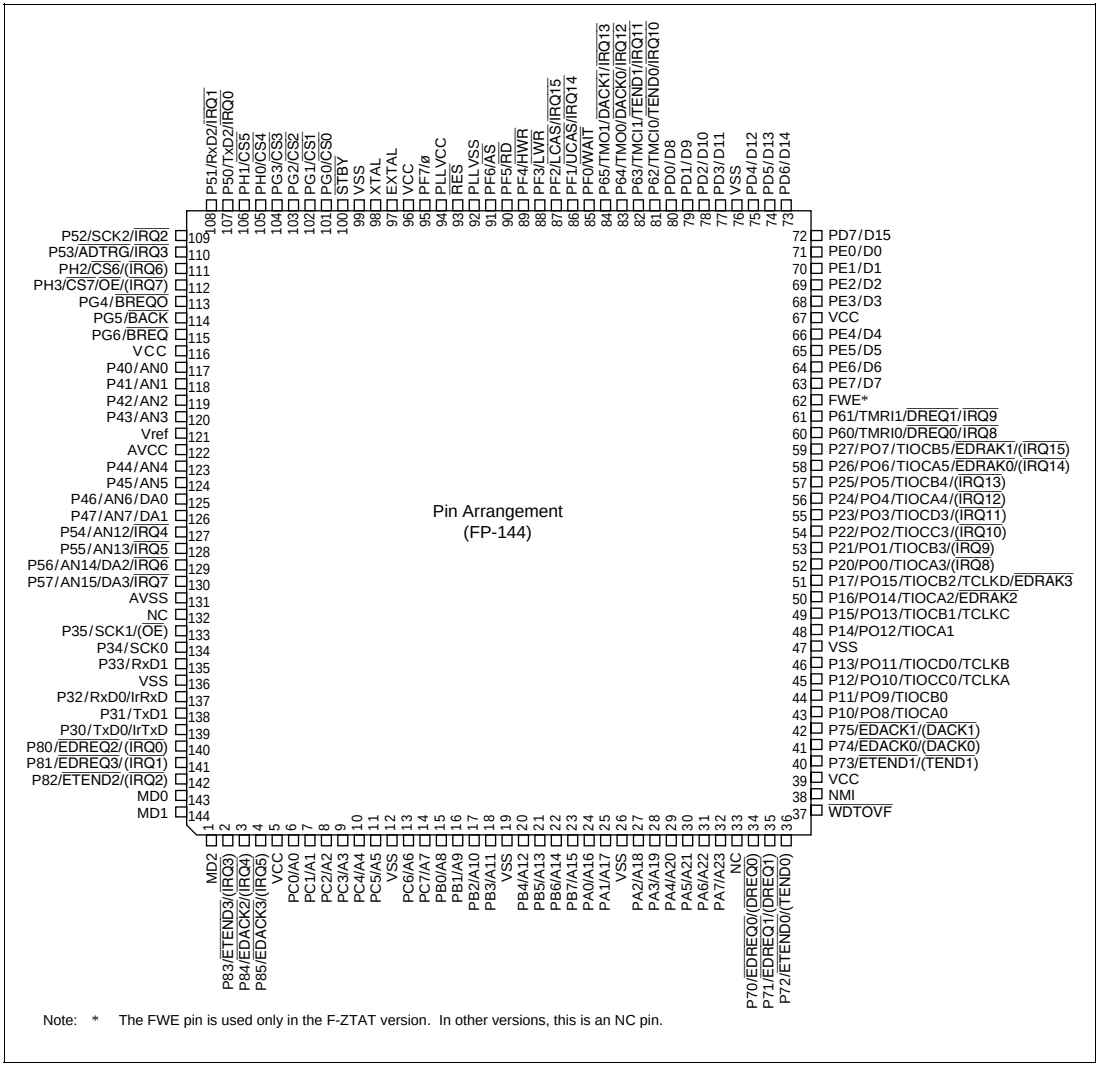
1.2 Block Diagram



Notes: 1. ROM is not supported in the ROMless version.
2. The FWE pin is used only in the F-ZTAT version. In other versions, this is an NC pin.

Figure 1.1 Internal Block Diagram

1.3 Pin Arrangement



Note: * The FWE pin is used only in the F-ZTAT version. In other versions, this is an NC pin.

Figure 1.2 Pin Arrangement (FP-144: Top View)

1.4 Pin Functions in Each Operating Mode

Table 1.2 Pin Functions in Each Operating Mode

Pin No.	Pin Name						Flash Memory Programmer Mode
	Mode 1	Mode 2	Mode 4	Mode 5	Mode 6	Mode 7	
1	MD2	MD2	MD2	MD2	MD2	MD2	VSS
2	P83/ETEND3/(IRQ3)	P83/ETEND3/(IRQ3)	P83/ETEND3/(IRQ3)	P83/ETEND3/(IRQ3)	P83/ETEND3/(IRQ3)	When EXPE = 1: P83/ETEND3/(IRQ3) When EXPE = 0: P83/(IRQ3)	NC
3	P84/EDACK2/(IRQ4)	P84/EDACK2/(IRQ4)	P84/EDACK2/(IRQ4)	P84/EDACK2/(IRQ4)	P84/EDACK2/(IRQ4)	When EXPE = 1: P84/EDACK2/(IRQ4) When EXPE = 0: P84/(IRQ4)	NC
4	P85/EDACK3/(IRQ5)	P85/EDACK3/(IRQ5)	P85/EDACK3/(IRQ5)	P85/EDACK3/(IRQ5)	P85/EDACK3/(IRQ5)	When EXPE = 1: P85/EDACK3/(IRQ5) When EXPE = 0: P85/(IRQ5)	NC
5	VCC	VCC	VCC	VCC	VCC	VCC	VCC
6	A0	A0	PC0/A0	A0	A0	When EXPE = 1: PC0/A0 When EXPE = 0: PC0	A0
7	A1	A1	PC1/A1	A1	A1	When EXPE = 1: PC1/A1 When EXPE = 0: PC1	A1
8	A2	A2	PC2/A2	A2	A2	When EXPE = 1: PC2/A2 When EXPE = 0: PC2	A2
9	A3	A3	PC3/A3	A3	A3	When EXPE = 1: PC3/A3 When EXPE = 0: PC3	A3
10	A4	A4	PC4/A4	A4	A4	When EXPE = 1: PC4/A4 When EXPE = 0: PC4	A4

Pin No.	Pin Name						Flash Memory Programmer Mode
	Mode 1	Mode 2	Mode 4	Mode 5	Mode 6	Mode 7	
11	A5	A5	PC5/A5	A5	A5	When EXPE = 1: PC5/A5 When EXPE = 0: PC5	A5
12	VSS	VSS	VSS	VSS	VSS	VSS	VSS
13	A6	A6	PC6/A6	A6	A6	When EXPE = 1: PC6/A6 When EXPE = 0: PC6	A6
14	A7	A7	PC7/A7	A7	A7	When EXPE = 1: PC7/A7 When EXPE = 0: PC7	A7
15	A8	A8	PB0/A8	A8	A8	When EXPE = 1: PB0/A8 When EXPE = 0: PB0	A8
16	A9	A9	PB1/A9	A9	A9	When EXPE = 1: PB1/A9 When EXPE = 0: PB1	A9
17	A10	A10	PB2/A10	A10	A10	When EXPE = 1: PB2/A10 When EXPE = 0: PB2	A10
18	A11	A11	PB3/A11	A11	A11	When EXPE = 1: PB3/A11 When EXPE = 0: PB3	A11
19	VSS	VSS	VSS	VSS	VSS	VSS	VSS
20	A12	A12	PB4/A12	A12	A12	When EXPE = 1: PB4/A12 When EXPE = 0: PB4	A12
21	A13	A13	PB5/A13	A13	A13	When EXPE = 1: PB5/A13 When EXPE = 0: PB5	A13

Pin No.	Pin Name						Flash Memory Programmer Mode
	Mode 1	Mode 2	Mode 4	Mode 5	Mode 6	Mode 7	
22	A14	A14	PB6/A14	A14	A14	When EXPE = 1: PB6/A14 When EXPE = 0: PB6	A14
23	A15	A15	PB7/A15	A15	A15	When EXPE = 1: PB7/A15 When EXPE = 0: PB7	A15
24	A16	A16	PA0/A16	A16	A16	When EXPE = 1: PA0/A16 When EXPE = 0: PA0	A16
25	A17	A17	PA1/A17	A17	A17	When EXPE = 1: PA1/A17 When EXPE = 0: PA1	A17
26	VSS	VSS	VSS	VSS	VSS	VSS	VSS
27	A18	A18	PA2/A18	A18	A18	When EXPE = 1: PA2/A18 When EXPE = 0: PA2	A18
28	A19	A19	PA3/A19	A19	A19	When EXPE = 1: PA3/A19 When EXPE = 0: PA3	NC
29	A20	A20	PA4/A20	A20	A20	When EXPE = 1: PA4/A20 When EXPE = 0: PA4	NC
30	PA5/A21	PA5/A21	PA5/A21	PA5/A21	PA5/A21	When EXPE = 1: PA5/A21 When EXPE = 0: PA5	NC
31	PA6/A22	PA6/A22	PA6/A22	PA6/A22	PA6/A22	When EXPE = 1: PA6/A22 When EXPE = 0: PA6	NC

Pin No.	Pin Name						Flash Memory Programmer Mode
	Mode 1	Mode 2	Mode 4	Mode 5	Mode 6	Mode 7	
32	PA7/A23	PA7/A23	PA7/A23	PA7/A23	PA7/A23	When EXPE = 1: PA7/A23 When EXPE = 0: PA7	NC
33	NC	NC	NC	NC	NC	NC	NC
34	P70/$\overline{\text{EDREQ0}}$/($\overline{\text{DREQ0}}$)	P70/$\overline{\text{EDREQ0}}$/($\overline{\text{DREQ0}}$)	P70/$\overline{\text{EDREQ0}}$/($\overline{\text{DREQ0}}$)	P70/$\overline{\text{EDREQ0}}$/($\overline{\text{DREQ0}}$)	P70/$\overline{\text{EDREQ0}}$/($\overline{\text{DREQ0}}$)	When EXPE = 1: P70/$\overline{\text{EDREQ0}}$/($\overline{\text{DREQ0}}$) When EXPE = 0: P70/($\overline{\text{DREQ0}}$)	NC
35	P71/$\overline{\text{EDREQ1}}$/($\overline{\text{DREQ1}}$)	P71/$\overline{\text{EDREQ1}}$/($\overline{\text{DREQ1}}$)	P71/$\overline{\text{EDREQ1}}$/($\overline{\text{DREQ1}}$)	P71/$\overline{\text{EDREQ1}}$/($\overline{\text{DREQ1}}$)	P71/$\overline{\text{EDREQ1}}$/($\overline{\text{DREQ1}}$)	When EXPE = 1: P71/$\overline{\text{EDREQ1}}$/($\overline{\text{DREQ1}}$) When EXPE = 0: P71/($\overline{\text{DREQ1}}$)	NC
36	P72/$\overline{\text{ETEND0}}$/($\overline{\text{TEND0}}$)	P72/$\overline{\text{ETEND0}}$/($\overline{\text{TEND0}}$)	P72/$\overline{\text{ETEND0}}$/($\overline{\text{TEND0}}$)	P72/$\overline{\text{ETEND0}}$/($\overline{\text{TEND0}}$)	P72/$\overline{\text{ETEND0}}$/($\overline{\text{TEND0}}$)	When EXPE = 1: P72/$\overline{\text{ETEND0}}$/($\overline{\text{TEND0}}$) When EXPE = 0: P72/(TEND0)	NC
37	$\overline{\text{WDTOVF}}$	$\overline{\text{WDTOVF}}$	$\overline{\text{WDTOVF}}$	$\overline{\text{WDTOVF}}$	$\overline{\text{WDTOVF}}$	$\overline{\text{WDTOVF}}$	NC
38	NMI	NMI	NMI	NMI	NMI	NMI	VCC
39	VCC	VCC	VCC	VCC	VCC	VCC	VCC
40	P73/$\overline{\text{ETEND1}}$/($\overline{\text{TEND1}}$)	P73/$\overline{\text{ETEND1}}$/($\overline{\text{TEND1}}$)	P73/$\overline{\text{ETEND1}}$/($\overline{\text{TEND1}}$)	P73/$\overline{\text{ETEND1}}$/($\overline{\text{TEND1}}$)	P73/$\overline{\text{ETEND1}}$/($\overline{\text{TEND1}}$)	When EXPE = 1: P73/$\overline{\text{ETEND1}}$/($\overline{\text{TEND1}}$) When EXPE = 0: P73/($\overline{\text{TEND1}}$)	NC
41	P74/$\overline{\text{EDACK0}}$/($\overline{\text{DACK0}}$)	P74/$\overline{\text{EDACK0}}$/($\overline{\text{DACK0}}$)	P74/$\overline{\text{EDACK0}}$/($\overline{\text{DACK0}}$)	P74/$\overline{\text{EDACK0}}$/($\overline{\text{DACK0}}$)	P74/$\overline{\text{EDACK0}}$/($\overline{\text{DACK0}}$)	When EXPE = 1: P74/$\overline{\text{EDACK0}}$/($\overline{\text{DACK0}}$) When EXPE = 0: P74/($\overline{\text{DACK0}}$)	NC
42	P75/$\overline{\text{EDACK1}}$/($\overline{\text{DACK1}}$)	P75/$\overline{\text{EDACK1}}$/($\overline{\text{DACK1}}$)	P75/$\overline{\text{EDACK1}}$/($\overline{\text{DACK1}}$)	P75/$\overline{\text{EDACK1}}$/($\overline{\text{DACK1}}$)	P75/$\overline{\text{EDACK1}}$/($\overline{\text{DACK1}}$)	When EXPE = 1: P75/$\overline{\text{EDACK1}}$/($\overline{\text{DACK1}}$) When EXPE = 0: P75/($\overline{\text{DACK1}}$)	NC
43	P10/PO8/TIOCA0	P10/PO8/TIOCA0	P10/PO8/TIOCA0	P10/PO8/TIOCA0	P10/PO8/TIOCA0	P10/PO8/TIOCA0	NC

Pin No.	Pin Name						Flash Memory Programmer Mode
	Mode 1	Mode 2	Mode 4	Mode 5	Mode 6	Mode 7	
44	P11/PO9/ TIOCB0	P11/PO9/ TIOCB0	P11/PO9/ TIOCB0	P11/PO9/ TIOCB0	P11/PO9/ TIOCB0	P11/PO9/ TIOCB0	NC
45	P12/PO10/ TIOCC0/ TCLKA	P12/PO10/ TIOCC0/ TCLKA	P12/PO10/ TIOCC0/ TCLKA	P12/PO10/ TIOCC0/ TCLKA	P12/PO10/ TIOCC0/ TCLKA	P12/PO10/ TIOCC0/ TCLKA	NC
46	P13/PO11/ TIOCD0/ TCLKB	P13/PO11/ TIOCD0/ TCLKB	P13/PO11/ TIOCD0/ TCLKB	P13/PO11/ TIOCD0/ TCLKB	P13/PO11/ TIOCD0/ TCLKB	P13/PO11/ TIOCD0/ TCLKB	NC
47	VSS	VSS	VSS	VSS	VSS	VSS	VSS
48	P14/PO12/ TIOCA1	P14/PO12/ TIOCA1	P14/PO12/ TIOCA1	P14/PO12/ TIOCA1	P14/PO12/ TIOCA1	P14/PO12/ TIOCA1	NC
49	P15/PO13/ TIOCB1/ TCLKC	P15/PO13/ TIOCB1/ TCLKC	P15/PO13/ TIOCB1/ TCLKC	P15/PO13/ TIOCB1/ TCLKC	P15/PO13/ TIOCB1/ TCLKC	P15/PO13/ TIOCB1/ TCLKC	NC
50	P16/PO14/ TIOCA2/ $\overline{\text{EDRAK2}}$	P16/PO14/ TIOCA2/ $\overline{\text{EDRAK2}}$	P16/PO14/ TIOCA2/ $\overline{\text{EDRAK2}}$	P16/PO14/ TIOCA2/ $\overline{\text{EDRAK2}}$	P16/PO14/ TIOCA2/ $\overline{\text{EDRAK2}}$	When EXPE = 1: P16/PO14/ TIOCA2/ $\overline{\text{EDRAK2}}$ When EXPE = 0: P16/PO14/ TIOCA2	NC
51	P17/PO15/ TIOCB2/ TCLKD/ $\overline{\text{EDRAK3}}$	P17/PO15/ TIOCB2/ TCLKD/ $\overline{\text{EDRAK3}}$	P17/PO15/ TIOCB2/ TCLKD/ $\overline{\text{EDRAK3}}$	P17/PO15/ TIOCB2/ TCLKD/ $\overline{\text{EDRAK3}}$	P17/PO15/ TIOCB2/ TCLKD/ $\overline{\text{EDRAK3}}$	When EXPE = 1: P17/PO15/ TIOCB2/TCLKD/$\overline{\text{E}}$ $\overline{\text{DRAK3}}$ When EXPE = 0: P17/PO15/ TIOCB2/TCLKD	NC
52	P20/PO0/ TIOCA3/ ($\overline{\text{IRQ8}}$)	P20/PO0/ TIOCA3/ ($\overline{\text{IRQ8}}$)	P20/PO0/ TIOCA3/ ($\overline{\text{IRQ8}}$)	P20/PO0/ TIOCA3/ ($\overline{\text{IRQ8}}$)	P20/PO0/ TIOCA3/ ($\overline{\text{IRQ8}}$)	P20/PO0/ TIOCA3/ ($\overline{\text{IRQ8}}$)	NC
53	P21/PO1/ TIOCB3/ ($\overline{\text{IRQ9}}$)	P21/PO1/ TIOCB3/ ($\overline{\text{IRQ9}}$)	P21/PO1/ TIOCB3/ ($\overline{\text{IRQ9}}$)	P21/PO1/ TIOCB3/ ($\overline{\text{IRQ9}}$)	P21/PO1/ TIOCB3/ ($\overline{\text{IRQ9}}$)	P21/PO1/ TIOCB3/ ($\overline{\text{IRQ9}}$)	NC
54	P22/PO2/ TIOCC3/ ($\overline{\text{IRQ10}}$)	P22/PO2/ TIOCC3/ ($\overline{\text{IRQ10}}$)	P22/PO2/ TIOCC3/ ($\overline{\text{IRQ10}}$)	P22/PO2/ TIOCC3/ ($\overline{\text{IRQ10}}$)	P22/PO2/ TIOCC3/ ($\overline{\text{IRQ10}}$)	P22/PO2/ TIOCC3/ ($\overline{\text{IRQ10}}$)	$\overline{\text{OE}}$
55	P23/PO3/ TIOCD3/ ($\overline{\text{IRQ11}}$)	P23/PO3/ TIOCD3/ ($\overline{\text{IRQ11}}$)	P23/PO3/ TIOCD3/ ($\overline{\text{IRQ11}}$)	P23/PO3/ TIOCD3/ ($\overline{\text{IRQ11}}$)	P23/PO3/ TIOCD3/ ($\overline{\text{IRQ11}}$)	P23/PO3/ TIOCD3/ ($\overline{\text{IRQ11}}$)	$\overline{\text{CE}}$

Pin No.	Pin Name						Flash Memory Programmer Mode
	Mode 1	Mode 2	Mode 4	Mode 5	Mode 6	Mode 7	
56	P24/PO4/ TIOCA4/ ($\overline{\text{IRQ12}}$)	P24/PO4/ TIOCA4/ ($\overline{\text{IRQ12}}$)	P24/PO4/ TIOCA4/ ($\overline{\text{IRQ12}}$)	P24/PO4/ TIOCA4/ ($\overline{\text{IRQ12}}$)	P24/PO4/ TIOCA4/ ($\overline{\text{IRQ12}}$)	P24/PO4/ TIOCA4/ ($\overline{\text{IRQ12}}$)	$\overline{\text{WE}}$
57	P25/PO5/ TIOCB4/ ($\overline{\text{IRQ13}}$)	P25/PO5/ TIOCB4/ ($\overline{\text{IRQ13}}$)	P25/PO5/ TIOCB4/ ($\overline{\text{IRQ13}}$)	P25/PO5/ TIOCB4/ ($\overline{\text{IRQ13}}$)	P25/PO5/ TIOCB4/ ($\overline{\text{IRQ13}}$)	P25/PO5/ TIOCB4/ ($\overline{\text{IRQ13}}$)	VSS
58	P26/PO6/ TIOCA5/ $\overline{\text{EDRAK0}}$/ ($\overline{\text{IRQ14}}$)	P26/PO6/ TIOCA5/ $\overline{\text{EDRAK0}}$/ ($\overline{\text{IRQ14}}$)	P26/PO6/ TIOCA5/ $\overline{\text{EDRAK0}}$/ ($\overline{\text{IRQ14}}$)	P26/PO6/ TIOCA5/ $\overline{\text{EDRAK0}}$/ ($\overline{\text{IRQ14}}$)	P26/PO6/ TIOCA5/ $\overline{\text{EDRAK0}}$/ ($\overline{\text{IRQ14}}$)	When EXPE = 1: P26/PO6/ TIOCA5/ $\overline{\text{EDRAK0}}$/ ($\overline{\text{IRQ14}}$) When EXPE = 0: P26/PO6/ TIOCA5/($\overline{\text{IRQ14}}$)	NC
59	P27/PO7/ TIOCB5/ $\overline{\text{EDRAK1}}$/ ($\overline{\text{IRQ15}}$)	P27/PO7/ TIOCB5/ $\overline{\text{EDRAK1}}$/ ($\overline{\text{IRQ15}}$)	P27/PO7/ TIOCB5/ $\overline{\text{EDRAK1}}$/ ($\overline{\text{IRQ15}}$)	P27/PO7/ TIOCB5/ $\overline{\text{EDRAK1}}$/ ($\overline{\text{IRQ15}}$)	P27/PO7/ TIOCB5/ $\overline{\text{EDRAK1}}$/ ($\overline{\text{IRQ15}}$)	When EXPE = 1: P27/PO7/ TIOCB5/ $\overline{\text{EDRAK1}}$/ ($\overline{\text{IRQ15}}$) When EXPE = 0: P27/PO7/ TIOCB5/($\overline{\text{IRQ15}}$)	NC
60	P60/TMRI0/ $\overline{\text{DREQ0}}$/ $\overline{\text{IRQ8}}$	P60/TMRI0/ $\overline{\text{DREQ0}}$/ $\overline{\text{IRQ8}}$	P60/TMRI0/ $\overline{\text{DREQ0}}$/ $\overline{\text{IRQ8}}$	P60/TMRI0/ $\overline{\text{DREQ0}}$/ $\overline{\text{IRQ8}}$	P60/TMRI0/ $\overline{\text{DREQ0}}$/ $\overline{\text{IRQ8}}$	P60/TMRI0/ $\overline{\text{DREQ0}}$/ $\overline{\text{IRQ8}}$	NC
61	P61/TMRI1/ $\overline{\text{DREQ1}}$/ $\overline{\text{IRQ9}}$	P61/TMRI1/ $\overline{\text{DREQ1}}$/ $\overline{\text{IRQ9}}$	P61/TMRI1/ $\overline{\text{DREQ1}}$/ $\overline{\text{IRQ9}}$	P61/TMRI1/ $\overline{\text{DREQ1}}$/ $\overline{\text{IRQ9}}$	P61/TMRI1/ $\overline{\text{DREQ1}}$/ $\overline{\text{IRQ9}}$	P61/TMRI1/ $\overline{\text{DREQ1}}$/ $\overline{\text{IRQ9}}$	NC
62	FWE*	FWE*	FWE*	FWE*	FWE*	FWE*	FWE*
63	D7	PE7/D7	PE7/D7	D7	PE7/D7	When EXPE = 1: PE7/D7 When EXPE = 0: PE7	NC
64	D6	PE6/D6	PE6/D6	D6	PE6/D6	When EXPE = 1: PE6/D6 When EXPE = 0: PE6	NC
65	D5	PE5/D5	PE5/D5	D5	PE5/D5	When EXPE = 1: PE5/D5 When EXPE = 0: PE5	NC

Pin No.	Pin Name						Flash Memory Programmer Mode
	Mode 1	Mode 2	Mode 4	Mode 5	Mode 6	Mode 7	
66	D4	PE4/D4	PE4/D4	D4	PE4/D4	When EXPE = 1: PE4/D4 When EXPE = 0: PE4	NC
67	VCC	VCC	VCC	VCC	VCC	VCC	VCC
68	D3	PE3/D3	PE3/D3	D3	PE3/D3	When EXPE = 1: PE3/D3 When EXPE = 0: PE3	NC
69	D2	PE2/D2	PE2/D2	D2	PE2/D2	When EXPE = 1: PE2/D2 When EXPE = 0: PE2	NC
70	D1	PE1/D1	PE1/D1	D1	PE1/D1	When EXPE = 1: PE1/D1 When EXPE = 0: PE1	NC
71	D0	PE0/D0	PE0/D0	D0	PE0/D0	When EXPE = 1: PE0/D0 When EXPE = 0: PE0	NC
72	D15	D15	D15	D15	D15	When EXPE = 1: D15 When EXPE = 0: PD7	I/O7
73	D14	D14	D14	D14	D14	When EXPE = 1: D14 When EXPE = 0: PD6	I/O6
74	D13	D13	D13	D13	D13	When EXPE = 1: D13 When EXPE = 0: PD5	I/O5
75	D12	D12	D12	D12	D12	When EXPE = 1: D12 When EXPE = 0: PD4	I/O4
76	VSS	VSS	VSS	VSS	VSS	VSS	VSS

Pin No.	Pin Name						Flash Memory Programmer Mode
	Mode 1	Mode 2	Mode 4	Mode 5	Mode 6	Mode 7	
77	D11	D11	D11	D11	D11	When EXPE = 1: D11 When EXPE = 0: PD3	I/O3
78	D10	D10	D10	D10	D10	When EXPE = 1: D10 When EXPE = 0: PD2	I/O2
79	D9	D9	D9	D9	D9	When EXPE = 1: D9 When EXPE = 0: PD1	I/O1
80	D8	D8	D8	D8	D8	When EXPE = 1: D8 When EXPE = 0: PD0	I/O0
81	P62/TMCI0/ $\overline{\text{TEND0}}$/ $\overline{\text{IRQ10}}$	P62/TMCI0/ $\overline{\text{TEND0}}$/ $\overline{\text{IRQ10}}$	P62/TMCI0/ $\overline{\text{TEND0}}$/ $\overline{\text{IRQ10}}$	P62/TMCI0/ $\overline{\text{TEND0}}$/ $\overline{\text{IRQ10}}$	P62/TMCI0/ $\overline{\text{TEND0}}$/ $\overline{\text{IRQ10}}$	P62/TMCI0/ $\overline{\text{TEND0}}$/ $\overline{\text{IRQ10}}$	NC
82	P63/TMCI1/ $\overline{\text{TEND1}}$/ $\overline{\text{IRQ11}}$	P63/TMCI1/ $\overline{\text{TEND1}}$/ $\overline{\text{IRQ11}}$	P63/TMCI1/ $\overline{\text{TEND1}}$/ $\overline{\text{IRQ11}}$	P63/TMCI1/ $\overline{\text{TEND1}}$/ $\overline{\text{IRQ11}}$	P63/TMCI1/ $\overline{\text{TEND1}}$/ $\overline{\text{IRQ11}}$	P63/TMCI1/ $\overline{\text{TEND1}}$/ $\overline{\text{IRQ11}}$	NC
83	P64/TMO0/ $\overline{\text{DACK0}}$/ $\overline{\text{IRQ12}}$	P64/TMO0/ $\overline{\text{DACK0}}$/ $\overline{\text{IRQ12}}$	P64/TMO0/ $\overline{\text{DACK0}}$/ $\overline{\text{IRQ12}}$	P64/TMO0/ $\overline{\text{DACK0}}$/ $\overline{\text{IRQ12}}$	P64/TMO0/ $\overline{\text{DACK0}}$/ $\overline{\text{IRQ12}}$	P64/TMO0/ $\overline{\text{DACK0}}$/ $\overline{\text{IRQ12}}$	NC
84	P65/TMO1/ $\overline{\text{DACK1}}$/ $\overline{\text{IRQ13}}$	P65/TMO1/ $\overline{\text{DACK1}}$/ $\overline{\text{IRQ13}}$	P65/TMO1/ $\overline{\text{DACK1}}$/ $\overline{\text{IRQ13}}$	P65/TMO1/ $\overline{\text{DACK1}}$/ $\overline{\text{IRQ13}}$	P65/TMO1/ $\overline{\text{DACK1}}$/ $\overline{\text{IRQ13}}$	P65/TMO1/ $\overline{\text{DACK1}}$/ $\overline{\text{IRQ13}}$	NC
85	PF0/ $\overline{\text{WAIT}}$	PF0/ $\overline{\text{WAIT}}$	PF0/ $\overline{\text{WAIT}}$	PF0/ $\overline{\text{WAIT}}$	PF0/ $\overline{\text{WAIT}}$	When EXPE = 1: PF0/ $\overline{\text{WAIT}}$ When EXPE = 0: PF0	NC
86	PF1/ $\overline{\text{UCAS}}$/ $\overline{\text{IRQ14}}$	PF1/ $\overline{\text{UCAS}}$/ $\overline{\text{IRQ14}}$	PF1/ $\overline{\text{UCAS}}$/ $\overline{\text{IRQ14}}$	PF1/ $\overline{\text{UCAS}}$/ $\overline{\text{IRQ14}}$	PF1/ $\overline{\text{UCAS}}$/ $\overline{\text{IRQ14}}$	When EXPE = 1: PF1/ $\overline{\text{UCAS}}$/ $\overline{\text{IRQ14}}$ When EXPE = 0: PF1/ $\overline{\text{IRQ14}}$	NC

Pin No.	Pin Name						Flash Memory Programmer Mode
	Mode 1	Mode 2	Mode 4	Mode 5	Mode 6	Mode 7	
87	PF2/$\overline{\text{LCAS}}$/$\overline{\text{IRQ15}}$	PF2/$\overline{\text{LCAS}}$/$\overline{\text{IRQ15}}$	PF2/$\overline{\text{LCAS}}$/$\overline{\text{IRQ15}}$	PF2/$\overline{\text{LCAS}}$/$\overline{\text{IRQ15}}$	PF2/$\overline{\text{LCAS}}$/$\overline{\text{IRQ15}}$	When EXPE = 1: PF2/$\overline{\text{LCAS}}$/$\overline{\text{IRQ15}}$ When EXPE = 0: PF2/$\overline{\text{IRQ15}}$	NC
88	PF3/$\overline{\text{LWR}}$	PF3/$\overline{\text{LWR}}$	PF3/$\overline{\text{LWR}}$	PF3/$\overline{\text{LWR}}$	PF3/$\overline{\text{LWR}}$	When EXPE = 1: PF3/$\overline{\text{LWR}}$ When EXPE = 0: PF3	NC
89	$\overline{\text{HWR}}$	$\overline{\text{HWR}}$	$\overline{\text{HWR}}$	$\overline{\text{HWR}}$	$\overline{\text{HWR}}$	When EXPE = 1: $\overline{\text{HWR}}$ When EXPE = 0: PF4	NC
90	$\overline{\text{RD}}$	$\overline{\text{RD}}$	$\overline{\text{RD}}$	$\overline{\text{RD}}$	$\overline{\text{RD}}$	When EXPE = 1: $\overline{\text{RD}}$ When EXPE = 0: PF5	NC
91	PF6/$\overline{\text{AS}}$	PF6/$\overline{\text{AS}}$	PF6/$\overline{\text{AS}}$	PF6/$\overline{\text{AS}}$	PF6/$\overline{\text{AS}}$	When EXPE = 1: PF6/$\overline{\text{AS}}$ When EXPE = 0: PF6	NC
92	PLLVSS	PLLVSS	PLLVSS	PLLVSS	PLLVSS	PLLVSS	VSS
93	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$
94	PLLVCC	PLLVCC	PLLVCC	PLLVCC	PLLVCC	PLLVCC	VCC
95	PF7/ø	PF7/ø	PF7/ø	PF7/ø	PF7/ø	PF7/ø	NC
96	VCC	VCC	VCC	VCC	VCC	VCC	VCC
97	EXTAL	EXTAL	EXTAL	EXTAL	EXTAL	EXTAL	EXTAL
98	XTAL	XTAL	XTAL	XTAL	XTAL	XTAL	XTAL
99	VSS	VSS	VSS	VSS	VSS	VSS	VSS
100	$\overline{\text{STBY}}$	$\overline{\text{STBY}}$	$\overline{\text{STBY}}$	$\overline{\text{STBY}}$	$\overline{\text{STBY}}$	$\overline{\text{STBY}}$	VCC
101	PG0/$\overline{\text{CS0}}$	PG0/$\overline{\text{CS0}}$	PG0/$\overline{\text{CS0}}$	PG0/$\overline{\text{CS0}}$	PG0/$\overline{\text{CS0}}$	When EXPE = 1: PG0/$\overline{\text{CS0}}$ When EXPE = 0: PG0	NC
102	PG1/$\overline{\text{CS1}}$	PG1/$\overline{\text{CS1}}$	PG1/$\overline{\text{CS1}}$	PG1/$\overline{\text{CS1}}$	PG1/$\overline{\text{CS1}}$	When EXPE = 1: PG1/$\overline{\text{CS1}}$ When EXPE = 0: PG1	NC

Pin No.	Pin Name						Flash Memory Programmer Mode
	Mode 1	Mode 2	Mode 4	Mode 5	Mode 6	Mode 7	
103	PG2/$\overline{CS2}$	PG2/$\overline{CS2}$	PG2/$\overline{CS2}$	PG2/$\overline{CS2}$	PG2/$\overline{CS2}$	When EXPE = 1: PG2/$\overline{CS2}$ When EXPE = 0: PG2	NC
104	PG3/$\overline{CS3}$	PG3/$\overline{CS3}$	PG3/$\overline{CS3}$	PG3/$\overline{CS3}$	PG3/$\overline{CS3}$	When EXPE = 1: PG3/$\overline{CS3}$ When EXPE = 0: PG3	NC
105	PH0/$\overline{CS4}$	PH0/$\overline{CS4}$	PH0/$\overline{CS4}$	PH0/$\overline{CS4}$	PH0/$\overline{CS4}$	When EXPE = 1: PH0/$\overline{CS4}$ When EXPE = 0: PH0	NC
106	PH1/$\overline{CS5}$	PH1/$\overline{CS5}$	PH1/$\overline{CS5}$	PH1/$\overline{CS5}$	PH1/$\overline{CS5}$	When EXPE = 1: PH1/$\overline{CS5}$ When EXPE = 0: PH1	NC
107	P50/TxD2/ $\overline{IRQ0}$	P50/TxD2/ $\overline{IRQ0}$	P50/TxD2/ $\overline{IRQ0}$	P50/TxD2/ $\overline{IRQ0}$	P50/TxD2/ $\overline{IRQ0}$	P50/TxD2/ $\overline{IRQ0}$	VSS
108	P51/RxD2/ $\overline{IRQ1}$	P51/RxD2/ $\overline{IRQ1}$	P51/RxD2/ $\overline{IRQ1}$	P51/RxD2/ $\overline{IRQ1}$	P51/RxD2/ $\overline{IRQ1}$	P51/RxD2/ $\overline{IRQ1}$	VSS
109	P52/SCK2/ $\overline{IRQ2}$	P52/SCK2/ $\overline{IRQ2}$	P52/SCK2/ $\overline{IRQ2}$	P52/SCK2/ $\overline{IRQ2}$	P52/SCK2/ $\overline{IRQ2}$	P52/SCK2/ $\overline{IRQ2}$	VCC
110	P53/ $\overline{ADTRG}$/ $\overline{IRQ3}$	P53/ $\overline{ADTRG}$/ $\overline{IRQ3}$	P53/ $\overline{ADTRG}$/ $\overline{IRQ3}$	P53/ $\overline{ADTRG}$/ $\overline{IRQ3}$	P53/$\overline{ADTRG}$/ $\overline{IRQ3}$	P53/$\overline{ADTRG}$/ $\overline{IRQ3}$	NC
111	PH2/$\overline{CS6}$/ ($\overline{IRQ6}$)	PH2/$\overline{CS6}$/ ($\overline{IRQ6}$)	PH2/$\overline{CS6}$/ ($\overline{IRQ6}$)	PH2/$\overline{CS6}$/ ($\overline{IRQ6}$)	PH2/$\overline{CS6}$/ ($\overline{IRQ6}$)	When EXPE = 1: PH2/$\overline{CS6}$/($\overline{IRQ6}$) When EXPE = 0: PH2/($\overline{IRQ6}$)	NC
112	PH3/$\overline{CS7}$/ $\overline{OE}$/($\overline{IRQ7}$)	PH3/$\overline{CS7}$/ $\overline{OE}$/($\overline{IRQ7}$)	PH3/$\overline{CS7}$/ $\overline{OE}$/($\overline{IRQ7}$)	PH3/$\overline{CS7}$/ $\overline{OE}$/($\overline{IRQ7}$)	PH3/$\overline{CS7}$/ $\overline{OE}$/($\overline{IRQ7}$)	When EXPE = 1: PH3/$\overline{CS7}$/$\overline{OE}$/ ($\overline{IRQ7}$) When EXPE = 0: PH3/($\overline{IRQ7}$)	NC
113	PG4/ $\overline{BREQO}$	PG4/ $\overline{BREQO}$	PG4/ $\overline{BREQO}$	PG4/ $\overline{BREQO}$	PG4/$\overline{BREQO}$	When EXPE = 1: PG4/$\overline{BREQO}$ When EXPE = 0: PG4	NC

Pin No.	Pin Name						Flash Memory Programmer Mode
	Mode 1	Mode 2	Mode 4	Mode 5	Mode 6	Mode 7	
114	PG5/$\overline{\text{BACK}}$	PG5/$\overline{\text{BACK}}$	PG5/$\overline{\text{BACK}}$	PG5/$\overline{\text{BACK}}$	PG5/$\overline{\text{BACK}}$	When EXPE = 1: PG5/$\overline{\text{BACK}}$ When EXPE = 0: PG5	NC
115	PG6/$\overline{\text{BREQ}}$	PG6/$\overline{\text{BREQ}}$	PG6/$\overline{\text{BREQ}}$	PG6/$\overline{\text{BREQ}}$	PG6/$\overline{\text{BREQ}}$	When EXPE = 1: PG6/$\overline{\text{BREQ}}$ When EXPE = 0: PG6	NC
116	VCC	VCC	VCC	VCC	VCC	VCC	VCC
117	P40/AN0	P40/AN0	P40/AN0	P40/AN0	P40/AN0	P40/AN0	NC
118	P41/AN1	P41/AN1	P41/AN1	P41/AN1	P41/AN1	P41/AN1	NC
119	P42/AN2	P42/AN2	P42/AN2	P42/AN2	P42/AN2	P42/AN2	NC
120	P43/AN3	P43/AN3	P43/AN3	P43/AN3	P43/AN3	P43/AN3	NC
121	Vref	Vref	Vref	Vref	Vref	Vref	NC
122	AVCC	AVCC	AVCC	AVCC	AVCC	AVCC	VCC
123	P44/AN4	P44/AN4	P44/AN4	P44/AN4	P44/AN4	P44/AN4	NC
124	P45/AN5	P45/AN5	P45/AN5	P45/AN5	P45/AN5	P45/AN5	NC
125	P46/ AN6/DA0	P46/ AN6/DA0	P46/ AN6/DA0	P46/ AN6/DA0	P46/AN6/DA0	P46/AN6/DA0	NC
126	P47/AN7/ DA1	P47/AN7/ DA1	P47/AN7/ DA1	P47/AN7/ DA1	P47/AN7/DA1	P47/AN7/DA1	NC
127	P54/AN12/ $\overline{\text{IRQ4}}$	P54/AN12/ $\overline{\text{IRQ4}}$	P54/AN12/ $\overline{\text{IRQ4}}$	P54/AN12/ $\overline{\text{IRQ4}}$	P54/AN12/ $\overline{\text{IRQ4}}$	P54/AN12/ $\overline{\text{IRQ4}}$	NC
128	P55/AN13/ $\overline{\text{IRQ5}}$	P55/AN13/ $\overline{\text{IRQ5}}$	P55/AN13/ $\overline{\text{IRQ5}}$	P55/AN13/ $\overline{\text{IRQ5}}$	P55/AN13/ $\overline{\text{IRQ5}}$	P55/AN13/ $\overline{\text{IRQ5}}$	NC
129	P56/AN14/ DA2/$\overline{\text{IRQ6}}$	P56/AN14/ DA2/$\overline{\text{IRQ6}}$	P56/AN14/ DA2/$\overline{\text{IRQ6}}$	P56/AN14/ DA2/$\overline{\text{IRQ6}}$	P56/AN14/ DA2/$\overline{\text{IRQ6}}$	P56/AN14/ DA2/$\overline{\text{IRQ6}}$	NC
130	P57/AN15/ DA3/$\overline{\text{IRQ7}}$	P57/AN15/ DA3/$\overline{\text{IRQ7}}$	P57/AN15/ DA3/$\overline{\text{IRQ7}}$	P57/AN15/ DA3/$\overline{\text{IRQ7}}$	P57/AN15/ DA3/$\overline{\text{IRQ7}}$	P57/AN15/ DA3/$\overline{\text{IRQ7}}$	NC
131	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	VSS
132	NC	NC	NC	NC	NC	NC	NC
133	P35/SCK1/ ($\overline{\text{OE}}$)	P35/SCK1/ ($\overline{\text{OE}}$)	P35/SCK1/ ($\overline{\text{OE}}$)	P35/SCK1/ ($\overline{\text{OE}}$)	P35/SCK1/ ($\overline{\text{OE}}$)	When EXPE = 1: P35/SCK1/($\overline{\text{OE}}$) When EXPE = 0: P35/SCK1	NC
134	P34/SCK0	P34/SCK0	P34/SCK0	P34/SCK0	P34/SCK0	P34/SCK0	NC
135	P33/RxD1	P33/RxD1	P33/RxD1	P33/RxD1	P33/RxD1	P33/RxD1	NC
136	VSS	VSS	VSS	VSS	VSS	VSS	VSS

Pin No.	Pin Name						Flash Memory Programmer Mode
	Mode 1	Mode 2	Mode 4	Mode 5	Mode 6	Mode 7	
137	P32/RxD0/ IrRxD	P32/RxD0/ IrRxD	P32/RxD0/ IrRxD	P32/RxD0/ IrRxD	P32/RxD0/ IrRxD	P32/RxD0/ IrRxD	VCC
138	P31/TxD1	P31/TxD1	P31/TxD1	P31/TxD1	P31/TxD1	P31/TxD1	NC
139	P30/TxD0/ IrTxD	P30/TxD0/ IrTxD	P30/TxD0/ IrTxD	P30/TxD0/ IrTxD	P30/TxD0/ IrTxD	P30/TxD0/ IrTxD	NC
140	P80/ $\overline{\text{EDREQ2}}$/ ($\overline{\text{IRQ0}}$)	P80/ $\overline{\text{EDREQ2}}$/ ($\overline{\text{IRQ0}}$)	P80/ $\overline{\text{EDREQ2}}$/ ($\overline{\text{IRQ0}}$)	P80/ $\overline{\text{EDREQ2}}$/ ($\overline{\text{IRQ0}}$)	P80/ $\overline{\text{EDREQ2}}$/ ($\overline{\text{IRQ0}}$)	When EXPE = 1: P80/$\overline{\text{EDREQ2}}$/ ($\overline{\text{IRQ0}}$) When EXPE = 0: P80/($\overline{\text{IRQ0}}$)	NC
141	P81/ $\overline{\text{EDREQ3}}$/ ($\overline{\text{IRQ1}}$)	P81/ $\overline{\text{EDREQ3}}$/ ($\overline{\text{IRQ1}}$)	P81/ $\overline{\text{EDREQ3}}$/ ($\overline{\text{IRQ1}}$)	P81/ $\overline{\text{EDREQ3}}$/ ($\overline{\text{IRQ1}}$)	P81/ $\overline{\text{EDREQ3}}$/ ($\overline{\text{IRQ1}}$)	When EXPE = 1: P81/$\overline{\text{EDREQ3}}$/ ($\overline{\text{IRQ1}}$) When EXPE = 0: P81/($\overline{\text{IRQ1}}$)	NC
142	P82/ $\overline{\text{ETEND2}}$/ ($\overline{\text{IRQ2}}$)	P82/ $\overline{\text{ETEND2}}$/ ($\overline{\text{IRQ2}}$)	P82/ $\overline{\text{ETEND2}}$/ ($\overline{\text{IRQ2}}$)	P82/ $\overline{\text{ETEND2}}$/ ($\overline{\text{IRQ2}}$)	P82/ $\overline{\text{ETEND2}}$/ ($\overline{\text{IRQ2}}$)	When EXPE = 1: P82/$\overline{\text{ETEND2}}$/ ($\overline{\text{IRQ2}}$) When EXPE = 0: P82/($\overline{\text{IRQ2}}$)	NC
143	MD0	MD0	MD0	MD0	MD0	MD0	VSS
144	MD1	MD1	MD1	MD1	MD1	MD1	VSS

Note: * F-ZTAT version only. In other versions, this is an NC pin.

1.5 Pin Functions

Table 1.3 Pin Functions

Type	Symbol	Pin No. FP-144	I/O	Name and Function
Power	VCC	5, 39, 67, 96, 116	Input	**Power:** For connection to the power supply. All V_{CC} pins should be connected to the system power supply.
	VSS	12, 19, 26, 47, 76, 99, 136	Input	**Ground:** For connection to the power supply. All V_{SS} pins should be connected to the system power supply (0 V).
	PLLVCC	94	Input	**PLL power:** The on-chip PLL oscillator power supply.
	PLLVSS	92	Input	**PLL ground:** The on-chip PLL oscillator ground.
Clock	XTAL	98	Input	For connection to a crystal oscillator. See section 19, Clock Pulse Generator, in the H8S/2678 Series Hardware Manual for typical connection diagrams for a crystal oscillator and external clock input.
	EXTAL	97	Input	For connection to a crystal oscillator. The EXTAL pin can also input an external clock. See section 19, Clock Pulse Generator, in the H8S/2678 Series Hardware Manual for typical connection diagrams for a crystal oscillator and external clock input.
	ø	95	Output	**System clock:** Supplies the system clock to external devices.

Type	Symbol	Pin No. FP-144	I/O	Name and Function
Operating mode control	MD2 to MD0	1, 144, 143	Input	**Mode pins:** These pins set the operating mode. The relation between the settings of pins MD2 to MD0 and the operating mode is shown below. These pins should not be changed while the MCU is operating.

MD0	MD1	MD0	Operating Mode
0	0	0	—
		1	Mode 1
	1	0	Mode 2
		1	—
1	0	0	Mode 4
		1	Mode 5
	1	0	Mode 6
		1	Mode 7

System control	$\overline{\text{RES}}$	93	Input	**Reset input:** When this pin is driven low, the chip is reset.
	$\overline{\text{STBY}}$	100	Input	**Standby:** When this pin is driven low, a transition is made to hardware standby mode.
	$\overline{\text{BREQ}}$	115	Input	**Bus request:** Requests chip to release the bus to an external bus master.
	$\overline{\text{BREQO}}$	113	Output	**Bus request output:** External bus request signal used when an internal bus master accesses external space when the external bus is released.
	$\overline{\text{BACK}}$	114	Output	**Bus request acknowledge:** Indicates that the bus has been released to an external bus master.
	FWE*	62	Input	**Flash write enable:** Enables/disables flash memory.

Type	Symbol	Pin No. FP-144	I/O	Name and Function
Interrupt signals	NMI	38	Input	**Nonmaskable interrupt:** Requests a nonmaskable interrupt. Fix high when not used.
	$\overline{IRQ15}$ to $\overline{IRQ0}$ ($\overline{IRQ15}$) to ($\overline{IRQ0}$)	87, 86, 84 to 81, 61, 60, 130 to 127, 110 to 107, 59 to 52, 112, 111, 4 to 2, 142 to 140	Input	**Interrupt request 15 to 0:** These pins request a maskable interrupt.
Address bus	A23 to A0	32 to 27, 25 to 20, 18 to 13, 11 to 6	Output	**Address bus:** These pins output an address.
Data bus	D15 to D0	72 to 75, 77 to 80, 63 to 66, 68 to 71	Input/ output	**Data bus:** These pins constitute a bidirectional data bus.
Bus control	$\overline{CS7}$ to $\overline{CS0}$	112, 111, 106 to 101	Output	**Chip select:** Signals that select areas 7 to 0.
	$\overline{AS}$	91	Output	**Address strobe:** When this pin is low, it indicates that address output on the address bus is valid.
	$\overline{RD}$	90	Output	**Read:** When this pin is low, it indicates that the external address space is being read.
	$\overline{HWR}$	89	Output	**High write/write enable:** Strobe signal indicating that external space is to be written, and the upper half (D15 to D8) of the data bus is enabled. Write enable signal for DRAM interface space.
	$\overline{LWR}$	88	Output	**Low write:** Strobe signal indicating that external space is to be written, and the lower half (D7 to D0) of the data bus is enabled.

Type	Symbol	Pin No. FP-144	I/O	Name and Function
Bus control	$\overline{\text{UCAS}}$	86	Output	**Upper column address strobe:** Upper column address strobe signal for 16-bit DRAM interface space. Column address strobe signal for 8-bit DRAM interface space.
	$\overline{\text{LCAS}}$	87	Output	**Lower column address strobe:** Lower column address strobe signal for 16-bit DRAM interface space.
	$\overline{\text{WAIT}}$	85	Input	**Wait:** Requests insertion of a wait state in the bus cycle when accessing external 3-state address space.
	$\overline{\text{OE}}$ ($\overline{\text{OE}}$)	112 133	Output	**Output enable:** Output enable signal for DRAM interface space.
DMA controller (DMAC)	DREQ1, DREQ0, (DREQ1), (DREQ0)	61 60 35 34	Input	**DMA transfer request 1, 0:** These signals request DMAC activation.
	TEND1, TEND0, (TEND1), (TEND0)	82 81 40 36	Output	**DMA transfer end 1, 0:** These signals indicate the end of DMAC data transfer.
	DACK1, DACK0, (DACK1), (DACK0),	84 83 42 41	Output	**DMA transfer acknowledge 1, 0:** DMAC single address transfer acknowledge signals.
EXDMA controller (EXDMAC)	$\overline{\text{EDREQ3}}$ to $\overline{\text{EDREQ0}}$	141, 140, 35, 34	Input	**EXDMA transfer request 3 to 0:** These signals request EXDMAC activation.
	$\overline{\text{ETEND3}}$ to $\overline{\text{ETEND0}}$	2, 142, 40, 36	Output	**EXDMA transfer end 3 to 0:** These signals indicate the end of EXDMAC data transfer.
	$\overline{\text{EDACK3}}$ to $\overline{\text{EDACK0}}$	4, 3, 42, 41	Output	**EXDMA transfer acknowledge 3 to 0:** EXDMAC single address transfer acknowledge signals.
	$\overline{\text{EDRAK3}}$ to $\overline{\text{EDRAK0}}$	51, 50, 59, 58	Output	**$\overline{\text{EDREQ}}$ acknowledge 3 to 0:** These signals notify an external device of acceptance and start of execution of an external request.

Type	Symbol	Pin No. FP-144	I/O	Name and Function
16-bit timer pulse unit (TPU)	TCLKD to TCLKA	51, 49, 46, 45	Input	**Clock input D to A:** External clock input pins.
	TIOCA0, TIOCB0, TIOCC0, TIOCD0	43 to 46	Input/ output	**Input capture/output compare match A0 to D0:** TGR0A to TGR0D input capture input/output compare output/PWM output pins.
	TIOCA1, TIOCB1	48, 49	Input/ output	**Input capture/output compare match A1, B1:** TGR1A and TGR1B input capture input/output compare output/PWM output pins.
	TIOCA2, TIOCB2	50, 51	Input/ output	**Input capture/output compare match A2, B2:** TGR2A and TGR2B input capture input/output compare output/PWM output pins.
	TIOCA3, TIOCB3, TIOCC3, TIOCD3	52 to 55	Input/ output	**Input capture/output compare match A3 to D3:** TGR3A to TGR3D input capture input/output compare output/PWM output pins.
	TIOCA4, TIOCB4	56, 57	Input/ output	**Input capture/output compare match A4, B4:** TGR4A and TGR4B input capture input/output compare output/PWM output pins.
	TIOCA5, TIOCB5	58, 59	Input/ output	**Input capture/output compare match A5, B5:** TGR5A and TGR5B input capture input/output compare output/PWM output pins.
Programmable pulse generator (PPG)	PO15 to PO0	51 to 48, 46 to 43, 59 to 52	Output	**Pulse output 15 to 0:** Pulse output pins.
8-bit timer	TMO0, TMO1	83, 84	Output	**Compare match output:** Compare match output pins.
	TMCI0, TMCI1	81, 82	Input	**Counter external clock input:** Input pins for the external clock input to the counter.
	TMRI0, TMRI1	60, 61	Input	**Counter external reset input:** Counter reset input pins.

Type	Symbol	Pin No. FP-144	I/O	Name and Function
Watchdog timer (WDT)	$\overline{\text{WDTOVF}}$	37	Output	**Watchdog timer overflow:** Counter overflow signal output pin in watchdog timer mode.
Serial communication interface (SCI)/smart card interface (SCI0 with IrDA function)	TxD2, TxD1, TxD0/IrTxD	107, 138, 139	Output	**Transmit data (channels 0, 1, 2):** Data output pins.
	RxD2, RxD1, RxD0/IrRxD	108, 135, 137	Input	**Receive data (channels 0, 1, 2):** Data input pins.
	SCK2, SCK1, SCK0	109, 133, 134	Input/ output	**Serial clock (channels 0, 1, 2):** Clock input/output pins.
A/D converter	AN15 to AN12, AN7 to AN0	130 to 127, 126 to 123, 120 to 117	Input	**Analog 15 to 12, 7 to 0:** Analog input pins.
	$\overline{\text{ADTRG}}$	110	Input	**A/D conversion external trigger input:** Pin for input of an external trigger to start A/D conversion.
D/A converter	DA3, DA2, DA1, DA0	130, 129, 126, 125	Output	**Analog output:** D/A converter analog output pins.
A/D converter, D/A converter	AVCC	122	Input	The power supply pin for the A/D converter and D/A converter. When the A/D converter and D/A converter are not used, this pin should be connected to the system power supply (+3 V).
	AVSS	131	Input	The ground pin for the A/D converter and D/A converter. This pin should be connected to the system power supply (0 V).
	Vref	121	Input	The reference voltage input pin for the A/D converter and D/A converter. When the A/D converter and D/A converter are not used, this pin should be connected to the system power supply (+3 V).

Type	Symbol	Pin No. FP-144	I/O	Name and Function
I/O ports	P17 to P10	51 to 48, 46 to 43	Input/ output	**Port 1:** Eight input/output pins. The direction of each pin can be selected in the port 1 data direction register (P1DDR).
	P27 to P20	59 to 52	Input/ output	**Port 2:** Eight input/output pins. The direction of each pin can be selected in the port 2 data direction register (P2DDR).
	P35 to P30	133 to 135, 137 to 139	Input/ output	**Port 3:** Six input/output pins. The direction of each pin can be selected in the port 3 data direction register (P3DDR).
	P47 to P40	126 to 123, 120 to 117	Input	**Port 4:** Eight input pins.
	P57 to P50	130 to 127, 110 to 107	Input Input/ output	**Port 5:** Four input pins and four input/output pins. The direction of each input/output pin can be selected in the port 5 data direction register (P5DDR).
	P65 to P60	84 to 81, 61, 60	Input/ output	**Port 6:** Six input/output pins. The direction of each pin can be selected in the port 6 data direction register (P6DDR).
	P75 to P70	42 to 40, 36 to 34	Input/ output	**Port 7:** Six input/output pins. The direction of each pin can be selected in the port 7 data direction register (P7DDR).
	P85 to P80	4 to 2, 142 to 140	Input/ output	**Port 8:** Six input/output pins. The direction of each pin can be selected in the port 8 data direction register (P8DDR).
	PA7 to PA0	32 to 27, 25, 24	Input/ output	**Port A:** Eight input/output pins. The direction of each pin can be selected in the port A data direction register (PADDR).
	PB7 to PB0	23 to 20, 18 to 15	Input/ output	**Port B:** Eight input/output pins. The direction of each pin can be selected in the port B data direction register (PBDDR).

Type	Symbol	Pin No. FP-144	I/O	Name and Function
I/O ports	PC7 to PC0	14, 13, 11 to 6	Input/ output	**Port C:** Eight input/output pins. The direction of each pin can be selected in the port C data direction register (PCDDR).
	PD7 to PD0	72 to 75, 77 to 80	Input/ output	**Port D:** Eight input/output pins. The direction of each pin can be selected in the port D data direction register (PDDDR).
	PE7 to PE0	63 to 66, 68 to 71	Input/ output	**Port E:** Eight input/output pins. The direction of each pin can be selected in the port E data direction register (PEDDR).
	PF7 to PF0	95, 91 to 85	Input/ output	**Port F:** Eight input/output pins. The direction of each pin can be selected in the port F data direction register (PFDDR).
	PG6 to PG0	115 to 113, 104 to 101	Input/ output	**Port G:** Seven input/output pins. The direction of each pin can be selected in the port G data direction register (PGDDR).
	PH3 to PH0	112, 111, 106, 105	Input/ output	**Port H:** Four input/output pins. The direction of each pin can be selected in the port H data direction register (PHDDR).

Note: * F-ZTAT version only. In other versions, this is an NC pin.

1.6 Product Lineup

Table 1.4 H8S/2678 Series Product Lineup

Product Type		Model	Marking	Package (Hitachi Package Code)
H8S/2677*[2]	F-ZTAT™ version	HD64F2677	HD64F2677VFC	144-pin plastic QFP (FP-144)
H8S/2676*[1]	F-ZTAT™ version	HD64F2676	HD64F2676VFC	144-pin plastic QFP (FP-144)
	Mask ROM version	HD6432676	HD6432676FC	
H8S/2675*[2]	Mask ROM version	HD6432675	HD6432675FC	144-pin plastic QFP (FP-144)
H8S/2673*[1]	Mask ROM version	HD6432673	HD6432673FC	144-pin plastic QFP (FP-144)
H8S/2670*[1]	ROMless version	HD6412670	HD6412670VFC	144-pin plastic QFP (FP-144)

Notes: 1. Under development
2. In planning stage

1.7 Package Dimensions

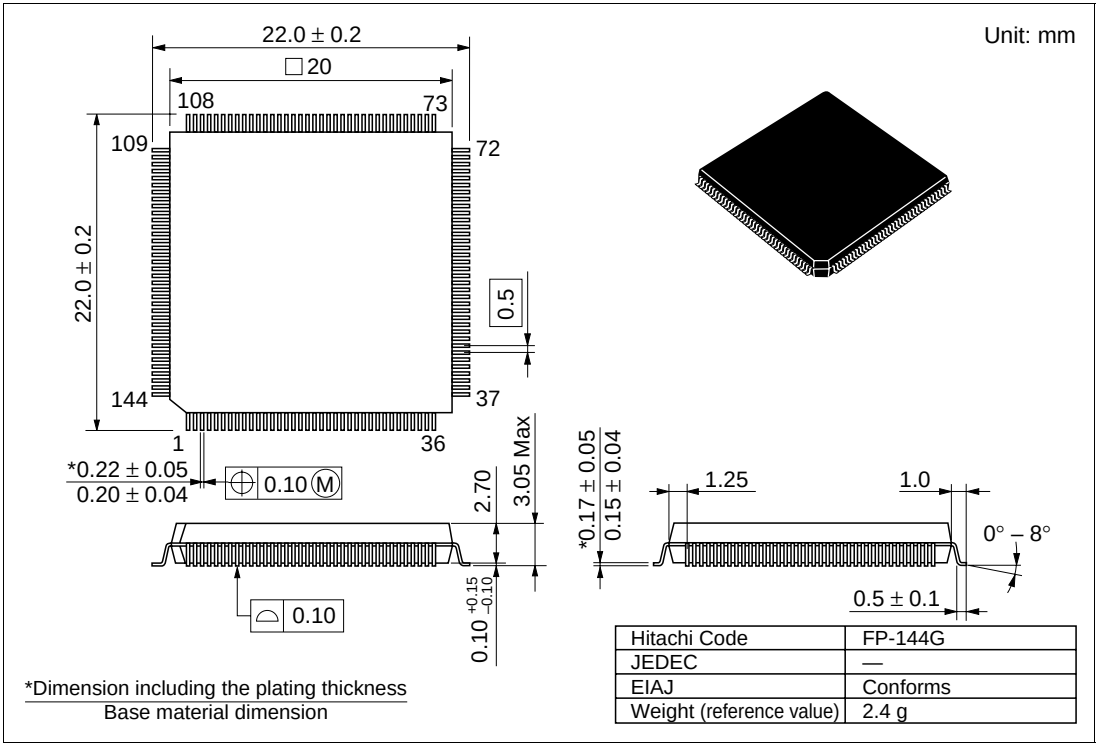


Figure 1.3 FP-144 Package Dimensions

Section 2 MCU Operating Modes

2.1 Overview

2.1.1 Operating Mode Selection (F-ZTAT Version)

The H8S/2678 Series F-ZTAT version has twelve operating modes (modes 1, 2, 4 to 7, and 10 to 15) that are selected by the flash write enable pin (FWE) and the mode pins (MD2 to MD0). The input at these pins determines the CPU operating mode and the initial bus width, as shown in table 2.1.

Table 2.1 lists the MCU operating modes.

Table 2.1 MCU Operating Mode Selection (F-ZTAT Version)

MCU Operating Mode	FWE	MD2	MD1	MD0	CPU Operating Mode	Description	On-Chip ROM	External Data Bus	
								Initial Width	Max. Width
0	0	0	0	0	—	—	—	—	—
1				1	Advanced	Expanded mode with on-chip ROM disabled	Disabled	16 bits	16 bits
2			1	0				8 bits	16 bits
3				1		—	—	—	—
4		1	0	0		Expanded mode with on-chip ROM enabled	Enabled	8 bits	16 bits
5				1		External ROM activation expanded mode with on-chip ROM enabled	Enabled	16 bits	16 bits
6			1	0				8 bits	16 bits
7				1		Single-chip activation mode with on-chip ROM enabled	Enabled	—	16 bits
8	1	0	0	0	—	—	—	—	—
9				1					
10			1	0	Advanced	Boot mode	Enabled	8 bits	16 bits
11				1				—	—
12		1	0	0	Advanced	User program mode	Enabled	8 bits	16 bits
13				1				16 bits	16 bits
14			1	0	Advanced	User program mode	Enabled	8 bits	16 bits
15				1				—	16 bits

The CPU's architecture allows for 4 gigabytes of address space, but the H8S/2678 Series chip actually accesses a maximum of 16 Mbytes.

Modes 1, 2, and 4 to 6 are externally expanded modes that allow access to external memory and peripheral devices.

The externally expanded modes allow switching between 8-bit and 16-bit bus modes. After program execution starts, an 8-bit or 16-bit address space can be set for each area, depending on the bus controller setting. If 16-bit access is selected for any one area, 16-bit bus mode is set; if 8-bit access is selected for all areas, 8-bit bus mode is set. Pin functions depend on the operating mode.

Mode 7 is a single-chip activation externally expanded mode that allows access to external memory and peripheral devices to be switched at the start of program execution.

In the single-chip activation externally expanded mode, it is possible to switch between externally expanded mode and single-chip mode by means of the EXPE bit in the system control register (SYSCR). Immediately after a reset, the chip starts up in single-chip mode, but after the start of program execution, it is possible to change to externally expanded mode by setting EXPE accordingly. Pin functions depend on the operating mode.

Modes 10 to 15 are boot modes and user program modes that allow programming and erasing of flash memory. For details see section 18, ROM, in the H8S/2678 Series Hardware Manual.

The H8S/2678 Series F-ZTAT Version can be used only in modes 1, 2, 4 to 7, and 10 to 15. This means that the flash write enable pin and mode pins must be set to select one of these modes.

Do not change the inputs at the mode pins during operation.

2.1.2 Operating Mode Selection (ROMless and Mask ROM Versions)

The H8S/2678 Series ROMless and mask ROM versions have six operating modes* (modes 1, 2, and 4 to 7) that are selected by the mode pins (MD2 to MD0). The input at these pins determines the CPU operating mode, enabling or disabling of on-chip ROM, and the initial bus width, as shown in table 2.2.

Table 2.2 lists the MCU operating modes.

Table 2.2 MCU Operating Mode Selection* (ROMless and Mask ROM Versions)

MCU Operating Mode	MD2	MD1	MD0	CPU Operating Mode	Description	On-Chip ROM	External Data Bus	
							Initial Width	Max. Width
0	0	0	0	—	—	—	—	—
1			1	Advanced	Expanded mode with on-chip ROM disabled	Disabled	16 bits	16 bits
2		1	0				8 bits	16 bits
3			1	—	—	—	—	—
4	1	0	0	Advanced	Expanded mode with on-chip ROM enabled	Enabled	8 bits	16 bits
5			1		External ROM activation expanded mode with on-chip ROM enabled		16 bits	16 bits
6		1	0				8 bits	16 bits
7			1		Single-chip activation mode with on-chip ROM enabled		—	16 bits

Note: * Only modes 1 and 2 are available in the ROMless version.

The CPU's architecture allows for 4 gigabytes of address space, but the H8S/2678 Series chip actually accesses a maximum of 16 Mbytes.

Modes 1, 2, and 4 to 6 are externally expanded modes that allow access to external memory and peripheral devices.

The externally expanded modes allow switching between 8-bit and 16-bit bus modes. After program execution starts, an 8-bit or 16-bit address space can be set for each area, depending on the bus controller setting. If 16-bit access is selected for any one area, 16-bit bus mode is set; if 8-bit access is selected for all areas, 8-bit bus mode is set. Pin functions depend on the operating mode.

In the single-chip activation externally expanded mode, it is possible to switch between externally expanded mode and single-chip mode. Immediately after a reset, the chip starts up in single-chip mode, but after the start of program execution, it is possible to change to externally expanded mode by setting the EXPE bit in the system control register (SYSCR) accordingly. Pin functions depend on the operating mode.

The H8S/2678 Series mask ROM version can be used only in modes 1, 2, and 4 to 7, and the ROMless version only in modes 1 and 2. This means that the mode pins must be set to select one of these modes.

Do not change the inputs at the mode pins during operation.

2.1.3 Register Configuration

The H8S/2678 Series has a mode control register (MDCR) that indicates the inputs at the mode pins (MD2 to MD0), and a system control register (SYSCR) that controls the operation of the chip. Table 2.3 summarizes these registers.

Table 2.3 Registers

Name	Abbreviation	R/W	Initial Value	Address*[1]
Mode control register	MDCR	R	Undefined	H'FF3E
System control register	SYSCR	R/W	H'C1/H'C3*[2]	H'FF3D

Notes: 1. Lower 16 bits of the address.
2. Determined by pins MD2 to MD0.

2.2 Register Descriptions

2.2.1 Mode Control Register (MDCR)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	MDS2	MDS1	MDS0
Initial value	0	0	0	0	0	—*	—*	—*
Read/Write	—	—	—	—	—	R	R	R

Note: * Determined by pins MD2 to MD0.

MDCR is an 8-bit read-only register that monitors the current operating mode of the H8S/2678 Series chip.

Bits 7 to 3—Reserved: These bits are always read as 0 and cannot be modified. The write value should always be 1.

Bits 2 to 0—Mode Select 2 to 0 (MD2 to MD0): These bits indicate the input levels at pins MD2 to MD0 (the current operating mode). Bits MDS2 to MDS0 correspond to pins MD2 to MD0. MDS2 to MDS0 are read-only bits—they cannot be written to. The mode pin (MD2 to MD0) input levels are latched into these bits when MDCR is read. These latches are canceled by a reset.

2.2.2 System Control Register (SYSCR)

Bit	7	6	5	4	3	2	1	0
	—	—	MACS	—	FLSHE	—	EXPE	RAME
Initial value	1	1	0	0	0	0	—*	1
Read/Write	R/W	R/W	R/W	R/W	R/W	—	R/W	R/W

Note: * Determined by pins MD2 to MD0.

Bits 7 and 6—Reserved: These are readable/writable bits, but the write value should always be 1.

Bit 5—MAC Saturation (MACS): Selects either saturating or non-saturating calculation for the MAC instruction.

Bit 5 MACS	Description	
0	Non-saturating calculation for MAC instruction	(Initial value)
1	Saturating calculation for MAC instruction	

Bit 4—Reserved: This is a readable/writable bit, but the write value should always be 0.

Bit 3—Flash Memory Control Register Enable (FLSHE): Controls CPU access to the flash memory control registers (FLMCR1, FLMCR2, EBR1, and EBR2). For details see section 18, ROM, in the H8S/2678 Series Hardware Manual.

In the mask ROM and ROMless versions, 0 should be written to this bit.

Bit 3 FLSHE	Description	
0	Flash memory control registers are not selected for area H'FFFFC8 to H'FFFFCB	(Initial value)
1	Flash memory control registers are selected for area H'FFFFC8 to H'FFFFCB	

Bit 2—Reserved: This bit is always read as 0 and cannot be modified. The write value should always be 0.

Bit 1—External Bus Mode Enable (EXPE): Sets external bus mode.

In modes 1, 2, 4, 5, 6, 10, 12, 13, and 14, this bit is fixed at 1 and cannot be modified. In modes 7, 11, and 15, this bit has an initial value of 0, and can be read and written.

Writing of 0 to EXPE when its value is 1 should only be carried out when an external bus cycle* is not being executed.

Note: * There are cases where external and internal bus cycles are executed in parallel due to the write data buffer function, the refresh control function, the EXDMAC, the bus-released state, and so forth.

Bit 1 EXPE	Description
0	External bus disabled
1	External bus enabled

Bit 0—RAM Enable (RAME): Enables or disables the on-chip RAM. The RAME bit is initialized when the reset state is released. It is not initialized in software standby mode.

Bit 0 RAME	Description	
0	On-chip RAM disabled	
1	On-chip RAM enabled	(Initial value)

2.3 Operating Mode Descriptions

2.3.1 Mode 1 (Expanded Mode with On-Chip ROM Disabled)

The CPU can access a 16-Mbyte address space in advanced mode. The on-chip ROM is disabled. Ports A, B, and C function as an address bus, ports D and E function as a data bus, and parts of ports F and G carry bus control signals.

The initial bus mode after a reset is 16 bits, with 16-bit access to all areas. However, if 8-bit access is designated for all areas by the bus controller, the bus mode switches to 8 bits.

2.3.2 Mode 2 (Expanded Mode with On-Chip ROM Disabled)

This is an externally expanded mode with on-chip ROM disabled.

Operation is the same as in mode 1, except that the initial external bus mode after a reset is 8 bits.

2.3.3 Mode 3

This mode is not supported in the H8S/2678 Series, and must not be selected.

2.3.4 Mode 4 (Expanded Mode with On-Chip ROM Enabled)

The CPU can access a 16-Mbyte address space in advanced mode. The on-chip ROM is enabled. Ports A, B, and C function as input ports immediately after a reset, but can be set to function as an address bus. For details see section 5, I/O Ports. Port D functions as a data bus, and parts of ports F and G carry bus control signals.

The initial bus mode after a reset is 8 bits, with 8-bit access to all areas. The program in on-chip ROM connected to the first half of area 0 is executed. However, if 16-bit access is designated for any area by the bus controller, the bus mode switches to 16 bits and port E functions as a data bus.

2.3.5 Mode 5 (External ROM Activation Expanded Mode with On-Chip ROM Enabled)

The CPU can access a 16-Mbyte address space in advanced mode. The on-chip ROM*[1] is enabled. Ports A, B, and C function as an address bus, ports D and E function as a data bus, and parts of ports F and G carry bus control signals.

The initial bus mode after a reset is 16 bits, with 16-bit access to all areas. The program in on-chip ROM*[2] connected to the first half of area 0 is executed. However, if 8-bit access is designated for any area by the bus controller, the bus mode switches to 8 bits.

Notes: 1. H8S/2678: H'100000 to H'180000; H8S/2675: H'100000 to H'140000
2. H8S/2678, H8S/2675: H'000000 to H'100000

2.3.6 Mode 6 (External ROM Activation Expanded Mode with On-Chip ROM Enabled)

This is an external ROM activation expanded mode with on-chip ROM disabled.

Operation is the same as in mode 5, except that the initial external bus mode after a reset is 8 bits.

2.3.7 Mode 7 (Single-Chip Activation Mode with On-Chip ROM Enabled)

The CPU can access a 16-Mbyte address space in advanced mode. The on-chip ROM is enabled, and the chip starts up in single-chip mode. External addresses cannot be used in single-chip mode, but they can be made accessible by means of a setting in the system control register (SYSCR).

When external addresses are enabled, settings can be made to designate ports A, B, and C for address output, and ports D and E as data bus. For details see section 5, I/O Ports.

The initial mode after a reset is single-chip mode, with all I/O ports available for use as input/output ports. However, the mode can be switched to externally expanded mode by means of a setting in SYSCR. When externally expanded mode is selected, all areas are initially designated as 16-bit access space. The function of pins in ports A to H is the same as in externally expanded mode with on-chip ROM enabled.

2.3.8 Modes 8 and 9 [F-ZTAT Version Only]

Modes 8 and 9 are not supported in the H8S/2678 Series, and must not be selected.

2.3.9 Mode 10 [F-ZTAT Version Only]

This is a flash memory boot mode. For details see section 18, ROM, in the H8S/2678 Series Hardware Manual.

Except for flash memory erasing and programming, operation is the same as in mode 4 (advanced expanded mode with on-chip ROM enabled).

2.3.10 Mode 11

This is a flash memory boot mode. For details see section 18, ROM, in the H8S/2678 Series Hardware Manual.

Except for flash memory erasing and programming, operation is the same as in mode 7 (advanced single-chip activation expanded mode with on-chip ROM enabled).

2.3.11 Mode 12

This is a flash memory user program mode. For details see section 18, ROM, in the H8S/2678 Series Hardware Manual.

Except for flash memory erasing and programming, operation is the same as in mode 4 (advanced expanded mode with on-chip ROM enabled).

2.3.12 Modes 13 and 14 [F-ZTAT Version Only]

This is a flash memory user program mode. For details see section 18, ROM, in the H8S/2678 Series Hardware Manual.

Except for flash memory erasing and programming, operation is the same as in modes 5 and 6 (advanced external ROM activation expanded mode with on-chip ROM enabled).

2.3.13 Mode 15 [F-ZTAT Version Only]

This is a flash memory user program mode. For details see section 18, ROM, in the H8S/2678 Series Hardware Manual.

Except for flash memory erasing and programming, operation is the same as in mode 7 (advanced single-chip activation expanded mode with on-chip ROM enabled).

2.4 Pin Functions in Each Operating Mode

The pin functions of ports A to H vary depending on the operating mode. Table 2.4 shows their functions in each operating mode.

Table 2.4 Pin Functions in Each Operating Mode

Port		Mode 1	Mode 2	Mode 4	Mode 5	Mode 6	Mode 7	Mode 10	Mode 11	Mode 12	Mode 13	Mode 14	Mode 15
Port A	PA7 to PA5	P*/A	P*/A	P*/A	P*/A	P*/A	P*/A	P*/A	P*/A	P*/A	P*/A	P*/A	P*/A
	PA4 to PA0	A	A		A	A				A		A	
Port B		A	A	P*/A	A	A	P*/A	P*/A	P*/A	P*/A	A	A	P*/A
Port C		A	A	P*/A	A	A	P*/A	P*/A	P*/A	P*/A	A	A	P*/A
Port D		D	D	D	D	D	P*/D	D	P*/D	D	D	D	P*/D
Port E		P/D*	P*/D	P/D*	P/D*	P*/D	P*/D	P*/D	P*/D	P*/D	P/D*	P*/D	P*/D
Port F	PF7, PF6	P/C*	P/C*	P/C*	P/C*	P/C*	P*/C	P*/C	P*/C	P/C*	P/C*	P/C*	P*/C
	PF5, PF4	C	C	C	C	C		C		C	C	C	
	PF3	P/C*	P/C*	P/C*	P/C*	P/C*		P/C*		P/C*	P/C*	P/C*	
	PF2 to PF0	P*/C	P*/C	P*/C	P*/C	P*/C		P*/C		P*/C	P*/C	P*/C	
Port G	PG7 to PG1	P*/C	P*/C	P*/C	P*/C	P*/C	P*/C	P*/C	P*/C	P*/C	P*/C	P*/C	P*/C
	PG0	P/C*	P/C*	P*/C	P/C*	P/C*		P/C*		P*/C	P/C*	P/C*	
Port H		P*/C	P*/C	P*/C	P*/C	P*/C	P*/C	P*/C	P*/C	P*/C	P*/C	P*/C	P*/C

Legend: P: I/O port
A: Address bus output
D: Data bus input/output
C: Control signals, clock input/output

Note: * After reset

2.5 Memory Map in Each Operating Mode

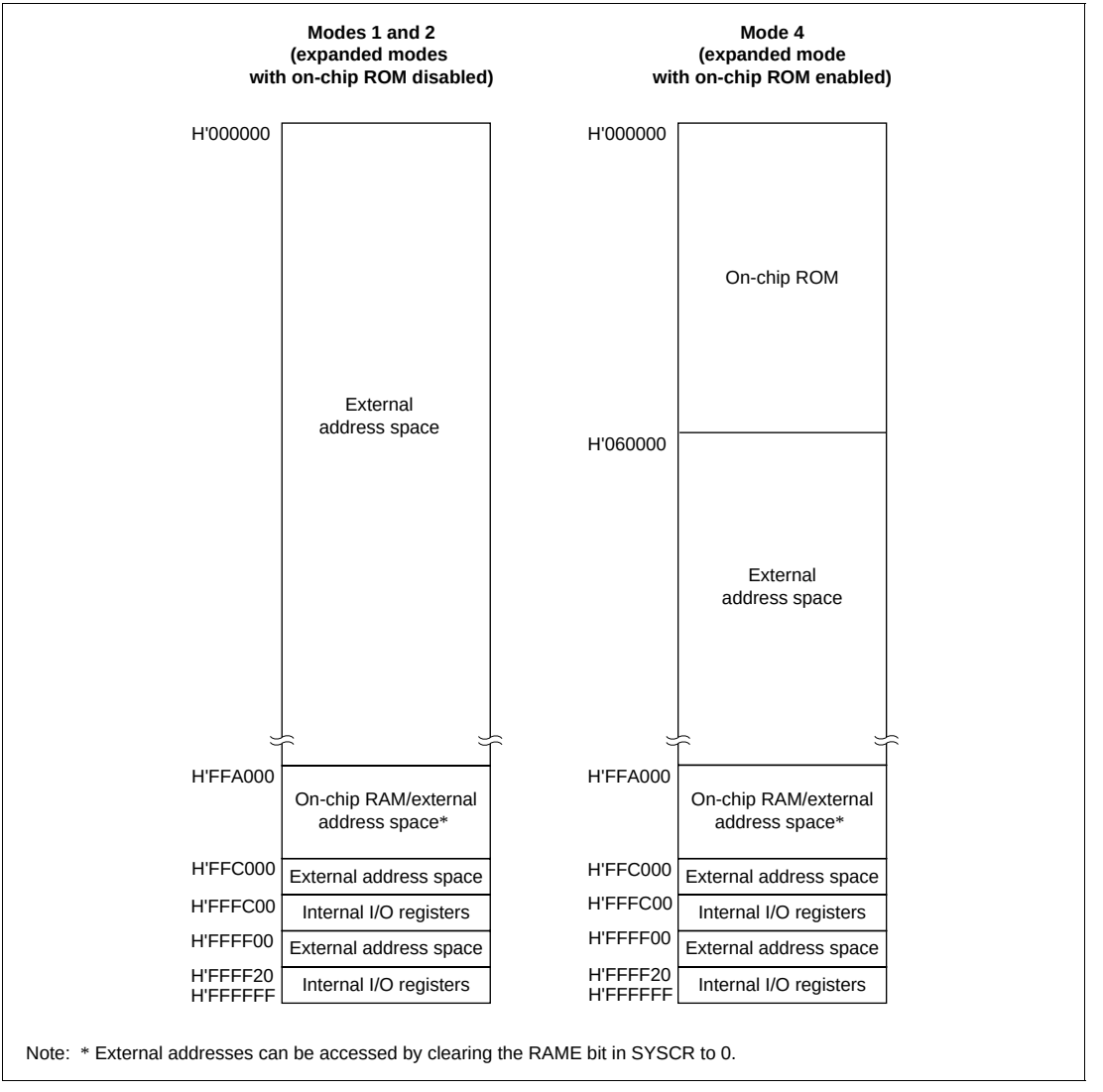
Figures 2.1 to 2.13 show memory maps for each of the operating modes.

The address space is 16 Mbytes.

The on-chip ROM capacity is 384 kbytes in the H8S/2677, 256 kbytes in the H8S/2676, 128 kbytes in the H8S/2675, and 64 kbytes in the H8S/2673; the on-chip RAM capacity is 8 kbytes.

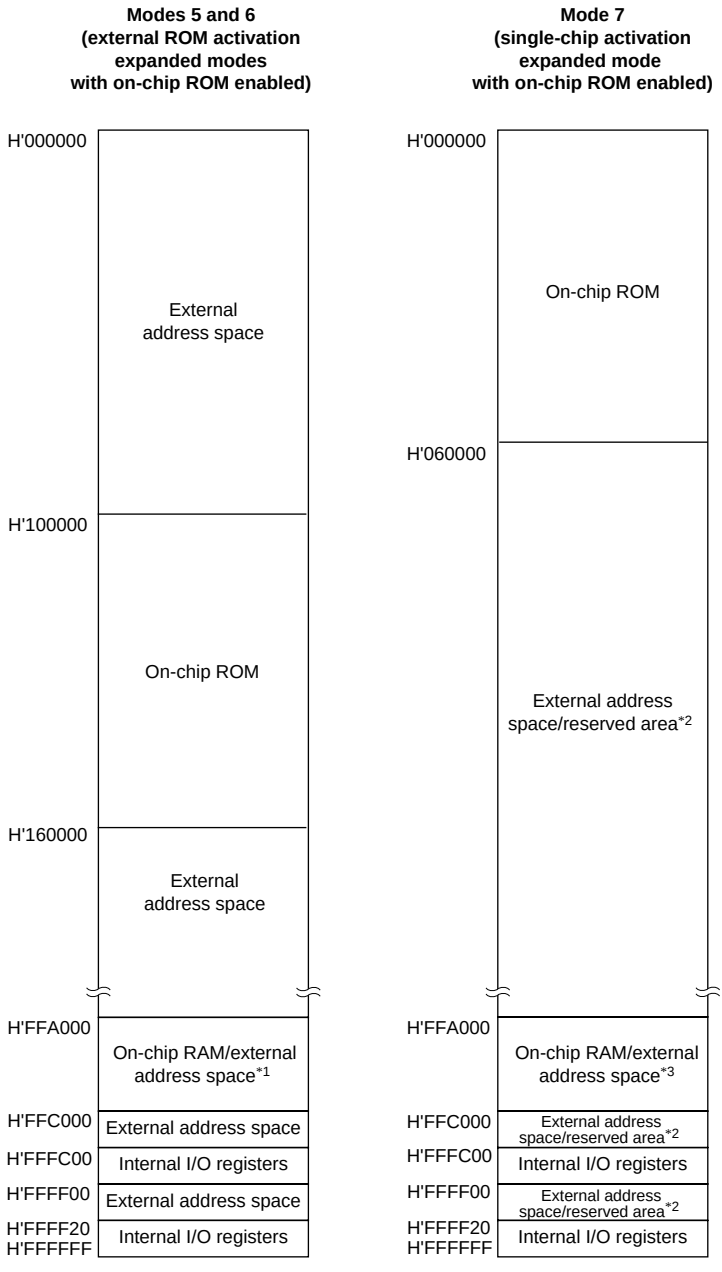
The address space is divided into eight areas. For details see section 4, Bus Controller.

Only advanced mode is supported in the H8S/2678 Series.



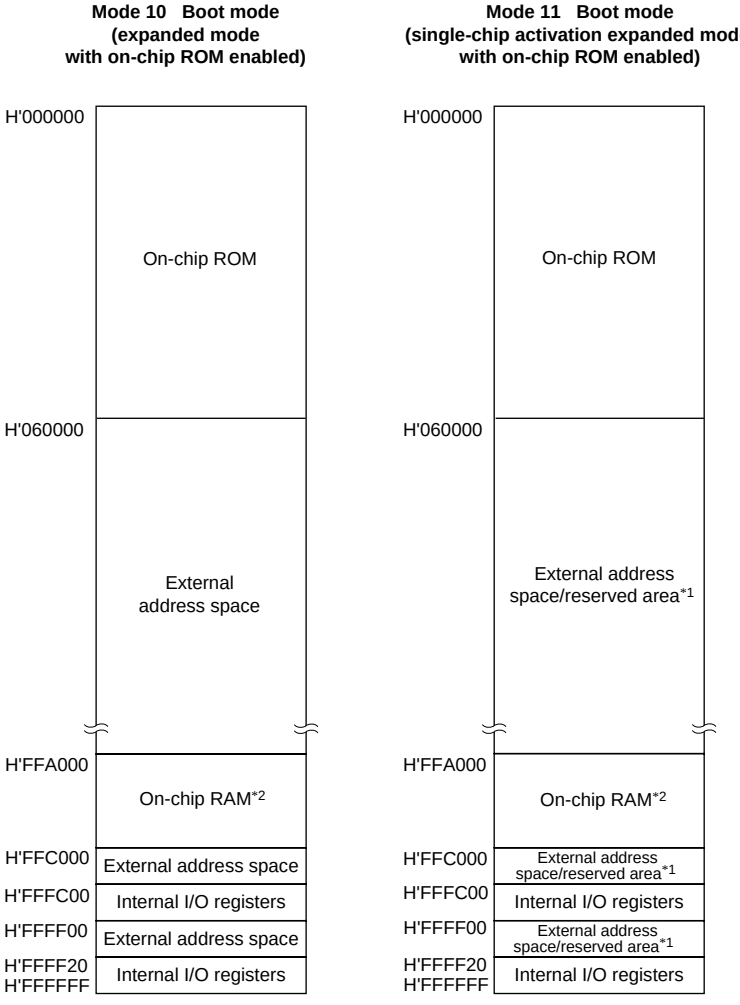
Note: * External addresses can be accessed by clearing the RAME bit in SYSCR to 0.

Figure 2.1 H8S/2677 Memory Map in Each Operating Mode (1)



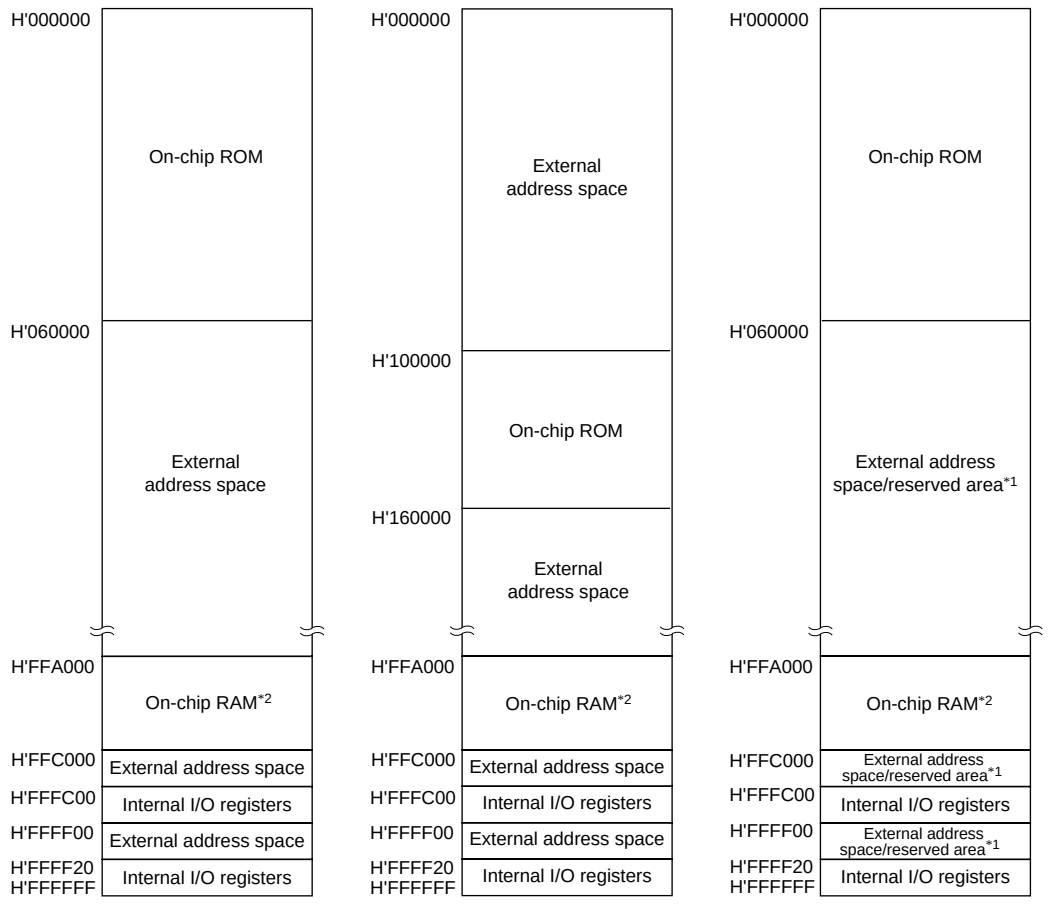
Notes: 1. External addresses can be accessed by clearing the RAME bit in SYSCR to 0.
2. When EXPE = 1, external address space; when EXPE = 0, reserved area.
3. When EXPE = 1, external address space when RAME = 0, on-chip RAM when RAME = 1.
When EXPE = 0, on-chip RAM area.

Figure 2.2 H8S/2677 Memory Map in Each Operating Mode (2)



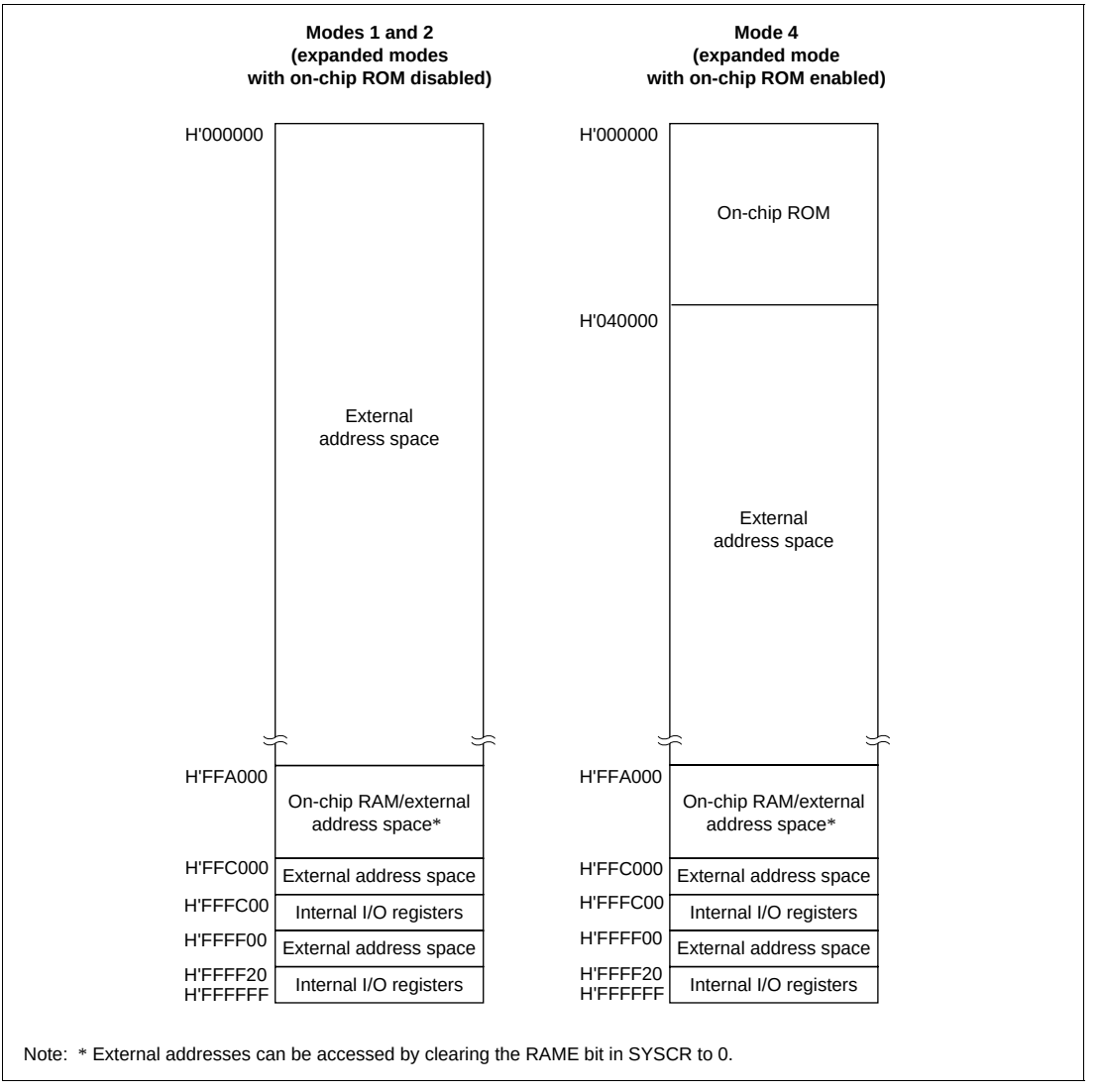
Notes: 1. When EXPE = 1, external address space; when EXPE = 0, reserved area.
2. On-chip RAM is used for flash memory programming. Do not clear the RAME bit in SYSCR to 0.

Figure 2.3 H8S/2677 Memory Map in Each Operating Mode (3)
[F-ZTAT™ Version Only]



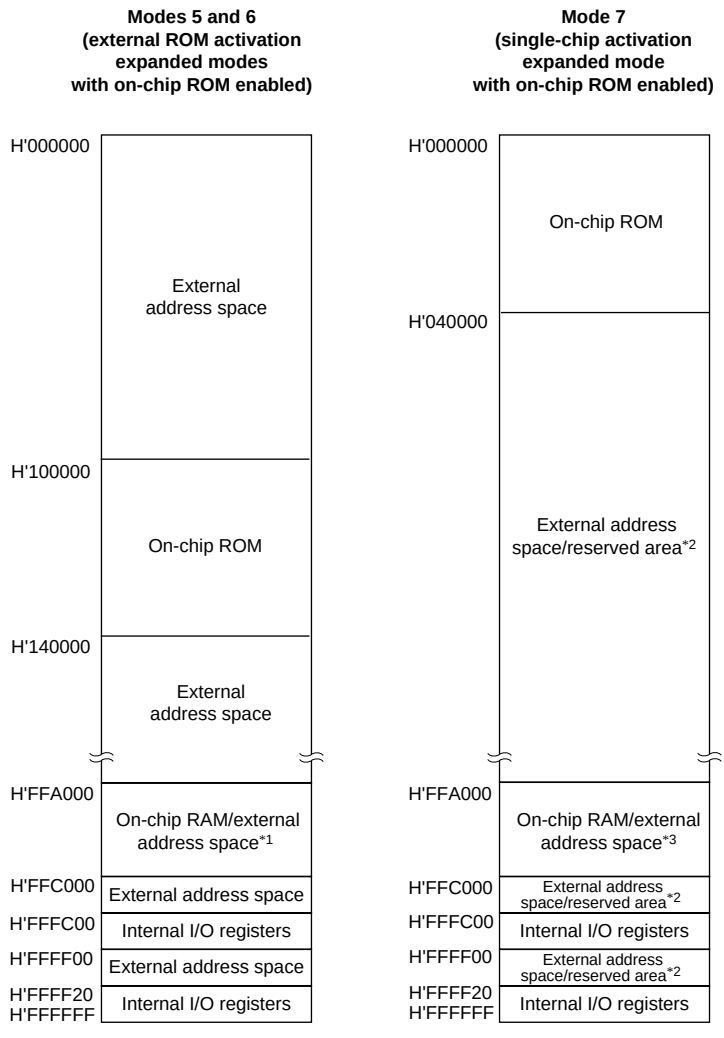
Notes: 1. When EXPE = 1, external address space; when EXPE = 0, reserved area.
2. On-chip RAM is used for flash memory programming. Do not clear the RAME bit in SYSCR to 0.

Figure 2.4 H8S/2677 Memory Map in Each Operating Mode (4)
[F-ZTAT™ Version Only]



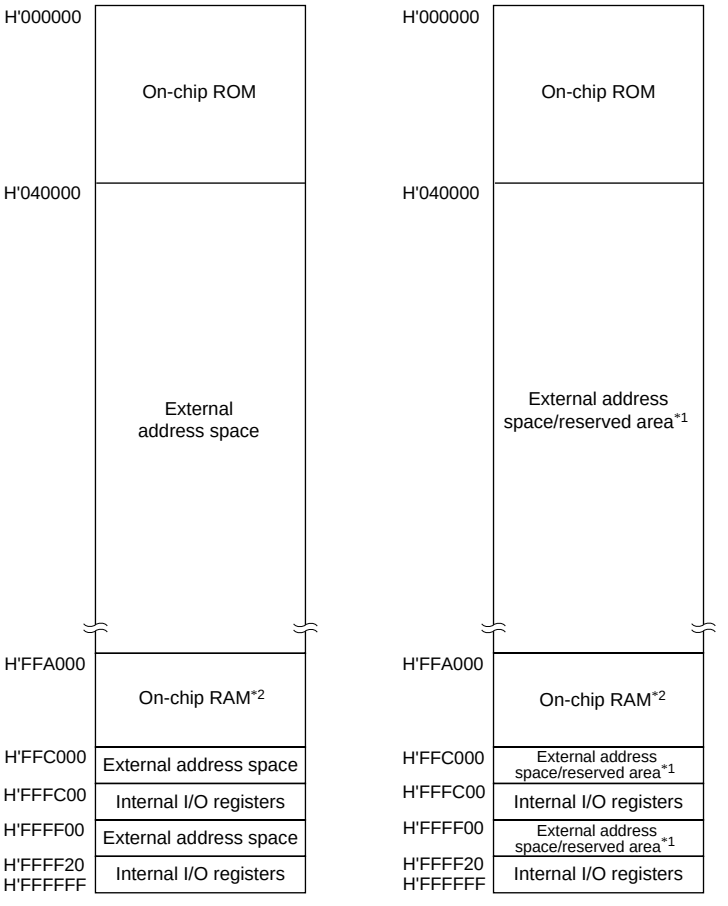
Note: * External addresses can be accessed by clearing the RAME bit in SYSCR to 0.

Figure 2.5 H8S/2676 Memory Map in Each Operating Mode (1)



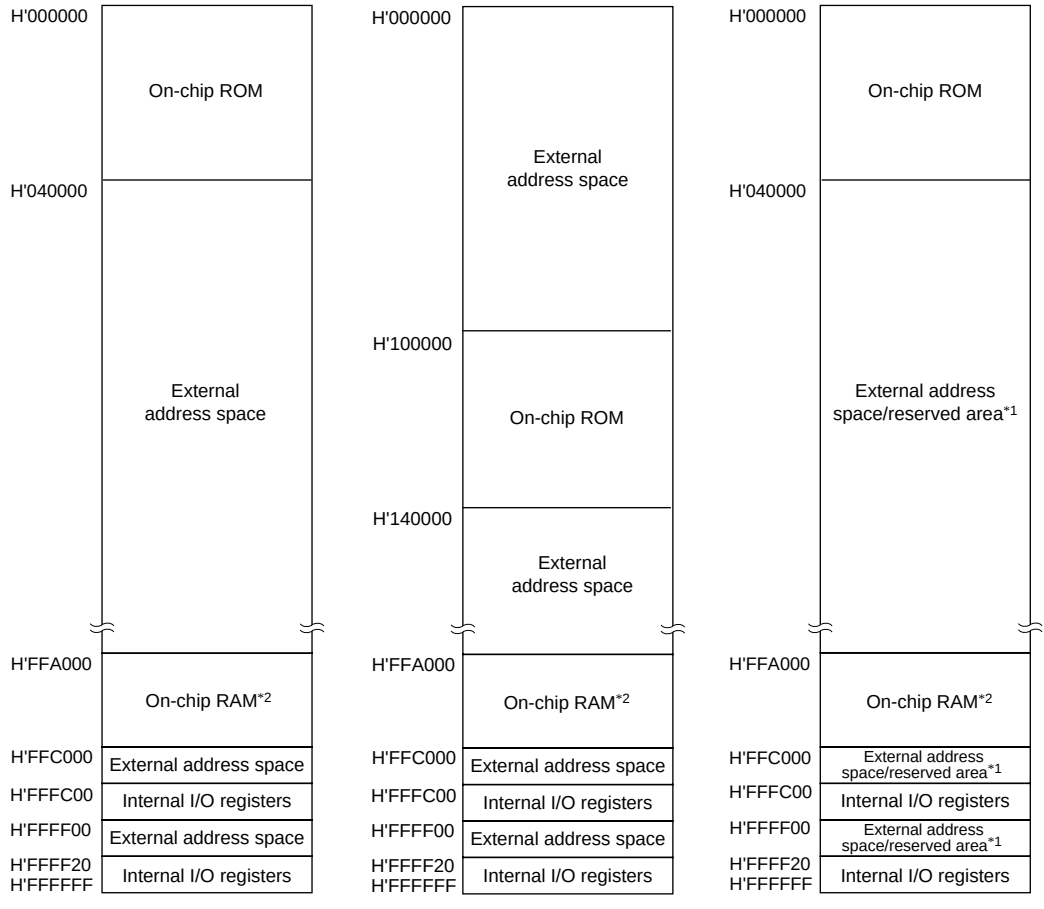
Notes: 1. External addresses can be accessed by clearing the RAME bit in SYSCR to 0.
2. When EXPE = 1, external address space; when EXPE = 0, reserved area.
3. When EXPE = 1, external address space when RAME = 0, on-chip RAM when RAME = 1.
When EXPE = 0, on-chip RAM area.

Figure 2.6 H8S/2676 Memory Map in Each Operating Mode (2)



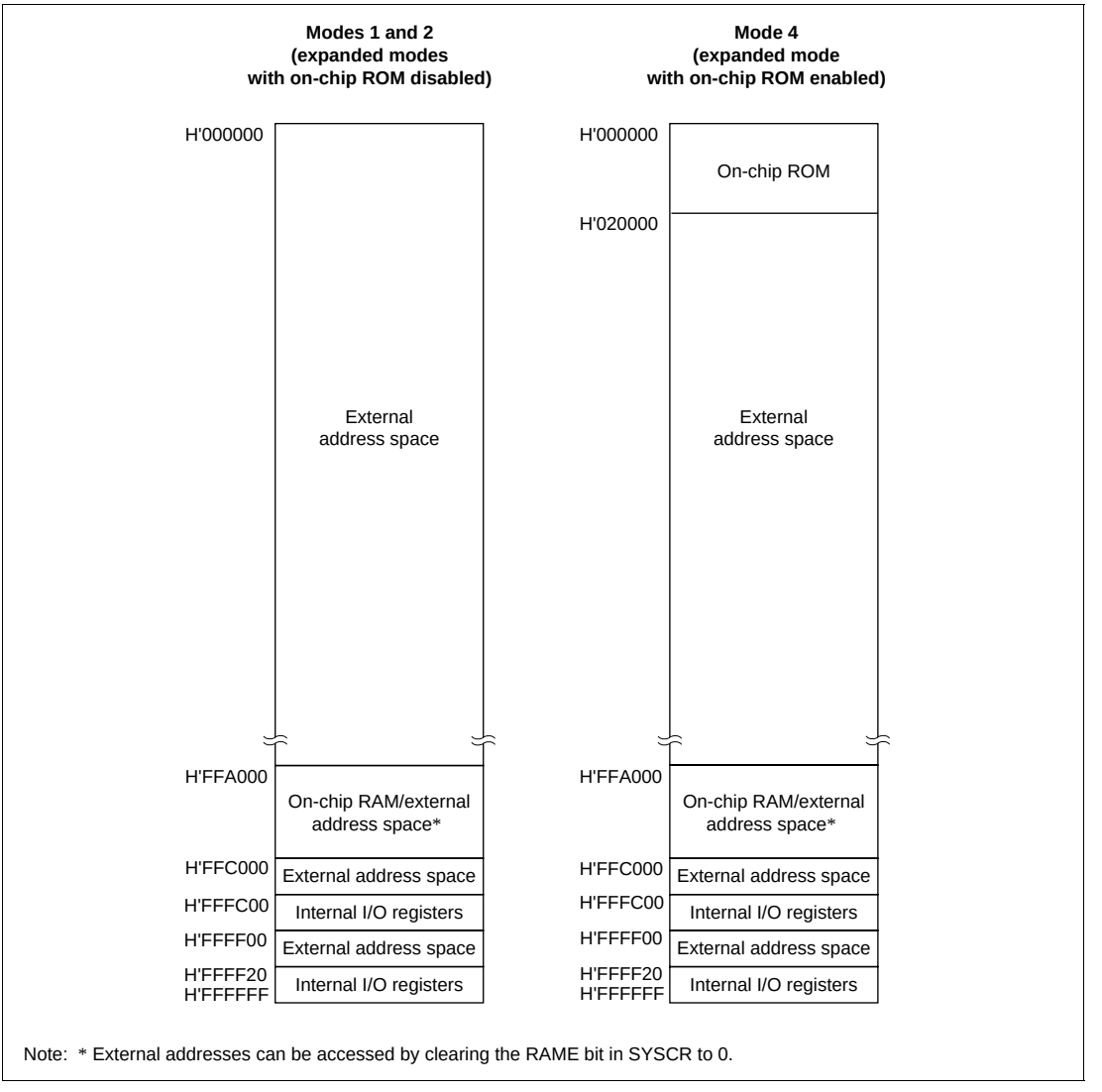
Notes: 1. When EXPE = 1, external address space; when EXPE = 0, reserved area.
2. On-chip RAM is used for flash memory programming. Do not clear the RAME bit in SYSCR to 0.

Figure 2.7 H8S/2676 Memory Map in Each Operating Mode (3)
[F-ZTAT™ Version Only]



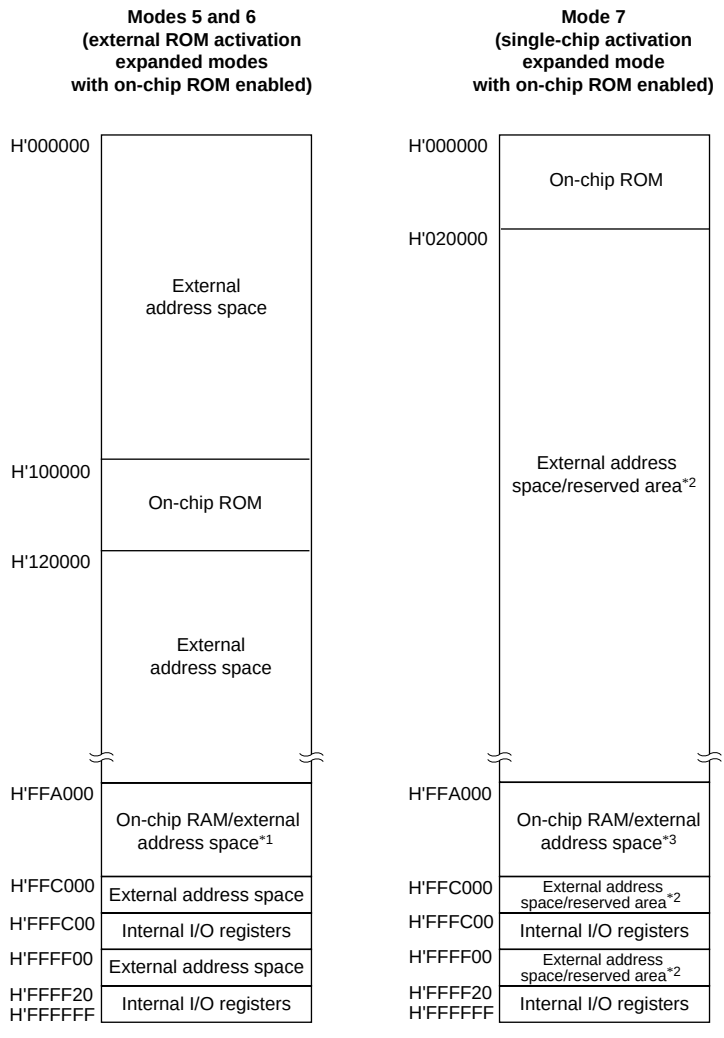
Notes: 1. When EXPE = 1, external address space; when EXPE = 0, reserved area.
2. On-chip RAM is used for flash memory programming. Do not clear the RAME bit in SYSCR to 0.

Figure 2.8 H8S/2676 Memory Map in Each Operating Mode (4)
[F-ZTAT™ Version Only]



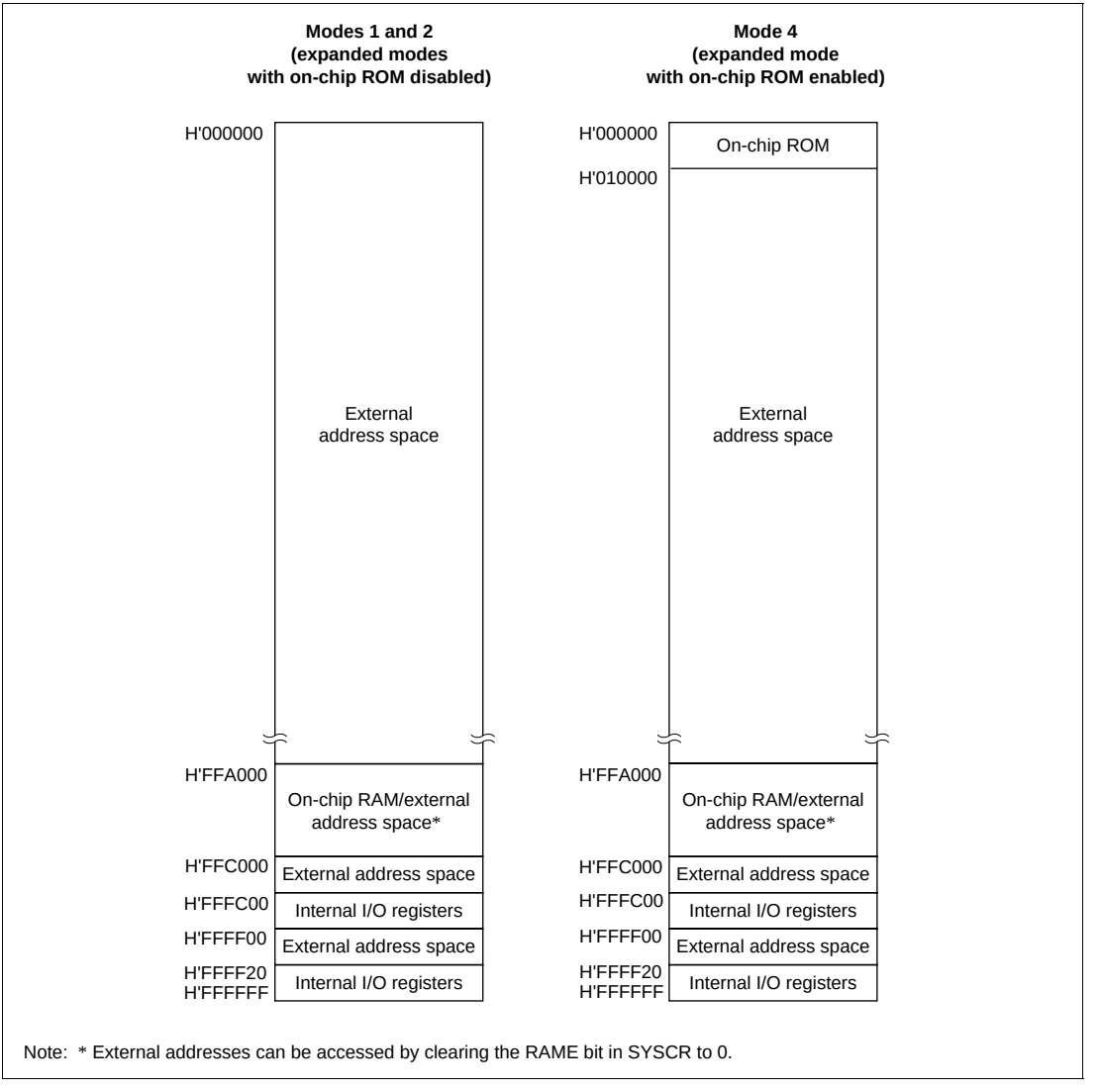
Note: * External addresses can be accessed by clearing the RAME bit in SYSCR to 0.

Figure 2.9 H8S/2675 Memory Map in Each Operating Mode (1)



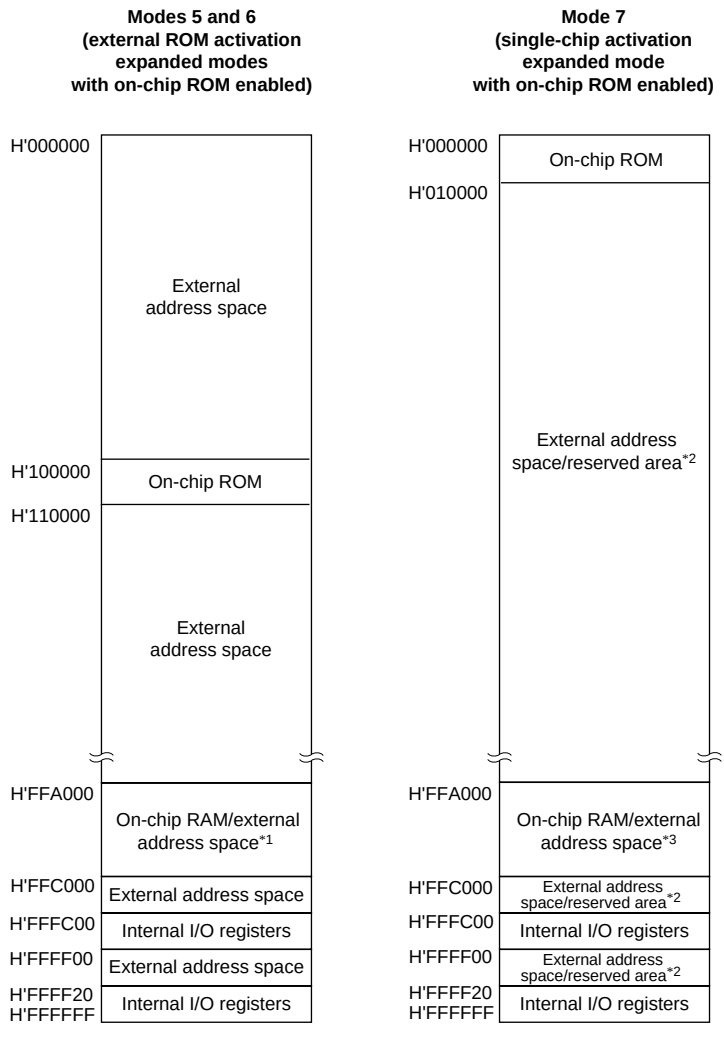
Notes: 1. External addresses can be accessed by clearing the RAME bit in SYSCR to 0.
2. When EXPE = 1, external address space; when EXPE = 0, reserved area.
3. When EXPE = 1, external address space when RAME = 0, on-chip RAM when RAME = 1.
When EXPE = 0, on-chip RAM area.

Figure 2.10 H8S/2675 Memory Map in Each Operating Mode (2)



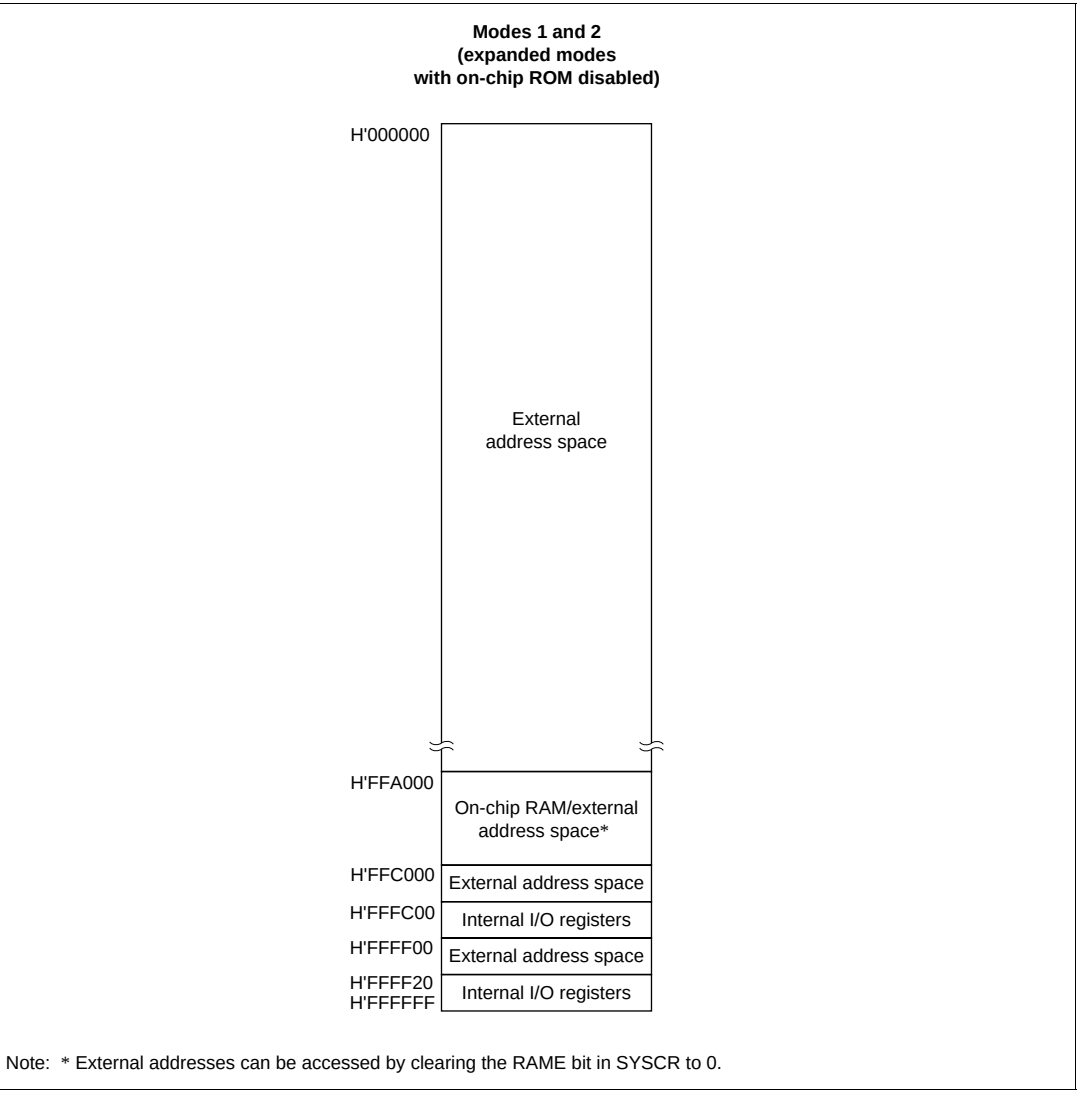
Note: * External addresses can be accessed by clearing the RAME bit in SYSCR to 0.

Figure 2.11 H8S/2673 Memory Map in Each Operating Mode (1)



Notes: 1. External addresses can be accessed by clearing the RAME bit in SYSCR to 0.
2. When EXPE = 1, external address space; when EXPE = 0, reserved area.
3. When EXPE = 1, external address space when RAME = 0, on-chip RAM when RAME = 1.
When EXPE = 0, on-chip RAM area.

Figure 2.12 H8S/2673 Memory Map in Each Operating Mode (2)



Note: * External addresses can be accessed by clearing the RAME bit in SYSCR to 0.

Figure 2.13 H8S/2670 Memory Map in Each Operating Mode

Section 3 Exception Handling and Interrupt Controller

3.1 Overview

3.1.1 Exception Handling Types and Priority

As table 3.1 indicates, exception handling may be caused by a reset, trap instruction, or interrupt. Exception handling is prioritized as shown in table 3.1. If two or more exceptions occur simultaneously, they are accepted and processed in order of priority. Trap instruction exceptions are accepted at all times in the program execution state.

Exception handling sources, the stack structure, and the operation of the CPU vary depending on the interrupt control mode set by the INTM0 and INTM1 bits in INTCR.

For details of exception handling and the interrupt controller, see section 2, Exception Handling, and section 3, Interrupt Controller, in the H8S/2678 Series Hardware Manual.

Table 3.1 Exception Types and Priority

Priority	Exception Type	Start of Exception Handling
High	Reset	Starts after a low-to-high transition at the $\overline{\text{RES}}$ pin, or when the watchdog timer overflows
	Trace*[1]	Starts when execution of the current instruction or exception handling ends, if the trace (T) bit is set to 1
	Interrupt	Starts when execution of the current instruction or exception handling ends, if an interrupt request has been issued*[2]
Low	Trap instruction*[3] (TRAPA)	Started by execution of a trap instruction (TRAPA)

Notes: 1. Traces are enabled only in interrupt control mode 2. Trace exception handling is not executed after execution of an RTE instruction.
2. Interrupt detection is not performed on completion of ANDC, ORC, XORC, or LDC instruction execution, or on completion of reset exception handling.
3. Trap instruction exception handling requests are accepted at all times in the program execution state.

3.2 Interrupt Controller

3.2.1 Interrupt Controller Features

- Two interrupt control modes
  - — Either of two interrupt control modes can be set by means of the INTM1 and INTM0 bits in the interrupt control register (INTCR).
- Priorities settable with IPRs
  - — Interrupt priority registers (IPRs) are provided for setting interrupt priorities. Eight priority levels can be set for each module for all interrupts except NMI.
  - — NMI is assigned the highest priority level of 8, and can be accepted at all times.
- Independent vector addresses
  - — All interrupt sources are assigned independent vector addresses, making it unnecessary for the source to be identified in the interrupt handling routine.
- Seventeen external interrupt pins
  - — NMI is the highest-priority interrupt, and is accepted at all times. Rising edge or falling edge can be selected for NMI.
  - — Falling edge, rising edge, or both edge detection, or level sensing, can be selected independently for IRQ15 to IRQ0.
- DTC and DMAC control
  - — DTC and DMAC activation is controlled by means of interrupts.

3.2.2 Block Diagram

Figure 3.1 shows a block diagram of the interrupt controller.

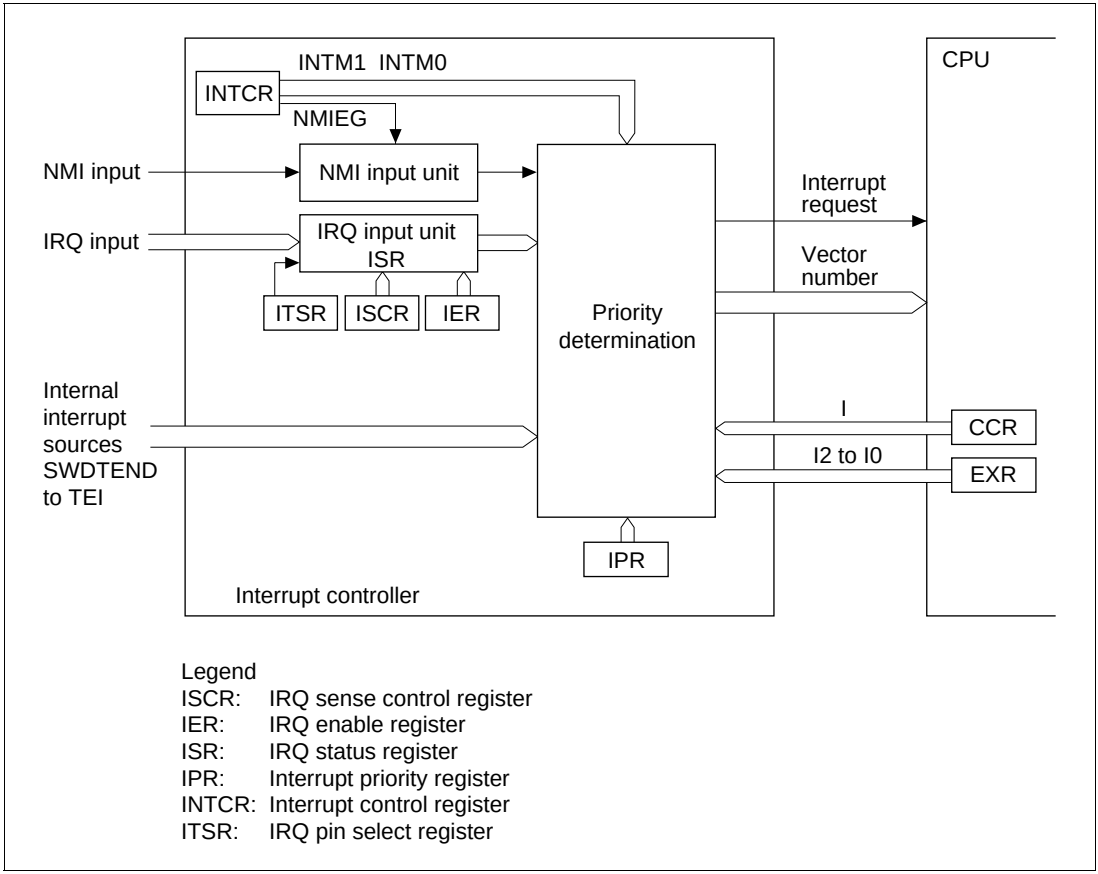


Figure 3.1 Block Diagram of Interrupt Controller

3.2.3 Pin Configuration

Table 3.2 summarizes the interrupt controller pins.

Table 3.2 Interrupt Controller Pins

Name	Abbreviation	I/O	Function
Nonmaskable interrupt	NMI	Input	Nonmaskable external interrupt; rising or falling edge can be selected
External interrupt request 15 to 0	$\overline{\text{IRQ15}}$ to $\overline{\text{IRQ0}}$	Input	Maskable external interrupts; rising, falling, or both edges, or level sensing, can be selected

3.2.4 Register Configuration

Table 3.3 summarizes the registers of the interrupt controller.

Table 3.3 Interrupt Controller Registers

Name	Abbreviation	R/W	Initial Value	Address*[1]
Interrupt control register	INTCR	R/W	H'00	H'FF31
IRQ sense control register H	ISCRH	R/W	H'0000	H'FE1A
IRQ sense control register L	ISCRL	R/W	H'0000	H'FE1C
IRQ enable register	IER	R/W	H'0000	H'FF32
IRQ status register	ISR	R/(W)*[2]	H'0000	H'FF34
IRQ pin select register	ITSR	R/W	H'0000	H'FE16
Software standby release IRQ enable register	SSIER	R/W	H'0007	H'FE18
Interrupt priority register A	IPRA	R/W	H'7777	H'FE00
Interrupt priority register B	IPRB	R/W	H'7777	H'FE02
Interrupt priority register C	IPRC	R/W	H'7777	H'FE04
Interrupt priority register D	IPRD	R/W	H'7777	H'FE06
Interrupt priority register E	IPRE	R/W	H'7777	H'FE08
Interrupt priority register F	IPRF	R/W	H'7777	H'FE0A
Interrupt priority register G	IPRG	R/W	H'7777	H'FE0C
Interrupt priority register H	IPRH	R/W	H'7777	H'FE0E
Interrupt priority register I	IPRI	R/W	H'7777	H'FE10
Interrupt priority register J	IPRJ	R/W	H'7777	H'FE12
Interrupt priority register K	IPRK	R/W	H'7777	H'FE14

Notes: 1. Lower 16 bits of the address.
2. Only 0 can be written, to clear flags.

3.3 Register Descriptions

3.3.1 Interrupt Control Register (INTCR)

Bit	7	6	5	4	3	2	1	0
	—	—	INTM1	INTM0	NMIEG	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	—	—	—

INTCR is an 8-bit readable/writable register that selects the interrupt control mode, and the detected edge for NMI.

INTCR is initialized to H'00 by a reset and in hardware standby mode. It is not initialized in software standby mode.

Bits 7 and 6—Reserved: These bits are always read as 0 and cannot be modified.

Bits 5 and 4—Interrupt Control Mode 1 and 0 (INTM1, INTM0): These bits select either of two interrupt control modes for the interrupt controller.

Bit 5 INTM1	Bit 4 INTM0	Interrupt Control Mode	Description	
0	0	0	Interrupts are controlled by I bit	(Initial value)
	1	—	Setting prohibited	
1	0	2	Interrupts are controlled by bits I2 to I0, and IPR	
	1	—	Setting prohibited	

Bit 3—NMI Edge Select (NMIEG): Selects the input edge for the NMI pin.

Bit 3 NMIEG	Description	
0	Interrupt request generated at falling edge of NMI input	(Initial value)
1	Interrupt request generated at rising edge of NMI input	

Bits 2 to 0—Reserved: These bits are always read as 0 and cannot be modified.

3.3.2 Interrupt Priority Registers A to K (IPRA to IPRK)

Bit	15	14	13	12	11	10	9	8
	—	IPR14	IPR13	IPR12	—	IPR10	IPR9	IPR8
Initial value	0	1	1	1	0	1	1	1
Read/Write	—	R/W	R/W	R/W	—	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0
Initial value	0	1	1	1	0	1	1	1
Read/Write	—	R/W	R/W	R/W	—	R/W	R/W	R/W

The IPR registers are eleven 16-bit readable/writable registers that set priorities (levels 7 to 0) for interrupts other than NMI.

The correspondence between interrupt sources and IPR settings is shown in table 3.4.

The IPR registers set a priority (level 7 to 0) for each interrupt source other than NMI.

The IPR registers are initialized to H'7777 by a reset and in hardware standby mode.

Bits 15, 11, 7, and 3—Reserved: These bits are always read as 0 and cannot be modified.

Table 3.4 Correspondence between Interrupt Sources and IPR Settings

Register	Bits 14 to 12	Bits 10 to 8	Bits 6 to 4	Bits 2 to 0
IPRA	IRQ0	IRQ1	IRQ2	IRQ3
IPRB	IRQ4	IRQ5	IRQ6	IRQ7
IPRC	IRQ8	IRQ9	IRQ10	IRQ11
IPRD	IRQ12	IRQ13	IRQ14	IRQ15
IPRE	DTC	Interval timer	—*	Refresh timer
IPRF	—*	A/D converter	TPU channel 0	TPU channel 1
IPRG	TPU channel 2	TPU channel 3	TPU channel 4	TPU channel 5
IPRH	8-bit timer channel 0	8-bit timer channel 1	DMAC	EXDMAC channel 0
IPRI	EXDMAC channel 1	EXDMAC channel 2	EXDMAC channel 3	SCI channel 0
IPRJ	SCI channel 1	SCI channel 2	—*	—*
IPRK	—*	—*	—*	—*

Note: * Reserved bits. These bits are read as H'7, and the write value should be H'7.

As shown in table 3.4, multiple interrupts are assigned to one IPR. Setting a value in the range from H'0 to H'7 in the 3-bit groups of bits 14 to 12, 10 to 8, 6 to 4, and 2 to 0 sets the priority of the corresponding interrupt. The lowest priority level, level 0, is assigned by setting H'0, and the highest priority level, level 7, by setting H'7.

When interrupt requests are generated, the highest-priority interrupt according to the priority levels set in the IPR registers is selected. This interrupt level is then compared with the interrupt mask level set by the interrupt mask bits (I2 to I0) in the extend register (EXR) in the CPU, and if the priority level of the interrupt is higher than the set mask level, an interrupt request is issued to the CPU.

3.3.3 IRQ Enable Register (IER)

Bit	15	14	13	12	11	10	9	8
	IRQ15E	IRQ14E	IRQ13E	IRQ12E	IRQ11E	IRQ10E	IRQ9E	IRQ8E
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	IRQ7E	IRQ6E	IRQ5E	IRQ4E	IRQ3E	IRQ2E	IRQ1E	IRQ0E
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IER is a 16-bit readable/writable register that controls enabling and disabling of interrupt requests IRQ15 to IRQ0.

IER is initialized to H'0000 by a reset and in hardware standby mode.

Bits 15 to 0—IRQ15 to IRQ0 Enable (IRQ15E to IRQ0E): These bits select whether interrupts IRQ15 to IRQ0 are enabled or disabled.

Bit n IRQnE	Description	
0	IRQn interrupts disabled	(Initial value)
1	IRQn interrupts enabled	

(n = 15 to 0)

3.3.4 IRQ Sense Control Registers H and L (ISCRH, ISCRL)

ISCRH

Bit	15	14	13	12	11	10	9	8
	IRQ15SCB	IRQ15SCA	IRQ14SCB	IRQ14SCA	IRQ13SCB	IRQ13SCA	IRQ12SCB	IRQ12SCA
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	IRQ11SCB	IRQ11SCA	IRQ10SCB	IRQ10SCA	IRQ9SCB	IRQ9SCA	IRQ8SCB	IRQ8SCA
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ISCRL

Bit	15	14	13	12	11	10	9	8
	IRQ7SCB	IRQ7SCA	IRQ6SCB	IRQ6SCA	IRQ5SCB	IRQ5SCA	IRQ4SCB	IRQ4SCA
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	IRQ3SCB	IRQ3SCA	IRQ2SCB	IRQ2SCA	IRQ1SCB	IRQ1SCA	IRQ0SCB	IRQ0SCA
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The ISCR registers are two 16-bit readable/writable registers that select rising edge, falling edge, or both edge detection, or level sensing, for the input at pins $\overline{\text{IRQ15}}$ to $\overline{\text{IRQ0}}$.

The ISCR registers are initialized to H'0000 by a reset and in hardware standby mode.

Bits 15 to 0—IRQ15 Sense Control A and B (IRQ15SCA, IRQ15SCB) to IRQ0 Sense Control A and B (IRQ0SCA, IRQ0SCB)

IRQnSCB	IRQnSCA	Description
0	0	Interrupt request generated at $\overline{\text{IRQn}}$ input low level (Initial value)
	1	Interrupt request generated at falling edge of $\overline{\text{IRQn}}$ input
1	0	Interrupt request generated at rising edge of $\overline{\text{IRQn}}$ input
	1	Interrupt request generated at both falling and rising edges of $\overline{\text{IRQn}}$ input

(n = 15 to 0)

3.3.5 IRQ Status Register (ISR)

Bit	15	14	13	12	11	10	9	8
	IRQ15F	IRQ14F	IRQ13F	IRQ12F	IRQ11F	IRQ10F	IRQ9F	IRQ8F
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Bit	7	6	5	4	3	2	1	0
	IRQ7F	IRQ6F	IRQ5F	IRQ4F	IRQ3F	IRQ2F	IRQ1F	IRQ0F
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: * Only 0 can be written, to clear the flag.

ISR is a 16-bit readable/writable register that indicates the status of IRQ15 to IRQ0 interrupt requests.

ISR is initialized to H'0000 by a reset and in hardware standby mode.

As IRQnF may be set to 1 depending on the pin states after a reset, it is necessary to read ISR, and then write 0s to it, following a reset.

Bits 15 to 0—IRQ15 to IRQ0 Flags (IRQ15F to IRQ0F): These bits indicate the status of IRQ15 to IRQ0 interrupt requests.

Bit n IRQnF	Description
0	[Clearing conditions] (Initial value) • When 0 is written to IRQnF after reading IRQnF = 1 • When interrupt exception handling is executed when low-level detection is set (IRQnSCB = IRQnSCA = 0) and $\overline{\text{IRQn}}$ input is high • When IRQn interrupt exception handling is executed when falling, rising, or both-edge detection is set (IRQnSCB = 1 or IRQnSCA = 1) • When the DTC is activated by an IRQn interrupt and the DISEL bit in MRB of the DTC is 0
1	[Setting conditions] • When $\overline{\text{IRQn}}$ input goes low when low-level detection is set (IRQnSCB = IRQnSCA = 0) • When a falling edge occurs in $\overline{\text{IRQn}}$ input when falling edge detection is set (IRQnSCB = 0, IRQnSCA = 1) • When a rising edge occurs in $\overline{\text{IRQn}}$ input when rising edge detection is set (IRQnSCB = 1, IRQnSCA = 0) • When a falling or rising edge occurs in $\overline{\text{IRQn}}$ input when both-edge detection is set (IRQnSCB = IRQnSCA = 1)

(n = 15 to 0)

3.3.6 IRQ Pin Select Register (ITSR)

Bit	15	14	13	12	11	10	9	8
	ITS15	ITS14	ITS13	ITS12	ITS11	ITS10	ITS9	ITS8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	ITS7	ITS6	ITS5	ITS4	ITS3	ITS2	ITS1	ITS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ITSR is a 16-bit readable/writable register that selects input pins IRQ15 to IRQ0.

ITSR is initialized to H'0000 by a reset and in hardware standby mode.

Bits 15 to 0—IRQ Input Pin Select (ITS15 to ITS0): IRQn input pins can be used as the pins shown below according to the value of ITSn. (n = 15 to 0)

Bit	ITS = 0 (Initial Value)	ITS = 1
ITS15	PF2	P27
ITS14	PF1	P26
ITS13	P65	P25
ITS12	P64	P24
ITS11	P63	P23
ITS10	P62	P22
ITS9	P61	P21
ITS8	P60	P20
ITS7	P57	PH3
ITS6	P56	PH2
ITS5	P55	P85
ITS4	P54	P84
ITS3	P53	P83
ITS2	P52	P82
ITS1	P51	P81
ITS0	P50	P80

When an ITSR setting is changed, if the selected pin level before the change is different from the selected pin level after the change, an edge may be generated internally and IRQnF (n = 0 to 15) in ISR may be set at an unintended timing. If the IRQn interrupt (n = 0 to 15) is enabled at this time, the associated interrupt exception handling will be executed.

To prevent unintended interrupts, make changes to ITSR settings with IRQn interrupts (n = 0 to 15) disabled, and then clear IRQnF (n = 0 to 15).

3.3.7 Software Standby Release IRQ Enable Register (SSIER)

Bit	15	14	13	12	11	10	9	8
	SSI15	SSI14	SSI13	SSI12	SSI11	SSI10	SSI9	SSI8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	SSI7	SSI6	SSI5	SSI4	SSI3	SSI2	SSI1	SSI0
Initial value	0	0	0	0	0	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SSIER is a 16-bit readable/writable register that selects the $\overline{\text{IRQ}}$ pins used to recover from the software standby state.

SSIER is initialized to H'0007 by a reset and in hardware standby mode.

An IRQ interrupt used to recover from the software standby state must not be set as a DTC activation source.

Bits 15 to 0—Software Standby Release IRQ Setting (SSI15 to SSI0): These bits select the $\overline{\text{IRQ}}$ pins used to recover from the software standby state.

Bit n SSIn	Description
0	IRQn requests are not sampled in the software standby state (Initial value when n = 15 to 3)
1	When an IRQn request occurs in the software standby state, the chip recovers from the software standby state after the elapse of the oscillation settling time (Initial value when n = 2 to 0)

3.4 Interrupt Sources

Interrupt sources comprise external interrupts (NMI and IRQ15 to IRQ0) and internal interrupts (56 sources).

3.4.1 External Interrupts

There are 17 external interrupt sources: NMI and IRQ15 to IRQ0. Setting an SSI bit to 1 in SSIER enables the corresponding IRQ15–IRQ0 interrupt to be used as a software standby mode release source.

NMI Interrupt: NMI is the highest-priority interrupt, and is always accepted by the CPU regardless of the interrupt control mode and the status of the CPU interrupt mask bits. The NMIEG bit in INTCR specifies whether an interrupt is requested at a rising edge or a falling edge on the NMI pin.

The vector number for NMI interrupt exception handling is 7.

IRQ15 to IRQ0 Interrupts: Interrupts IRQ15 to IRQ0 are requested by an input signal at pins $\overline{\text{IRQ15}}$ to $\overline{\text{IRQ0}}$. Interrupts IRQ15 to IRQ0 have the following features:

- Using ISCR, it is possible to select whether an interrupt is generated by a low level, falling edge, rising edge, or both edges, at pins $\overline{\text{IRQ15}}$ to $\overline{\text{IRQ0}}$.
- Enabling or disabling of interrupt requests IRQ15 to IRQ0 can be selected with IER.
- The interrupt priority level can be set with IPR.
- The status of interrupt requests IRQ15 to IRQ0 is indicated in ISR. ISR flags can be cleared to 0 by software.

A block diagram of interrupts IRQ15 to IRQ0 is shown in figure 3.2.

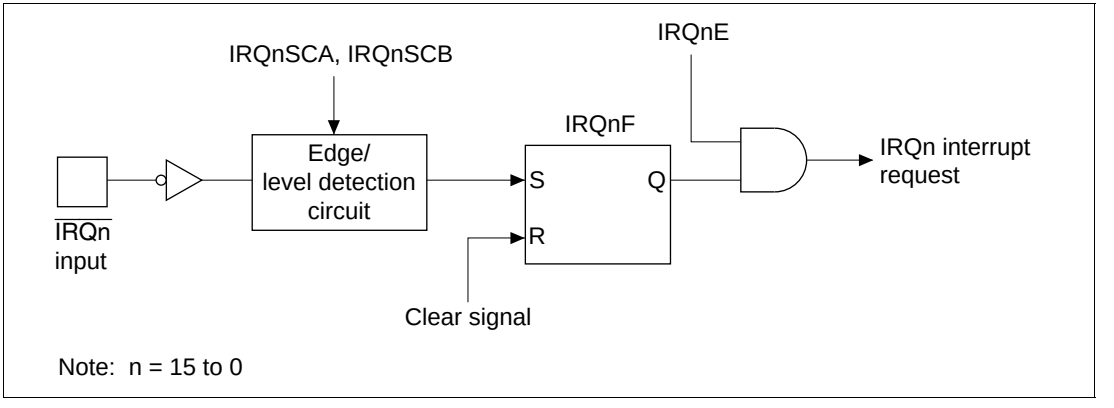


Figure 3.2 Block Diagram of Interrupts IRQ15 to IRQ0

Figure 3.3 shows the timing of the setting of IRQnF.

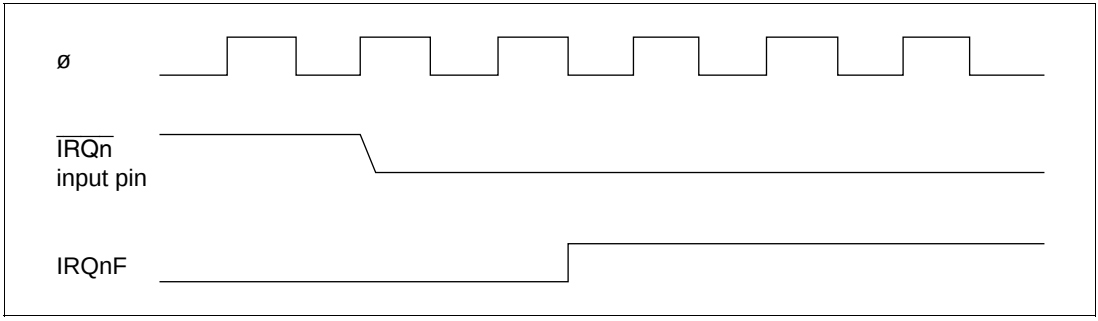


Figure 3.3 Timing of Setting of IRQnF

The vector numbers for IRQ15 to IRQ0 interrupt exception handling are 31 to 16.

Detection of IRQ15 to IRQ0 interrupts does not depend on whether the relevant pin has been set for input or output. When a pin is used as an external interrupt input pin, clear the corresponding DDR bit to 0 and do not use the pin as an I/O pin for another function.

When interrupt request generation by a low level at the $\overline{\text{IRQ}}$ pin is selected for an IRQ15 to IRQ0 interrupt by means of an ISCR setting, when an interrupt is requested the relevant $\overline{\text{IRQ}}$ pin should be held low until interrupt handling starts. The $\overline{\text{IRQ}}$ pin should then be returned to the high level, and IRQnF (n = 0 to 15) cleared, in the interrupt handling routine. If the $\overline{\text{IRQ}}$ pin is returned to the high level before interrupt handling is started, the associated interrupt may not be executed.

3.4.2 Internal Interrupts

There are 56 sources for internal interrupts from on-chip supporting modules.

1. For each on-chip supporting module there are flags that indicate the interrupt request status, and enable bits that select enabling or disabling of these interrupts. If any one of these is set to 1, an interrupt request is issued to the interrupt controller.
2. The interrupt priority level can be set by means of IPR.
3. The DMAC and DTC can be activated by a TPU, SCI, or other interrupt request. When the DMAC or DTC is activated by an interrupt, the interrupt control mode and CPU interrupt mask bits have no effect.

3.4.3 Interrupt Vector Table

Table 3.5 shows interrupt exception handling sources, their vector addresses, and their priority order. In the default priority order, smaller vector numbers have higher priority.

Priorities among modules can be set by means of IPR. The priority order when two or more modules are set to the same priority, and the priority order within a module, are fixed as shown in table 3.5.

Table 3.5 Interrupt Sources, Vector Addresses, and Priority Order

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address*	IPR	Priority	DTC Activation	DMAC Activation
Power-on reset		0	H'0000	—	High	—	—
Reserved		1	H'0004				
Reserved for system		2	H'0008				
		3	H'000C				
		4	H'0010				
Trace		5	H'0014				
Reserved for system		6	H'0018				
NMI	External pin	7	H'001C				
Trap instruction (4 sources)		8	H'0020				
		9	H'0024				
		10	H'0028				
		11	H'002C				
Reserved for system		12	H'0030				
		13	H'0034				
		14	H'0038				
IRQ0	External pin	16	H'0040	IPRA14–IPRA12		○	—
IRQ1		17	H'0044	IPRA10–IPRA8		○	—
IRQ2		18	H'0048	IPRA6–IPRA4		○	—
IRQ3		19	H'004C	IPRA2–IPRA0		○	—
IRQ4		20	H'0050	IPRB14–IPRB12		○	—
IRQ5		21	H'0054	IPRB10–IPRB8		○	—
IRQ6		22	H'0058	IPRB6–IPRB4		○	—
IRQ7		23	H'005C	IPRB2–IPRB0		○	—
IRQ8		24	H'0060	IPRC14–IPRC12		○	—
IRQ9		25	H'0064	IPRC10–IPRC8		○	—
IRQ10		26	H'0068	IPRC6–IPRC4		○	—
IRQ11		27	H'006C	IPRC2–IPRC0		○	—
IRQ12		28	H'0070	IPRD14–IPRD12		○	—
IRQ13		29	H'0074	IPRD10–IPRD8		○	—
IRQ14		30	H'0078	IPRD6–IPRD4		○	—
IRQ15		31	H'007C	IPRD2–IPRD0	Low	○	—

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address*	IPR	Priority	DTC Activation	DMAC Activation
SWDTEND (software-activated data transfer end)	DTC	32	H'0080	IPRE14–IPRE12	High	○	—
WOVI (interval timer)	Watchdog timer	33	H'0084	IPRE10–IPRE8		—	—
Reserved	—	34	H'0088	IPRE6–IPRE4		—	—
CMI (compare match)	Refresh controller	35	H'008C	IPRE2–IPRE0		—	—
Reserved	—	36	H'0090	IPRF14–IPRF12		—	—
		37	H'0094			—	—
ADI (A/D conversion end)	A/D	38	H'0098	IPRF10–IPRF8		○	○
Reserved	—	39	H'009C			—	—
TGI0A (TGR0A input capture/compare match)	TPU channel 0	40	H'00A0	IPRF6–IPRF4		○	○
TGI0B (TGR0B input capture/compare match)		41	H'00A4			○	—
TGI0C (TGR0C input capture/compare match)		42	H'00A8			○	—
TGI0D (TGR0D input capture/compare match)		43	H'00AC			○	—
TCI0V (overflow 0)		44	H'00B0			—	—
Reserved	—	45	H'00B4			—	—
		46	H'00B8				
		47	H'00BC				
TGI1A (TGR1A input capture/compare match)	TPU channel 1	48	H'00C0	IPRF2–IPRF0		○	○
TGI1B (TGR1B input capture/compare match)		49	H'00C4			○	—
TCI1V (overflow 1)		50	H'00C8			—	—
TCI1U (underflow 1)		51	H'00CC			—	—
TGI2A (TGR2A input capture/compare match)	TPU channel 2	52	H'00D0	IPRG14–IPRG12		○	○
TGI2B (TGR2B input capture/compare match)		53	H'00D4			○	—
TCI2V (overflow 2)		54	H'00D8			—	—
TCI2U (underflow 2)		55	H'00DC		Low	—	—

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address*	IPR	Priority	DTC Activation	DMAC Activation
TGI3A (TGR3A input capture/compare match)	TPU channel 3	56	H'00E0	IPRG10–IPRG8	High	○	○
TGI3B (TGR3B input capture/compare match)		57	H'00E4			○	—
TGI3C (TGR3C input capture/compare match)		58	H'00E8			○	—
TGI3D (TGR3D input capture/compare match)		59	H'00EC			○	—
TCI3V (overflow 3)		60	H'00F0			—	—
Reserved	—	61	H'00F4			—	—
		62	H'00F8				
		63	H'00FC				
TGI4A (TGR4A input capture/compare match)	TPU channel 4	64	H'0100	IPRG6–IPRG4		○	○
TGI4B (TGR4B input capture/compare match)		65	H'0104			○	—
TCI4V (overflow 4)		66	H'0108			—	—
TCI4U (underflow 4)		67	H'010C			—	—
TGI5A (TGR5A input capture/compare match)	TPU channel 5	68	H'0110	IPRG2–IPRG0		○	○
TGI5B (TGR5B input capture/compare match)		69	H'0114			○	—
TCI5V (overflow 5)		70	H'0118			—	—
TCI5U (underflow 5)		71	H'011C			—	—
CMIA0 (compare match A)	8-bit timer channel 0	72	H'0120	IPRH14–IPRH12		○	—
CMIB0 (compare match B)		73	H'0124			○	—
OVI0 (overflow 0)		74	H'0128			—	—
Reserved	—	75	H'012C			—	—
CMIA1 (compare match A)	8-bit timer channel 1	76	H'0130	IPRH10–IPRH8		○	—
CMIB1 (compare match B)		77	H'0134			○	—
OVI1 (overflow 1)		78	H'0138			—	—
Reserved	—	79	H'013C		Low	—	—

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address*	IPR	Priority	DTC Activation	DMAC Activation
DMTEND0A (channel 0/channel 0A transfer end)	DMAC	80	H'0140	IPRH6–IPRH4	High	○	—
DMTEND0B (channel 0B transfer end)		81	H'0144			○	—
DMTEND1A (channel 1/channel 1A transfer end)		82	H'0148			○	—
DMTEND1B (channel 1B transfer end)		83	H'014C			○	—
EXDMTEND0 (channel 0 transfer end)	EXDMAC	84	H'0150	IPRH2–IPRH0		—	—
EXDMTEND1 (channel 1 transfer end)		85	H'0154	IPRI14–IPRI12		—	—
EXDMTEND2 (channel 2 transfer end)		86	H'0158	IPRI10–IPRI8		—	—
EXDMTEND3 (channel 3 transfer end)		87	H'015C	IPRI6–IPRI4		—	—
ERI0 (receive error 0)	SCI channel 0	88	H'0160	IPRI2–IPRI0		—	—
RXI0 (receive completed 0)		89	H'0164			○	○
TXI0 (transmit data empty 0)		90	H'0168			○	○
TEI0 (transmit end 0)		91	H'016C			—	—
ERI1 (receive error 1)	SCI channel 1	92	H'0170	IPRJ14–IPRJ12		—	—
RXI1 (receive completed 1)		93	H'0174			○	○
TXI1 (transmit data empty 1)		94	H'0178			○	○
TEI1 (transmit end 1)		95	H'017C			—	—
ERI2 (receive error 2)	SCI channel 2	96	H'0180	IPRJ10–IPRJ8		—	—
RXI2 (receive completed 2)		97	H'0184			○	—
TXI2 (transmit data empty 2)		98	H'0188			○	—
TEI2 (transmit end 2)		99	H'018C		Low	—	—

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address*	IPR	Priority	DTC Activation	DMAC Activation
Reserved	—	100	H'0190	IPRJ6–IPRJ4	High	—	—
		101	H'0194				
		102	H'0198				
		103	H'019C				
		104	H'01A0	IPRJ2–IPRJ0			
		105	H'01A4				
		106	H'01A8				
		107	H'01AC				
		108	H'01B0	IPRK14–IPRK12			
		109	H'01B4				
		110	H'01B8				
		111	H'01BC				
		112	H'01C0	IPRK10–IPRK8			
		113	H'01C4				
		114	H'01C8				
		115	H'01CC				
		116	H'01D0	IPRK6–IPRK4			
		117	H'01D4				
		118	H'01D8				
		119	H'01DC				
		120	H'01E0	IPRK2–IPRK2			
		121	H'01E4				
		122	H'01E8				
		123	H'01EC				
		124	H'01F0				
		125	H'01F4				
		126	H'01F8				
		127	H'01FC		Low		

Notes: Interrupt sources vary depending on the model. See the reference manual for the relevant model for details.

* Lower 16 bits of the start address.

3.5 Interrupt Operation

3.5.1 Interrupt Control Modes and Interrupt Operation

Interrupt operations in the H8S/2678 Series differ depending on the interrupt control mode.

NMI interrupts are accepted at all times except in the reset state and the hardware standby state. In the case of IRQ interrupts and on-chip supporting module interrupts, an enable bit is provided for each interrupt. Clearing an enable bit to 0 disables the corresponding interrupt request. Interrupt sources for which the enable bits are set to 1 are controlled by the interrupt controller.

Table 3.6 shows the interrupt control modes.

The interrupt controller performs interrupt control according to the interrupt control mode set by the INTM1 and INTM0 bits in INTCR, the priorities set in IPR, and the masking state indicated by the I bit in the CPU's CCR, and bits I2 to I0 in EXR.

Table 3.6 Interrupt Control Modes

Interrupt Control Mode	INTCR		Priority Setting Registers	Interrupt Mask Bits	Description
	INTM1	INTM0			
0	0	0	—	I	Interrupt mask control is performed by the I bit.
—		1	—	—	Setting prohibited
2	1	0	IPR	I2 to I0	8-level interrupt mask control is performed by bits I2 to I0. 8 priority levels can be set with IPR.
—		1	—	—	Setting prohibited

Figure 3.4 shows a block diagram of the priority decision circuit.

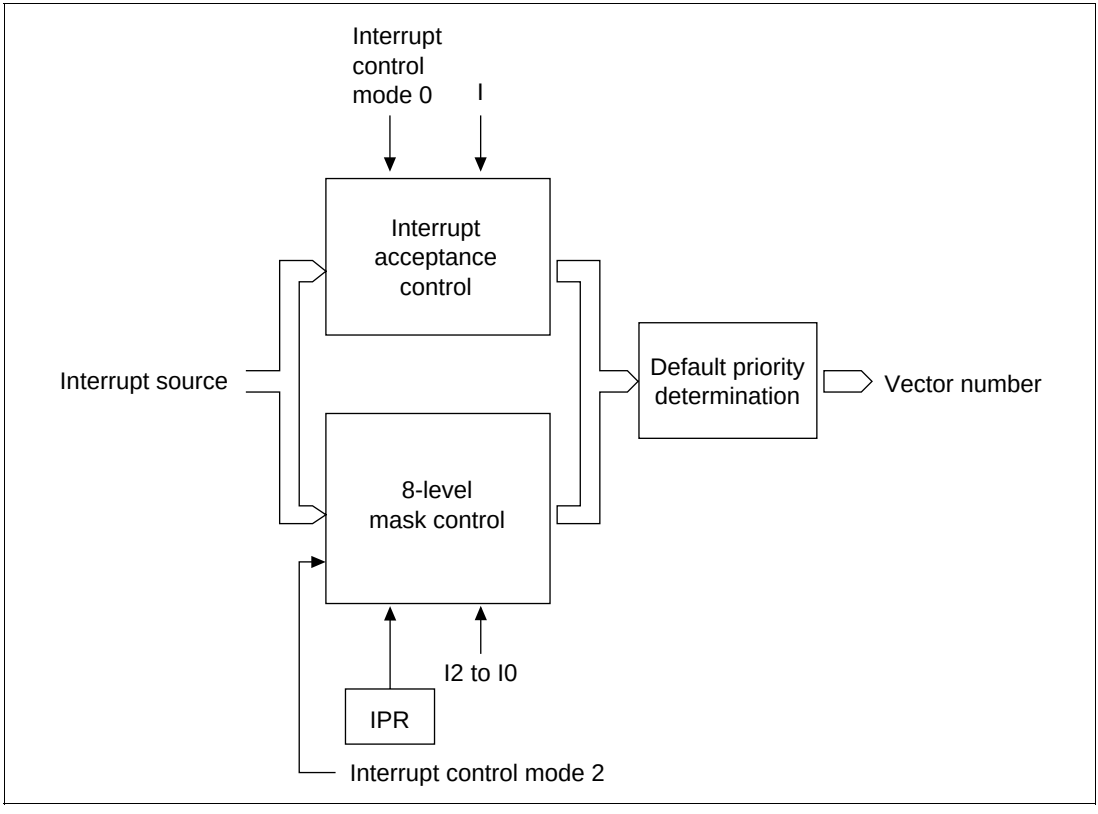


Figure 3.4 Block Diagram of Interrupt Control Operation

Interrupt Acceptance Control: In interrupt control mode 0, interrupt acceptance control is performed by means of the I bit in CCR.

Table 3.7 shows the interrupts that can be selected in each interrupt control mode.

Table 3.7 Interrupts Selected in Each Interrupt Control Mode (1)

	Interrupt Mask Bit	
Interrupt Control Mode	**I**	**Selected Interrupts**
0	0	All interrupts
	1	NMI interrupt
2	*	All interrupts

*: Don't care

8-Level Control: In interrupt control mode 2, 8-level mask level determination is performed according to the interrupt priority level (IPR) for interrupts selected in interrupt acceptance control.

The interrupt source selected is the interrupt with the highest priority level, and for which the priority level set in IPR is higher than the mask level.

Table 3.8 Interrupts Selected in Each Interrupt Control Mode (2)

Interrupt Control Mode	Selected Interrupts
0	All interrupts
2	Highest-priority-level (IPR) interrupt whose priority level is greater than the mask level (IPR > I2 to I0)

Default Priority Determination: When an interrupt is selected by 8-level control, its priority is determined and a vector number is generated.

If the same value is set for IPR, acceptance of multiple interrupts is enabled, and so only the interrupt source with the highest priority according to the preset default priorities is selected and has a vector number generated.

Interrupt sources with a lower priority than the accepted interrupt source are held pending.

Table 3.9 shows operations and control signal functions in each interrupt control mode.

Table 3.9 Operations and Control Signal Functions in Each Interrupt Control Mode

Interrupt Control Mode	Setting		Interrupt Acceptance Control		8-Level Control			Default Priority Determination	T (Trace)
	INTM1	INTM0		I		I2–I0	IPR		
0	0	0	O	IM	X	—	—*[2]	O	—
2	1	0	X	—*[1]	O	IM	PR	O	T

Legend

O: Interrupt operation control performed

X: No operation (all interrupts enabled)

IM: Used as interrupt mask bit

PR: Sets priority.

—: Not used.

Notes: 1. Set to 1 when interrupt is accepted.

2. Keep the initial setting (IPR writes prohibited).

3.5.2 Interrupt Control Mode 0

Enabling and disabling of IRQ interrupts and on-chip supporting module interrupts can be set by means of the I bit in the CPU's CCR. Interrupts are enabled when the I bit is cleared to 0, and disabled when the I bit is set to 1.

Figure 3.5 shows a flowchart of the interrupt acceptance operation in this case.

1. If an interrupt source occurs when the corresponding interrupt enable bit is set to 1, an interrupt request is sent to the interrupt controller.
2. The I bit is then referenced. If the I bit is cleared to 0, the interrupt request is accepted. If the I bit is set to 1, only an NMI interrupt is accepted, and other interrupt requests are held pending.
3. Interrupt requests are sent to the interrupt controller, the highest-priority interrupt according to the priority order is selected, and the others are held pending.
4. When an interrupt request is accepted, processing for the instruction being executed at that time is completed before interrupt exception handling is started.
5. PC and CCR are saved to the stack area in interrupt exception handling. The PC value saved on the stack shows the address of the first instruction to be executed after returning from the interrupt service routine.
6. Next, the I bit in CCR is set to 1. This masks all interrupts except NMI.
7. A vector address is generated for the accepted interrupt, and execution of the interrupt service routine starts at the address indicated by the contents of that vector address.

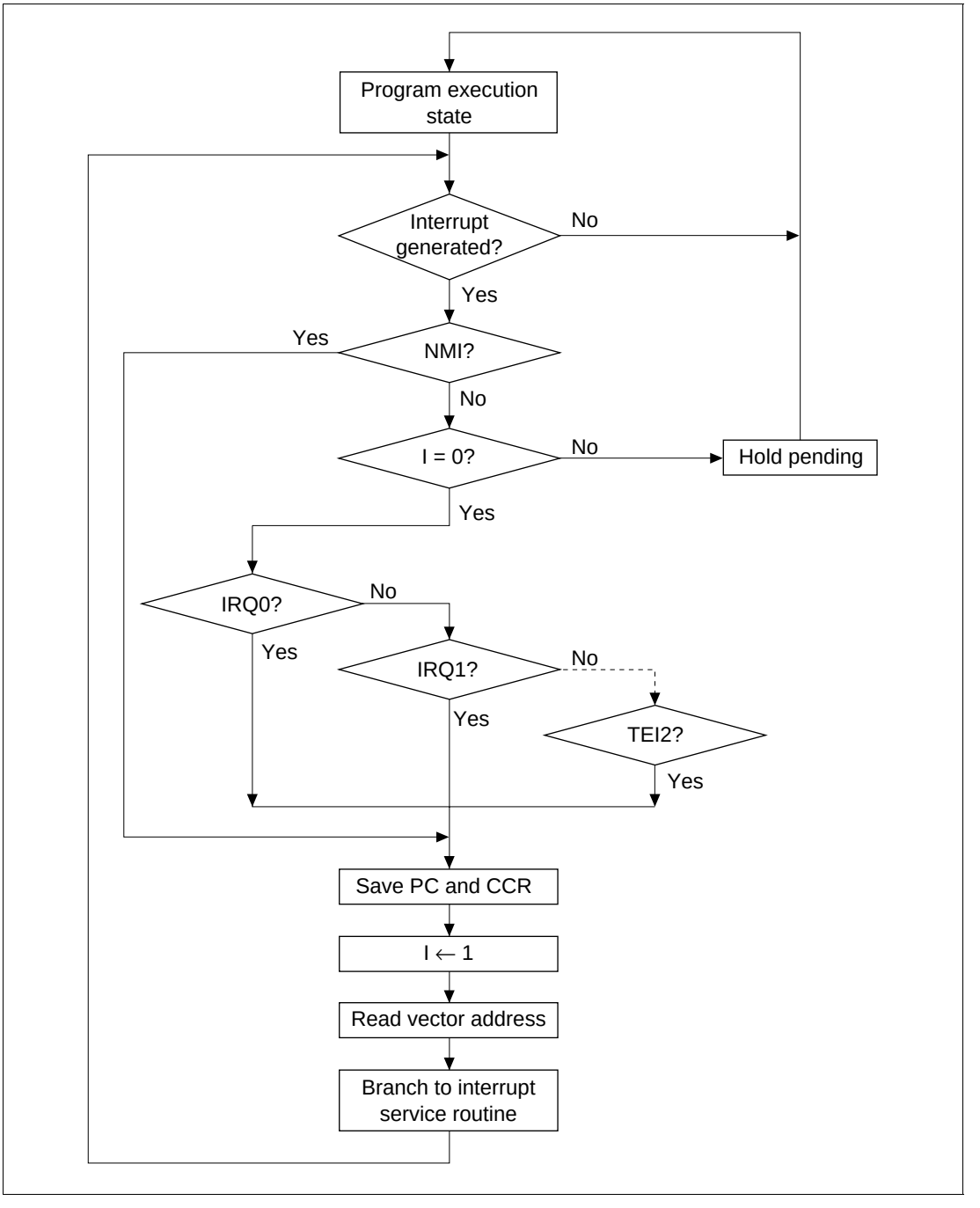


Figure 3.5 Flowchart of Procedure Up to Interrupt Acceptance in Interrupt Control Mode 0

3.5.3 Interrupt Control Mode 2

Eight-level masking is implemented for IRQ interrupts and on-chip supporting module interrupts by comparing the interrupt mask level set by bits I2 to I0 of EXR in the CPU with IPR.

Figure 3.6 shows a flowchart of the interrupt acceptance operation in this case.

1. If an interrupt source occurs when the corresponding interrupt enable bit is set to 1, an interrupt request is sent to the interrupt controller.
2. When interrupt requests are sent to the interrupt controller, the interrupt with the highest priority level according to the interrupt priority levels set in IPR is selected, and lower-priority interrupt requests are held pending. If a number of interrupt requests with the same priority are generated at the same time, the interrupt request with the highest priority according to the priority system shown in table 3.4 is selected.
3. Next, the priority of the selected interrupt request is compared with the interrupt mask level set in EXR. An interrupt request with a priority no higher than the mask level set at that time is held pending, and only an interrupt request with a priority higher than the interrupt mask level is accepted.
4. When an interrupt request is accepted, processing for the instruction being executed at that time is completed before interrupt exception handling is started.
5. PC, CCR, and EXR are saved to the stack area in interrupt exception handling. The PC value saved on the stack shows the address of the first instruction to be executed after returning from the interrupt service routine.
6. The T bit in EXR is cleared to 0. As a result, the interrupt mask level is rewritten with the priority level of the accepted interrupt.

   If the accepted interrupt is NMI, the interrupt mask level is set to H'7.
7. A vector address is generated for the accepted interrupt, and execution of the interrupt service routine starts at the address indicated by the contents of that vector address.

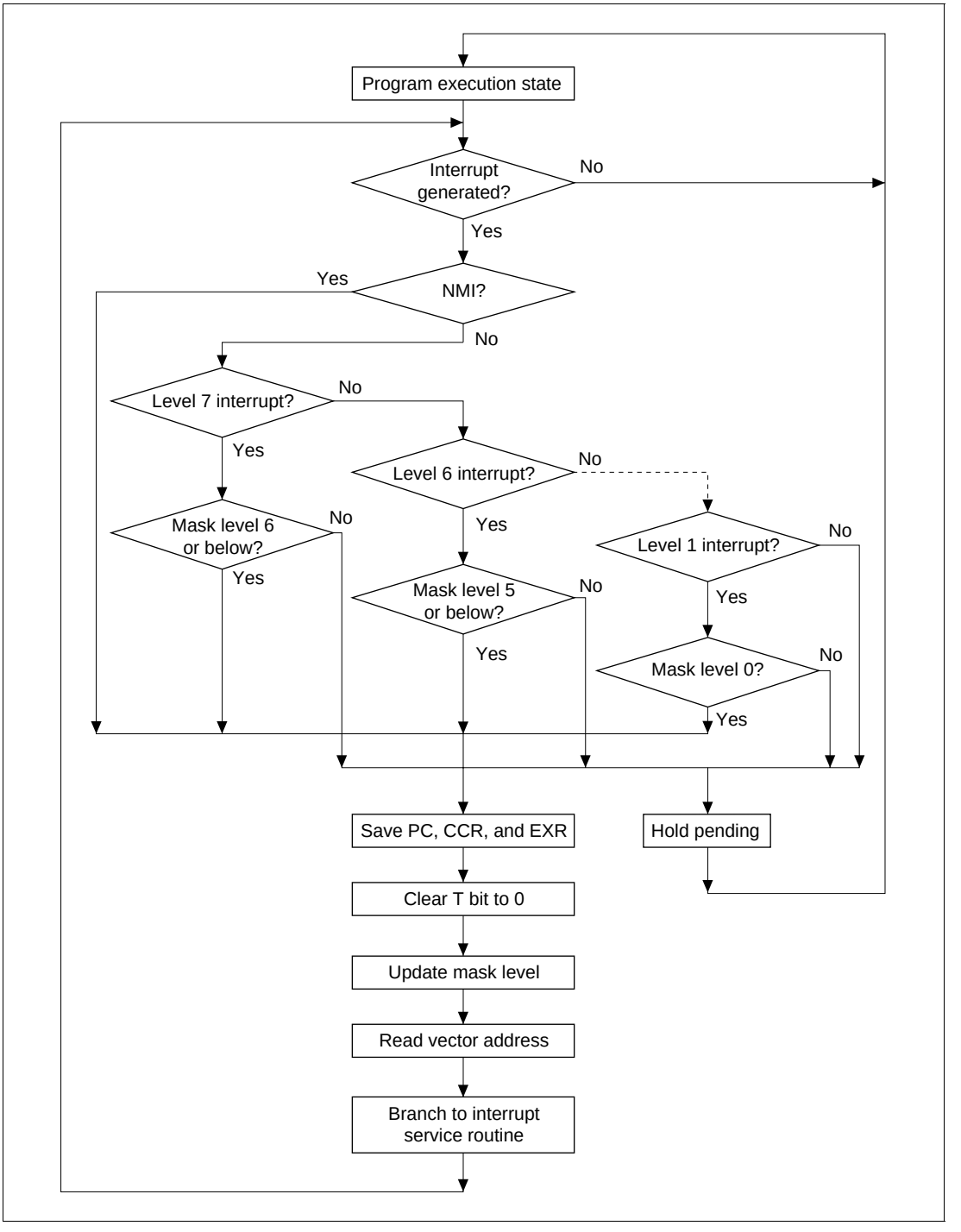
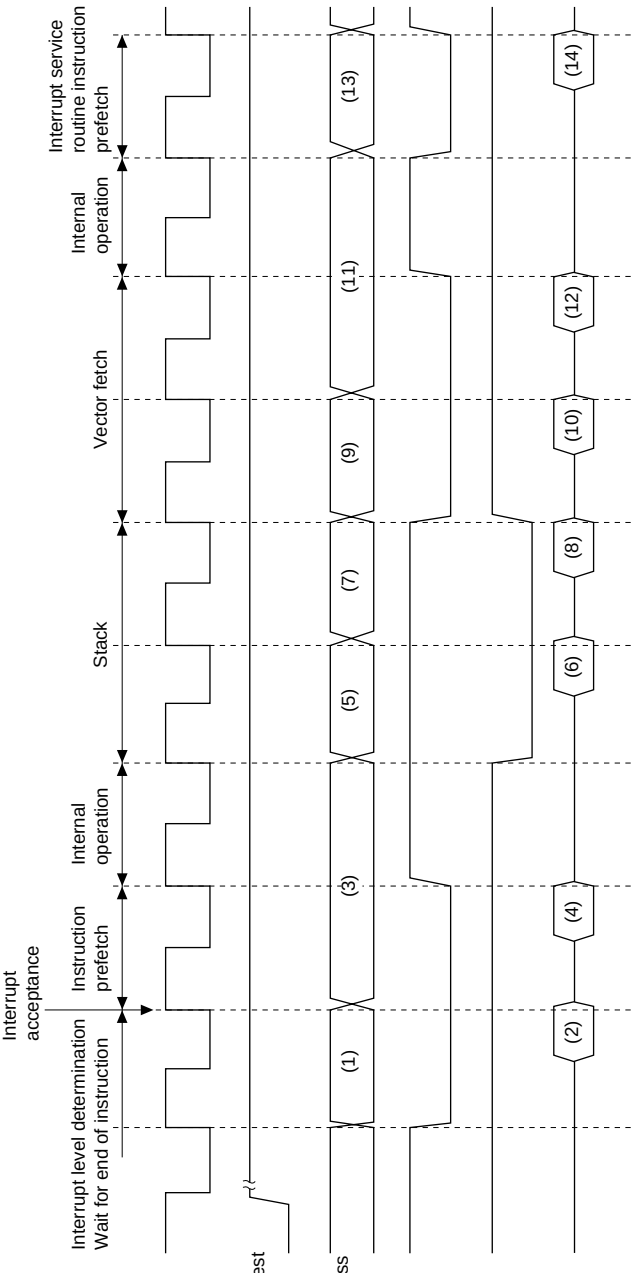


Figure 3.6 Flowchart of Procedure Up to Interrupt Acceptance in Interrupt Control Mode 2

3.5.4 Interrupt Exception Handling Sequence

Figure 3.7 shows the interrupt exception handling sequence. The example shown is for the case where interrupt control mode 0 is set in advanced mode, and the program area and stack area are in on-chip memory.



(1) Instruction prefetch address (not executed; saved PC contents (return address))
(2), (4) Instruction code (not executed)
(3) Instruction prefetch address (not executed)
(5) SP – 2
(7) SP – 4
(6), (8) Saved PC and saved CCR
(9), (11) Vector address
(10), (12) Interrupt service routine start address (vector address contents)
(13) Interrupt service routine start address ((13) = (10), (12))
(14) First instruction of interrupt service routine

Figure 3.7 Interrupt Exception Handling

3.5.5 Interrupt Response Times

The H8S/2678 Series is capable of fast word access to on-chip memory, and the program area is provided in on-chip ROM and the stack area in on-chip RAM, enabling high-speed processing.

Table 3.10 shows interrupt response times—the interval between generation of an interrupt request and execution of the first instruction in the interrupt service routine. The symbols used in table 3.10 are explained in table 3.11.

Table 3.10 Interrupt Response Times

		Advanced Mode	
No.	**Item**	**INTM1 = 0**	**INTM1 = 1**
1	Interrupt priority determination*[1]	3	3
2	Number of wait states until executing instruction ends*[2]	1 to 19 + 2 · S_I	1 to 19 + 2 · S_I
3	Saving PC, CCR, EXR to stack	2 · S_K	3 · S_K
4	Vector fetch	2 · S_I	2 · S_I
5	Instruction fetch*[3]	2 · S_I	2 · S_I
6	Internal processing*[4]	2	2
Total (using on-chip memory)		12 to 32	13 to 33

Notes: 1. Two states in case of internal interrupt.
2. Refers to MULXS and DIVXS instructions.
3. Prefetch after interrupt acceptance and interrupt service routine prefetch.
4. Internal processing after interrupt acceptance and internal processing after vector fetch.

Table 3.11 Number of States in Interrupt Exception Handling

	Object of Access				
		External Device			
		8-Bit Bus		16-Bit Bus	
Symbol	**Internal Memory**	**2-State Access**	**3-State Access**	**2-State Access**	**3-State Access**
Instruction fetch S_I	1	4	6 + 2m	2	3 + m
Branch address read S_J					
Stack manipulation S_K					

Legend
m: Number of wait states in an external device access

3.6 Usage Notes

3.6.1 Contention between Interrupt Generation and Disabling

When an interrupt enable bit is cleared to 0 to disable interrupts, the disabling becomes effective after execution of the instruction.

In other words, when an interrupt enable bit is cleared to 0 by an instruction such as BCLR or MOV, if an interrupt is generated during execution of the instruction, the interrupt concerned will still be enabled on completion of the instruction, and so interrupt exception handling for that interrupt will be executed on completion of the instruction. However, if there is an interrupt request of higher priority than that interrupt, interrupt exception handling will be executed for the higher-priority interrupt, and the lower-priority interrupt will be ignored.

The same also applies when an interrupt source flag is cleared to 0.

Figure 3.8 shows an example in which the TGIEA bit in the TPU's TIER0 register is cleared to 0.

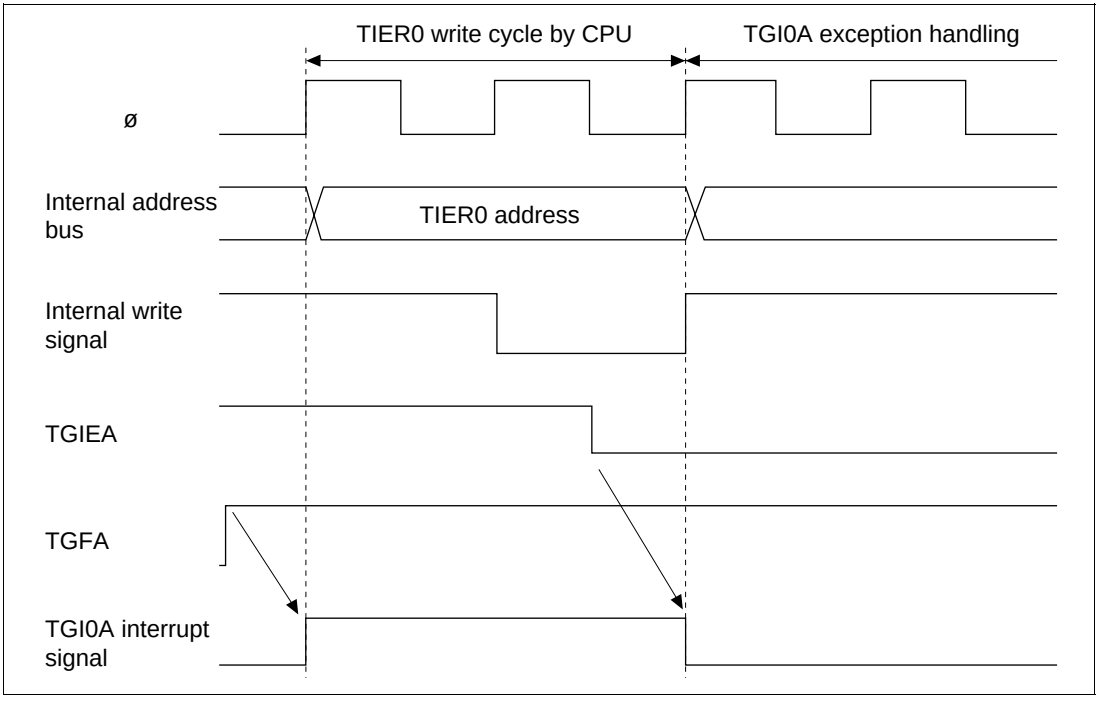


Figure 3.8 Contention between Interrupt Generation and Disabling

The above contention will not occur if an enable bit or interrupt source flag is cleared to 0 while the interrupt is masked.

3.6.2 Instructions that Disable Interrupts

Instructions that disable interrupts are LDC, ANDC, ORC, and XORC. After any of these instructions is executed, all interrupts except NMI are disabled and the next instruction is always executed.

When the I bit is set by one of these instructions, the new value is valid two states after instruction execution is completed.

3.6.3 Periods when Interrupts are Disabled

There are periods during which interrupt acceptance by the interrupt controller is disabled.

The interrupt controller disables interrupt acceptance for a 3-state period after the CPU has updated the mask level with an LDC, ANDC, ORC, or XORC instruction.

3.6.4 Interrupts during Execution of EEPMOV Instruction

The EEPMOV.B instruction and EEPMOV.W instruction differ in their reaction to interrupt requests.

With the EEPMOV.B instruction, an interrupt request (including NMI) issued during the transfer is not accepted until the transfer is completed.

With the EEPMOV.W instruction, if an interrupt request is issued during the transfer, interrupt exception handling starts at a break in the transfer cycle. The PC value saved on the stack in this case is the address of the next instruction.

The following coding should be used to allow for interrupts generated during execution of an EEPMOV.W instruction.

```
L1:    EEPMOV.W
MOV.W  R4,R4
BNE    L1
```

3.7 DTC and DMAC Activation by Interrupt

3.7.1 Overview

The DTC and DMAC can be activated by an interrupt. In this case, the following options are available. Some models do not have an on-chip DMAC; see the reference manual for the relevant model for details.

1. Interrupt request to CPU
2. Activation request to DTC
3. Activation request to DMAC
4. Selection of a number of the above

For details of interrupt requests that can be used to activate the DTC or DMAC, see section 6, Data Transfer Controller, and section 5, DMA Controller, in the H8S/2678 Series Hardware Manual.

3.7.2 Block Diagram

Figure 3.9 shows a block diagram of the DTC, DMAC, and interrupt controller.

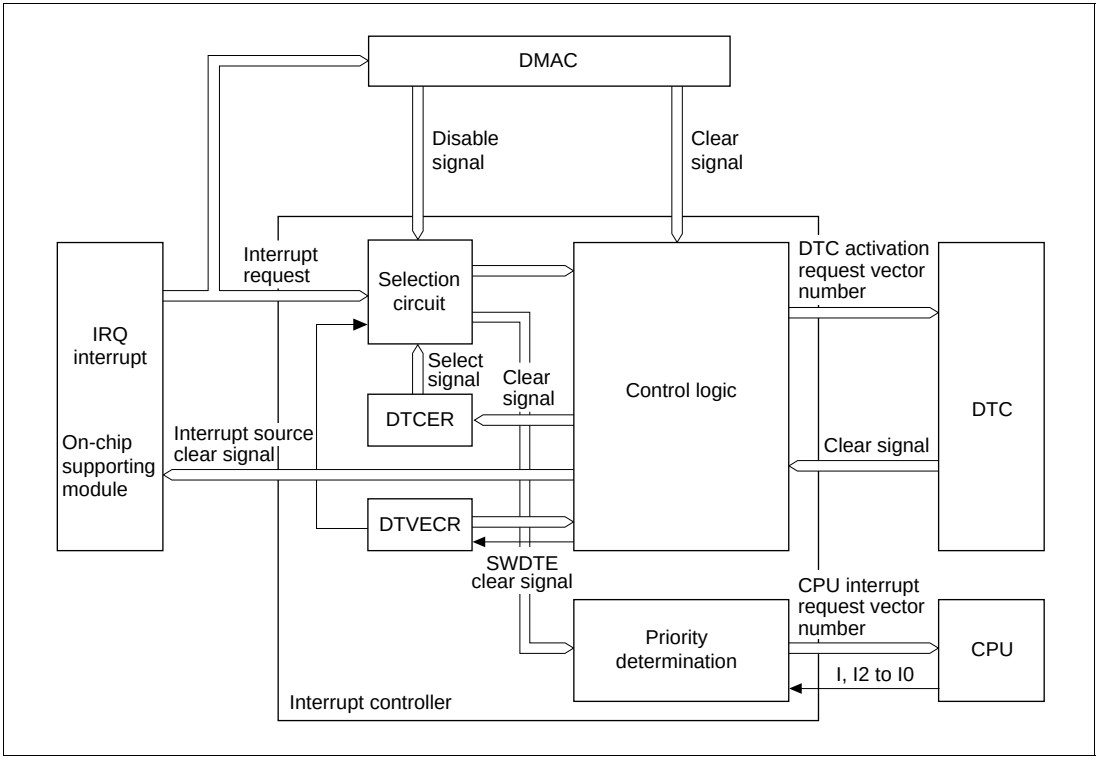


Figure 3.9 Interrupt Control for DTC and DMAC

3.7.3 Operation

The interrupt controller has three main functions in DTC and DMAC control.

Selection of Interrupt Source: With the DMAC, the activation source is input directly to each channel. The activation source for each DMAC channel is selected with bits DTF3 to DTF0 in DMACR. The selected activation source can be managed by the DMAC or selected with the DTA bit in DMABCR. When the DTA bit is set to 1, the interrupt source constituting that DMAC activation source does not function as a DTC activation source or CPU interrupt source.

For interrupt sources other than interrupts managed by the DMAC, it is possible to select DTC activation request or CPU interrupt request with the DTCE bit of DTCERA to DTCERH in the DTC.

The DISEL bit in the DTC's MRB register can be used to specify clearing of the DTCE bit to 0 and issuance of an interrupt request to the CPU after a DTC data transfer.

When the DTC has performed the specified number of data transfers and the transfer counter value is 0, following the DTC data transfer the DTCE bit is cleared to 0 and an interrupt request is sent to the CPU.

Determination of Priority: The DTC activation source is selected in accordance with the default priority order, and is not affected by mask or priority levels. Priorities are shown in table 3.12.

With the DMAC, the activation source is input directly to each channel.

Operation Order: If the same interrupt is selected as a DTC activation source and a CPU interrupt source, the DTC data transfer is performed first, followed by CPU interrupt exception handling.

If the same interrupt is selected as a DMAC activation source and a DTC activation source or CPU interrupt source, operations are performed for them independently according to their respective operating statuses and bus mastership priorities.

Table 3.13 summarizes interrupt source selection and interrupt source clearance control according to the settings of the DTA bit of DMABCR in the DMAC, the DTCE bit of DTCERA to DTCERH in the DTC, and the DISEL bit of MRB in the DTC.

Table 3.12 Interrupt Sources, DTC Vector Addresses, and Corresponding DTCE Bits

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address Advanced Mode	DTCE*	Priority
Write to DTVECR	Software	DTVECR	H'0400+ (DTVECR[6:0]<<1)	—	High
IRQ0	External pin	16	H'0420	DTCEA7	
IRQ1		17	H'0422	DTCEA6	
IRQ2		18	H'0424	DTCEA5	
IRQ3		19	H'0426	DTCEA4	
IRQ4		20	H'0428	DTCEA3	
IRQ5		21	H'042A	DTCEA2	
IRQ6		22	H'042C	DTCEA1	
IRQ7		23	H'042E	DTCEA0	
IRQ8		24	H'0430	DTCEB7	
IRQ9		25	H'0432	DTCEB6	
IRQ10		26	H'0434	DTCEB5	
IRQ11		27	H'0436	DTCEB4	
IRQ12		28	H'0438	DTCEB3	
IRQ13		29	H'043A	DTCEB2	
IRQ14		30	H'043C	DTCEB1	
IRQ15		31	H'043E	DTCEB0	
ADI (A/D conversion end)	A/D	38	H'044C	DTCEC6	
TGI0A (TGR0A compare match/input capture)	TPU channel 0	40	H'0450	DTCEC5	
TGI0B (TGR0B compare match/input capture)		41	H'0452	DTCEC4	
TGI0C (TGR0C compare match/input capture)		42	H'0454	DTCEC3	
TGI0D (TGR0D compare match/input capture)		43	H'0456	DTCEC2	
TGI1A (TGR1A compare match/input capture)	TPU channel 1	48	H'0460	DTCEC1	
TGI1B (TGR1B compare match/input capture)		49	H'0462	DTCEC0	
TGI2A (TGR2A compare match/input capture)	TPU channel 2	52	H'0468	DTCED7	
TGI2B (TGR2B compare match/input capture)		53	H'046A	DTCED6	Low

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address Advanced Mode	DTCE*	Priority
TGI3A (TGR3A compare match/input capture)	TPU channel 3	56	H'0470	DTCED5	High
TGI3B (TGR3B compare match/input capture)		57	H'0472	DTCED4	
TGI3C (TGR3C compare match/input capture)		58	H'0474	DTCED3	
TGI3D (TGR3D compare match/input capture)		59	H'0476	DTCED2	
TGI4A (TGR4A compare match/input capture)	TPU channel 4	64	H'0480	DTCED1	
TGI4B (TGR4B compare match/input capture)		65	H'0482	DTCED0	
TGI5A (TGR5A compare match/input capture)	TPU channel 5	68	H'0488	DTCEE7	
TGI5B (TGR5B compare match/input capture)		69	H'048A	DTCEE6	
CMI0A (compare match A)	8-bit timer channel 0	72	H'0490	DTCEE3	
CMI0B (compare match B)		73	H'0492	DTCEE2	
CMI1A (compare match A)	8-bit timer channel 1	76	H'0498	DTCEE1	
CMI1B (compare match B)		77	H'049A	DTCEE0	
DMTEND0A (channel 0/channel 0A transfer end)	DMAC	80	H'04A0	DTCEF7	
DMTEND0B (channel 0B transfer end)		81	H'04A2	DTCEF6	
DMTEND1A (channel 1/channel 1A transfer end)		82	H'04A4	DTCEF5	
DMTEND1B (channel 1B transfer end)		83	H'04A6	DTCEF4	
RXI0 (receive completed 0)	SCI channel 0	89	H'04B2	DTCEF3	
TXI0 (transmit data empty 0)		90	H'04B4	DTCEF2	
RXI1 (receive completed 1)	SCI channel 1	93	H'04BA	DTCEF1	
TXI1 (transmit data empty 1)		94	H'04BC	DTCEF0	
RXI2 (receive completed 2)	SCI channel 2	97	H'04C2	DTCEG7	
TXI2 (transmit data empty 2)		98	H'04C4	DTCEG6	Low

Note: * DTCE bits with no corresponding interrupt are reserved, and should be written with 0.
When clearing the software standby state or all-module-clocks-stop mode with an interrupt, write 0 to the corresponding DTCE bit.

Table 3.13 Interrupt Source Selection and Clearing Control

Settings			Interrupt Source Selection/Clearing Control		
DMAC	**DTC**				
DTA	**DTCE**	**DISEL**	**DMAC**	**DTC**	**CPU**
0	0	*	○	X	◎
	1	0	○	◎	X
		1	○	○	◎
1	*	*	◎	X	X

Legend

◎: The relevant interrupt is used. Interrupt source clearing is performed.
(The CPU should clear the source flag in the interrupt service routine.)

○: The relevant interrupt is used. The interrupt source is not cleared.

X : The relevant bit cannot be used.

* : Don't care

Usage Note: SCI and A/D converter interrupt sources are cleared when the DMAC or DTC reads or writes to the prescribed register, and are not dependent on the DTA and DISEL bits.

Section 4 Bus Controller

4.1 Overview

The H8S/2678 Series has an on-chip bus controller (BSC) that manages the external address space divided into eight areas. The bus specifications, such as bus width and number of access states, can be set independently for each area, enabling multiple memories and external I/O devices to be connected easily.

The bus controller also has a bus arbitration function, and controls the operation of the internal bus masters—the CPU, DMA controller (DMAC), data transfer controller (DTC), and external bus transfer DMAC (EXDMAC).

4.1.1 Features

The features of the bus controller are listed below.

- Manages external address space in area units
  - Manages the external space as eight areas of 2 Mbytes
  - Bus specifications can be set independently for each area
  - 8-bit access or 16-bit access can be selected for each area
  - DRAM and burst ROM interfaces can be set
- Basic bus interface
  - Chip select signals ($\overline{CS0}$ to $\overline{CS7}$) can be output for areas 0 to 7
  - 2-state access or 3-state access can be selected for each area
  - Program wait states can be inserted for each area
  - $\overline{CS}$ assertion period extension states can be inserted for each area
- DRAM interface
  - DRAM interface can be set for areas 2 to 5
  - Row address/column address multiplexed output (8/9/10/11 bits)
  - 2-CAS access method for byte control
  - Burst operation using fast page mode
  - T_P cycle insertion to secure RAS precharging time
  - Selection of CAS-before-RAS (CBR) refreshing or self-refreshing
  - $\overline{OE}$ signal can be output
  - Continuous DRAM space can be designated for areas 2 to 5
- Burst ROM interface
  - Burst ROM interface can be set for area 0 and area 1
  - Area 0 and area 1 burst ROM interfaces can be set independently

- Idle cycle insertion
  - — An idle cycle can be inserted in case of external read cycles in different areas
  - — An idle cycle can be inserted in case of an external write cycle immediately after an external read cycle
- Write buffer function
  - — External write cycle and internal access can be executed in parallel
  - — DMAC single address mode and internal access can be executed in parallel
- Bus arbitration function
  - — Includes a bus arbiter that arbitrates bus mastership between the CPU, DMAC, DTC, and EXDMAC
- Other features
  - — Refresh counter (refresh timer) can be used as an interval timer
  - — External bus release function
  - — EXDMAC external bus transfer and internal access can be executed in parallel

4.1.2 Block Diagram

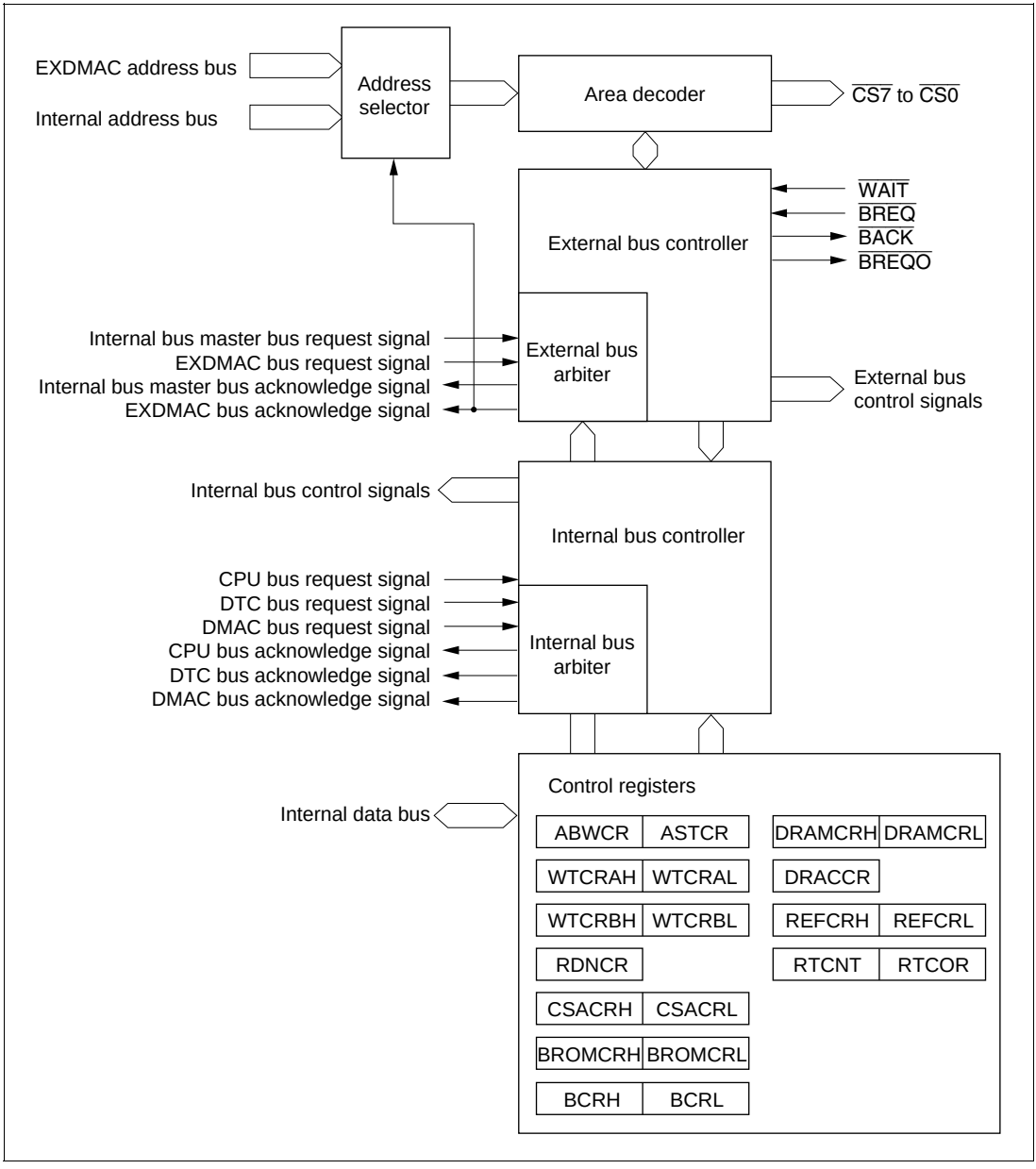


Figure 4.1 Block Diagram of Bus Controller

4.1.3 Pin Configuration

Table 4.1 summarizes the pins of the bus controller.

Table 4.1 Bus Controller Pins

Name	Abbreviation	I/O	Function
Address strobe	$\overline{AS}$	Output	Strobe signal indicating that address output on address bus is enabled during access to basic bus interface space.
Read	$\overline{RD}$	Output	Strobe signal indicating that basic bus interface space is being read.
High write/write enable	$\overline{HWR}$	Output	Strobe signal indicating that basic bus interface space is being written to, and upper half (D15 to D8) of data bus is enabled. DRAM interface space write enable signal.
Low write	$\overline{LWR}$	Output	Strobe signal indicating that basic bus interface space is being written to, and lower half (D7 to D0) of data bus is enabled.
Chip select 0	$\overline{CS0}$	Output	Strobe signal indicating that area 0 is selected.
Chip select 1	$\overline{CS1}$	Output	Strobe signal indicating that area 1 is selected.
Chip select 2/row address strobe 2	$\overline{CS2}$	Output	Strobe signal indicating that area 2 is selected. DRAM row address strobe signal when area 2 is DRAM interface space or areas 2 to 5 are continuous DRAM interface space.
Chip select 3/row address strobe 3	$\overline{CS3}$	Output	Strobe signal indicating that area 3 is selected. DRAM row address strobe signal when area 3 is DRAM interface space.
Chip select 4/row address strobe 4	$\overline{CS4}$	Output	Strobe signal indicating that area 4 is selected. DRAM row address strobe signal when area 4 is DRAM interface space.

Name	Abbre-viation	I/O	Function
Chip select 5/row address strobe 5	$\overline{CS5}$	Output	Strobe signal indicating that area 5 is selected. DRAM row address strobe signal when area 5 is DRAM interface space.
Chip select 6	$\overline{CS6}$	Output	Strobe signal indicating that area 6 is selected.
Chip select 7	$\overline{CS7}$	Output	Strobe signal indicating that area 7 is selected.
Upper column address strobe	$\overline{UCAS}$	Output	16-bit DRAM interface space upper column address strobe signal. 8-bit DRAM interface space column address strobe signal.
Lower column strobe	$\overline{LCAS}$	Output	16-bit DRAM interface space lower column address strobe signal.
Output enable	$\overline{OE}$	Output	DRAM interface space output enable signal.
Wait	$\overline{WAIT}$	Input	Wait request signal when accessing external space.
Bus request	$\overline{BREQ}$	Input	Request signal for release of bus to external device.
Bus request acknowledge	$\overline{BACK}$	Output	Acknowledge signal indicating that bus has been released.
Bus request output	$\overline{BREQO}$	Output	External bus request signal used when internal bus master accesses external space when external bus is released.
Data transfer acknowledge 1 (DMAC)	$\overline{DACK1}$	Output	Data transfer acknowledge signal for single address transfer by DMAC channel 1.
Data transfer acknowledge 0 (DMAC)	$\overline{DACK0}$	Output	Data transfer acknowledge signal for single address transfer by DMAC channel 0.
Data transfer acknowledge 3 (EXDMAC)	$\overline{EDACK3}$	Output	Data transfer acknowledge signal for single address transfer by EXDMAC channel 3.
Data transfer acknowledge 2 (EXDMAC)	$\overline{EDACK2}$	Output	Data transfer acknowledge signal for single address transfer by EXDMAC channel 2.
Data transfer acknowledge 1 (EXDMAC)	$\overline{EDACK1}$	Output	Data transfer acknowledge signal for single address transfer by EXDMAC channel 1.
Data transfer acknowledge 0 (EXDMAC)	$\overline{EDACK0}$	Output	Data transfer acknowledge signal for single address transfer by EXDMAC channel 0.

4.1.4 Register Configuration

Table 4.2 summarizes the registers of the bus controller.

Table 4.2 Bus Controller Registers

Name	Abbreviation	R/W	Initial Value Reset	Address*[1]	Register Size (Bits)
Bus width control register	ABWCR	R/W	H'FF/H'00*[2]	H'FEC0	8
Access state control register	ASTCR	R/W	H'FF	H'FEC1	8
Wait control register A	WTCRA	R/W	H'7777	H'FEC2	16
Wait control register B	WTCRB	R/W	H'7777	H'FEC4	16
Read strobe timing control register	RDNCR	R/W	H'00	H'FEC6	8
Chip select assertion period control registers	CSACRH	R/W	H'00	H'FEC8	8
	CSACRL	R/W	H'00	H'FEC9	8
Burst ROM interface control registers	BROMCRH	R/W	H'00	H'FECA	8
	BROMCRL	R/W	H'00	H'FECB	8
Bus control register	BCR	R/W	H'1C00	H'FECC	16
DRAM control register	DRAMCR	R/W	H'0000	H'FED0	16
DRAM access control register	DRACCR	R/W	H'00	H'FED2	8
Refresh control register	REFCR	R/W	H'0000	H'FED4	16
Refresh timer counter	RTCNT	R/W	H'00	H'FED6	8
Refresh time constant register	RTCOR	R/W	H'FF	H'FED7	8

Notes: 1. Lower 16 bits of the address.
2. Determined by the MCU operating mode.

4.2 Register Descriptions

4.2.1 Bus Width Control Register (ABWCR)

Bit	7	6	5	4	3	2	1	0
	ABW7	ABW6	ABW5	ABW4	ABW3	ABW2	ABW1	ABW0
Modes 2, 4, 6								
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Modes 1, 5, 7								
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ABWCR is an 8-bit readable/writable register that designates each area as either 8-bit access space or 16-bit access space.

ABWCR sets the data bus width for the external memory space. The bus width for on-chip memory and internal I/O registers is fixed regardless of the settings in ABWCR.

After a reset and in hardware standby mode, ABWCR is initialized to H'FF in modes 2, 4, and 6, and to H'00 in modes 1, 5, and 7. It is not initialized in software standby mode.

Bits 7 to 0—Area 7 to 0 Bus Width Control (ABW7 to ABW0): These bits select whether the corresponding area is to be designated as 8-bit access space or 16-bit access space.

Bit n ABWn	Description
0	Area n is designated as 16-bit access space
1	Area n is designated as 8-bit access space

(n = 7 to 0)

4.2.2 Access State Control Register (ASTCR)

Bit	7	6	5	4	3	2	1	0
	AST7	AST6	AST5	AST4	AST3	AST2	AST1	AST0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASTCR is an 8-bit readable/writable register that designates each area as either 2-state access space or 3-state access space.

ASTCR sets the number of access states for the external memory space. The number of access states for on-chip memory and internal I/O registers is fixed regardless of the settings in ASTCR.

ASTCR is initialized to H'FF by a reset and in hardware standby mode. It is not initialized in software standby mode.

Bits 7 to 0—Area 7 to 0 Access State Control (AST7 to AST0): These bits select whether the corresponding area is to be designated as 2-state access space or 3-state access space.

Wait state insertion is enabled or disabled at the same time.

Bit n ASTn	Description	
0	Area n is designated as 2-state access space Wait state insertion in area n external space access is disabled	
1	Area n is designated as 3-state access space Wait state insertion in area n external space access is enabled	(Initial value)

(n = 7 to 0)

4.2.3 Wait Control Registers A and B (WTCRA, WTCRB)

WTCRA and WTCRB are 16-bit readable/writable registers that select the number of program wait states for each area.

Program waits are not inserted in on-chip memory or internal I/O register access.

WTCRA and WTCRB are initialized to H'7777 by a reset and in hardware standby mode. They are not initialized in software standby mode.

WTCRA

Bit	15	14	13	12	11	10	9	8
	—	W72	W71	W70	—	W62	W61	W60
Initial value	0	1	1	1	0	1	1	1
Read/Write	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	—	W52	W51	W50	—	W42	W41	W40
Initial value	0	1	1	1	0	1	1	1
Read/Write	R	R/W	R/W	R/W	R	R/W	R/W	R/W

WTCRB

Bit	15	14	13	12	11	10	9	8
	—	W32	W31	W30	—	W22	W21	W20
Initial value	0	1	1	1	0	1	1	1
Read/Write	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	—	W12	W11	W10	—	W02	W01	W00
Initial value	0	1	1	1	0	1	1	1
Read/Write	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bits 15, 11, 7, and 3—Reserved: These bits are always read as 0 and cannot be modified.

Bits 14 to 12, 10 to 8, 6 to 4, 2 to 0—Wait Control (Wn2, Wn1, Wn0): These bits select the number of program wait states for areas designated as 3-state access space in ASTCR.

Wn2	Wn1	Wn0	Description
0	0	0	Program wait not inserted in area n external access
		1	1 program wait state inserted in area n external access
	1	0	2 program wait states inserted in area n external access
		1	3 program wait states inserted in area n external access
1	0	0	4 program wait states inserted in area n external access
		1	5 program wait states inserted in area n external access
	1	0	6 program wait states inserted in area n external access
		1	7 program wait states inserted in area n external access

(n = 7 to 0)

4.2.4 Read Strobe Timing Control Register (RDNCR)

Bit	7	6	5	4	3	2	1	0
	RDN7	RDN6	RDN5	RDN4	RDN3	RDN2	RDN1	RDN0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

RDNCR is an 8-bit readable/writable register that selects the read strobe ($\overline{RD}$) negation timing when an area is designated as basic bus interface space.

RDNCR is initialized to H'00 by a reset and in hardware standby mode. It is not initialized in software standby mode.

Bits 7 to 0—Read Strobe Timing Control (RDNn): As shown in figure 4.2, the read strobe for an area for which the RDNn bit is set to 1 is negated one half-state earlier than that for an area for which the RDNn bit is cleared to 0. The read data setup and hold time specifications are also one half-state earlier.

The read strobe is negated one half-state earlier regardless of 2-state or 3-state access designation, or the number of program waits.

Bits 7 to 0 RDNn	Description
0	In an area n read access, the $\overline{RD}$ strobe is negated at the end of the read cycle (Initial value)
1	In an area n read access, the $\overline{RD}$ strobe is negated one half-state before the end of the read cycle

(n = 7 to 0)

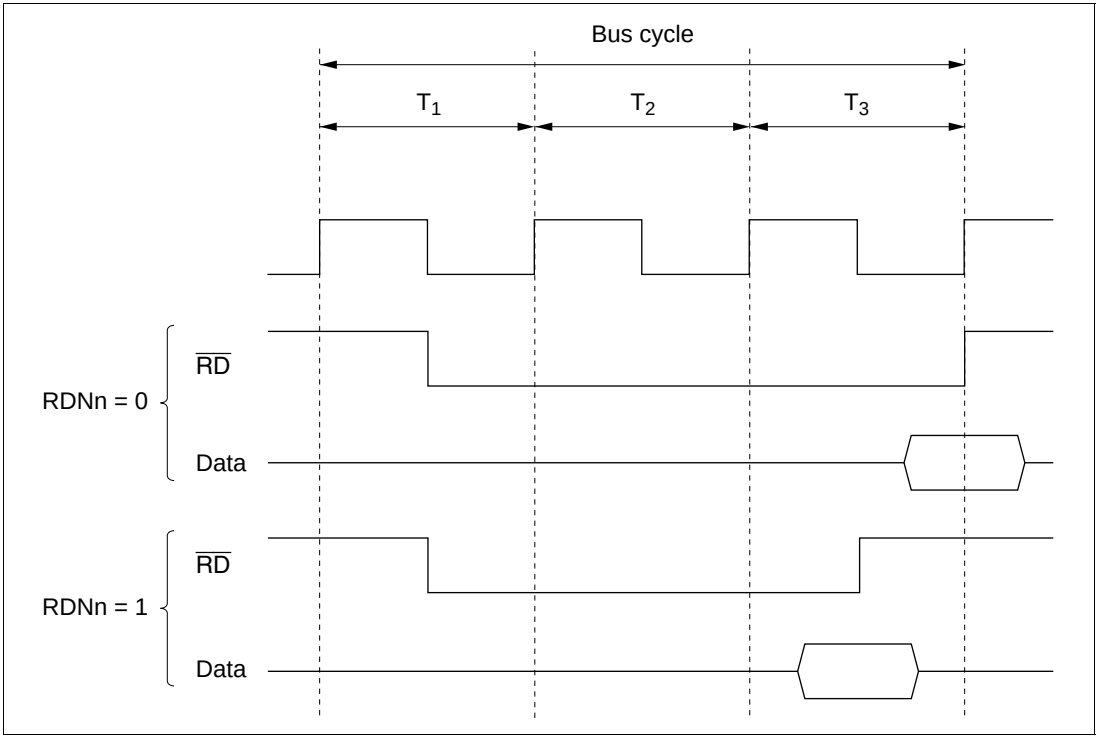


Figure 4.2 Read Strobe Negation Timing (Example of 3-State Access Space)

4.2.5 $\overline{\text{CS}}$ Assertion Period Control Registers (CSACRH, CSACRL)

CSACRH

Bit	7	6	5	4	3	2	1	0
	CSXH7	CSXH6	CSXH5	CSXH4	CSXH3	CSXH2	CSXH1	CSXH0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

CSACRL

Bit	7	6	5	4	3	2	1	0
	CSXT7	CSXT6	CSXT5	CSXT4	CSXT3	CSXT2	CSXT1	CSXT0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

CSACRH and CSACRL are 8-bit readable/writable registers that specify whether or not the assertion period of the basic bus interface chip select signals ($\overline{\text{CSn}}$) and address signals is to be extended.

Extending the assertion period of the $\overline{\text{CSn}}$ and address signals allows flexible interfacing to external I/O devices.

CSACRH and CSACRL are initialized to H'0000 by a reset and in hardware standby mode. They are not initialized in software standby mode.

CSACRH

Bits 7 to 0—$\overline{CS}$ and Address Signal Assertion Period Control 1 (CSXH7 to CSXH0): These bits specify whether or not the T_h cycle shown in figure 4.3 is to be inserted. When an area for which the CSXHn bit is set to 1 is accessed, a T_h state, in which only the $\overline{CSn}$ and address signals are asserted, is inserted before the normal access cycle.

A one-state T_h cycle is inserted regardless of 2-state or 3-state access designation, or the number of program waits.

Bit n CSXHn	Description
0	In area n basic bus interface access, the $\overline{CSn}$ and address assertion period (T_h) is not extended (Initial value)
1	In area n basic bus interface access, the $\overline{CSn}$ and address assertion period (T_h) is extended

(n = 7 to 0)

CSACRL

Bits 7 to 0—$\overline{CS}$ and Address Signal Assertion Period Control 2 (CSXT7 to CSXT0): These bits specify whether or not the T_t cycle shown in figure 4.3 is to be inserted. When an area for which the CSXTn bit is set to 1 is accessed, a T_t state, in which only the $\overline{CSn}$ and address signals are asserted, is inserted after the normal access cycle.

A one-state T_t cycle is inserted regardless of 2-state or 3-state access designation, or the number of program waits.

Bit n CSXTn	Description
0	In area n basic bus interface access, the $\overline{CSn}$ and address assertion period (T_t) is not extended (Initial value)
1	In area n basic bus interface access, the $\overline{CSn}$ and address assertion period (T_t) is extended

(n = 7 to 0)

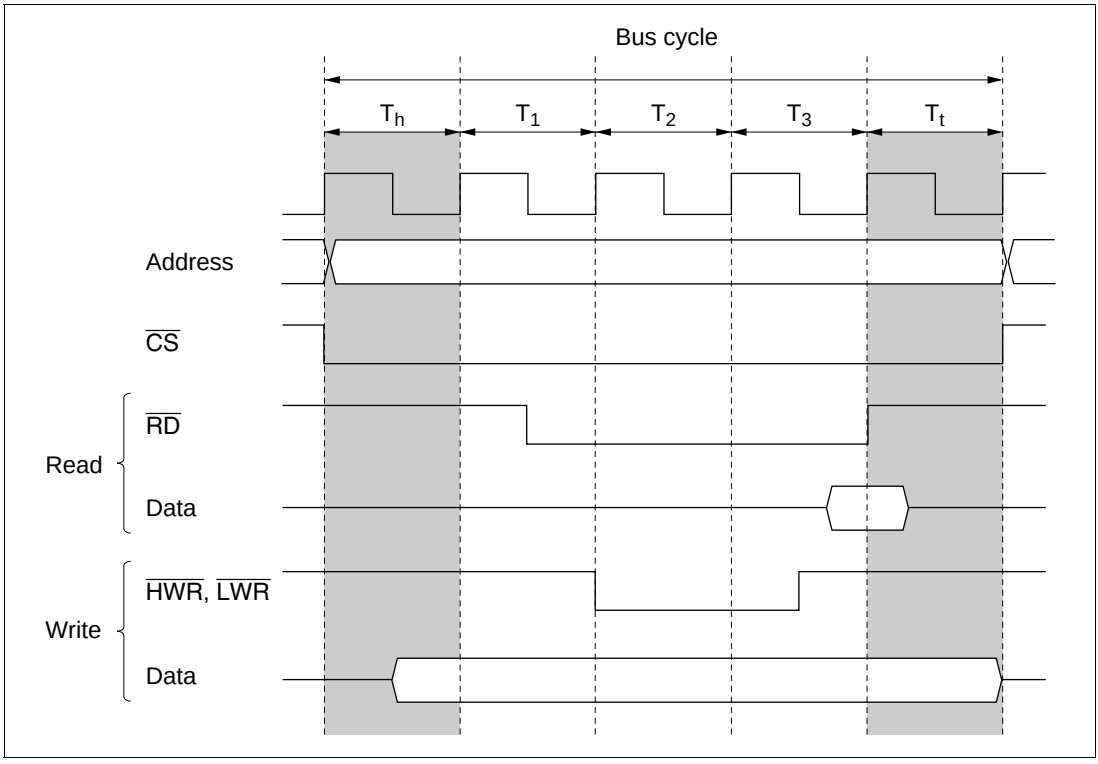


Figure 4.3 $\overline{CS}$ and Address Assertion Period Extension (Example of 3-State Access Space and RDWn = 0)

4.2.6 Area 0 Burst ROM I/F Control Register (BROMCRH)
Area 1 Burst ROM I/F Control Register (BROMCRL)

BROMCRH

Bit	7	6	5	4	3	2	1	0
	BSRM0	BSTS02	BSTS01	BSTS00	—	—	BSWD01	BSWD00
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BROMCRL

Bit	7	6	5	4	3	2	1	0
	BSRM1	BSTS12	BSTS11	BSTS10	—	—	BSWD11	BSWD10
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BROMCRH and BROMCRL are 8-bit readable/writable registers used to make burst ROM interface settings.

Area 1 and area 0 burst ROM interface settings can be made independently in BROMCRH and BROMCRL, respectively.

BROMCRH and BROMCRL are initialized to H'0000 by a reset and in hardware standby mode. They are not initialized in software standby mode.

Bit 7—Burst ROM Interface Select (BSRMn): Selects the burst ROM interface for area 0 or area 1.

Bit 7 BSRMn	Description	
0	Area n is basic bus interface space	(Initial value)
1	Area n is burst ROM interface space	

(n = 1 or 0)

Bits 6 to 4—Burst Cycle Select (BSTSn2, BSTSn1, BSTSn0): These bits select the number of burst cycle states.

Bit 6 BSTSn2	Bit 5 BSTSn1	Bit 4 BSTSn0	Description	
0	0	0	Area n burst cycle comprises 1 state	(Initial value)
		1	Area n burst cycle comprises 2 states	
	1	0	Area n burst cycle comprises 3 states	
		1	Area n burst cycle comprises 4 states	
1	0	0	Area n burst cycle comprises 5 states	
		1	Area n burst cycle comprises 6 states	
	1	0	Area n burst cycle comprises 7 states	
		1	Area n burst cycle comprises 8 states	

(n = 1 or 0)

Bits 3 and 2—Reserved: These are readable/writable bits, but the write value should always be 0.

Bits 1 and 0—Burst Word Length Select (BSWDn1, BSWDn0): These bits select the number of words that can be burst-accessed on the burst ROM interface.

Bit 1 BSWDn1	Bit 0 BSWDn0	Description	
0	0	Maximum 4 words in area n burst access	(Initial value)
	1	Maximum 8 words in area n burst access	
1	0	Maximum 16 words in area n burst access	
	1	Maximum 32 words in area n burst access	

(n = 1 or 0)

4.2.7 Bus Control Register (BCR)

Bit	15	14	13	12	11	10	9	8
	BRLE	BREQOE	—	IDLC	ICIS1	ICIS0	WDBE	WAITE
Initial value	0	0	0	1	1	1	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BCR is a 16-bit readable/writable register used for idle cycle settings, selection of the external bus released state protocol, enabling or disabling of the write data buffer function, and enabling or disabling of WAIT pin input.

BCR is initialized to H'1C00 by a reset and in hardware standby mode. It is not initialized in software standby mode.

Bit 15—External Bus Release Enable (BRLE): Enables or disables external bus release by means of the $\overline{\text{BREQ}}$ pin.

Bit 15 BRLE	Description	
0	External bus release disabled	
	$\overline{\text{BREQ}}$, $\overline{\text{BACK}}$, and $\overline{\text{BREQO}}$ pins can be used as I/O ports	(Initial value)
1	External bus release enabled	

Bit 14—$\overline{\text{BREQO}}$ Pin Enable (BREQOE): Selects whether or not to output a signal that requests the external bus master to drop the bus request signal ($\overline{\text{BREQ}}$) in the external bus released state,

when an internal bus master performs an external space access, or when a refresh request is generated.

Bit 14 BREQOE	Description
0	$\overline{\text{BREQO}}$ output disabled
	$\overline{\text{BREQO}}$ pin can be used as I/O port (Initial value)
1	$\overline{\text{BREQO}}$ output enabled

Bit 13—Reserved: This is a readable/writable bit, but the write value should always be 0.

Bit 12—Idle Cycle State Number Select (IDLC): Selects the number of states in the idle cycle set by ICIS1 and ICIS0.

Bit 12 IDLC	Description
0	Idle cycle comprises 1 state
1	Idle cycle comprises 2 states (Initial value)

Bit 11—Idle Cycle Insert 1 (ICIS1): When consecutive external read cycles are performed in different areas, an idle cycle can be inserted between the bus cycles. When this bit is set to 1, an idle cycle is inserted in the case of consecutive external read cycles in different areas.

Bit 11 ICIS1	Description
0	Idle cycle not inserted in case of consecutive external read cycles in different areas
1	Idle cycle inserted in case of consecutive external read cycles in different areas (Initial value)

Bit 10—Idle Cycle Insert 0 (ICIS0): When an external read cycle and external write cycle are performed consecutively, an idle cycle can be inserted between the bus cycles. When this bit is set to 1, an idle cycle is inserted when an external read cycle and external write cycle are performed consecutively.

Bit 10 ICIS0	Description
0	Idle cycle not inserted when external read cycle and external write cycle are performed consecutively
1	Idle cycle inserted when external read cycle and external write cycle are performed consecutively (Initial value)

Bit 9—Write Data Buffer Enable (WDBE): Selects whether or not the write data buffer function is used for an external write cycle or DMAC single address transfer cycle.

Bit 9 WDBE	Description	
0	Write data buffer function not used	(Initial value)
1	Write data buffer function used	

Bit 8—$\overline{\text{WAIT}}$ Pin Enable (WAITE): Selects enabling or disabling of wait input by the $\overline{\text{WAIT}}$ pin.

Bit 8 WAITE	Description	
0	Wait input by $\overline{\text{WAIT}}$ pin disabled	
	$\overline{\text{WAIT}}$ pin can be used as I/O port	(Initial value)
1	Wait input by $\overline{\text{WAIT}}$ pin enabled	

Bits 7 to 0—Reserved: These are readable/writable bits, but the write value should always be 0.

4.2.8 DRAM Control Register (DRAMCR)

Bit	15	14	13	12	11	10	9	8
	OEE	RAST	—	CAST	—	RMTS2	RMTS1	RMTS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	BE	RCDM	DDS	EDDS	—	MXC2	MXC1	MXC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

DRAMCR is a 16-bit readable/writable register used to make DRAM interface settings.

DRAMCR is initialized to H'0000 by a reset and in hardware standby mode. It is not initialized in software standby mode.

Bit 15—$\overline{\text{OE}}$ Output Enable (OEE): Enables or disables output from the $\overline{\text{OE}}$ pin of the $\overline{\text{OE}}$ signal used when EDO page mode DRAM is connected. The $\overline{\text{OE}}$ signal is common to all areas designated as DRAM space.

Bit 15 OEE	Description	
0	$\overline{OE}$ signal output disabled	
	$\overline{OE}$ pin can be used as I/O port	(Initial value)
1	$\overline{OE}$ signal output enabled	

Bit 14—$\overline{RAS}$ Assertion Timing Select (RAST): Selects whether, in DRAM access, the $\overline{RAS}$ signal is asserted from the start of the T_r cycle (rising edge of ø) or from the falling edge of ø.

Figure 4.4 shows the relationship between the RAST bit setting and the $\overline{RAS}$ assertion timing.

The setting of this bit applies to all areas designated as DRAM space.

Bit 14 RAST	Description	
0	$\overline{RAS}$ is asserted from ø falling edge in T_r cycle	(Initial value)
1	$\overline{RAS}$ is asserted from start of T_r cycle	

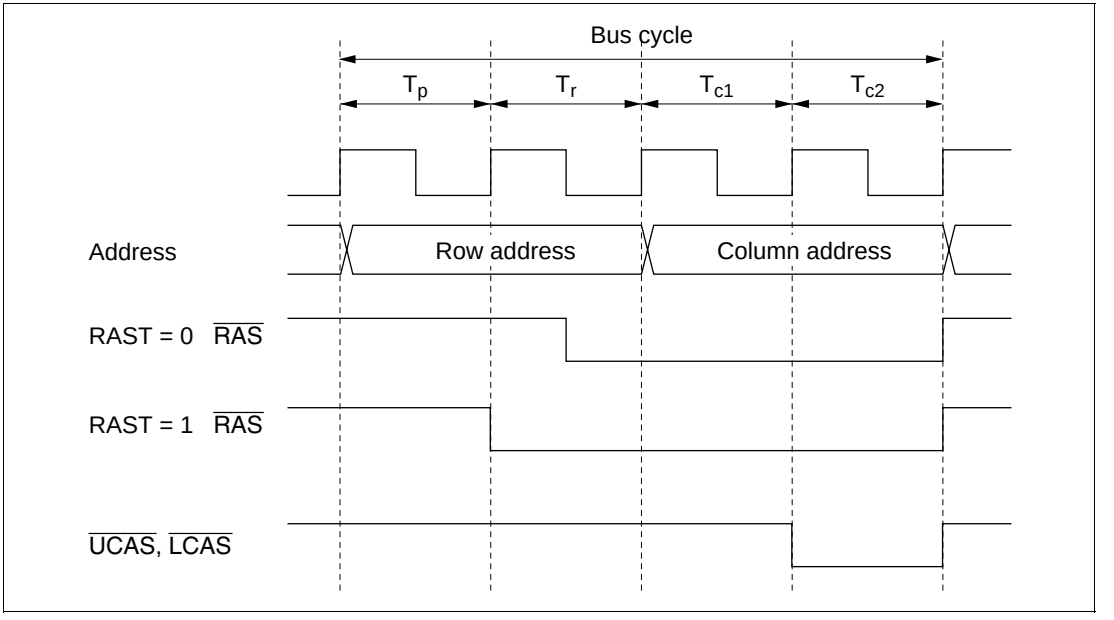


Figure 4.4 $\overline{RAS}$ Signal Assertion Timing (2-State Column Address Output Cycle, Full Access)

Bit 13—Reserved: This is a readable/writable bit, but the write value should always be 0.

Bit 12—Column Address Output Cycle Number Select (CAST): Selects whether the column address output cycle in DRAM access comprises 3 states or 2 states.

The setting of this bit applies to all areas designated as DRAM space.

Bit 12 CAST	Description	
0	Column address output cycle comprises 2 states	(Initial value)
1	Column address output cycle comprises 3 states	

Bit 11—Reserved: This is a readable/writable bit, but the write value should always be 0.

Bits 10 to 8—DRAM Space Select (RMTS2 to RMTS0): These bits designate DRAM space for areas 2 to 5.

When continuous DRAM space is set, it is possible to connect large-capacity DRAM exceeding 2 Mbytes per area. In this case, the $\overline{RAS}$ signal is output from the $\overline{RAS2}$ pin.

Bit 10 RMTS2	Bit 9 RMTS 1	Bit 8 RMTS 0	Description Area 5	Area 4	Area 3	Area 2
0	0	0	Normal space	Normal space	Normal space	Normal space
		1	Normal space	Normal space	Normal space	DRAM space
	1	0	Normal space	Normal space	DRAM space	DRAM space
		1	DRAM space	DRAM space	DRAM space	DRAM space
1	0	*	Reserved (setting prohibited)	Reserved (setting prohibited)	Reserved (setting prohibited)	Reserved (setting prohibited)
	1	0				
		1	Continuous DRAM space	Continuous DRAM space	Continuous DRAM space	Continuous DRAM space

*: Don't care

Bit 7—Burst Access Enable (BE): Selects enabling or disabling of burst access to areas designated as DRAM space. DRAM space burst access is performed in fast page mode. When using EDO page mode DRAM, the $\overline{OE}$ signal must be connected.

Bit 7 BE	Description	
0	Full access always used for DRAM space access	(Initial value)
1	DRAM space access performed in fast page mode	

Bit 6—$\overline{\text{RAS}}$ Down Mode (RCDM): When access to DRAM space is interrupted by an access to normal bus space, an access to an internal I/O register, etc., this bit selects whether the $\overline{\text{RAS}}$ signal is held low while waiting for the next DRAM access ($\overline{\text{RAS}}$ down mode), or is driven high again ($\overline{\text{RAS}}$ up mode).

The setting of this bit is valid only when the BE bit is set to 1.

If this bit is cleared to 0 when set to 1 in the $\overline{\text{RAS}}$ down state, the $\overline{\text{RAS}}$ down state is cleared at that point, and $\overline{\text{RAS}}$ goes high.

Bit 6 RCDM	Description	
0	$\overline{\text{RAS}}$ up mode selected for DRAM space access	(Initial value)
1	$\overline{\text{RAS}}$ down mode selected for DRAM space access	

Bit 5—DMAC Single Address Transfer Option (DDS): Specifies whether full access is always performed or burst access is enabled when DMAC single address transfer is performed on the DRAM interface.

When the BE bit is cleared to 0 in DRAMCR, disabling DRAM burst access, DMAC single address transfer is performed in full access mode regardless of the setting of the DDS bit.

This bit has no effect on other bus master external accesses or DMAC dual address transfers.

Bit 5 DDS	Description	
0	Full access is always executed when DMAC single address transfer is performed in DRAM space	(Initial value)
1	Burst access is possible when DMAC single address transfer is performed in DRAM space	

Bit 4—EXDMAC Single Address Transfer Option (EDDS): Specifies whether full access is always performed or burst access is enabled when EXDMAC single address transfer is performed on the DRAM interface.

When the BE bit is cleared to 0 in DRAMCR, disabling DRAM burst access, EXDMAC single address transfer is performed in full access mode regardless of the setting of the EDDS bit.

This bit has no effect on other bus master external accesses or EXDMAC dual address transfers.

Bit 4 EDDS	Description
0	Full access is always executed when EXDMAC single address transfer is performed in DRAM space (Initial value)
1	Burst access is possible when EXDMAC single address transfer is performed in DRAM space

Bit 3—Reserved: This is a readable/writable bit, but the write value should always be 0.

Bits 2 to 0—Address Multiplex Select (MXC2 to MXC0): These bits select the size of the shift toward the lower half of the row address in row address/column address multiplexing. In burst operation on the DRAM interface, these bits also select the row address bits to be used for comparison.

Bit 2 MXC2	Bit 1 MXC1	Bit 0 MXC0	Description
0	0	0	8-bit shift (Initial value) • When 8-bit access space is designated: Row address bits A23 to A8 used for comparison • When 16-bit access space is designated: Row address bits A23 to A9 used for comparison
		1	9-bit shift • When 8-bit access space is designated: Row address bits A23 to A9 used for comparison • When 16-bit access space is designated: Row address bits A23 to A10 used for comparison
	1	0	10-bit shift • When 8-bit access space is designated: Row address bits A23 to A10 used for comparison • When 16-bit access space is designated: Row address bits A23 to A11 used for comparison
		1	11-bit shift • When 8-bit access space is designated: Row address bits A23 to A11 used for comparison • When 16-bit access space is designated: Row address bits A23 to A12 used for comparison
1	—	—	Reserved (setting prohibited)

4.2.9 DRAM Access Control Register (DRACCR)

Bit	7	6	5	4	3	2	1	0
	DRMI	—	TPC1	TPC0	—	—	RCD1	RCD0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

DRACCR is an 8-bit readable/writable register used to set the DRAM interface bus specifications.

DRACCR is initialized to H'00 by a reset and in hardware standby mode. It is not initialized in software standby mode.

Bit 7—Idle Cycle Insertion (DRMI): Selects whether or not an idle cycle is inserted when a normal access cycle follows a DRAM read cycle.

Bit 7 DRMI	Description	
0	Idle cycle not inserted after DRAM space access	(Initial value)
1	Idle cycle inserted after DRAM space access Idle cycle insertion conditions, setting of number of states, etc., comply with settings of bits ICIS1, ICIS0, and IDLC in BCR register	

Bit 6—Reserved: This is a readable/writable bit, but the write value should always be 0.

Bits 5 and 4—Precharge State Control (TPC1, TPC0): These bits select the number of states in the RAS precharge cycle in normal access and refreshing. From 1 to 4 states can be set for the precharge cycle.

Bit 5 TPC1	Bit 4 TPC0	Description	
0	0	$\overline{\text{RAS}}$ precharge cycle comprises 1 state	(Initial value)
	1	$\overline{\text{RAS}}$ precharge cycle comprises 2 states	
1	0	$\overline{\text{RAS}}$ precharge cycle comprises 3 states	
	1	$\overline{\text{RAS}}$ precharge cycle comprises 4 states	

Bits 3 and 2—Reserved: These are readable/writable bits, but the write value should always be 0.

Bits 1 and 0—RAS-CAS Wait Control (RCD1, RCD0): These bits select whether or not a wait cycle is to be inserted between the $\overline{\text{RAS}}$ assert cycle and $\overline{\text{CAS}}$ assert cycle. A 1- to 4-state wait cycle can be inserted.

Bit 1 RCD1	Bit 0 RCD0	Description
0	0	Wait cycle not inserted between $\overline{RAS}$ assert cycle and $\overline{CAS}$ assert cycle (Initial value)
	1	1-state wait cycle inserted between $\overline{RAS}$ assert cycle and $\overline{CAS}$ assert cycle
1	0	2-state wait cycle inserted between $\overline{RAS}$ assert cycle and $\overline{CAS}$ assert cycle
	1	3-state wait cycle inserted between $\overline{RAS}$ assert cycle and $\overline{CAS}$ assert cycle

4.2.10 Refresh Control Register (REFCR)

Bit	15	14	13	12	11	10	9	8
	CMF	CMIE	RCW1	RCW0	—	RTCK2	RTCK1	RTCK0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W*	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	RFSHE	CBRM	RLW1	RLW0	SLFRF	TPCS2	TPCS1	TPCS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Only 0 can be written, to clear the flag.

REFCR is a 16-bit readable/writable register that specifies DRAM interface refresh control.

REFCR is initialized to H'0000 by a reset and in hardware standby mode. It is not initialized in software standby mode.

Bit 15—Compare match Flag (CMF): Status flag that indicates a match between the values of the refresh counter (RTCNT) and the refresh time constant register (RTCOR).

Bit 15 CMF	Description
0	[Clearing conditions] • When 0 is written to CMF after reading CMF = 1 while the RFSHE bit is cleared to 0 (Initial value) • When CBR refreshing is executed while the RFSHE bit is set to 1
1	[Setting condition] When RTCOR = RTCNT

Bit 14—Compare Match Interrupt Enable (CMIE): Enables or disables interrupt requests (CMI) by the CMF flag when the CMF flag is set to 1.

This bit is valid only when refresh control is not performed (when the RFSHE bit is cleared to 0). When the RFSHE bit is set to 1 and refresh control is performed, the CMIE bit is always cleared to 0 and cannot be modified.

Bit 14 CMIE	Description
0	Interrupt request by CMF flag disabled (Initial value)
1	Interrupt request by CMF flag enabled

Bits 13 and 12—$\overline{\text{CAS}}$-$\overline{\text{RAS}}$ Wait Control (RCW1, RCW0): These bits select whether or not a wait cycle is to be inserted between the $\overline{\text{CAS}}$ assert cycle and $\overline{\text{RAS}}$ assert cycle in a DRAM refresh cycle. A 1- to 3-state wait cycle can be inserted.

Bit 13 RCW1	Bit 12 RCW0	Description
0	0	Wait state not inserted between $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ in refresh cycle (Initial value)
	1	1 wait state inserted between $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ in refresh cycle
1	0	2 wait states inserted between $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ in refresh cycle
	1	3 wait states inserted between $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ in refresh cycle

Bit 11—Reserved: This is a readable/writable bit, but the write value should always be 0.

Bits 10 to 8—Refresh Counter Clock Select (RTCK2 to RTCK0): These bits select the clock to be used to increment the refresh counter from among seven internal clocks obtained by dividing the system clock (ø).

When the input clock is selected with bits RTCK2 to RTCK0, the refresh counter begins counting up.

Bit 10 RTCK2	Bit 9 RTCK1	Bit 8 RTCK0	Description	
0	0	0	Count operation halted	(Initial value)
		1	Count on ø/2	
	1	0	Count on ø/8	
		1	Count on ø/32	
1	0	0	Count on ø/128	
		1	Count on ø/512	
	1	0	Count on ø/2048	
		1	Count on ø/4096	

Bit 7—Refresh Control (RFSHE): Selects whether or not refresh control is performed. When refresh control is not performed, the refresh timer can be used as an interval timer.

Bit 7 RFSHE	Description	
0	Refresh control is not performed	
1	Refresh control is performed	(Initial value)

Bit 6—CBR Refresh Mode (CBRM): Allows selection of CBR refreshing performed in parallel with other external accesses, or execution of CBR refreshing alone.

Bit 6 CBRM	Description	
0	External access during CAS-before-RAS refreshing is enabled	(Initial value)
1	External access during CAS-before-RAS refreshing is disabled	

Bits 5 and 4—Refresh Cycle Wait Control (RLW1, RLW0): These bits select the number of wait states to be inserted in a DRAM interface CAS-before-RAS refresh cycle. This setting applies to all areas designated as DRAM space.

Bit 5 RLW1	Bit 4 RLW0	Description	
0	0	No wait state inserted in CBR refresh	(Initial value)
	1	1 wait state inserted in CBR refresh	
1	0	2 wait states inserted in CBR refresh	
	1	3 wait states inserted in CBR refresh	

Bit 3—Self-Refresh Enable (SLFRF): If this bit is set to 1, DRAM self-refresh mode is selected when a transition is made to the software standby state.

This bit is valid when the RFSHE bit is set to 1, enabling refresh operations. It is cleared after recovery from software standby mode.

Bit 3 SLFRF	Description	
0	Self-refreshing is disabled in software standby mode	(Initial value)
1	Self-refreshing is enabled in software standby mode	

Bits 2 to 0—Self-Refresh Precharge Cycle Control (TPCS2 to TPCS0): These bits select the number of states in the precharge cycle immediately after self-refreshing.

The number of states in the precharge cycle immediately after self-refreshing are added to the number of states set by bits TPC1 and TPC0 in the DRACCR register.

Bit 2 TPCS2	Bit 1 TPCS1	Bit 0 TPCS0	Description	
0	0	0	$\overline{\text{RAS}}$ precharge cycle after self-refresh = [TPC set value] states	(Initial value)
		1	$\overline{\text{RAS}}$ precharge cycle after self-refresh = [TPC set value + 1] states	
	1	0	$\overline{\text{RAS}}$ precharge cycle after self-refresh = [TPC set value + 2] states	
		1	$\overline{\text{RAS}}$ precharge cycle after self-refresh = [TPC set value + 3] states	
1	0	0	$\overline{\text{RAS}}$ precharge cycle after self-refresh = [TPC set value + 4] states	
		1	$\overline{\text{RAS}}$ precharge cycle after self-refresh = [TPC set value + 5] states	
	1	0	$\overline{\text{RAS}}$ precharge cycle after self-refresh = [TPC set value + 6] states	
		1	$\overline{\text{RAS}}$ precharge cycle after self-refresh = [TPC set value + 7] states	

4.2.11 Refresh Timer Counter (RTCNT)

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

RTCNT is an 8-bit readable/writable up-counter.

RTCNT counts up using the internal clock selected by bits RTCK2 to RTCK0 in REFCR.

When RTCNT matches RTCOR (compare match), the CMF flag in REFCR is set to 1 and RTCNT is cleared to H'00. If the RFSHE bit in REFCR is set to 1 at this time, a refresh cycle is started. If the RFSHE bit is cleared to 0 and the CMIE bit in REFCR is set to 1, a compare match interrupt (CMI) is generated.

RTCNT is initialized to H'00 by a reset and in hardware standby mode. It is not initialized in software standby mode.

4.2.12 Refresh Time Control Register (RTCOR)

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

RTCOR is an 8-bit readable/writable register that sets the period for compare match operations with RTCNT.

The values of RTCOR and RTCNT are constantly compared, and if they match, the CMF flag in REFCR is set to 1 and RTCNT is cleared to H'00.

RTCOR is initialized to H'FF by a reset and in hardware standby mode. It is not initialized in software standby mode.

4.3 Overview of Bus Control

4.3.1 Area Division

The bus controller divides the 16-Mbyte address space into eight areas, 0 to 7, in 2-Mbyte units, and performs bus control for external space in area units. Figure 4.5 shows an outline of the memory map.

Chip select signals ($\overline{CS0}$ to $\overline{CS7}$) can be output for each area.

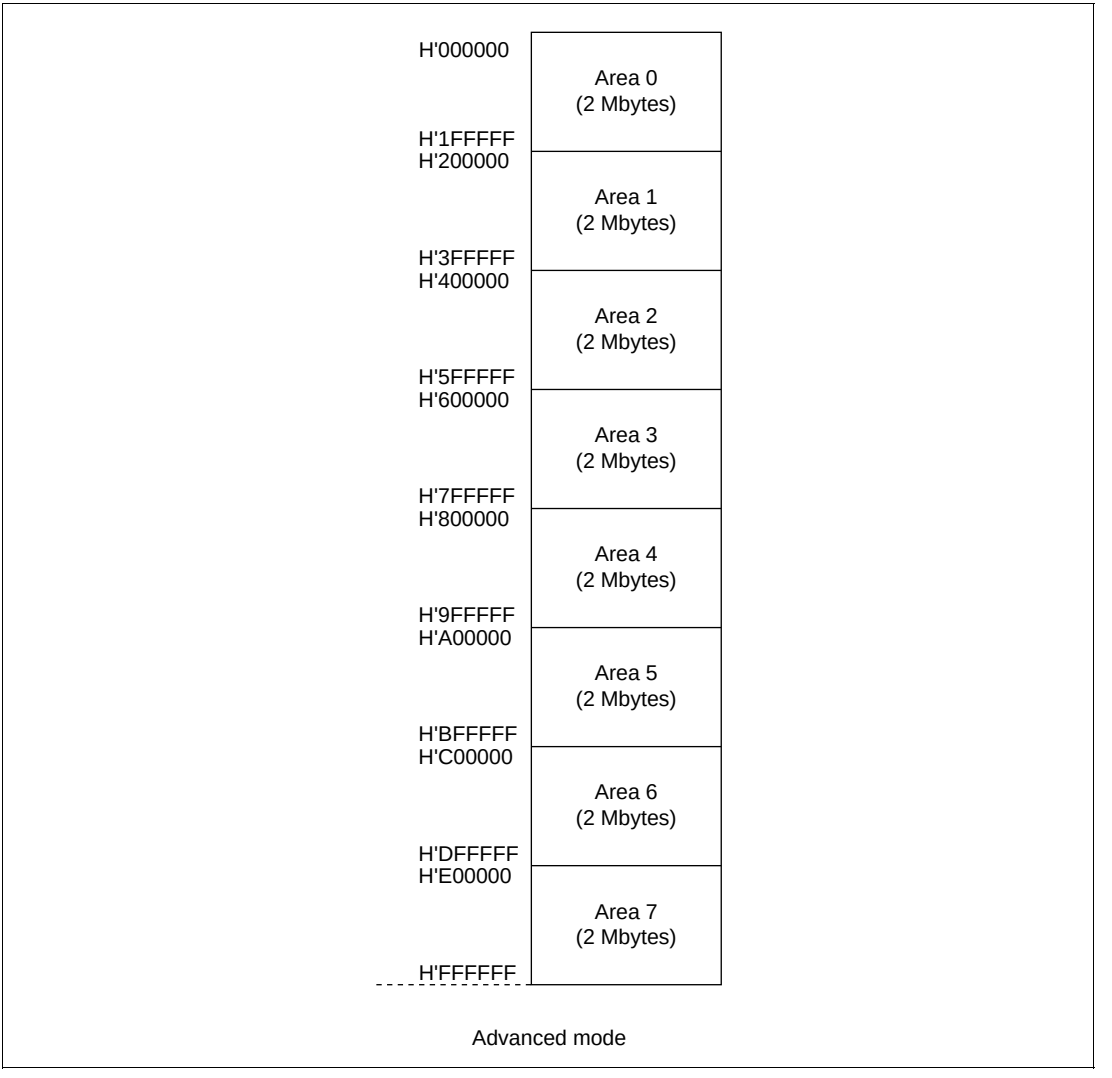


Figure 4.5 Area Divisions

4.3.2 Bus Specifications

The external space bus specifications consist of five elements: (1) bus width, (2) number of access states, (3) number of program wait states, (4) read strobe timing, and (5) chip select ($\overline{CS}$) assertion period extension states.

The bus width and number of access states for on-chip memory and internal I/O registers are fixed, and are not affected by the bus controller.

Bus Width: A bus width of 8 or 16 bits can be selected with ABWCR. An area for which an 8-bit bus is selected functions as an 8-bit access space, and an area for which a 16-bit bus is selected functions as a16-bit access space.

If all areas are designated for 8-bit access, 8-bit bus mode is set; if any area is designated for 16-bit access, 16-bit bus mode is always set.

Number of Access States: Two or three access states can be selected with ASTCR. An area for which 2-state access is selected functions as a 2-state access space, and an area for which 3-state access is selected functions as a 3-state access space.

With the DRAM interface and burst ROM interface, the number of access states may be determined without regard to ASTCR.

When 2-state access space is designated, wait insertion is disabled.

When 3-state access space is designated, it is possible to insert program waits by means of the WTCRA and WTCRB registers, and external waits by means of of the $\overline{WAIT}$ pin.

Number of Program Wait States: When 3-state access space is designated by ASTCR, the number of program wait states to be inserted automatically is selected with WTCRA and WTCRB. From 0 to 7 program wait states can be selected.

Table 4.3 shows the bus specifications (bus width, access states, and program wait states) for each basic bus interface area.

Table 4.3 Bus Specifications for Each Area (Basic Bus Interface)

ABWCR	ASTCR	WTCRA, WTCRB			Bus Specifications (Basic Bus Interface)		
ABWn	ASTn	Wn2	Wn1	Wn0	Bus Width	Access States	Program Wait States
0	0	—	—	—	16	2	0
	1	0	0	0		3	0
				1			1
			1	0			2
				1			3
		1	0	0			4
				1			5
			1	0			6
				1			7
1	0	—	—	—	8	2	0
	1	0	0	0		3	0
				1			1
			1	0			2
				1			3
		1	0	0			4
				1			5
			1	0			6
				1			7

Note: n = 0 to 7

Read Strobe Timing: A setting can be made in RDNCR to select either of two timings for the read strobe ($\overline{RD}$) used in the basic bus interface space.

Chip Select ($\overline{CS}$) Assertion Period Extension States: Some external I/O devices require a setup time and hold time between address and $\overline{CS}$ signals and strobe signals such as $\overline{RD}$, $\overline{HWR}$, and $\overline{LWR}$. Settings can be made in the CSACR registers to insert states in which only the $\overline{CS}$, $\overline{AS}$, and address signals are asserted before and after a basic bus space access cycle.

4.3.3 Memory Interfaces

The memory interfaces of the H8S/2678 Series comprise a basic bus interface that allows direct connection of ROM, SRAM, and so on; a DRAM interface that allows direct connection of DRAM; and a burst ROM interface that allows direct connection of burst ROM. The interface can be selected independently for each area.

An area for which the basic bus interface is designated functions as normal space, an area for which the DRAM interface is designated functions as DRAM space, and an area for which the burst ROM interface is designated functions as burst ROM space.

The initial state of each area is basic bus interface, 3-state access space. The initial bus width is selected according to the operating mode. The bus specifications described here cover basic items only, and the sections on each memory interface (4.4, 4.5, and 4.6) should be referred to for further details.

Area 0: Area 0 includes on-chip ROM*, and in expanded mode with on-chip ROM disabled, all of area 0 is external space. In expanded mode with on-chip ROM enabled, the space excluding on-chip ROM* is external space.

When area 0 external space is accessed, the $\overline{CS0}$ signal can be output.

Either basic bus interface or burst ROM interface can be selected for area 0.

Note: * Applies only to versions with ROM.

Area 1: In externally expanded mode, all of area 1 is external space.

When area 1 external space is accessed, the $\overline{CS1}$ signal can be output.

Either basic bus interface or burst ROM interface can be selected for area 1.

Areas 2 to 5: In externally expanded mode, areas 2 to 5 are all external space.

When area 2 to 5 external space is accessed, signals $\overline{CS2}$ to $\overline{CS5}$ can be output.

Basic bus interface or DRAM interface can be selected for areas 2 to 5. With the DRAM interface, signals $\overline{CS2}$ to $\overline{CS5}$ are used as $\overline{RAS}$ signals.

If areas 2 to 5 are designated as continuous DRAM space, large-capacity (e.g. 64-Mbit) DRAM can be connected. In this case, the $\overline{CS2}$ signal is used as the $\overline{RAS}$ signal for the continuous DRAM space.

Area 6: In externally expanded mode, all of area 6 is external space.

When area 6 external space is accessed, the $\overline{CS6}$ signal can be output.

Only the basic bus interface can be used for area 6.

Area 7: Area 7 includes the on-chip RAM and internal/O registers. In externally expanded mode, the space excluding the on-chip RAM and internal I/O registers is external space. The on-chip RAM is enabled when the RAME bit is set to 1 in the system control register (SYSCR); when the RAME bit is cleared to 0, the on-chip RAM is disabled and the corresponding addresses are in external space.

When area 7 external space is accessed, the $\overline{CS7}$ signal can be output.

Only the basic bus interface can be used for the area 7 memory interface.

4.3.4 Chip Select Signals

The chip can output chip select signals ($\overline{CS0}$ to $\overline{CS7}$) for areas 0 to 7, the signal being driven low when the corresponding external space area is accessed.

Figure 4.6 shows an example of $\overline{CSn}$ (n = 0 to 7) output timing.

Enabling or disabling of $\overline{CSn}$ signal output is performed by setting the data direction register (DDR) bit for the port corresponding to the particular $\overline{CSn}$ pin.

In expanded mode with on-chip ROM disabled, the $\overline{CS0}$ pin is placed in the output state after a reset. Pins $\overline{CS1}$ to $\overline{CS7}$ are placed in the input state after a reset and so the corresponding DDR bits should be set to 1 when outputting signals $\overline{CS1}$ to $\overline{CS7}$.

In expanded mode with on-chip ROM enabled, pins $\overline{CS0}$ to $\overline{CS7}$ are all placed in the input state after a reset and so the corresponding DDR bits should be set to 1 when outputting signals $\overline{CS0}$ to $\overline{CS7}$.

For details see section 5, I/O Ports.

When areas 2 to 5 are designated as DRAM space, outputs $\overline{CS2}$ to $\overline{CS5}$ are used as $\overline{RAS}$ signals.

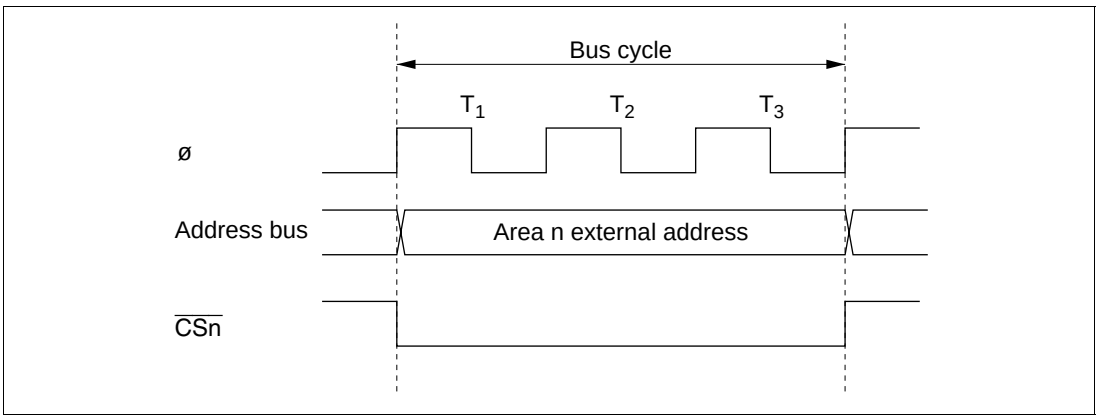


Figure 4.6 $\overline{CSn}$ Signal Output Timing (n = 0 to 7)

4.4 Basic Bus Interface

4.4.1 Overview

The basic bus interface enables direct connection of ROM, SRAM, and so on.

The bus specifications can be selected with ABWCR, ASTCR, WTCRA, WTCRB, RDNCR, and CSACR. For details see table 4.3.

4.4.2 Data Size and Data Alignment

Data sizes for the CPU and other internal bus masters are byte, word, and longword. The bus controller has a data alignment function, and when accessing external space, controls whether the upper data bus (D15 to D8) or lower data bus (D7 to D0) is used according to the bus specifications for the area being accessed (8-bit access space or 16-bit access space) and the data size.

8-Bit Access Space: Figure 4.7 illustrates data alignment control for the 8-bit access space. With the 8-bit access space, the upper data bus (D15 to D8) is always used for accesses. The amount of data that can be accessed at one time is one byte: a word access is performed as two byte accesses, and a longword access, as four byte accesses.

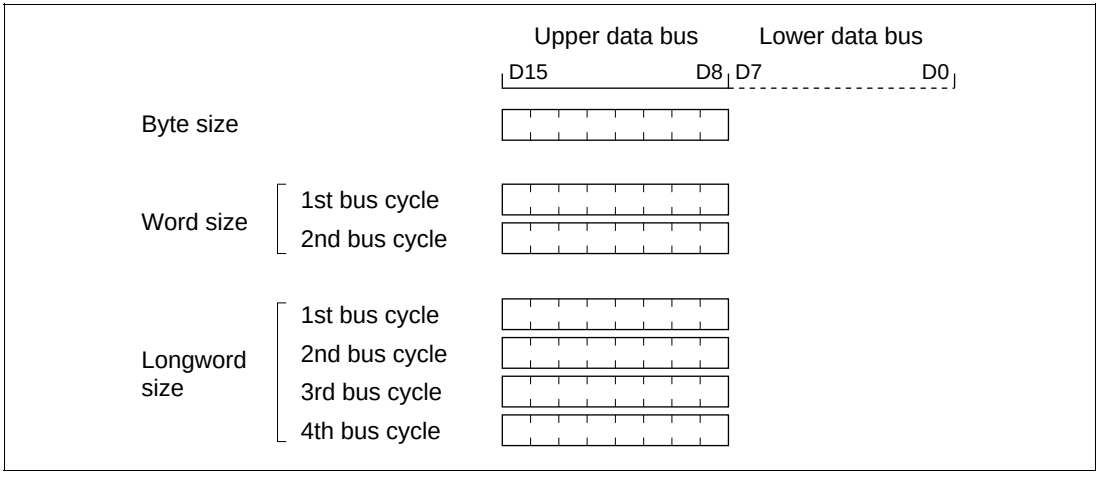


Figure 4.7 Access Sizes and Data Alignment Control (8-Bit Access Space)

16-Bit Access Space: Figure 4.8 illustrates data alignment control for the 16-bit access space. With the 16-bit access space, the upper data bus (D15 to D8) and lower data bus (D7 to D0) are used for accesses. The amount of data that can be accessed at one time is one byte or one word, and a longword access is executed as two word accesses.

In byte access, whether the upper or lower data bus is used is determined by whether the address is even or odd. The upper data bus is used for an even address, and the lower data bus for an odd address.

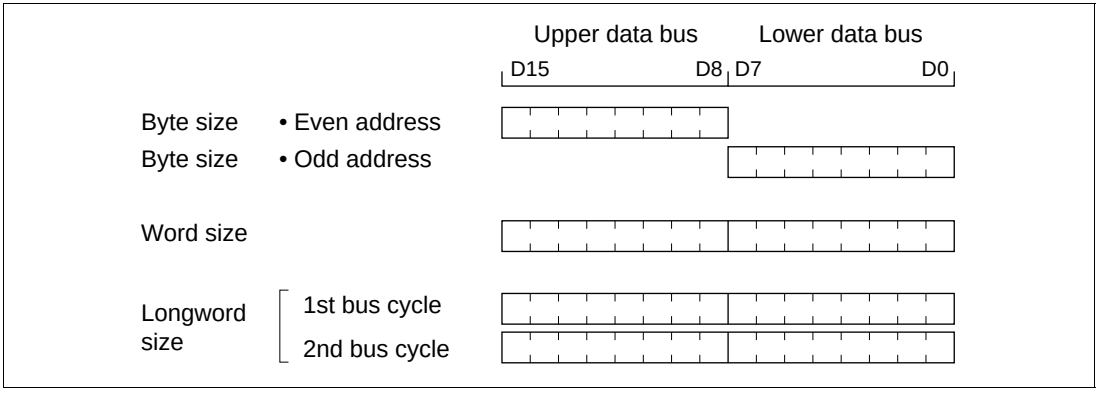


Figure 4.8 Access Sizes and Data Alignment Control (16-bit Access Space)

4.4.3 Valid Strobes

Table 4.4 shows the data buses used and valid strobes for the access spaces.

In a read, the $\overline{RD}$ signal is valid for both the upper and the lower half of the data bus.

In a write, the $\overline{HWR}$ signal is valid for the upper half of the data bus, and the $\overline{LWR}$ signal for the lower half.

Table 4.4 Data Buses Used and Valid Strobes

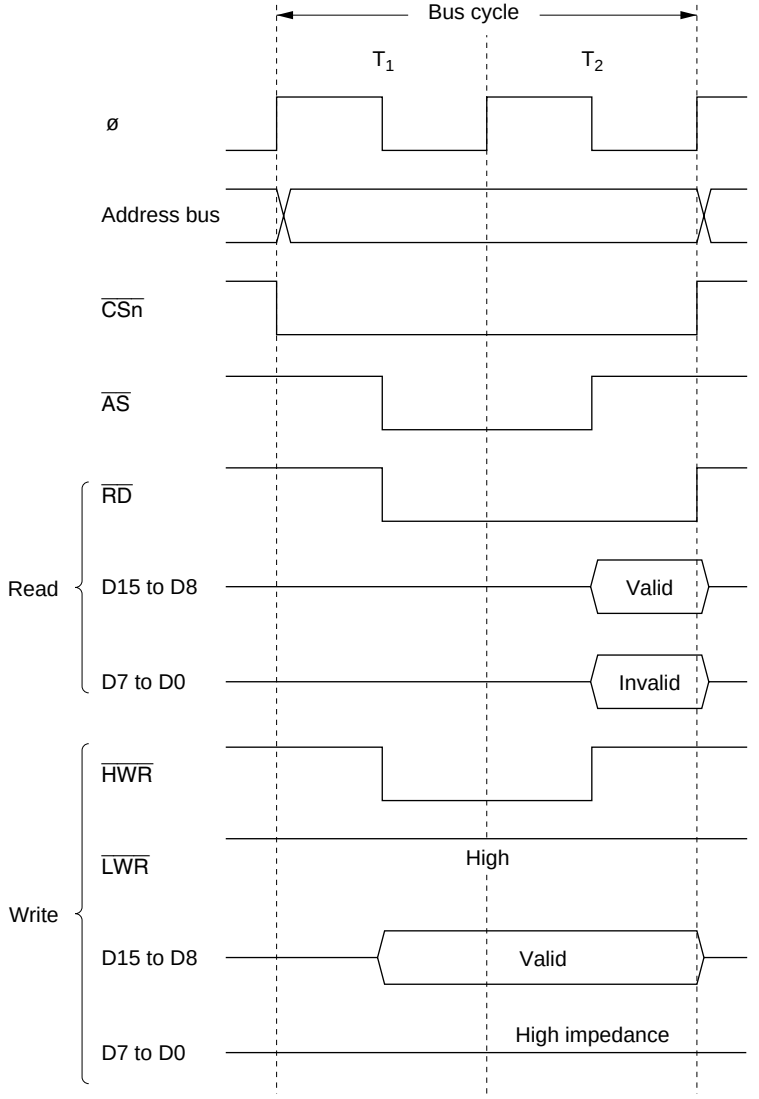
Area	Access Size	Read/ Write	Address	Valid Strobe	Upper Data Bus (D15 to D8)	Lower Data Bus (D7 to D0)
8-bit access space	Byte	Read	—	$\overline{RD}$	Valid	Invalid
		Write	—	$\overline{HWR}$		Hi-Z
16-bit access space	Byte	Read	Even	$\overline{RD}$	Valid	Invalid
			Odd		Invalid	Valid
		Write	Even	$\overline{HWR}$	Valid	Hi-Z
			Odd	$\overline{LWR}$	Hi-Z	Valid
	Word	Read	—	$\overline{RD}$	Valid	Valid
		Write	—	$\overline{HWR}$, $\overline{LWR}$	Valid	Valid

Note: Hi-Z: High-impedance state
Invalid: Input state; input value is ignored.

4.4.4 Basic Timing

8-Bit, 2-State Access Space: Figure 4.9 shows the bus timing for an 8-bit, 2-state access space. When an 8-bit access space is accessed, the upper half (D15 to D8) of the data bus is used.

The $\overline{\text{LWR}}$ pin is fixed high. Wait states cannot be inserted.



Notes: 1. n = 0 to 7
2. When RDNn = 0

Figure 4.9 Bus Timing for 8-Bit, 2-State Access Space

8-Bit, 3-State Access Space: Figure 4.10 shows the bus timing for an 8-bit, 3-state access space. When an 8-bit access space is accessed, the upper half (D15 to D8) of the data bus is used.

The $\overline{\text{LWR}}$ pin is fixed high. Wait states can be inserted.

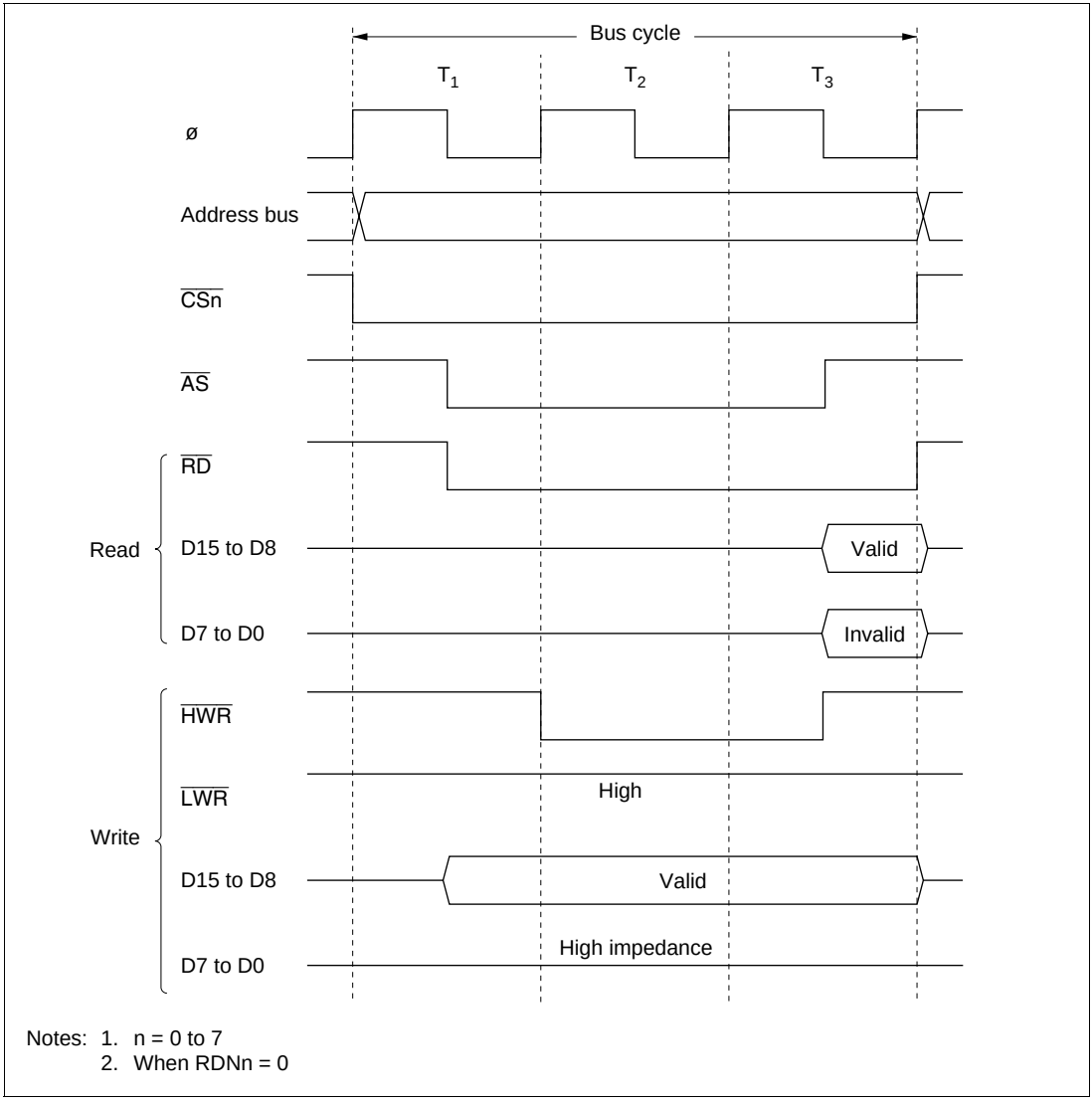
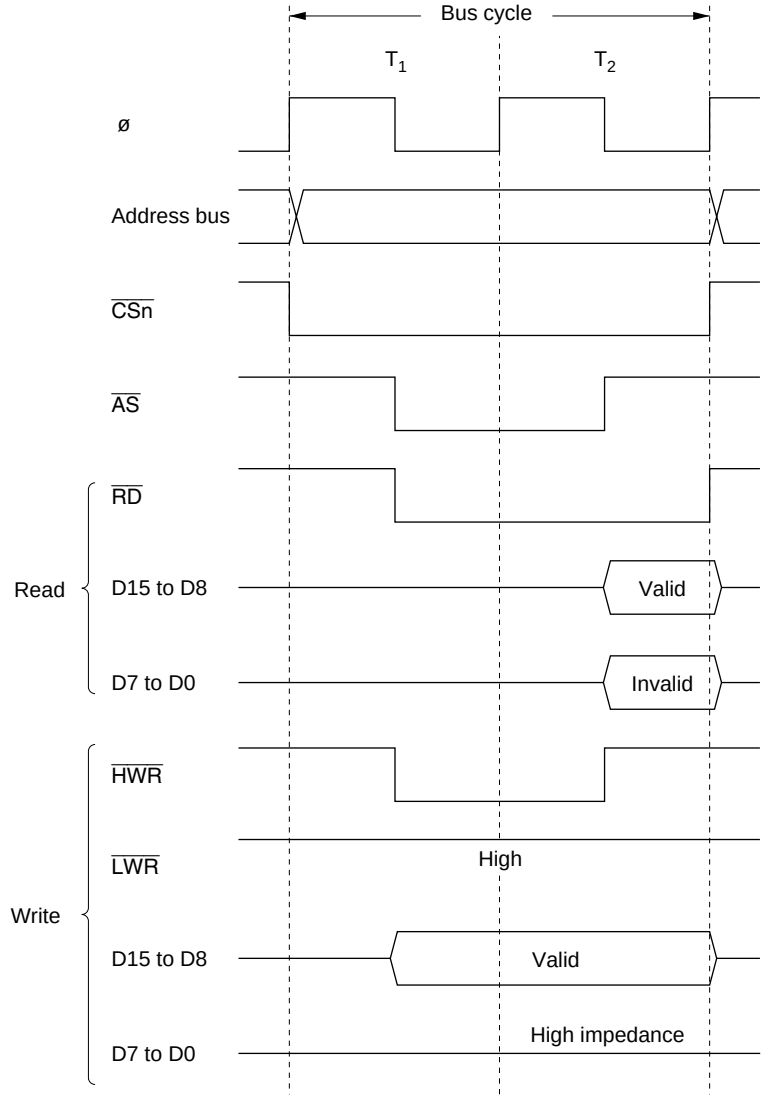


Figure 4.10 Bus Timing for 8-Bit, 3-State Access Space

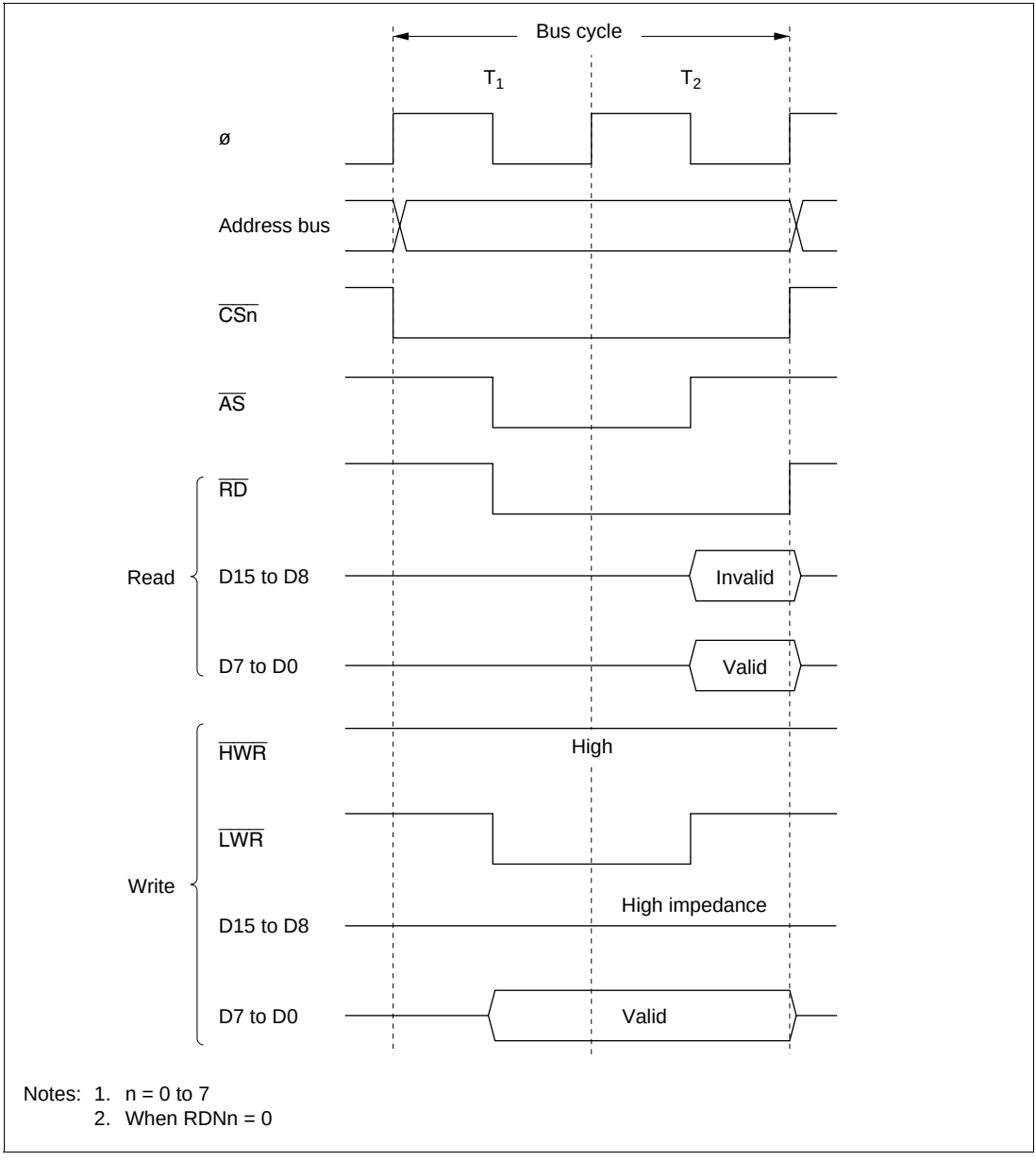
16-Bit, 2-State Access Space: Figures 4.11 to 4.13 show bus timings for a 16-bit, 2-state access space. When a 16-bit access space is accessed, the upper half (D15 to D8) of the data bus is used for odd addresses, and the lower half (D7 to D0) for even addresses.

Wait states cannot be inserted.



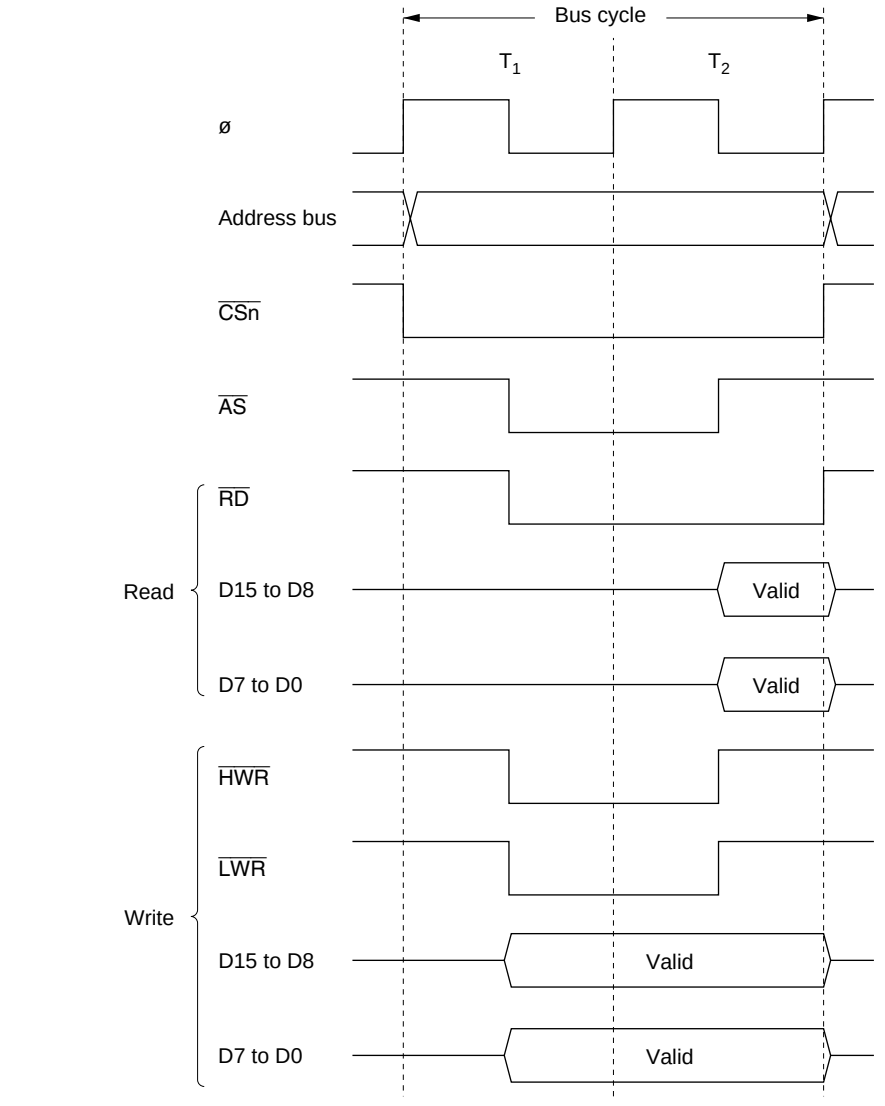
Notes: 1. n = 0 to 7
2. When RDNn = 0

Figure 4.11 Bus Timing for 16-Bit, 2-State Access Space (1)
(Even Address Byte Access)



Notes: 1. n = 0 to 7
2. When RDNn = 0

Figure 4.12 Bus Timing for 16-Bit, 2-State Access Space (2)
(Odd Address Byte Access)



Notes: 1. n = 0 to 7
2. When RDNn = 0

Figure 4.13 Bus Timing for 16-Bit, 2-State Access Space (3) (Word Access)

16-Bit, 3-State Access Space: Figures 4.14 to 4.16 show bus timings for a 16-bit, 3-state access space. When a 16-bit access space is accessed, the upper half (D15 to D8) of the data bus is used for the odd address, and the lower half (D7 to D0) for the even address.

Wait states can be inserted.

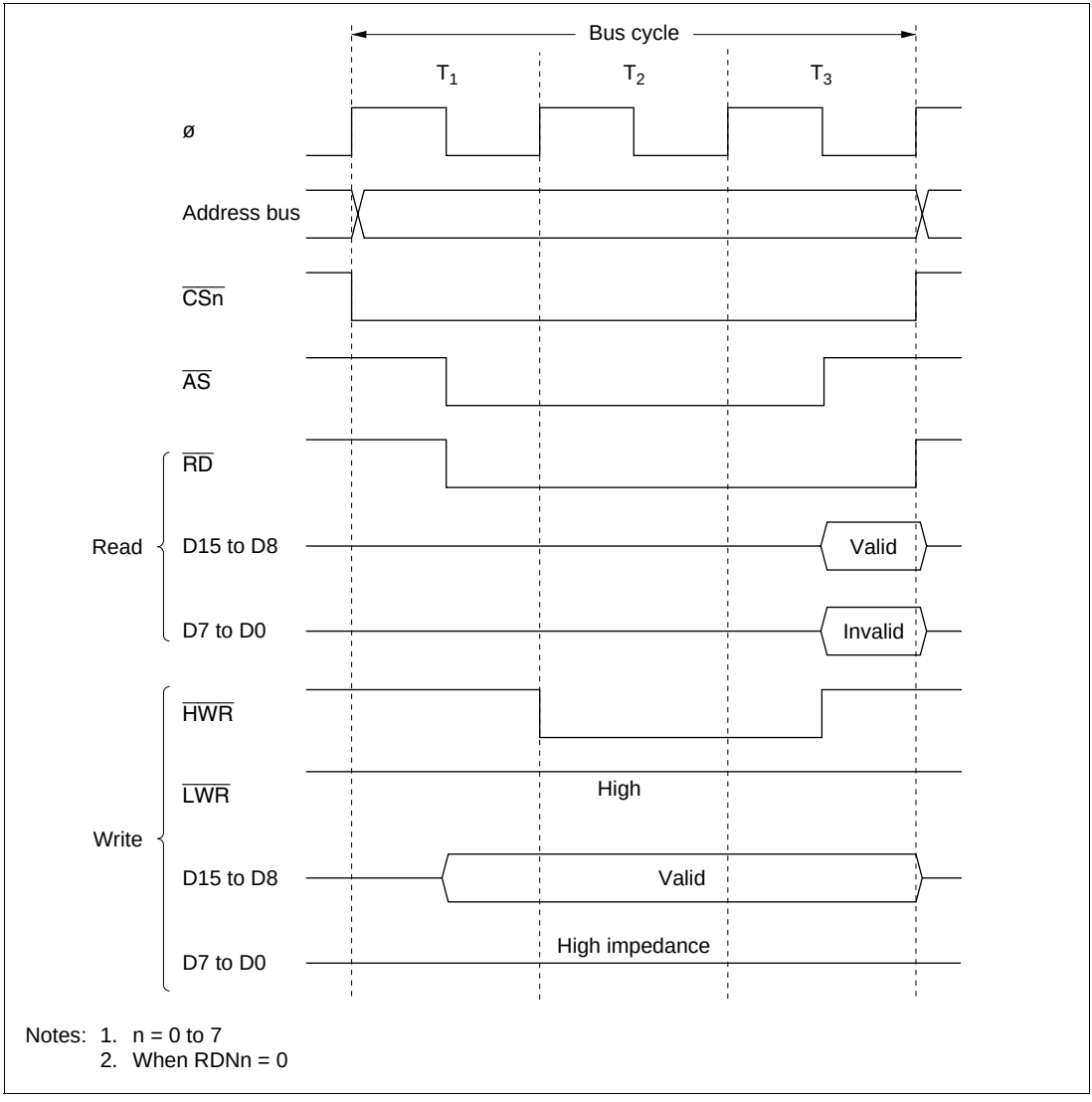
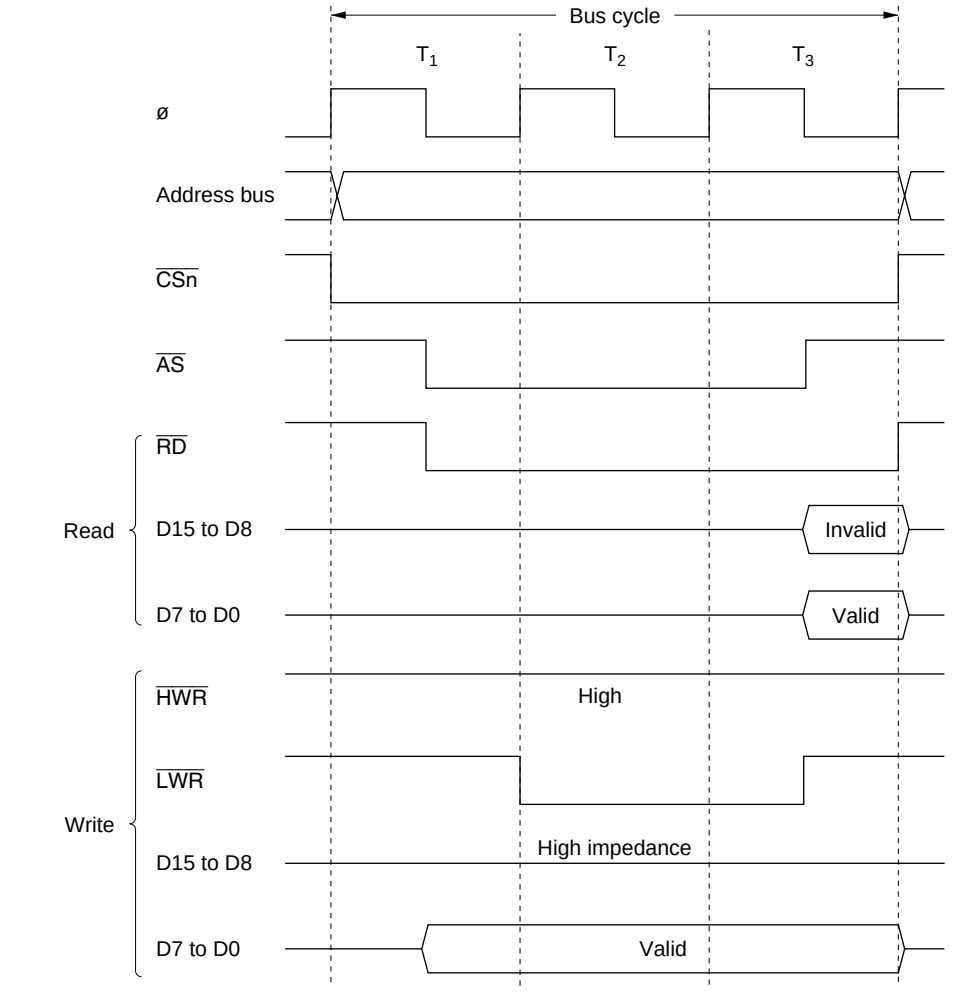
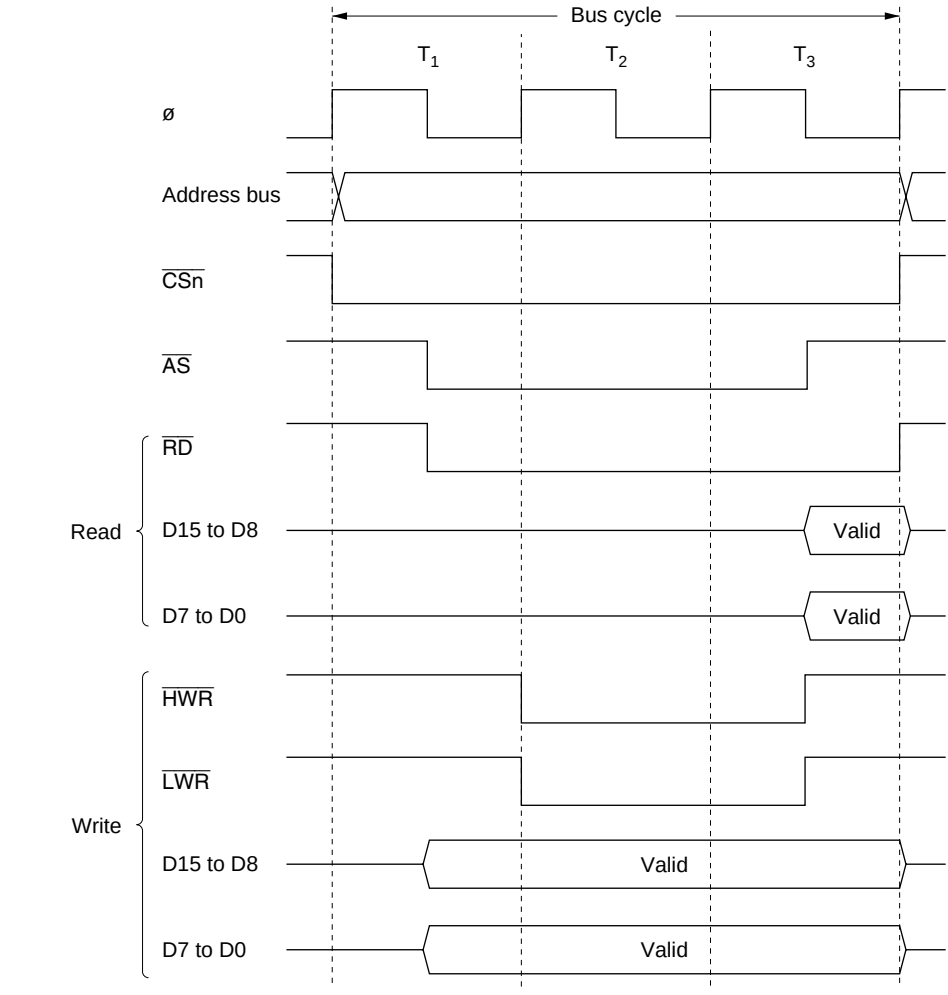


Figure 4.14 Bus Timing for 16-Bit, 3-State Access Space (1)
(Even Address Byte Access)



Notes: 1. n = 0 to 7
2. When RDNn = 0

Figure 4.15 Bus Timing for 16-Bit, 3-State Access Space (2) (Odd Address Byte Access)



Notes: 1. n = 0 to 7
2. When RDNn = 0

Figure 4.16 Bus Timing for 16-Bit, 3-State Access Space (3) (Word Access)

4.4.5 Wait Control

When accessing external space, the H8S/2678 Series chip can extend the bus cycle by inserting one or more wait states (T_w). There are two ways of inserting wait states: (1) program wait insertion and (2) pin wait insertion using the $\overline{\text{WAIT}}$ pin.

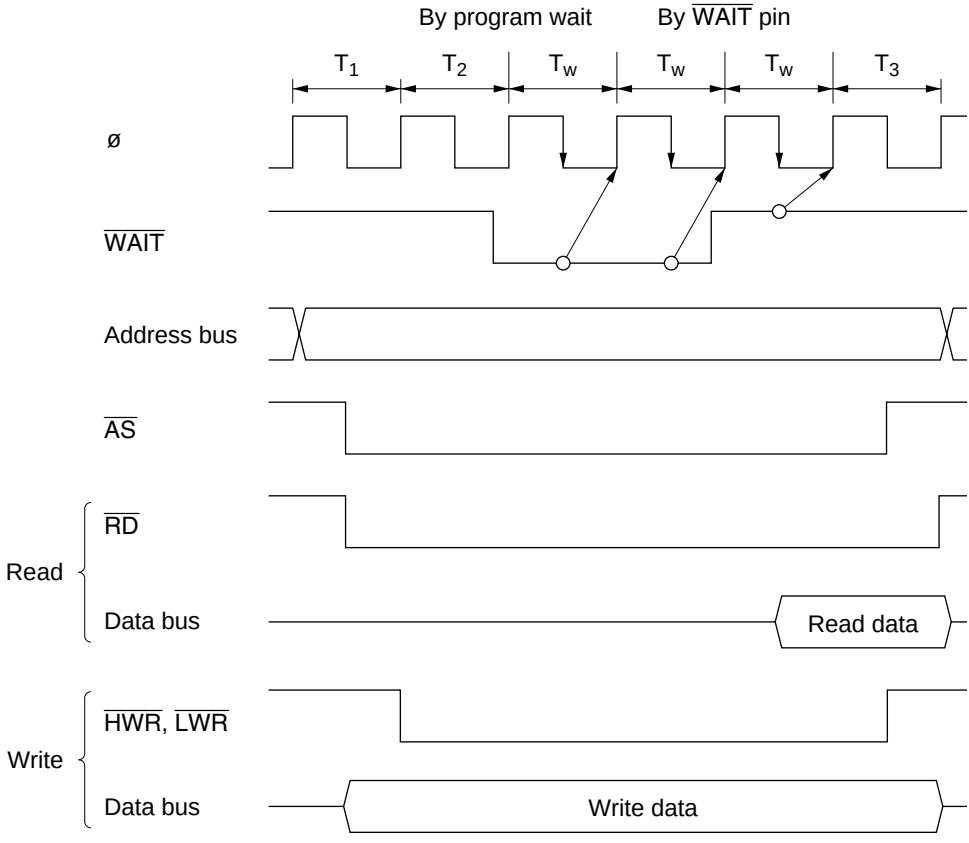
Program Wait Insertion: From 0 to 3 wait states can be inserted automatically between the T_2 state and T_3 state on an individual area basis in 3-state access space, according to the settings in WTCRA and WTCRB.

Pin Wait Insertion: Setting the WAITE bit to 1 in BCR enables wait input by means of the $\overline{\text{WAIT}}$ pin. When external space is accessed in this state, a program wait is first inserted in accordance with the settings in WTCRA and WTCRB. If the $\overline{\text{WAIT}}$ pin is low at the falling edge of ø in the last T_2 or T_w state, another T_w state is inserted. If the $\overline{\text{WAIT}}$ pin is held low, T_w states are inserted until it goes high.

This is useful when inserting seven or more T_w states, or when changing the number of T_w states to be inserted for different external devices.

The WAITE bit setting applies to all areas.

Figure 4.17 shows an example of wait state insertion timing.



Notes: 1. Downward arrows indicate the timing of $\overline{\text{WAIT}}$ pin sampling.
2. When RDNn = 0

Figure 4.17 Example of Wait State Insertion Timing

The settings after a reset are: 3-state access, insertion of 7 program wait states, and $\overline{\text{WAIT}}$ input disabled.

4.4.6 Read Strobe ($\overline{RD}$) Timing

The read strobe timing can be changed for individual areas by setting bits RDN7 to RDN0 to 1 in RDNCR.

When the DMAC or EXDMAC is used in single mode, note that if the read strobe timing is changed by setting RDNn to 1, the $\overline{RD}$ timing will change relative to the rise of $\overline{DACK}$ or $\overline{EDACK}$.

Figure 4.18 shows an example of the timing when the read strobe timing is changed in basic bus 3-state access space.

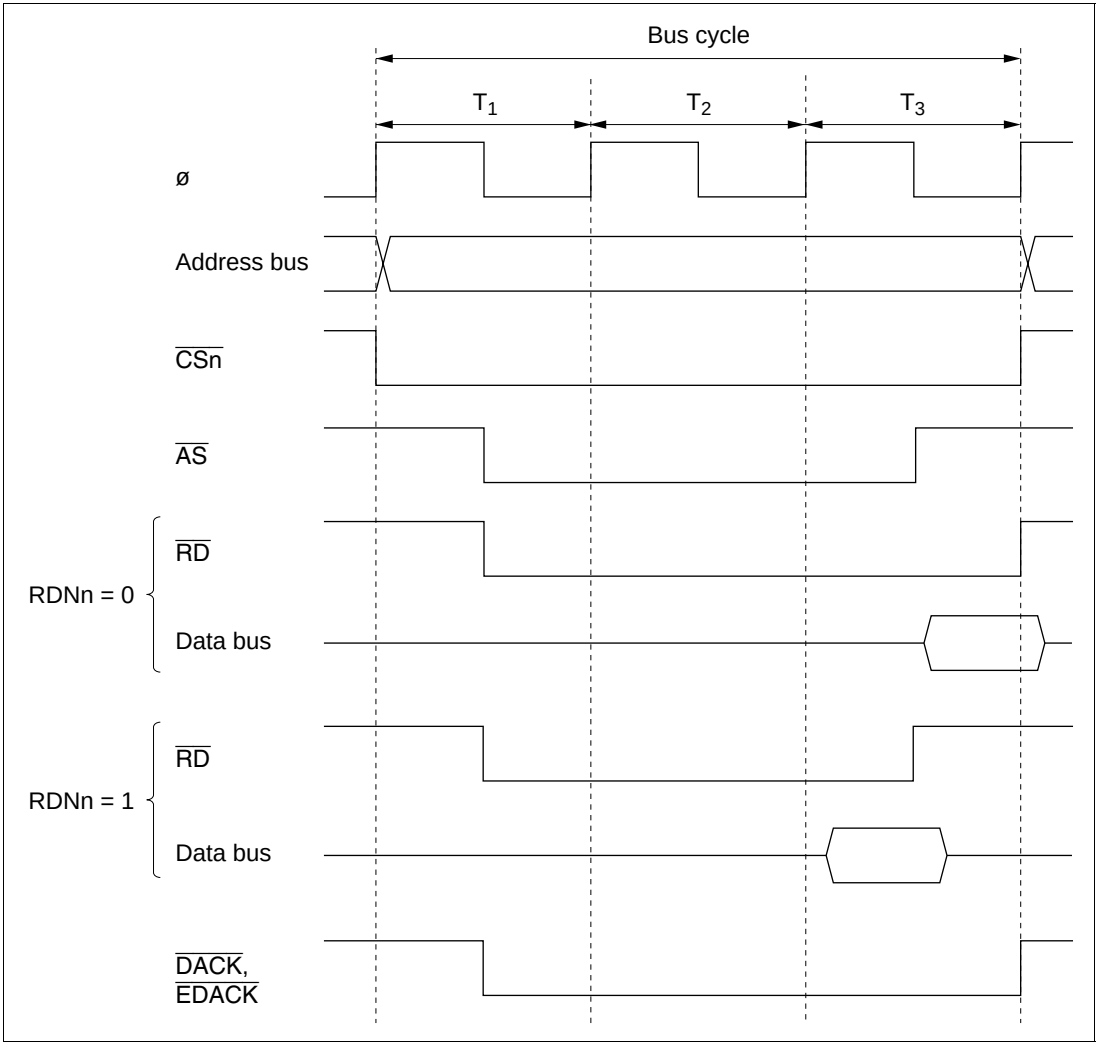


Figure 4.18 Example of Read Strobe Timing

4.4.7 Extension of Chip Select ($\overline{CS}$) Assertion Period

Some external I/O devices require a setup time and hold time between address and $\overline{CS}$ signals and strobe signals such as $\overline{RD}$, $\overline{HWR}$, and $\overline{LWR}$. Settings can be made in the CSACR register to insert states in which only the $\overline{CS}$, $\overline{AS}$, and address signals are asserted before and after a basic bus space access cycle. Extension of the $\overline{CS}$ assertion period can be set for individual areas.

With the $\overline{CS}$ assertion extension period in write access, the data setup and hold times are less stringent since the write data is output to the data bus.

Figure 4.19 shows an example of the timing when the $\overline{CS}$ assertion period is extended in basic bus 3-state access space.

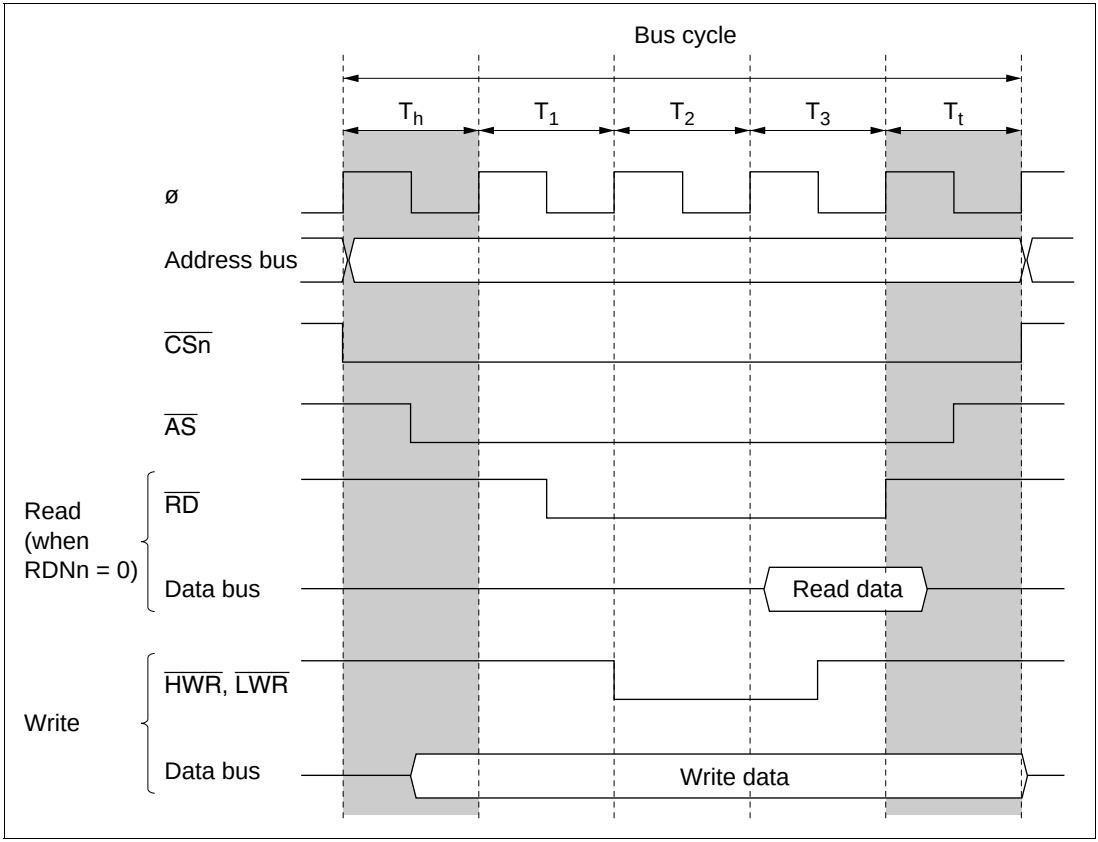


Figure 4.19 Example of Timing when Chip Select Assertion Period is Extended

Both extension state T_h inserted before the basic bus cycle and extension state T_t inserted after the basic bus cycle, or only one of these, can be specified for individual areas. Insertion or non-insertion can be specified for the T_h state with the upper 8 bits (CSXH7 to CSXH0) in the CSACR register, and for the T_t state with the lower 8 bits (CSXT7 to CSXT0).

4.5 DRAM Interface

4.5.1 Overview

In the H8S/2678 Series, external space areas 2 to 5 can be designated as DRAM space, and DRAM interfacing performed. The DRAM interface allows DRAM to be directly connected to the chip. A DRAM space of 2, 4, or 8 Mbytes can be set by means of bits RMTS2 to RMTS0 in DRAMCR. Burst operation is also possible, using fast page mode.

4.5.2 Setting DRAM Space

Areas 2 to 5 are designated as DRAM space by setting bits RMTS2 to RMTS0 in the DRAMCR register. The relation between the settings of bits RMTS2 to RMTS0 and DRAM space is shown in table 4.5. Possible DRAM space settings are: one area (area 2), two areas (areas 2 and 3), four areas (areas 2 to 5), and continuous area (areas 2 to 5).

Table 4.5 DRAM Space Settings by Bits RMTS2 to RMTS0

RMTS2	RMTS1	RMTS0	Area 5	Area 4	Area 3	Area 2
0	0	1	Normal space	Normal space	Normal space	DRAM space
	1	0	Normal space	Normal space	DRAM space	DRAM space
		1	DRAM space	DRAM space	DRAM space	DRAM space
1	0	*	Reserved (setting prohibited)	Reserved (setting prohibited)	Reserved (setting prohibited)	Reserved (setting prohibited)
	1	0				
		1	Continuous DRAM space	Continuous DRAM space	Continuous DRAM space	Continuous DRAM space

*: Don't care

With continuous DRAM space, $\overline{RAS2}$ is valid. The bus specifications (bus width, number of wait states, etc.) for continuous DRAM space conform to the settings for area 2.

4.5.3 Address Multiplexing

With DRAM space, the row address and column address are multiplexed. In address multiplexing, the size of the shift of the row address is selected with bits MXC2 to MXC0 in DRAMCR. Table 4.6 shows the correspondence between the settings of MXC2 to MXC0 and the shift size.

Table 4.6 Address Multiplexing Settings by Bits MXC2 to MXC0

	DRAMCR				Address Pins																
	MXC2	MXC1	MXC0	Shift Size	A23 to A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Row address	0	0	0	8 bits	A23 to A16	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8
			1	9 bits	A23 to A16	A15	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9
		1	0	10 bits	A23 to A16	A15	A14	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10
			1	11 bits	A23 to A16	A15	A14	A13	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11
	1	—	—	Reserved (setting prohibited)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Column address	—	—	—	—	A23 to A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

4.5.4 Data Bus

If a bit in ABWCR corresponding to an area designated as DRAM space is set to 1, that area is designated as 8-bit DRAM space; if the bit is cleared to 0, the area is designated as 16-bit DRAM space. In 16-bit DRAM space, ×16-bit configuration DRAM can be connected directly.

In 8-bit DRAM space the upper half of the data bus, D15 to D8, is enabled, while in 16-bit DRAM space both the upper and lower halves of the data bus, D15 to D0, are enabled.

Access sizes and data alignment are the same as for the basic bus interface: see section 4.4.2, Data Size and Data Alignment.

4.5.5 Pins Used for DRAM Interface

Table 4.7 shows the pins used for DRAM interfacing and their functions.

Table 4.7 DRAM Interface Pins

Pin	With DRAM Setting	Name	I/O	Function
$\overline{\text{HWR}}$	$\overline{\text{WE}}$	Write enable	Output	Write enable for DRAM space access
$\overline{\text{CS2}}$	$\overline{\text{RAS2}}$	Row address strobe 2	Output	Row address strobe when area 2 is designated as DRAM space Row address strobe when areas 2 to 5 are designated as continuous DRAM space
$\overline{\text{CS3}}$	$\overline{\text{RAS3}}$	Row address strobe 3	Output	Row address strobe when area 3 is designated as DRAM space
$\overline{\text{CS4}}$	$\overline{\text{RAS4}}$	Row address strobe 4	Output	Row address strobe when area 4 is designated as DRAM space
$\overline{\text{CS5}}$	$\overline{\text{RAS5}}$	Row address strobe 5	Output	Row address strobe when area 5 is designated as DRAM space
$\overline{\text{UCAS}}$	$\overline{\text{UCAS}}$	Upper column address strobe	Output	Upper column address strobe for 16-bit DRAM space access Column address strobe for 8-bit DRAM space access
$\overline{\text{LCAS}}$	$\overline{\text{LCAS}}$	Lower column address strobe	Output	Lower column address strobe signal for 16-bit DRAM space access
$\overline{\text{RD}}$, $\overline{\text{OE}}$	$\overline{\text{OE}}$	Output enable	Output	Output enable signal for DRAM space access
$\overline{\text{WAIT}}$	$\overline{\text{WAIT}}$	Wait	Input	Wait request signal
A15 to A0	A15 to A0	Address pins	Output	Row address/column address multiplexed output
D15 to D0	D15 to D0	Data pins	I/O	Data input/output pins

4.5.6 Basic Timing

Figure 4.20 shows the basic access timing for DRAM space.

The four states of the basic timing consist of one T_p (precharge cycle) state, one T_r (row address output cycle) state, and the T_{c1} and T_{c2} (column address output cycle) states.

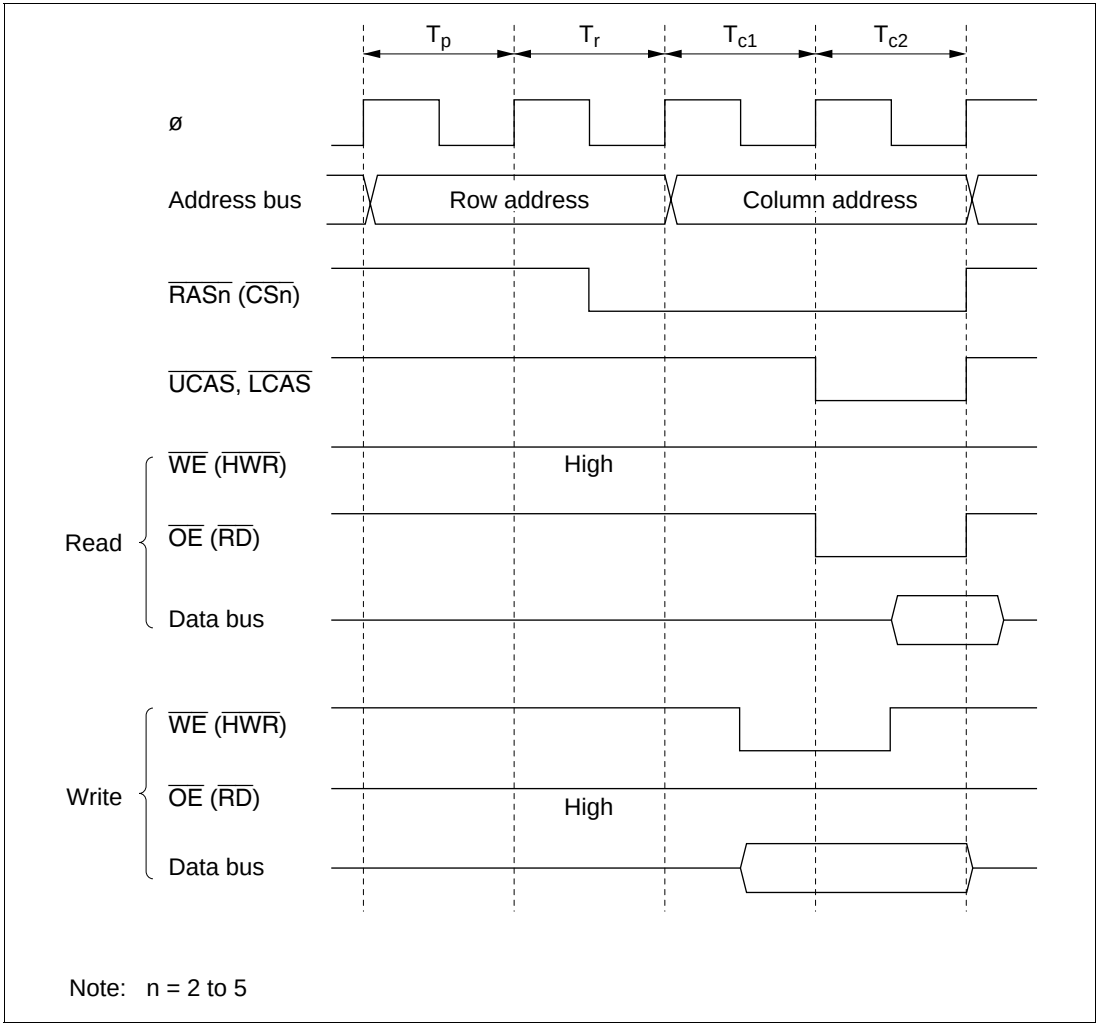


Figure 4.20 DRAM Basic Access Timing (RAST = 0, CAST = 0)

When DRAM space is accessed, the $\overline{RD}$ signal is output as the $\overline{OE}$ signal for DRAM. When connecting DRAM provided with an EDO page mode, the $\overline{OE}$ signal should be connected to the $\overline{OE}$ pin of the DRAM. Setting the OEE bit to 1 in the DRAMCR register enables the $\overline{OE}$ signal for DRAM space to be output from a dedicated $\overline{OE}$ pin. In this case, the $\overline{OE}$ signal for DRAM space is

output from both the $\overline{RD}$ pin and the $\overline{OE}$ pin, but in external read cycles for other than DRAM space, the signal is output only from the $\overline{RD}$ pin.

4.5.7 Column Address Output Cycle Control

The column address output cycle can be changed from 2 states to 3 states by setting the CAST bit to 1 in the DRAMCR register. Use the setting that gives the optimum specification values ($\overline{CAS}$ pulse width, etc.) according to the DRAM connected and the operating frequency of the chip. Figure 4.21 shows an example of the timing when a 3-state column address output cycle is selected.

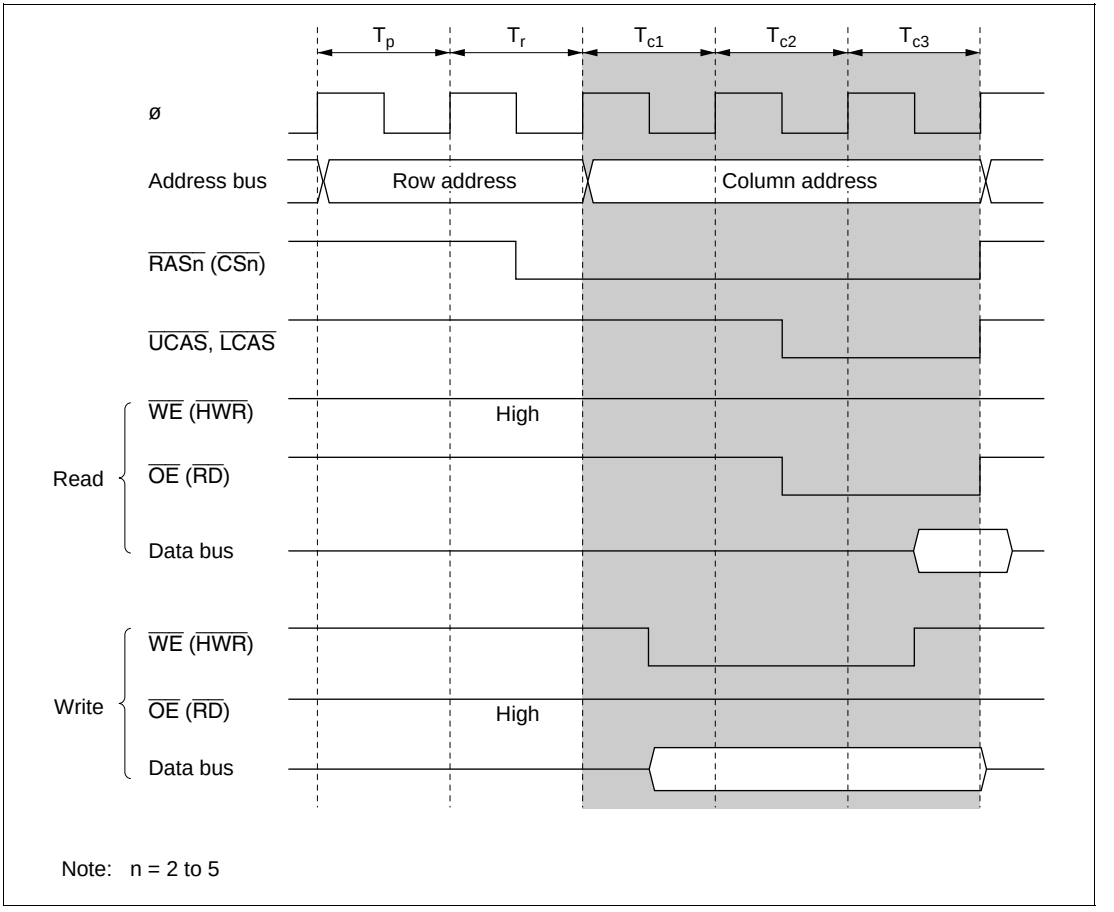


Figure 4.21 Example of Access Timing with 3-State Column Address Output Cycle (RAST = 0)

4.5.8 Row Address Output Cycle Control

If the RAST bit is set to 1 in the DRAMCR register, the $\overline{RAS}$ signal goes low from the beginning of the T_r state, and the row address hold time and DRAM read access time are changed relative to the fall of the $\overline{RAS}$ signal. Use the optimum setting according to the DRAM connected and the operating frequency of the chip. Figure 4.22 shows an example of the timing when the $\overline{RAS}$ signal goes low from the beginning of the T_r state.

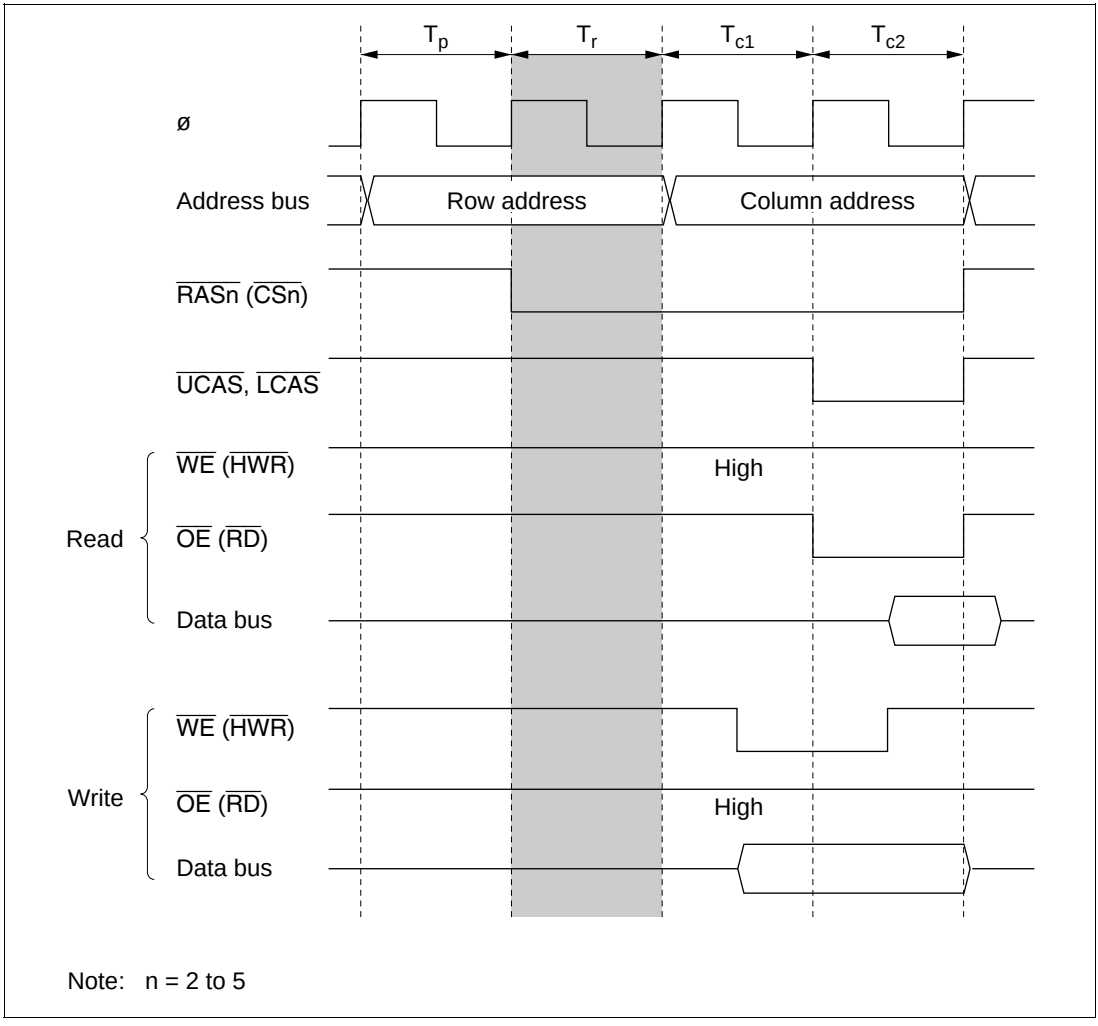


Figure 4.22 Example of Access Timing when $\overline{RAS}$ Signal Goes Low from Beginning of T_r State (CAST = 0)

If a row address hold time or read access time is necessary, making a setting in bits RCD1 and RCD0 in the DRACCR register allows from one to three T_{rw} states, in which row address output is maintained, to be inserted between the T_r cycle, in which the $\overline{RAS}$ signal goes low, and the T_{c1} cycle, in which the column address is output. Use the setting that gives the optimum row address signal hold time relative to the fall of the $\overline{RAS}$ signal according to the DRAM connected and the operating frequency of the chip. Figure 4.23 shows an example of the timing when one T_{rw} state is set.

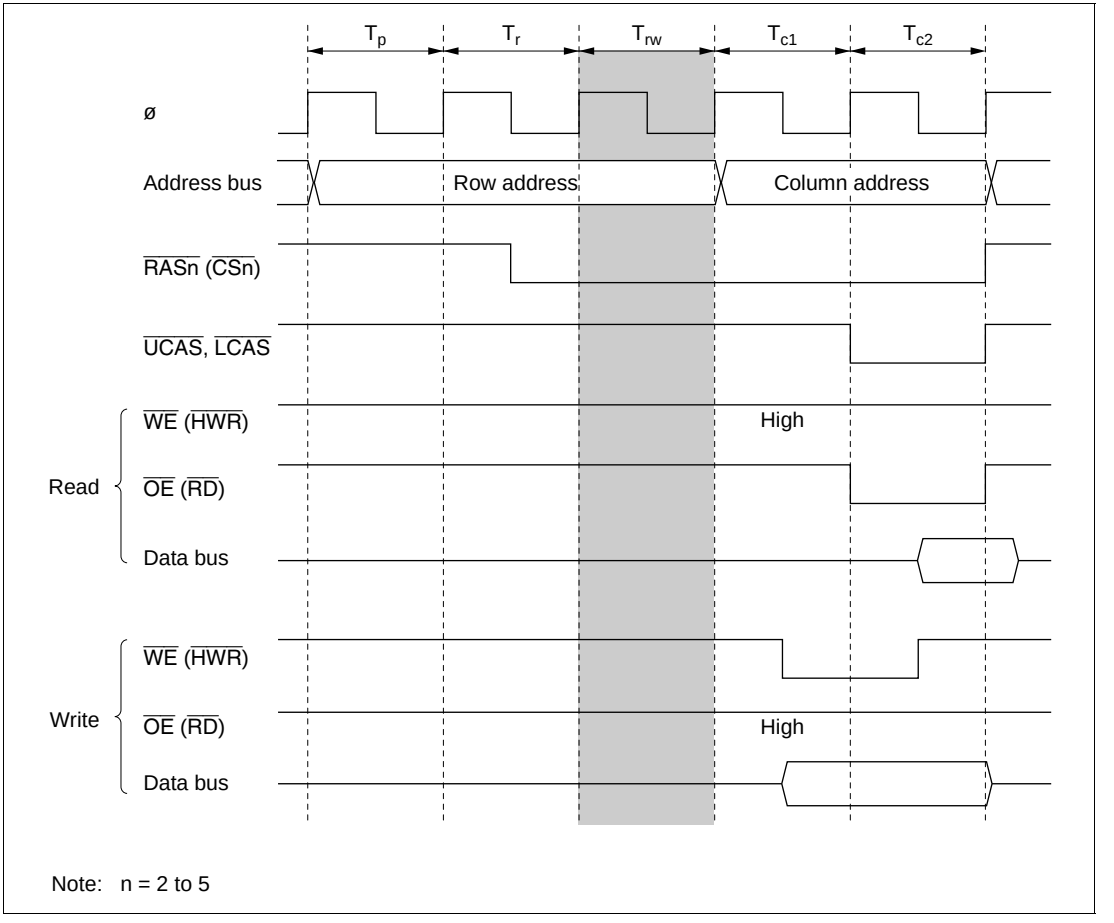


Figure 4.23 Example of Timing with One Row Address Output Maintenance State (RAST = 0, CAST = 0)

4.5.9 Precharge State Control

When DRAM is accessed, a $\overline{RAS}$ precharge time must be secured. With the H8S/2678 Series, one T_p state is always inserted when DRAM space is accessed. From one to four T_p states can be selected by setting bits TPC1 and TPC0 in DRACCR. Set the optimum number of T_p cycles according to the DRAM connected and the operating frequency of the chip. Figure 4.24 shows the timing when two Tp states are inserted.

The setting of bits TPC1 and TPC0 is also valid for T_p states in refresh cycles.

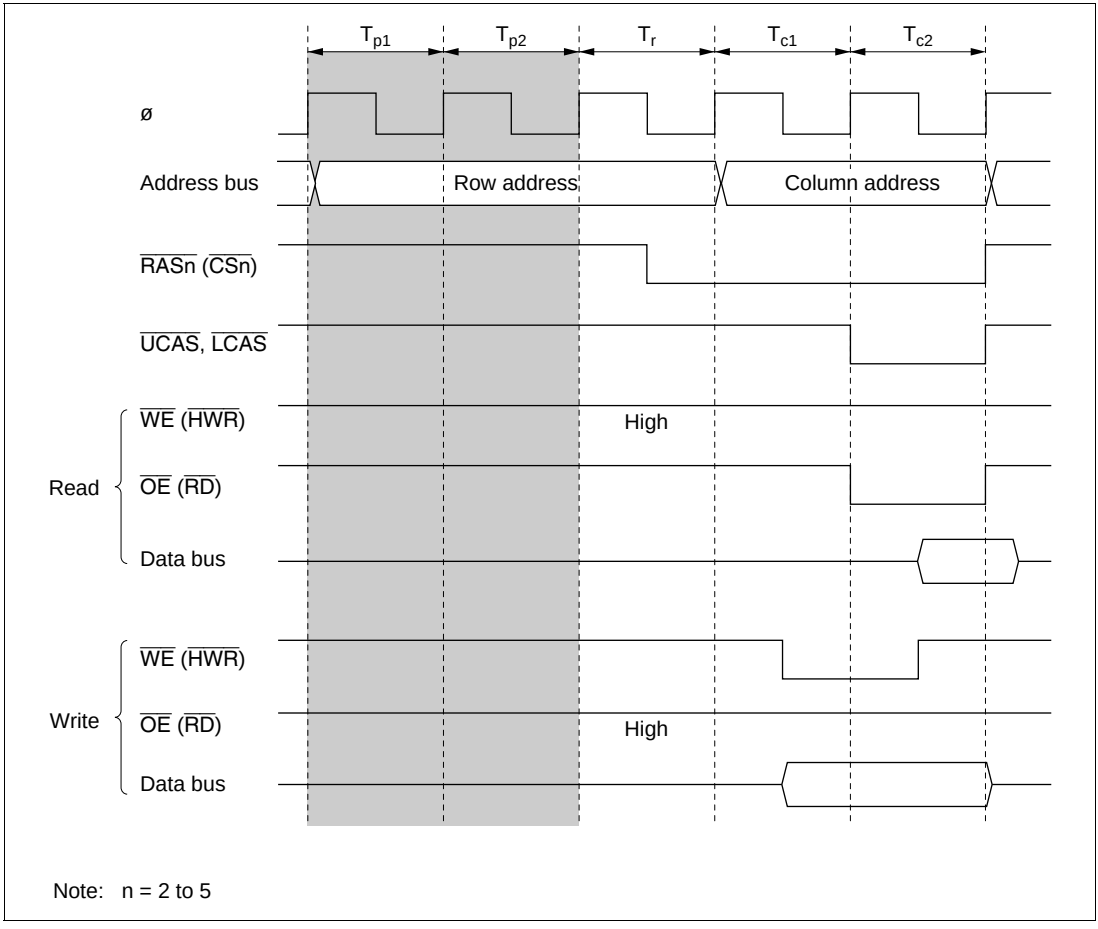


Figure 4.24 Example of Timing with Two-State Precharge Cycle (RAST = 0, CAST = 0)

4.5.10 Wait Control

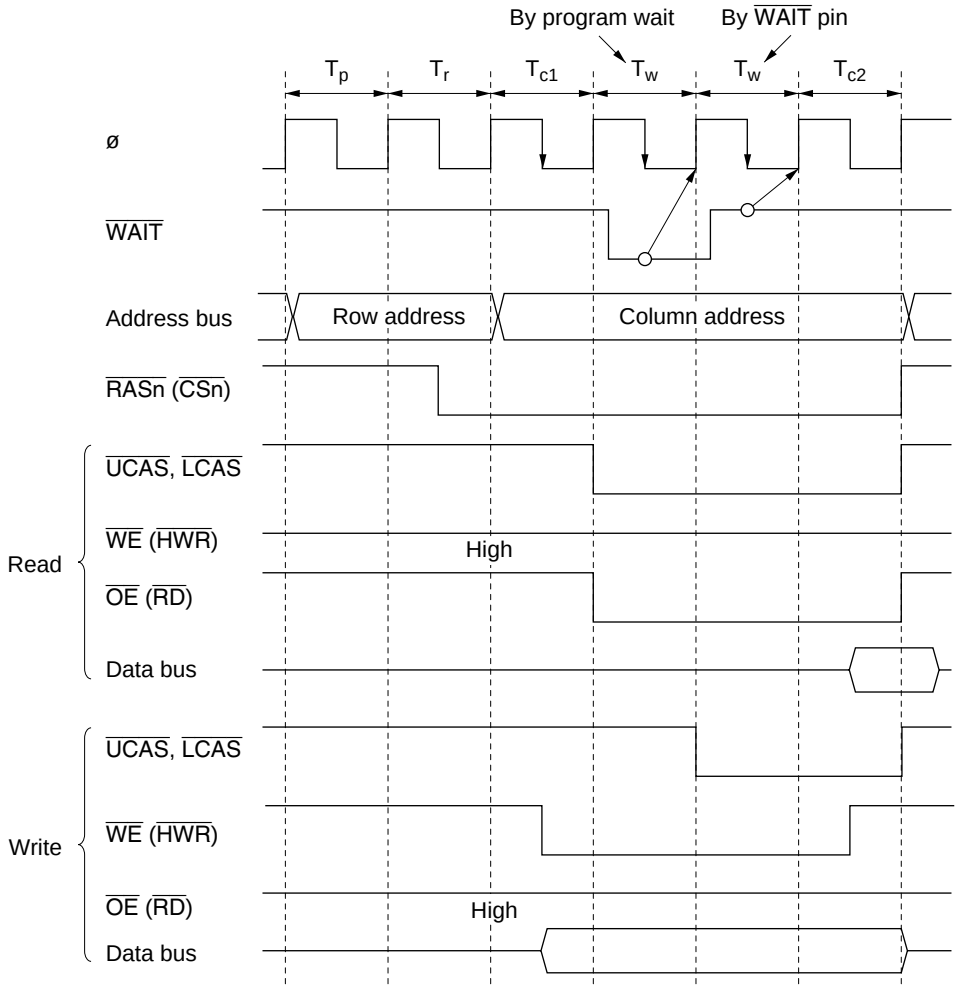
There are two ways of inserting wait states in a DRAM access cycle: (1) program wait insertion and (2) pin wait insertion using the $\overline{\text{WAIT}}$ pin.

Wait states are inserted to extend the $\overline{\text{CAS}}$ assertion period in a read access to DRAM space, and to extend the write data setup time relative to the falling edge of $\overline{\text{CAS}}$ in a write access.

Program Wait Insertion: When the bit in ASTCR corresponding to an area designated as DRAM space is set to 1, from 0 to 7 wait states can be inserted automatically between the T_{c1} state and T_{c2} state, according to the settings in registers WTCRA and WTCRB.

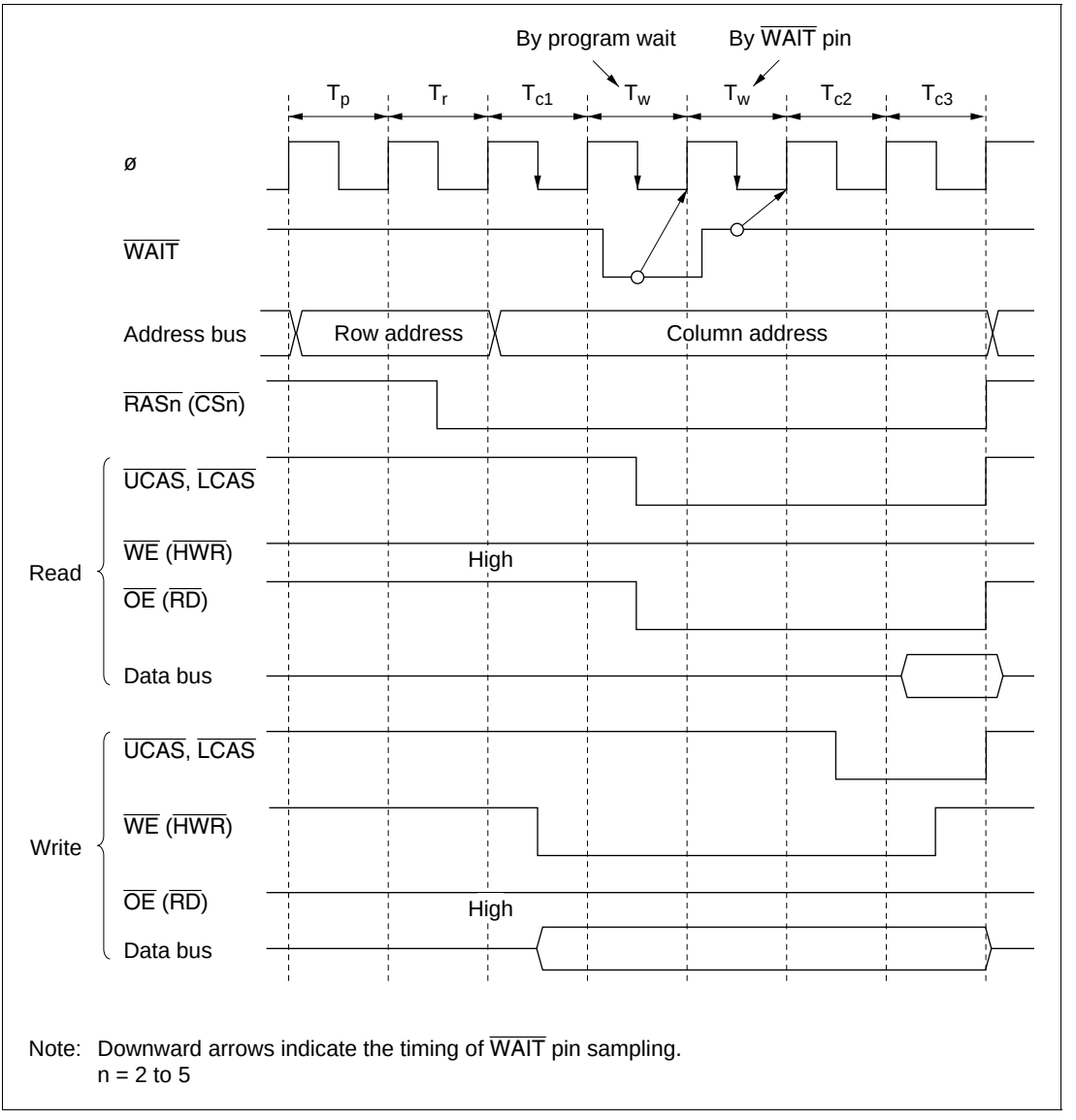
Pin Wait Insertion: When the WAITE bit in the BCR register is set to 1 and the ASTCR bit is set to 1, wait input by means of the $\overline{\text{WAIT}}$ pin is enabled. When DRAM space is accessed in this state, a program wait (T_w) is first inserted. If the $\overline{\text{WAIT}}$ pin is low at the falling edge of ø in the last T_{c1} or T_w state, another T_w state is inserted. If the $\overline{\text{WAIT}}$ pin is held low, T_w states are inserted until it goes high.

Figures 4.25 and 4.26 show examples of wait state insertion timing in the case of 2-state and 3-state column address output cycles.



Note: Downward arrows indicate the timing of WAIT pin sampling.
n = 2 to 5

Figure 4.25 Example of Wait State Insertion Timing (1)
(2-State Column Address Output)



Note: Downward arrows indicate the timing of WAIT pin sampling.
n = 2 to 5

Figure 4.26 Example of Wait State Insertion Timing (2)
(3-State Column Address Output)

4.5.11 Byte Access Control

When DRAM with a ×16 configuration is connected, the 2-CAS access method is used for the control signals needed for byte access.

Figure 4.27 shows the control timing for 2-CAS access, and figure 4.28 shows an example of 2-CAS DRAM connection.

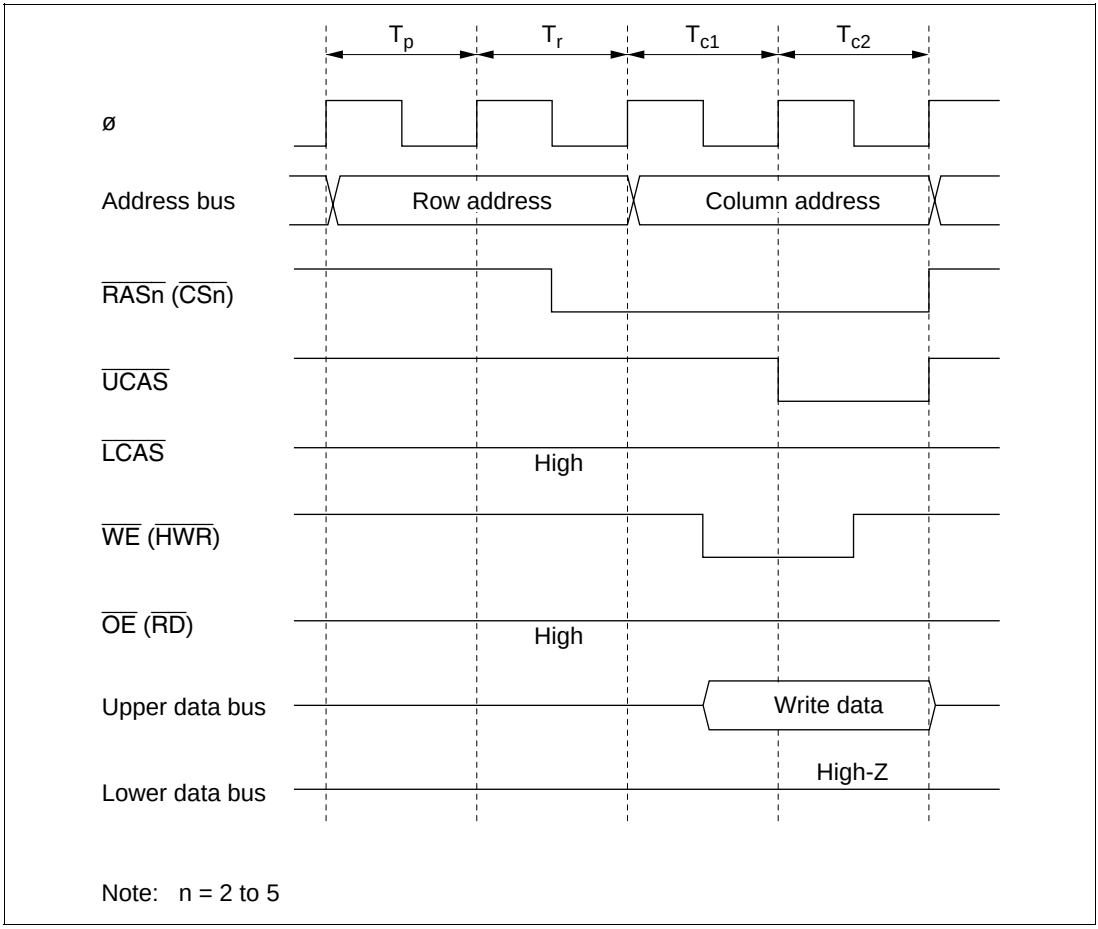


Figure 4.27 2-CAS Control Timing
(Upper Byte Write Access: RAST = 0, CAST = 0)

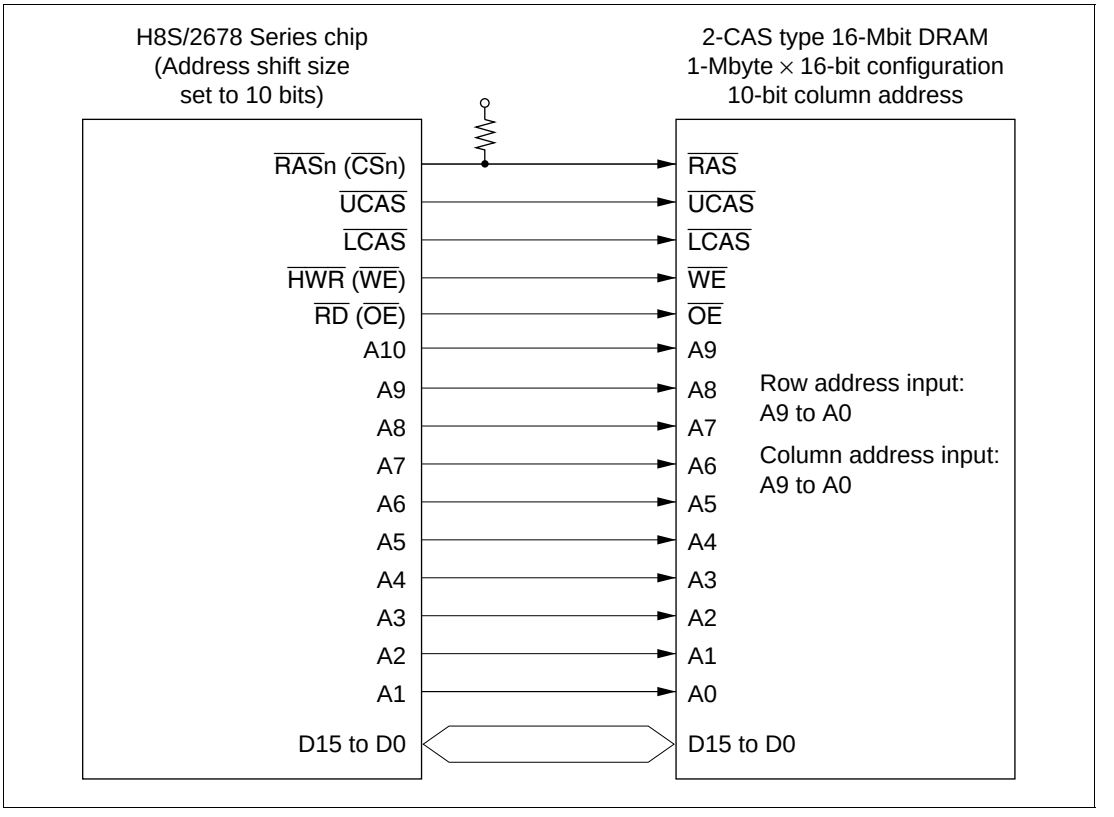


Figure 4.28 Example of 2-CAS DRAM Connection

4.5.12 Burst Operation

With DRAM, in addition to full access (normal access) in which data is accessed by outputting a row address for each access, a fast page mode is also provided which can be used when making consecutive accesses to the same row address. This mode enables fast (burst) access of data by simply changing the column address after the row address has been output. Burst access can be selected by setting the BE bit to 1 in DRAMCR.

Burst Access (Fast Page Mode) Operation Timing: Figures 4.29 and 4.30 show the operation timing for burst access. When there are consecutive access cycles for DRAM space, the $\overline{\text{CAS}}$ signal and column address output cycles (two states) continue as long as the row address is the same for consecutive access cycles. The row address used for the comparison is set with bits MXC2 to MXC0 in DRAMCR.

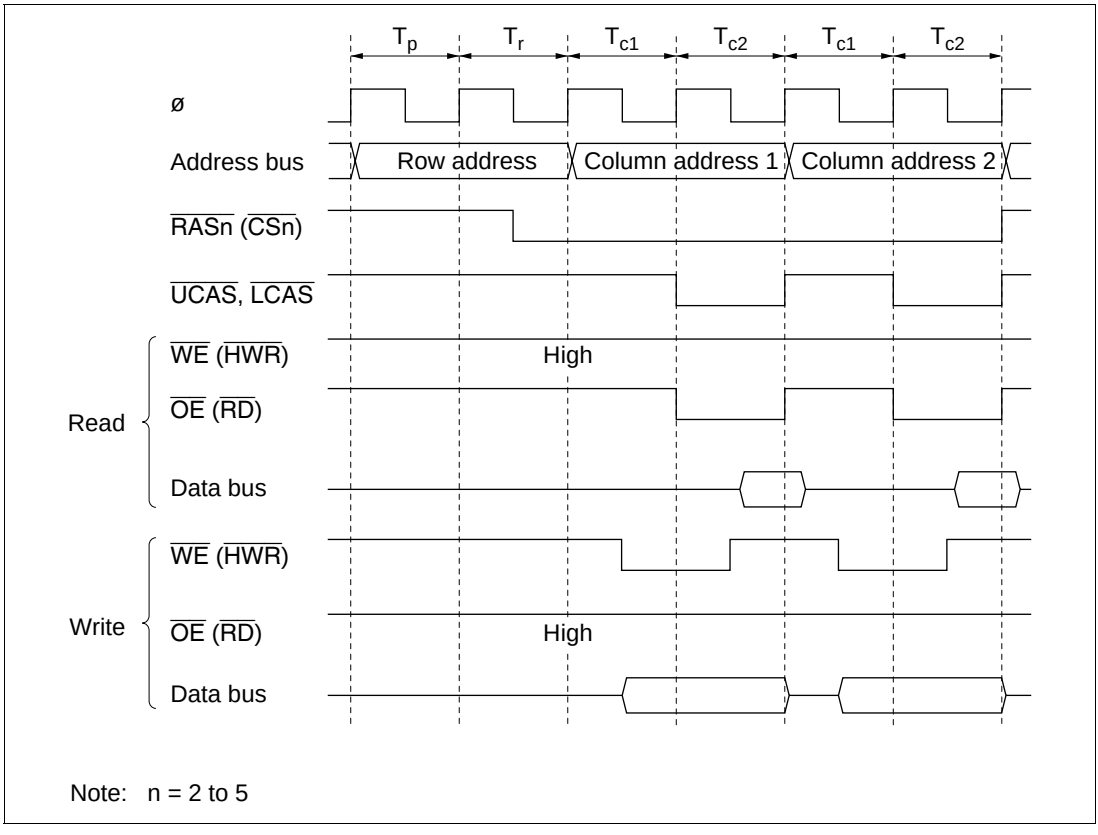


Figure 4.29 Operation Timing in Fast Page Mode (1)
(RAST = 0, CAST = 1)

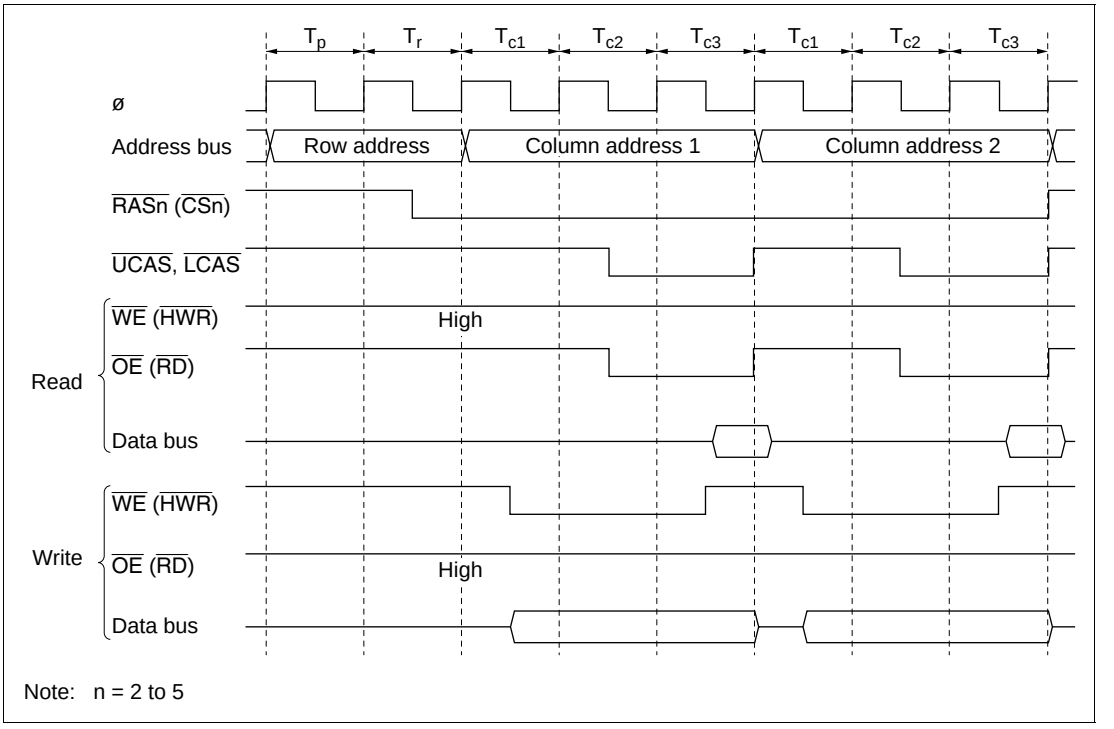


Figure 4.30 Operation Timing in Fast Page Mode (2)
(RAST = 0, CAST = 1)

The bus cycle can also be extended in burst access by inserting wait states. The wait state insertion method and timing are the same as for full access. For details see section 4.5.10, Wait Control.

RAS Down Mode and RAS Up Mode: Even when burst operation is selected, it may happen that access to DRAM space is not continuous, but is interrupted by access to another space. In this case, if the $\overline{RAS}$ signal is held low during the access to the other space, burst operation can be resumed when the same row address in DRAM space is accessed again.

- RAS Down Mode

  To select RAS down mode, set both the RCDM bit and the BE bit to 1 in DRAMCR. If access to DRAM space is interrupted and another space is accessed, the $\overline{RAS}$ signal is held low during the access to the other space, and burst access is performed when the row address of the next DRAM space access is the same as the row address of the previous DRAM space access. Figure 4.31 shows an example of the timing in RAS down mode.

  Note, however, that the $\overline{RAS}$ signal will go high if:

  — a refresh operation is initiated in the RAS down state

  — self-refreshing is performed

  — the chip enters software standby mode

— the external bus is released

— the RCDM bit or BE bit is cleared to 0

If a transition is made to the all-module-clocks-stopped mode in the $\overline{RAS}$ down state, the clock will stop with $\overline{RAS}$ low. To enter the all-module-clocks-stopped mode with $\overline{RAS}$ high, the RCDM bit must be cleared to 0 before executing the SLEEP instruction.

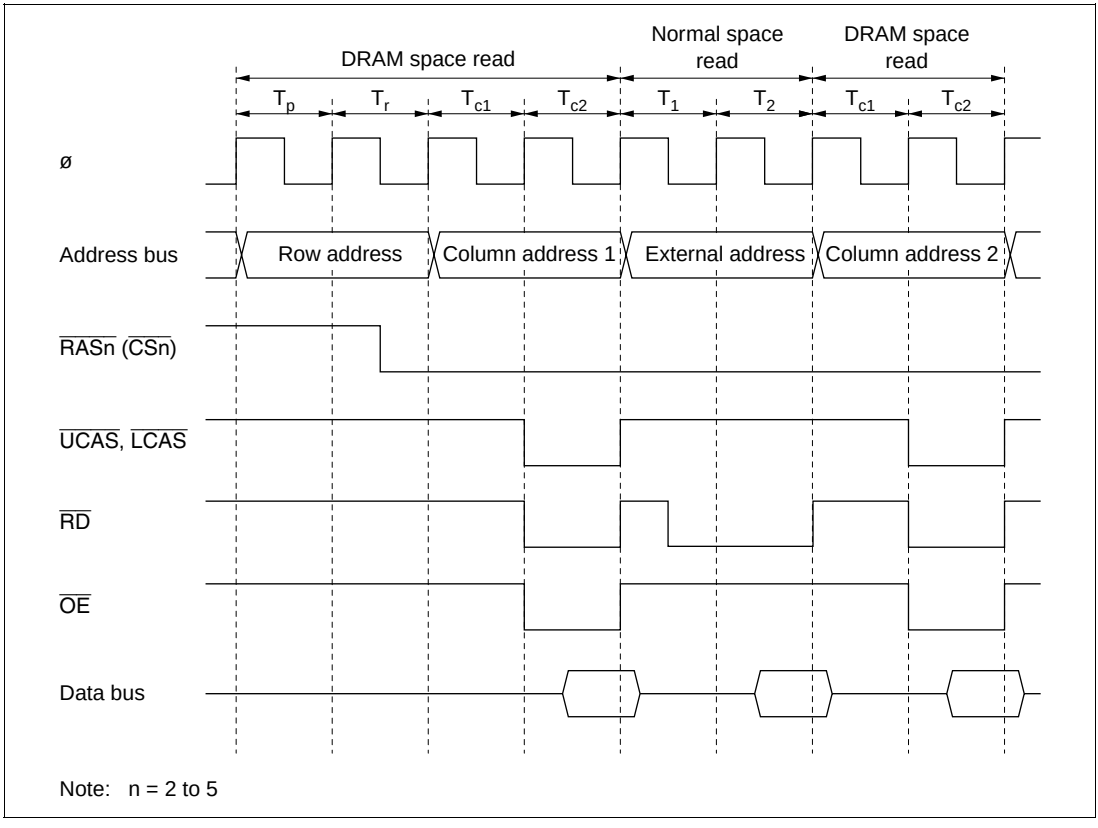


Figure 4.31 Example of Operation Timing in RAS Down Mode (RAST = 0, CAST = 0)

- RAS Up Mode

  To select RAS up mode, clear the RCDM bit to 0 in DRAMCR. Each time access to DRAM space is interrupted and another space is accessed, the $\overline{RAS}$ signal goes high again. Burst operation is only performed if DRAM space is continuous. Figure 4.32 shows an example of the timing in RAS up mode.

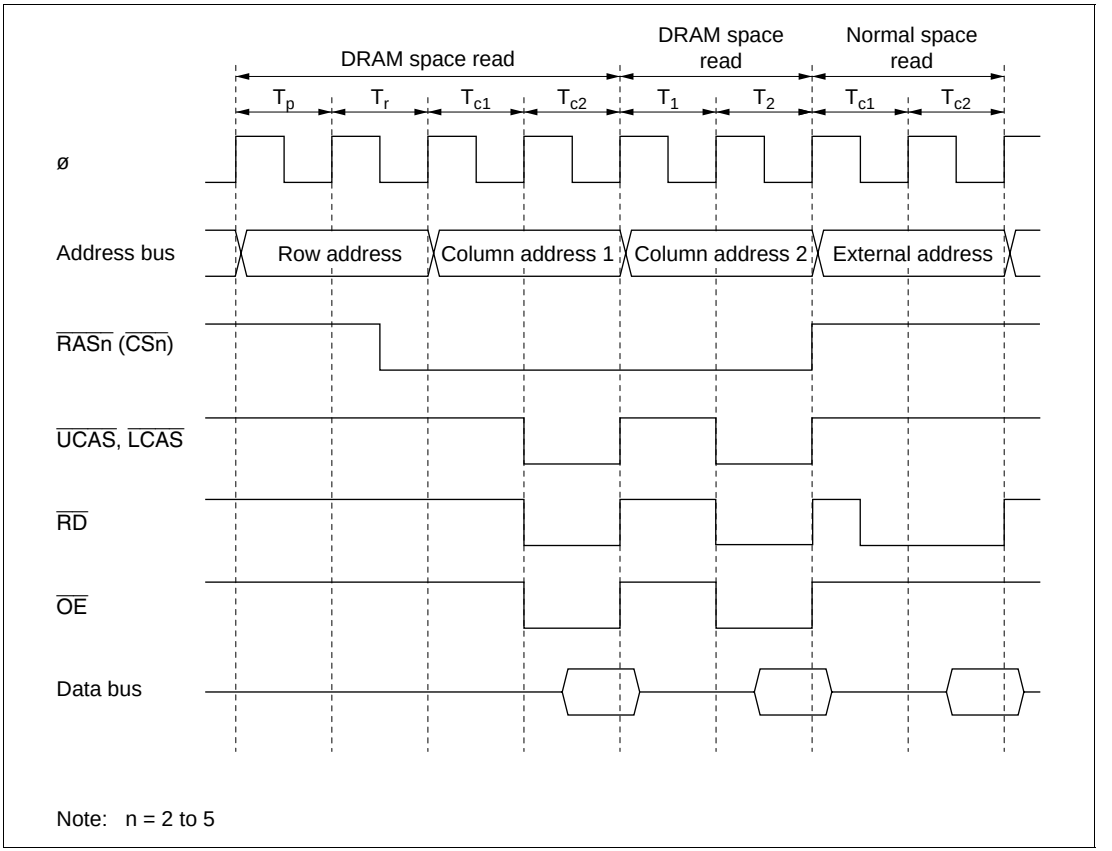


Figure 4.32 Example of Operation Timing in RAS Up Mode (RAST = 0, CAST = 0)

4.5.13 Refresh Control

The H8S/2678 Series is provided with a DRAM refresh control function. CAS-before-RAS (CBR) refreshing is used.

In addition, self-refreshing can be executed when the chip enters the software standby state.

Refresh control is enabled when any area is designated as DRAM space in accordance with the setting of bits RMTS2 to RMTS0 in the DRAMCR register.

CAS-before-RAS (CBR) Refreshing: To select CBR refreshing, set the RFSHE bit to 1 in DRAMCR.

With CBR refreshing, RTCNT counts up using the input clock selected by bits RTCK2 to RTCK0 in REFCR, and when the count matches the value set in RTCOR (compare match), refresh control is performed. At the same time, RTCNT is reset and starts counting up again from H'00.

Refreshing is thus repeated at fixed intervals determined by RTCOR and bits RTCK2 to RTCK0. Set a value in RTCOR and bits RTCK2 to RTCK0 that will meet the refreshing interval specification for the DRAM used.

When bits RTCK2 to RTCK0 are set, RTCNT starts counting up. RTCNT and RTCOR settings should therefore be completed before setting bits RTCK2 to RTCK0.

RTCNT operation is shown in figure 4.33, compare match timing in figure 4.34, and CBR refresh timing in figure 4.35.

When the CBRM bit is cleared to 0, access to external space other than DRAM space is performed in parallel during the CBR refresh period.

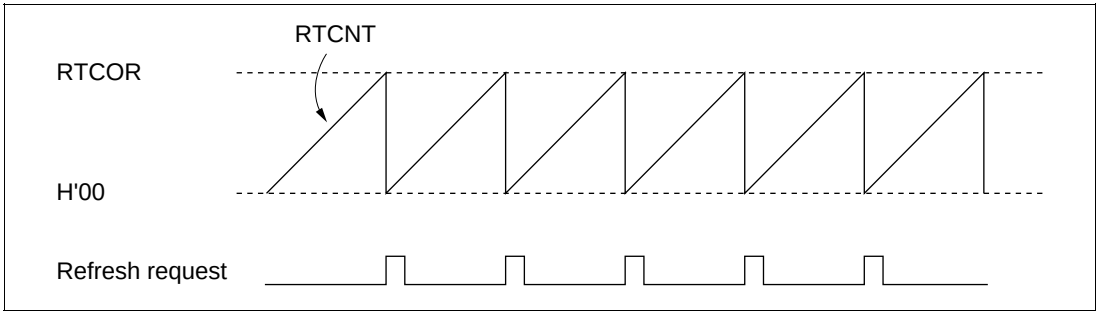


Figure 4.33 RTCNT Operation

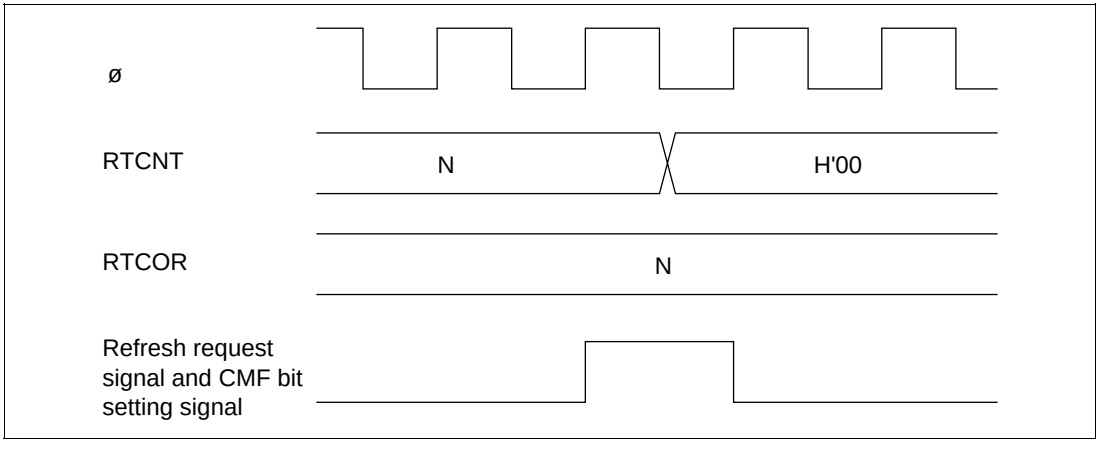


Figure 4.34 Compare match Timing

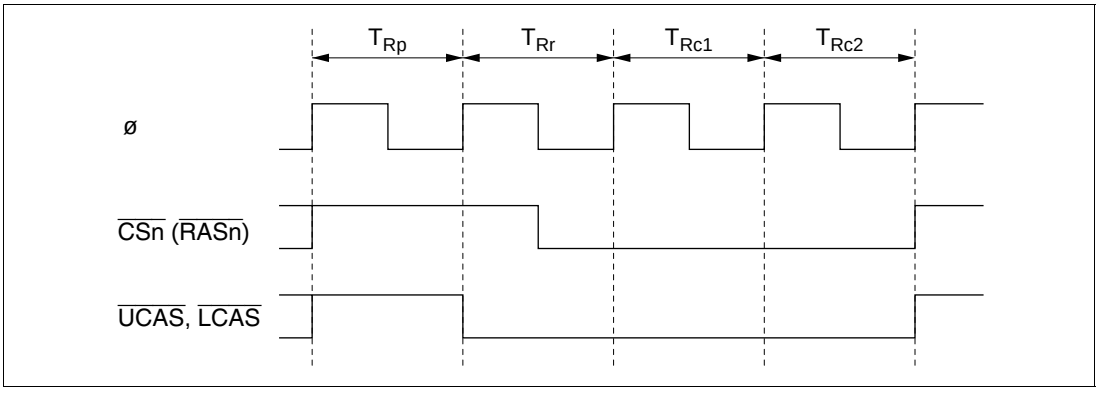


Figure 4.35 CBR Refresh Timing

A setting can be made in bits RCW1 and RCW0 to delay $\overline{RAS}$ signal output by one to three cycles. Use bits RLW1 and RLW0 to adjust the width of the $\overline{RAS}$ signal. The settings of bits RCW1, RCW0, RLW1, and RLW0 are valid only in refresh operations.

Figure 4.36 shows the timing when bits RCW1 and RCW0 are set to 0 and 1, respectively.

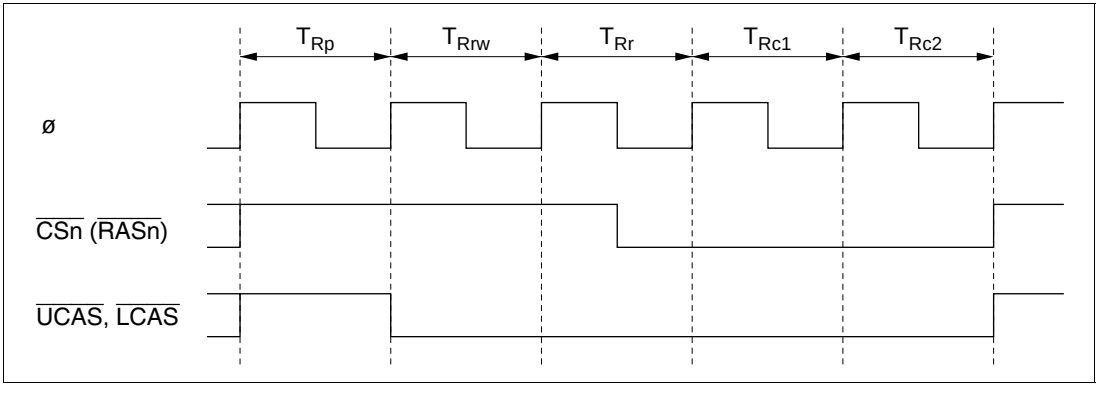


Figure 4.36 CBR Refresh Timing
(RCW1 = 0, RCW0 = 1, RLW1 = 0, RLW0 = 0)

Depending on the DRAM used, modification of the $\overline{WE}$ signal may not be permitted during the refresh period. In this case, the CBRM bit should be set to 1. The bus controller will then insert refresh cycles in appropriate breaks between bus cycles. Figure 4.37 shows an example of the timing when the CBRM bit is set to 1. In this case the $\overline{CS}$ signal is not controlled, and retains its value prior to the start of the refresh period.

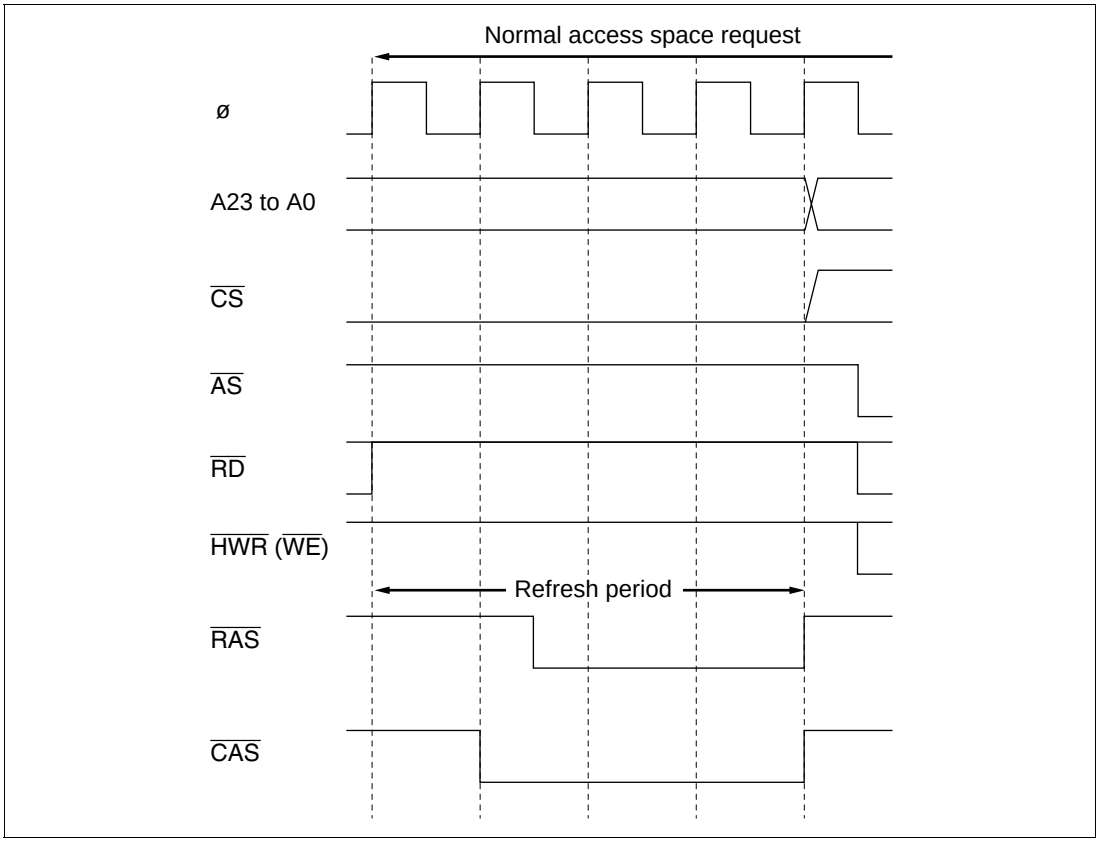


Figure 4.37 Example of CBR Refresh Timing (CBRM = 1)

Self-Refreshing: A self-refresh mode (battery backup mode) is provided for DRAM as a kind of standby mode. In this mode, refresh timing and refresh addresses are generated within the DRAM.

To select self-refreshing, set the RFSHE bit and SLFRF bit to 1 in the REFCR register. When a SLEEP instruction is executed to enter software standby mode, the $\overline{CAS}$ and $\overline{RAS}$ signals are output and DRAM enters self-refresh mode, as shown in figure 4.38.

When software standby mode is exited, the SLFRF bit is cleared to 0 and self-refresh mode is exited automatically.

If a CBR refresh request occurs when making a transition to software standby mode, CBR refreshing is executed, then self-refresh mode is entered.

When using self-refresh mode, the OPE bit must not be cleared to 0 in the SBYCR register.

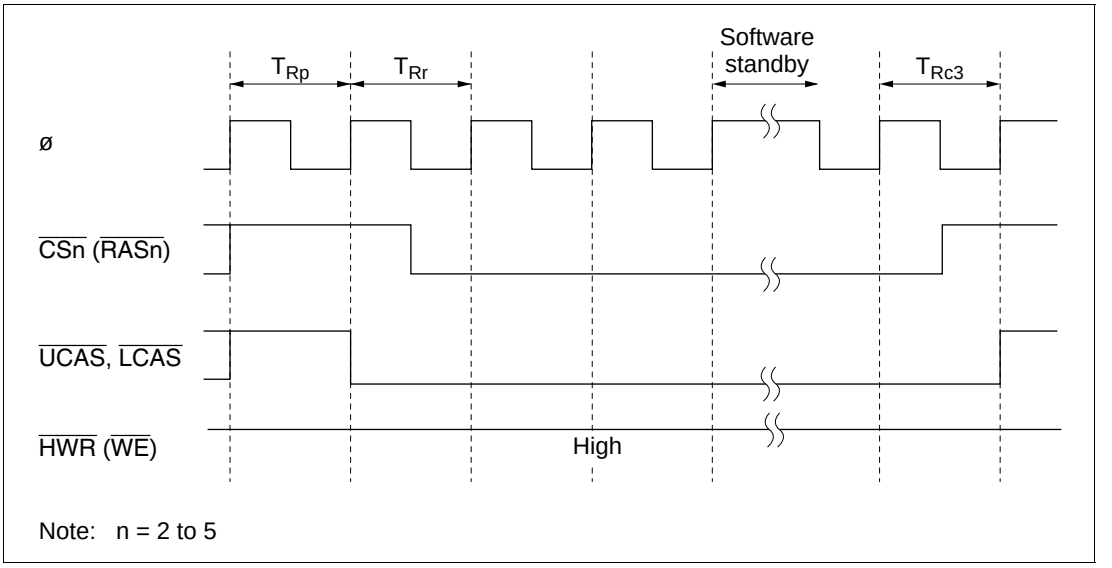


Figure 4.38 Self-Refresh Timing

In some DRAMs provided with a self-refresh mode, the $\overline{RAS}$ signal precharge time after self-refreshing is longer than the normal precharge time. A setting can be made in bits TPCS2 to TPCS0 in the REFCR register to make the precharge time after self-refreshing from 1 to 7 states longer than the normal precharge time. In this case, too, normal precharging is performed according to the setting of bits TPC1 and TPC0 in the DRACCR register, and therefore a setting should be made to give the optimum post-self-refresh precharge time, including this time. Figure 4.39 shows an example of the timing when the precharge time after self-refreshing is extended by 2 states.

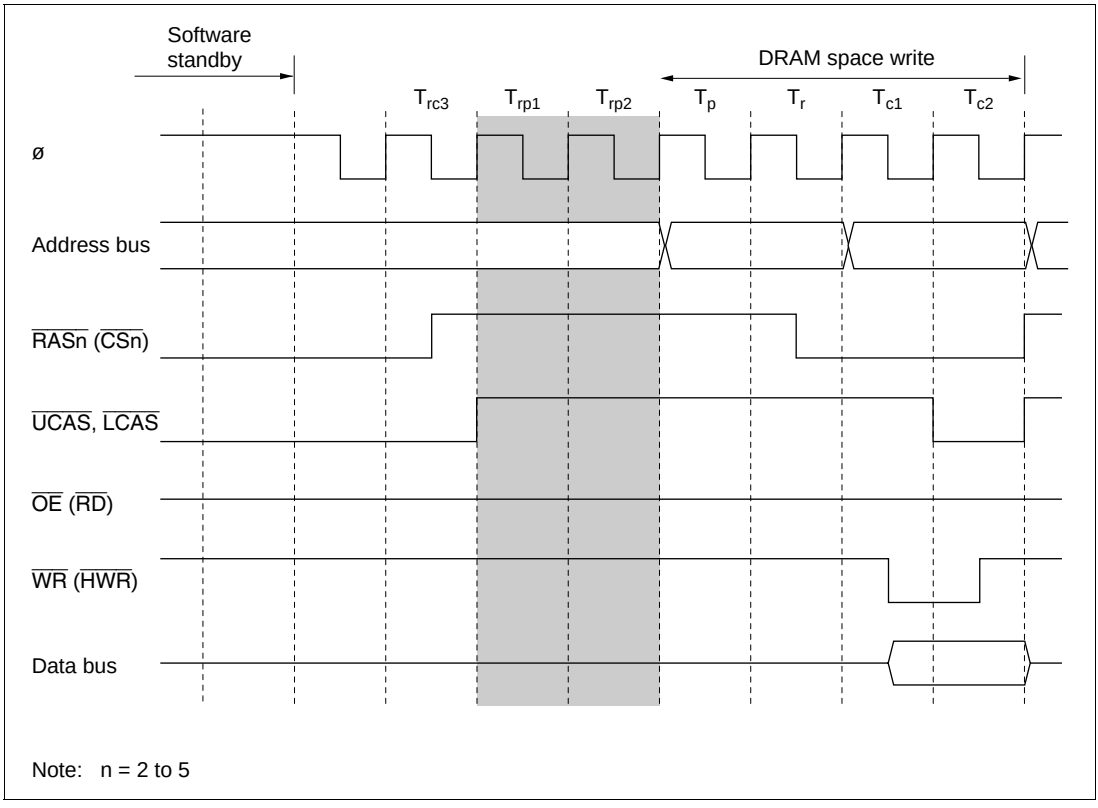


Figure 4.39 Example of Timing when Precharge Time after Self-Refreshing Is Extended by 2 States

Refreshing and All-Module-Clocks-Stopped Mode: In the H8S/2678 Series, if the ACSE bit is set to 1 in the MSTPCR register, and then a SLEEP instruction is executed with the setting for all supporting module clocks to be stopped (MSTPCR = H'FFFF) or for operation of the 8-bit timer module alone (MSTPCR = H'FFFE), and a transition is made to the sleep state, the all-module-clocks-stopped mode is entered, in which the bus controller and I/O port clocks are also stopped.

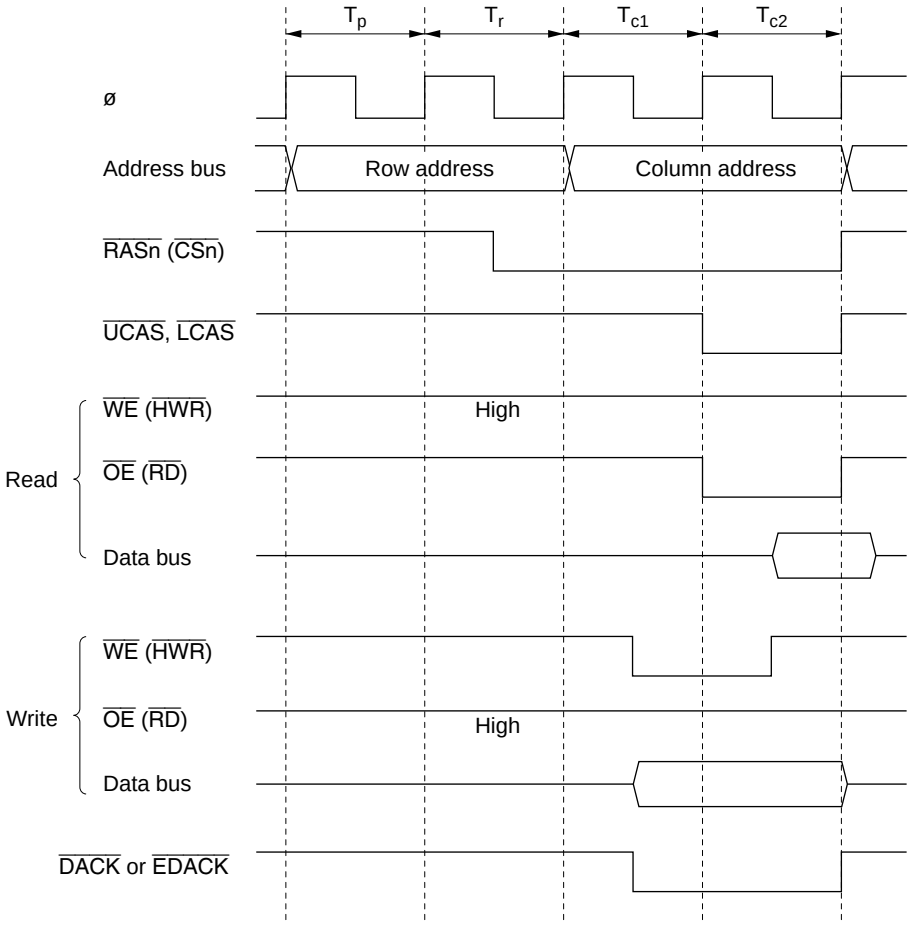
As the bus controller clock is also stopped in this mode, CBR refreshing is not executed. If DRAM is connected externally and DRAM data is to be retained in sleep mode, the ACSE bit must be cleared to 0 in MSTPCR.

4.5.14 DMAC and EXDMAC Single Address Transfer Mode and DRAM Interface

When burst mode is selected on the DRAM interface, the $\overline{DACK}$ and $\overline{EDACK}$ output timing can be selected with the DDS and EDDS bits. When DRAM space is accessed in DMAC/EXDMAC single address mode at the same time, these bits select whether or not burst access is to be performed.

When DDS = 1 or EDDS = 1: Burst access is performed by determining the address only, irrespective of the bus master. With the DRAM interface, the $\overline{\text{DACK}}$ or $\overline{\text{EDACK}}$ output goes low from the T_{c1} state.

Figure 4.40 shows the $\overline{\text{DACK}}$/$\overline{\text{EDACK}}$ output timing for the DRAM interface when DDS = 1 or EDDS = 1.



Note: n = 2 to 5

Figure 4.40 Example of $\overline{\text{DACK}}$/$\overline{\text{EDACK}}$ Output Timing when DDS = 1 or EDDS = 1 (1) (RAST = 0, CAST = 0)

When DDS = 0 or EDDS = 0: When DRAM space is accessed in DMAC or EXDMAC single address transfer mode, full access (normal access) is always performed. With the DRAM interface, the $\overline{\text{DACK}}$ or $\overline{\text{EDACK}}$ output goes low from the T_r state.

In modes other than DMAC or EXDMAC single address transfer mode, burst access can be used when accessing DRAM space.

Figure 4.41 shows the $\overline{\text{DACK}}$/$\overline{\text{EDACK}}$ output timing for the DRAM interface when DDS = 0 or EDDS = 0.

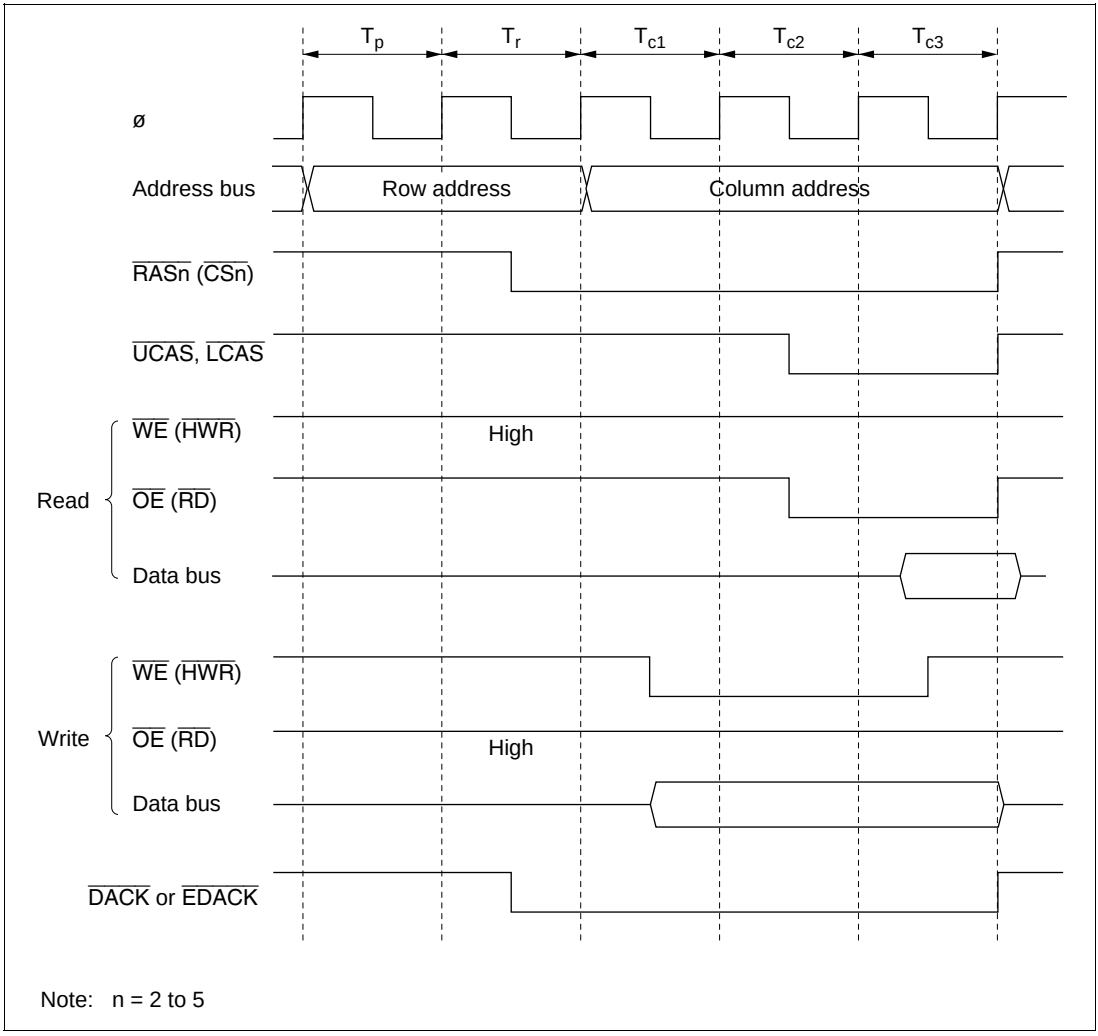


Figure 4.41 Example of $\overline{\text{DACK}}$/$\overline{\text{EDACK}}$ Output Timing when DDS = 0 or EDDS = 0 (2) (RAST = 0, CAST = 1)

4.6 Burst ROM Interface

4.6.1 Overview

In the H8S/2678 Series, external space areas 0 and 1 can be designated as burst ROM space, and burst ROM interfacing performed. The burst ROM space interface enables ROM with burst access capability to be accessed at high speed.

Areas 1 and 0 can be designated as burst ROM space by means of bits BSRM1 and BSRM0 in BROMCR. Consecutive burst accesses of a maximum or 4, 8, 16, or 32 words can be performed, according to the BROMCR register setting. From 1 to 8 states can be selected for burst access.

Settings can be made independently for area 0 and area 1.

In burst ROM interface space, burst access covers only CPU read accesses.

4.6.2 Basic Timing

The number of states in the initial cycle (full access) on the burst ROM interface is determined by the basic bus interface settings in the ASTCR, ABWCR, WTCRA, WTCRB, and CSACRH registers. When area 0 or area 1 is designated as burst ROM interface space, the settings in the RDCNR and CSACRL registers are ignored.

From 1 to 8 states can be selected for the burst cycle, according to the settings of bits BSTS02 to BSTS00 and BSTS12 to BSTS10 in BROMCR. Wait states cannot be inserted. Burst access of up to 32 words is performed, according to the settings of bits BSTS01, BSTS00, BSTS11, and BSTS10 in BROMCR

The basic access timing for burst ROM space is shown in figures 4.42 and 4.43. Figure 4.42 shows the timing when ASTn = 1 and a 2-state burst cycle is set, and figure 4.43 shows the timing when ASTn = 0 and a 1-state burst cycle is set.

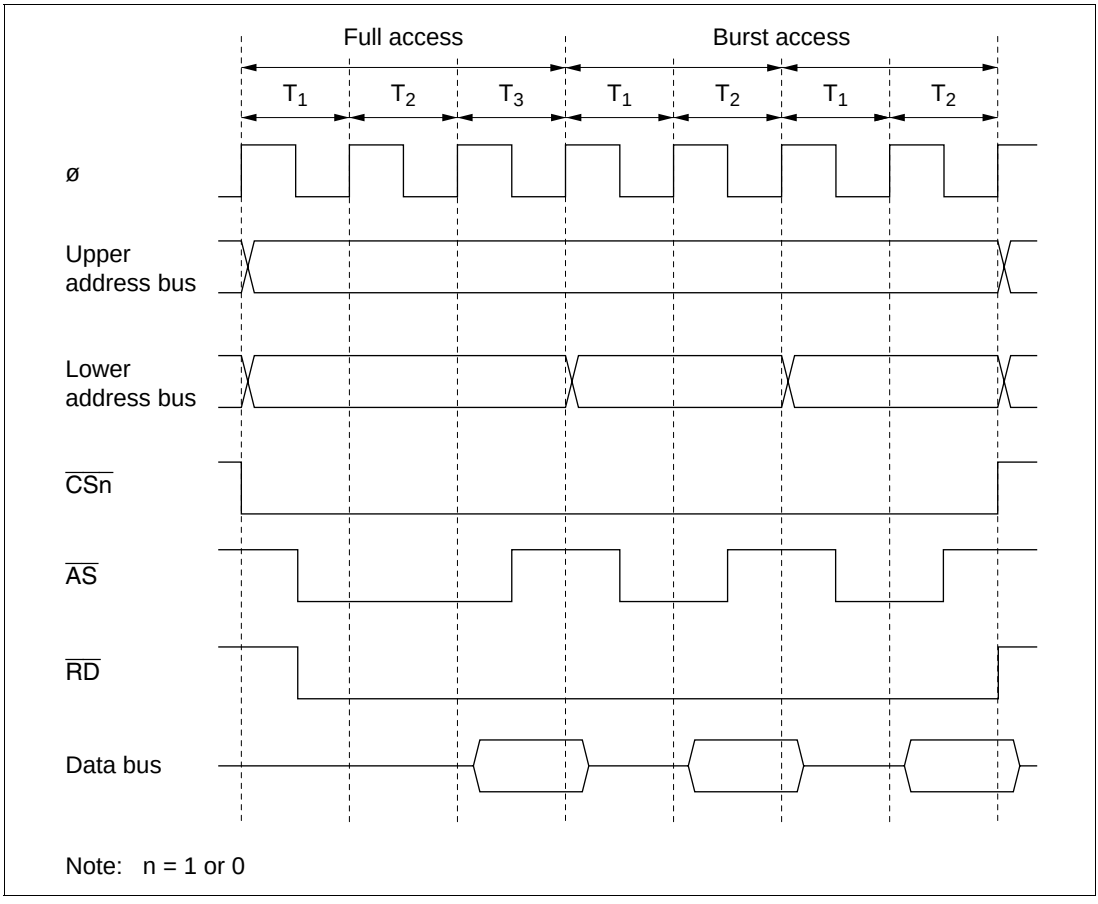


Figure 4.42 Example of Burst ROM Access Timing (1)
(ASTn = 1, 2-State Burst Cycle)

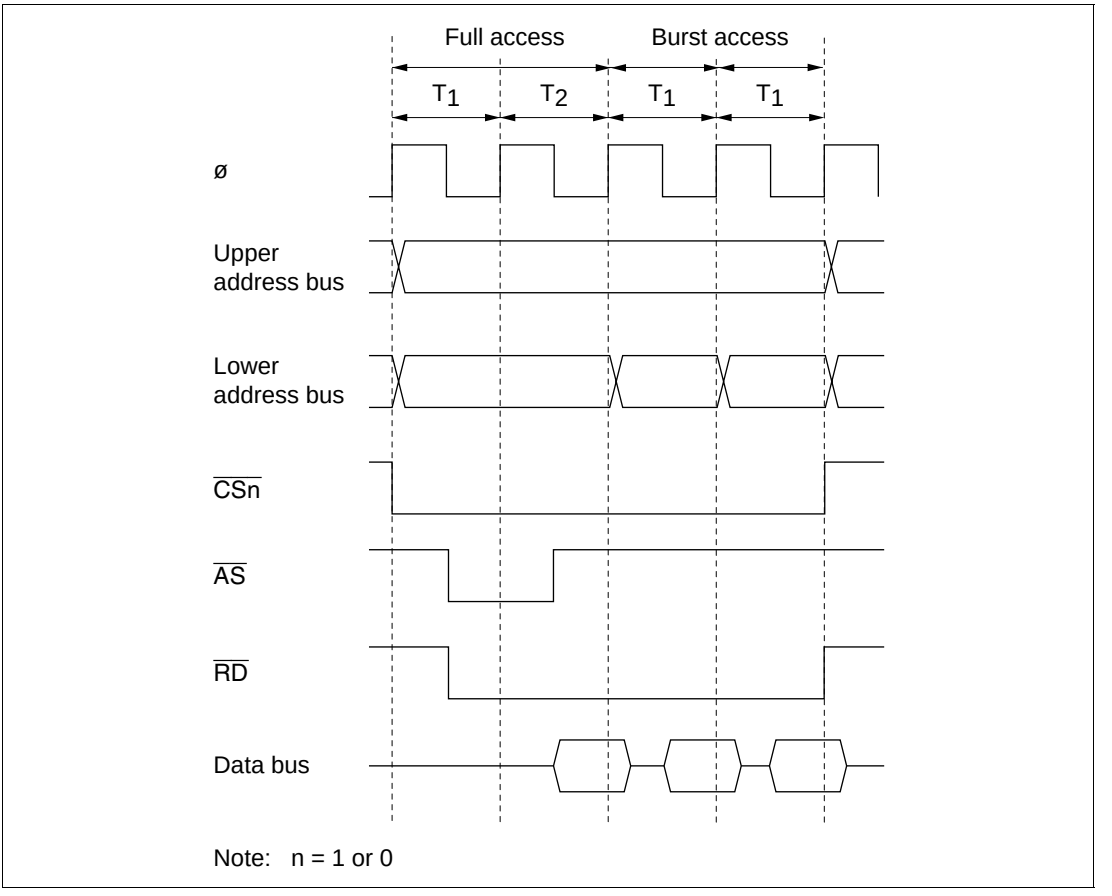


Figure 4.43 Example of Burst ROM Access Timing (2) (ASTn = 0, 1-State Burst Cycle)

4.6.3 Wait Control

As with the basic bus interface, either (1) program wait insertion or (2) pin wait insertion using the $\overline{\text{WAIT}}$ pin can be used in the initial cycle (full access) on the burst ROM interface. See section 4.4.5, Wait Control.

Wait states cannot be inserted in a burst cycle.

4.6.4 Write Access

When a write access to burst ROM interface space is executed, burst access is interrupted at that point and the write access is executed in line with the basic bus interface settings.

Write accesses are not performed in burst mode even though burst ROM space is designated.

4.7 Idle Cycle

4.7.1 Operation

When the H8S/2678 Series chip accesses external space, it can insert an idle cycle (T_i) between bus cycles in the following two cases: (1) when read accesses in different areas occur consecutively, and (2) when a write cycle occurs immediately after a read cycle. Insertion of a 1-state or 2-state idle cycle can be selected with the IDLC bit in the BCR register.

By inserting an idle cycle it is possible, for example, to avoid data collisions between ROM, etc., with a long output floating time, and high-speed memory, I/O interfaces, and so on.

Consecutive Reads in Different Areas: If consecutive reads in different areas occur while the ICIS1 bit is set to 1 in the BCR register, an idle cycle is inserted at the start of the second read cycle.

Figure 4.44 shows an example of the operation in this case. In this example, bus cycle A is a read cycle for ROM with a long output floating time, and bus cycle B is a read cycle for SRAM, each being located in a different area. In (a), an idle cycle is not inserted, and a collision occurs in bus cycle B between the read data from ROM and that from SRAM. In (b), an idle cycle is inserted, and a data collision is prevented.

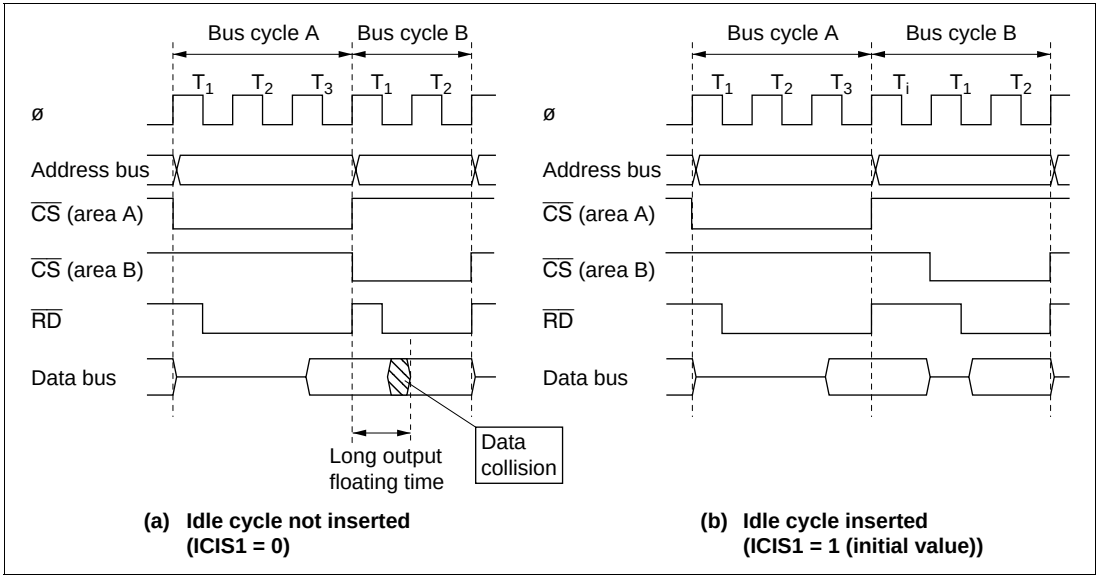


Figure 4.44 Example of Idle Cycle Operation (1) (Consecutive Reads in Different Areas)

Write after Read: If an external write occurs after an external read while the ICIS0 bit is set to 1 in the BCR register, an idle cycle is inserted at the start of the write cycle.

Figure 4.45 shows an example of the operation in this case. In this example, bus cycle A is a read cycle for ROM with a long output floating time, and bus cycle B is a CPU write cycle. In (a), an idle cycle is not inserted, and a collision occurs in bus cycle B between the read data from ROM and the CPU write data. In (b), an idle cycle is inserted, and a data collision is prevented.

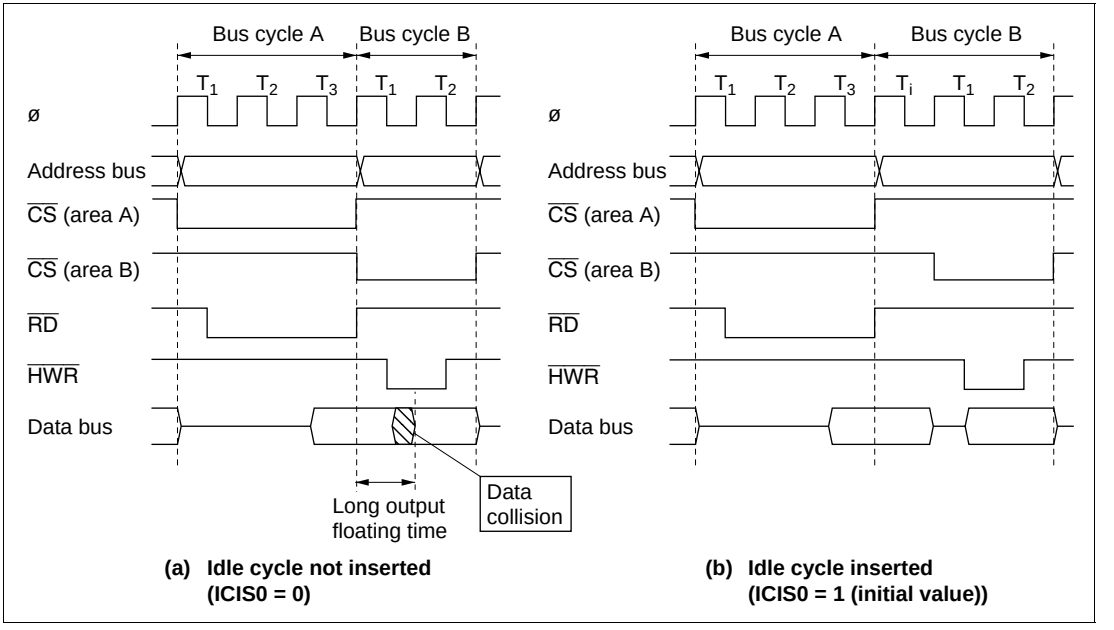


Figure 4.45 Example of Idle Cycle Operation (2) (Write after Read)

Relationship between Chip Select ($\overline{CS}$) Signal and Read ($\overline{RD}$) Signal: Depending on the system's load conditions, the $\overline{RD}$ signal may lag behind the $\overline{CS}$ signal. An example is shown in figure 4.46.

In this case, with the setting for no idle cycle insertion (a), there may be a period of overlap between the bus cycle A $\overline{RD}$ signal and the bus cycle B $\overline{CS}$ signal.

Setting idle cycle insertion, as in (b), however, will prevent any overlap between the $\overline{RD}$ and $\overline{CS}$ signals.

In the initial state after reset release, idle cycle insertion (b) is set.

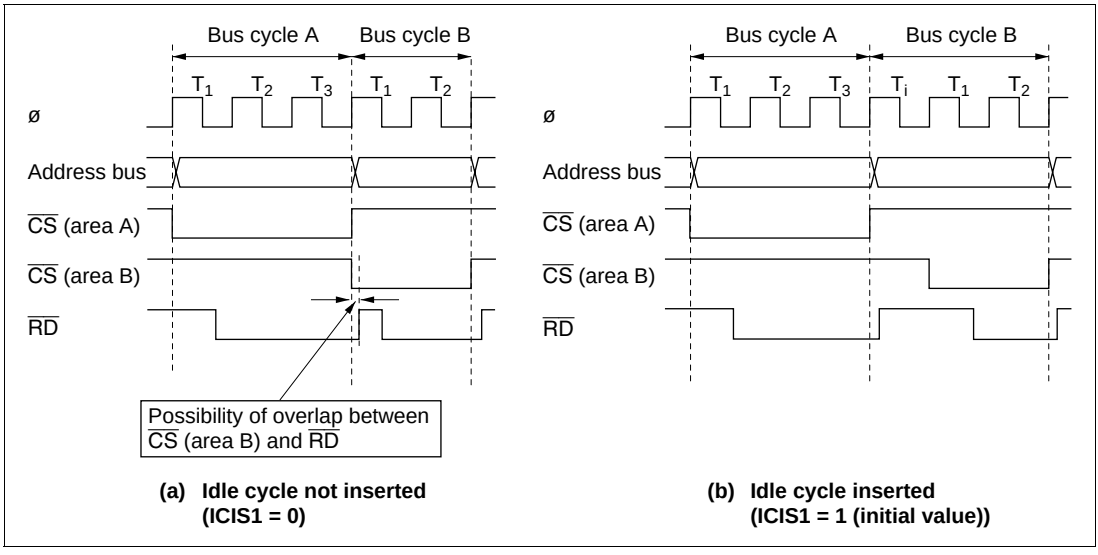


Figure 4.46 Relationship between Chip Select ($\overline{CS}$) and Read ($\overline{RD}$)

Idle Cycle in Case of DRAM Space Access after Normal Space Access: In a DRAM space access following a normal space access, the settings of bits ICIS1, ICIS0, and IDLC are valid.

However, in the case of consecutive reads in different areas, for example, if the second read is a full access to DRAM space, only a T_p cycle is inserted, and a T_i cycle is not. The timing in this case is shown figure 4.47.

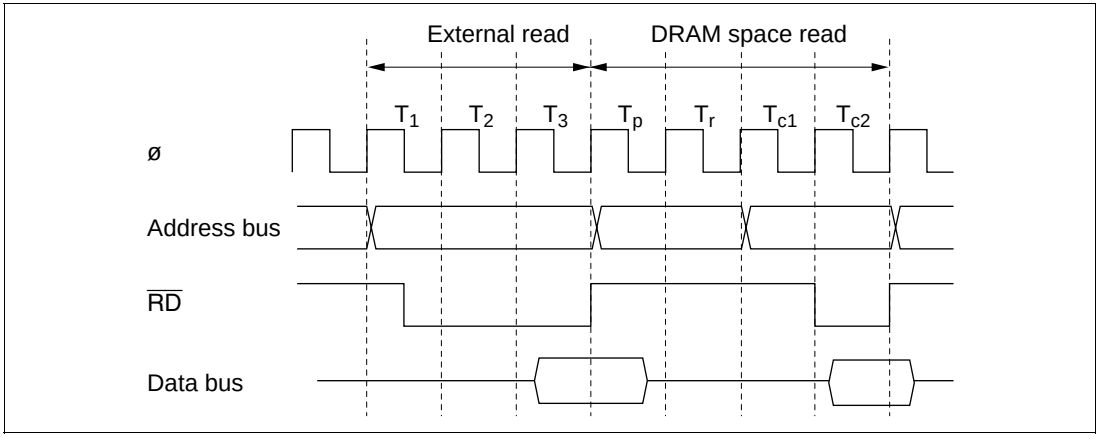


Figure 4.47 Example of DRAM Full Access after External Read (CAST = 0)

In burst access in RAS down mode, the settings of bits ICIS1, ICIS0, and IDLC are valid and an idle cycle is inserted. The timing in this case is illustrated in figures 4.48 and 4.49.

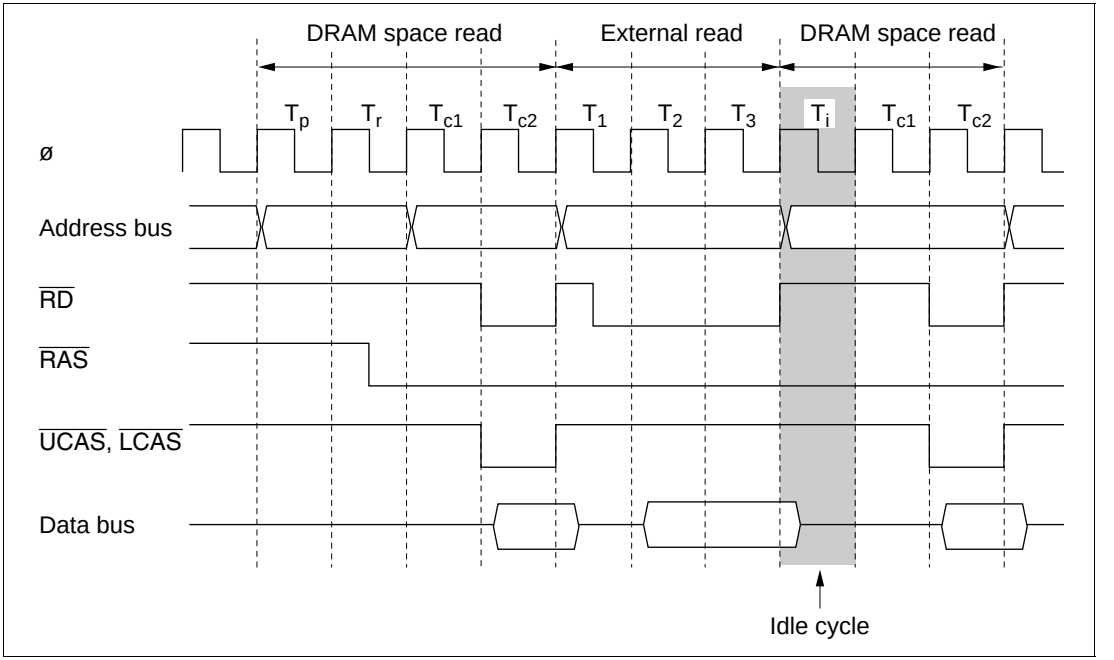


Figure 4.48 Example of Idle Cycle Operation in RAS Down Mode (1) (Consecutive Reads in Different Areas) (IDLC = 0, RAST = 0, CAST = 0)

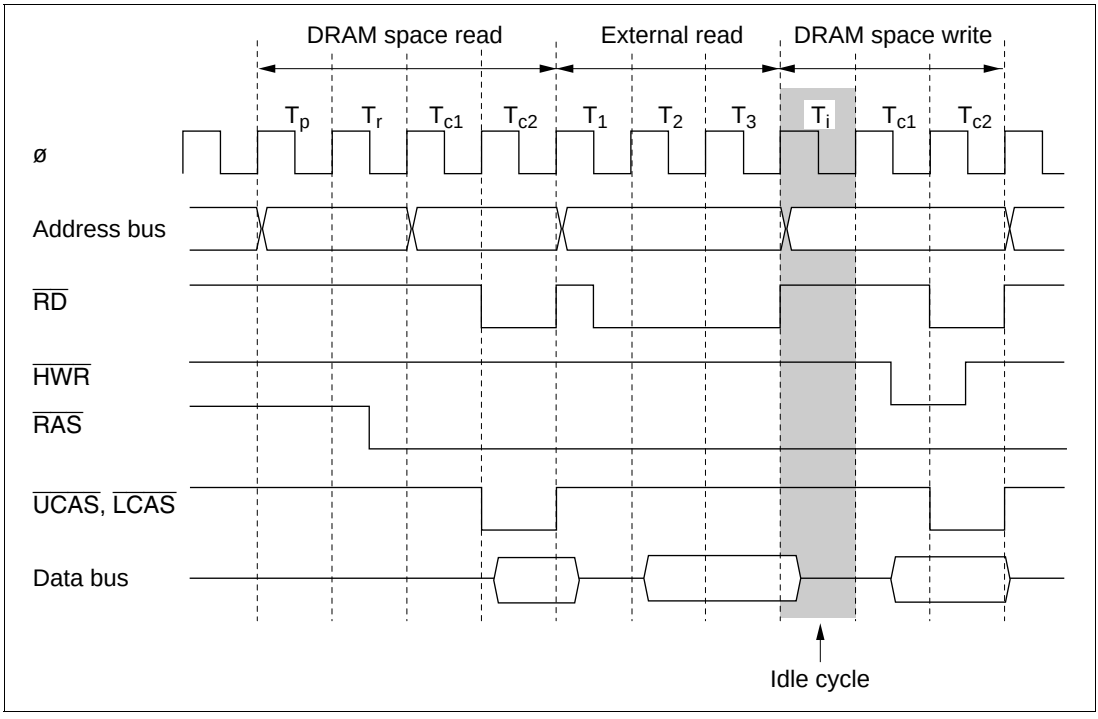


Figure 4.49 Example of Idle Cycle Operation in RAS Down Mode (2) (Read after Write) (IDLC = 0, RAST = 0, CAST = 0)

Idle Cycle in Case of Normal Space Access after DRAM Space Access: While the DRMI bit is cleared to 0 in the DRACCR register, idle cycle insertion after DRAM space access is disabled. Idle cycle insertion after DRAM space access can be enabled by setting the DRMI bit to 1. The conditions and number of states of the idle cycle to be inserted are in accordance with the settings of bits ICIS1, ICIS0, and IDLC are valid. Figures 4.50 and 4.51 show examples of idle cycle operation when the DRMI bit is set to 1.

When the DRMI bit is cleared to 0, an idle cycle is not inserted after DRAM space access even if bits ICIS1 and ICIS0 are set to 1.

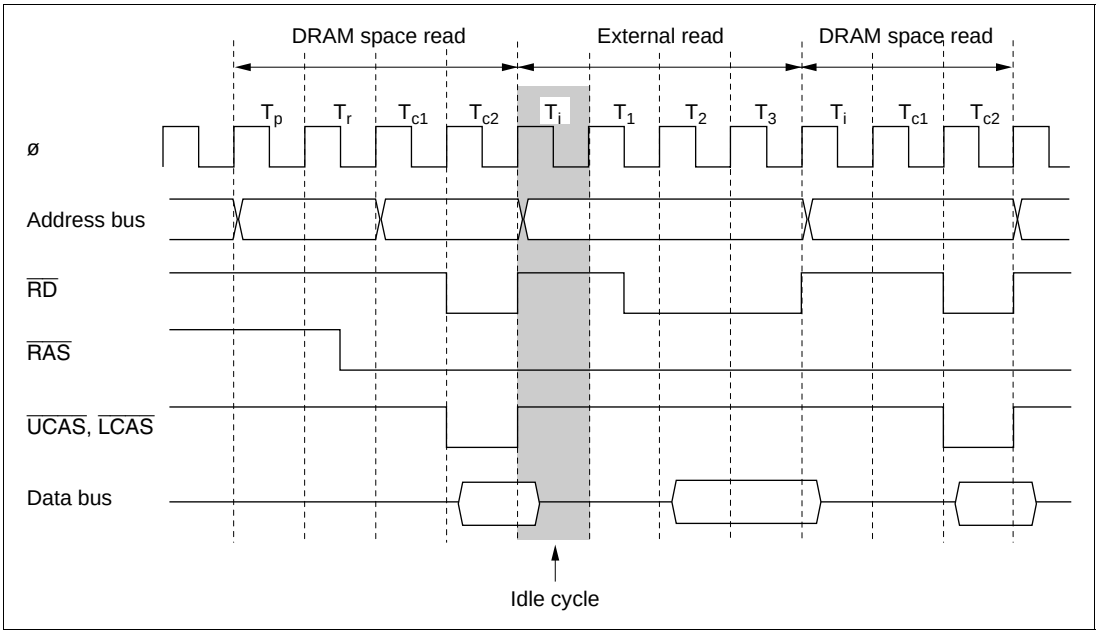


Figure 4.50 Example of Idle Cycle Operation after DRAM Access (1) (Consecutive Reads in Different Areas) (IDLC = 0, RAST = 0, CAST = 0)

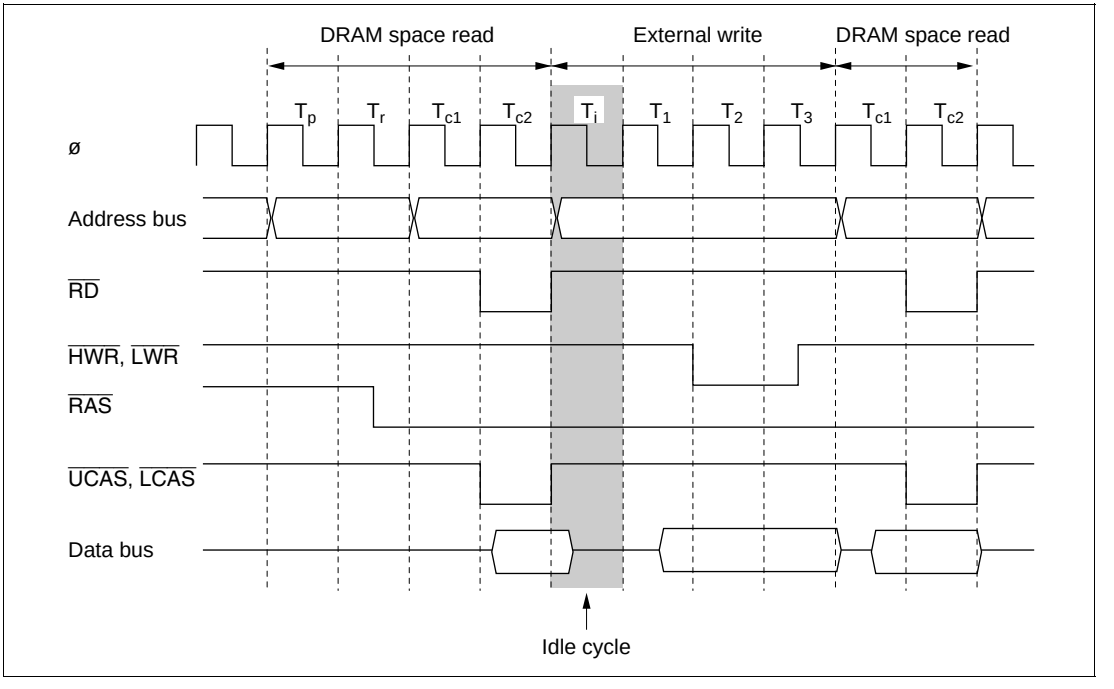


Figure 4.51 Example of Idle Cycle Operation after DRAM Access (2) (Read after Write) (IDLC = 0, RAST = 0, CAST = 0)

Table 4.8 shows when idle cycles are inserted in the case of mixed accesses to normal space and DRAM space.

Table 4.8 Idle Cycles in Mixed Accesses to Normal Space and DRAM Space

Previous Access	Next Access	ICIS1	ICIS0	DRMI	IDLC	Idle cycle
Normal space read	Normal space read (different area)	1	—	—	0	1 state inserted
					1	2 states inserted
Normal space read	DRAM space read	1	—	—	0	1 state inserted
					1	2 states inserted
Normal space read	Normal space write	—	1	—	0	1 state inserted
					1	2 states inserted
Normal space read	DRAM space write	—	1	—	0	1 state inserted
					1	2 states inserted
DRAM space read	Normal space read	1	—	0	—	Disabled
				1	0	1 state inserted
					1	2 states inserted
DRAM space read	DRAM space read	1	—	0	—	Disabled
				1	0	1 state inserted
					1	2 states inserted
DRAM space read	Normal space write	—	1	0	—	Disabled
				1	0	1 state inserted
					1	2 states inserted
DRAM space read	DRAM space write	—	1	0	—	Disabled
				1	0	1 state inserted
					1	2 states inserted

Setting the DRMI bit to 1 enables an idle cycle to be inserted in the case of consecutive read and write operations in DRAM space burst access. Figure 4.52 shows an example of the timing for idle cycle insertion in the case of consecutive read and write accesses to DRAM space.

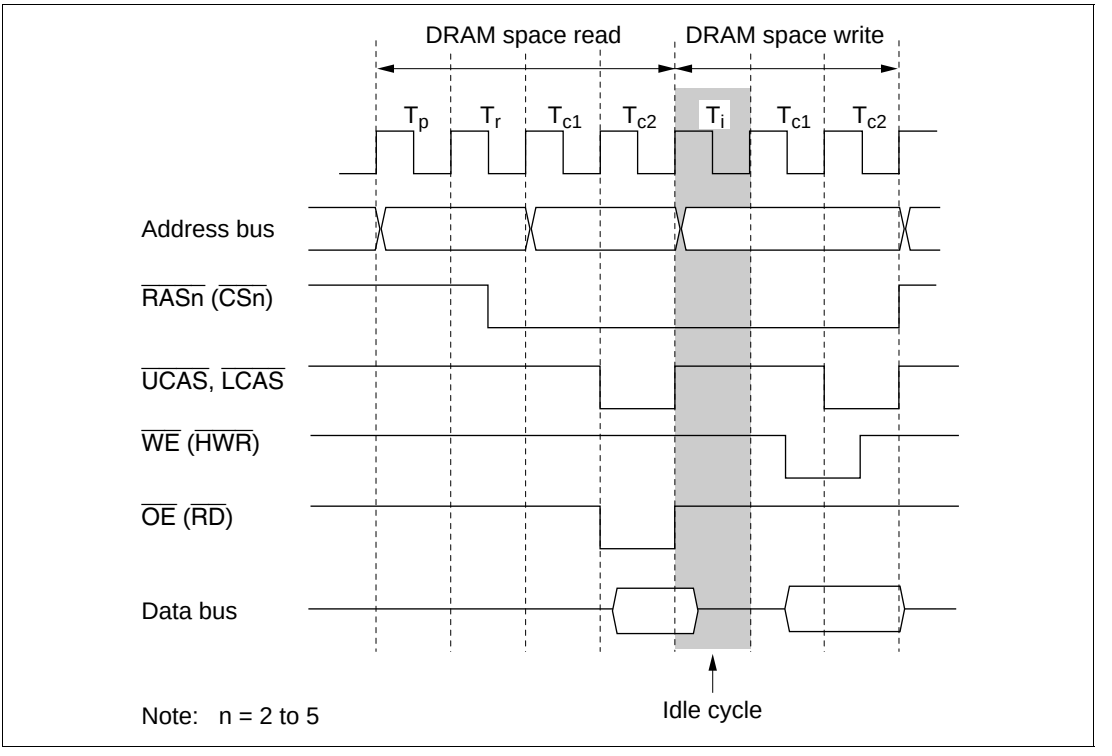


Figure 4.52 Example of Timing for Idle Cycle Insertion in Case of Consecutive Read and Write Accesses to DRAM Space in RAS Down Mode

4.7.2 Pin States in Idle Cycle

Table 4.9 shows the pin states in an idle cycle.

Table 4.9 Pin States in Idle Cycle

Pins	Pin State
A23 to A0	Contents of following bus cycle
D15 to D0	High impedance
$\overline{\text{CSn}}$ (n = 7 to 0)	High*1, *2
$\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$	High*2
$\overline{\text{AS}}$	High
$\overline{\text{RD}}$	High
$\overline{\text{OE}}$	High
$\overline{\text{HWR}}$, $\overline{\text{LWR}}$	High
$\overline{\text{DACKn}}$ (n = 1, 0)	High
$\overline{\text{EDACKn}}$ (n = 3 to 0)	High

Notes: 1. Remains low in DRAM space RAS down mode.
2. Remains low in a DRAM space refresh cycle.

4.8 Write Data Buffer Function

The H8S/2678 Series has a write data buffer function for the external data bus. Using the write data buffer function enables external writes and DMA single address mode transfers to be executed in parallel with internal accesses. The write data buffer function is made available by setting the WDBE bit to 1 in the BCR register.

Figure 4.53 shows an example of the timing when the write data buffer function is used. When this function is used, if an external write or DMA single address mode transfer continues for two states or longer, and there is an internal access next, an external write only is executed in the first state, but from the next state onward an internal access (on-chip memory or internal I/O register read/write) is executed in parallel with the external write rather than waiting until it ends.

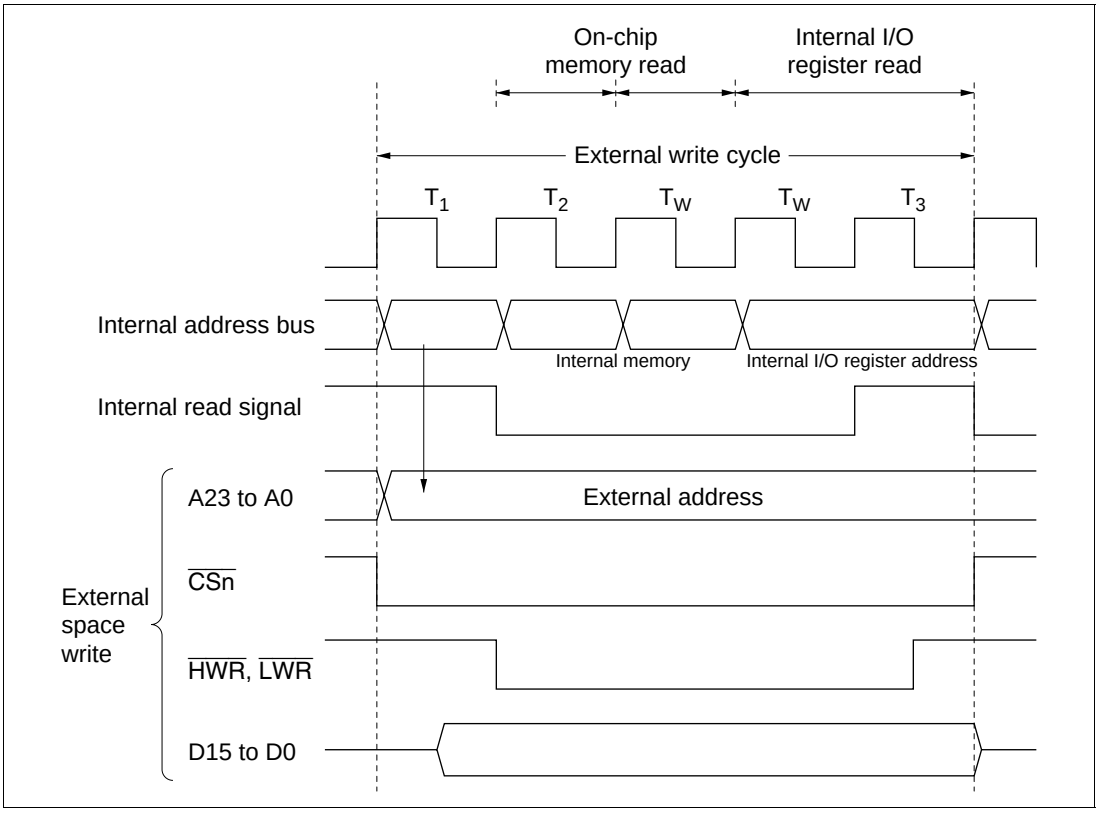


Figure 4.53 Example of Timing when Write Data Buffer Function is Used

4.9 Bus Release

4.9.1 Overview

The H8S/2678 Series chip can release the external bus in response to a bus request from an external device. In the external bus released state, internal bus masters (except the EXDMAC) continue to operate as long as there is no external access.

If any of the following requests are issued in the external bus released state, the $\overline{\text{BREQO}}$ signal can be driven low to output a bus request externally.

- When an internal bus master wants to perform an external access
- When a refresh request is generated
- When a SLEEP instruction is executed to place the chip in software standby mode or all-module-clocks-stopped mode

4.9.2 Operation

In externally expanded mode, the bus can be released to an external device by setting the BRLE bit to 1 in the BCR register. Driving the $\overline{\text{BREQ}}$ pin low issues an external bus request to the H8S/2678 Series chip. When the $\overline{\text{BREQ}}$ pin is sampled, at the prescribed timing the $\overline{\text{BACK}}$ pin is driven low, and the address bus, data bus, and bus control signals are placed in the high-impedance state, establishing the external bus released state.

In the external bus released state, an internal bus master can perform accesses using the internal bus. When an internal bus master wants to make an external access, it temporarily defers initiation of the bus cycle, and waits for the bus request from the external bus master to be canceled. If a refresh request is generated in the external bus released state, or if a SLEEP instruction is executed to place the chip in software standby mode or all-module-clocks-stopped mode, refresh control and software standby or all-module-clocks-stopped control is deferred until the bus request from the external bus master is canceled.

If the BREQOE bit is set to 1 in the BCR register, the $\overline{\text{BREQO}}$ signal can be driven low when any of the following requests are issued, to request cancellation of the bus request externally.

- When an internal bus master wants to perform an external access
- When a refresh request is generated
- When a SLEEP instruction is executed to place the chip in software standby mode or all-module-clocks-stopped mode

When the $\overline{\text{BREQ}}$ pin is driven high, the $\overline{\text{BACK}}$ pin is driven high at the prescribed timing and the external bus released state is terminated.

If an external bus release request and external access occur simultaneously, the order of priority is as follows:

(High) External bus release > External access by internal bus master (Low)

If a refresh request and external bus release request occur simultaneously, the order of priority is as follows:

(High) Refresh > External bus release (Low)

4.9.3 Pin States in External Bus Released State

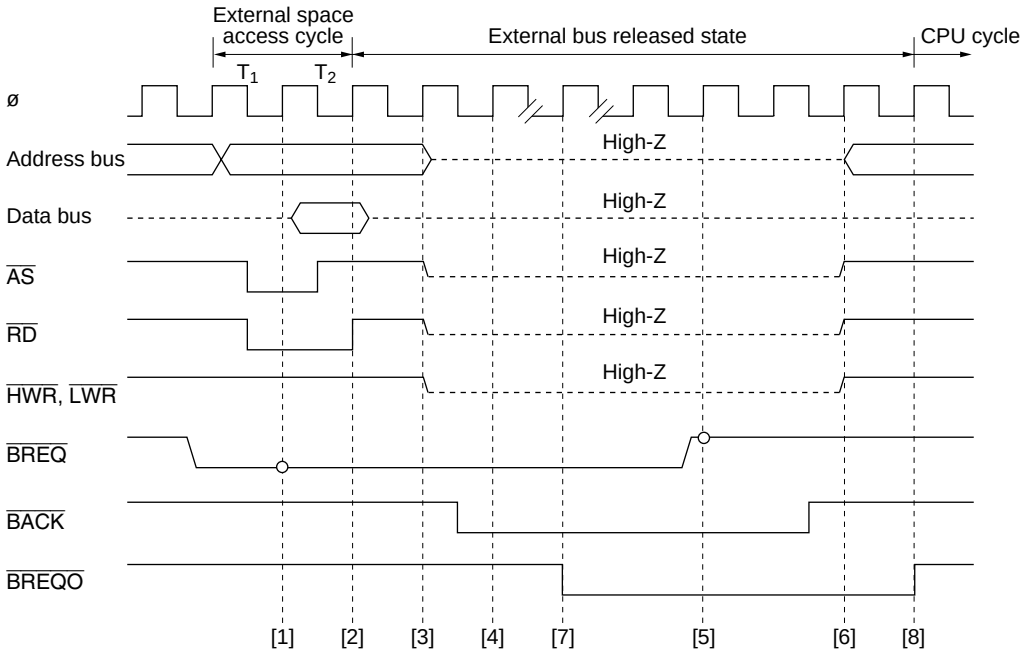
Table 4.10 shows pin states in the external bus released state.

Table 4.10 Pin States in Bus Released State

Pins	Pin State
A23 to A0	High impedance
D15 to D0	High impedance
$\overline{\text{CSn}}$ (n = 7 to 0)	High impedance
$\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$	High impedance
$\overline{\text{AS}}$	High impedance
$\overline{\text{RD}}$	High impedance
$\overline{\text{OE}}$	High impedance
$\overline{\text{HWR}}$, $\overline{\text{LWR}}$	High impedance
$\overline{\text{DACKn}}$ (n = 1, 0)	High
$\overline{\text{EDACKn}}$ (n = 3 to 0)	High

4.9.4 Transition Timing

Figure 4.54 shows the timing for transition to the bus released state.



[1] Low level of $\overline{\text{BREQ}}$ signal is sampled at rise of ø.

[2] Bus control signals temporarily return to high level at end of external space access cycle. Minimum of 1 state after $\overline{\text{BREQ}}$ signal sampling.

[3] $\overline{\text{BACK}}$ signal is driven low, releasing bus to external bus master.

[4] $\overline{\text{BREQ}}$ signal state is still sampled in external bus released state.

[5] High level of $\overline{\text{BREQ}}$ signal is sampled.

[6] $\overline{\text{BACK}}$ pin is driven high, ending external bus release cycle.

[7] In case of an external access from an internal bus master or refresh request during external bus release when the BREQOE bit is set to 1, the $\overline{\text{BREQO}}$ signal goes low.

[8] The $\overline{\text{BREQO}}$ signal normally goes high 1.5 states after the rise of the $\overline{\text{BACK}}$ signal. However, if $\overline{\text{BREQO}}$ has been asserted by a CBR refresh request, $\overline{\text{BREQO}}$ remains low until the CBR refresh cycle is initiated.

Figure 4.54 Bus Released State Transition Timing

4.9.5 Usage Notes

External Bus Release Function and All-Module-Clocks-Stopped Mode: In the H8S/2678 Series, if the ACSE bit is set to 1 in the MSTPCR register, and then a SLEEP instruction is executed with the setting for all supporting module clocks to be stopped (MSTPCR = H'FFFF) or for operation of the 8-bit timer module alone (MSTPCR = H'FFFE), and a transition is made to the sleep state, the all-module-clocks-stopped mode is entered in which the clock is also stopped for the bus controller and I/O ports.

In this state, the external bus release function is halted. To use the external bus release function in sleep mode, the ACSE bit in MSTPCR must be cleared to 0.

Conversely, if a SLEEP instruction to place the chip in all-module-clocks-stopped mode is executed in the external bus released state, the transition to all-module-clocks-stopped mode is deferred until after the bus is recovered.

External Bus Release Function and Software Standby: In the H8S/2678 Series, internal bus master operation does not stop even while the bus is released, as long as the program is running in on-chip ROM, etc., and no external access occurs. If a SLEEP instruction to place the chip in software standby mode is executed while the external bus is released, the transition to software standby mode is deferred until after the bus is recovered.

Also, since clock oscillation halts in software standby mode, if $\overline{\text{BREQ}}$ goes low in this mode, indicating an external bus release request, the request cannot be answered until the chip has recovered from the software standby state.

External Bus Release Function and CBR Refreshing: CBR refreshing cannot be executed while the external bus is released. Setting the BREQOE bit to 1 in the BCR register beforehand enables the $\overline{\text{BREQO}}$ signal to be output when a CBR refresh request is issued.

$\overline{\text{BREQO}}$ Output Timing: When the BREQOE bit is set to 1 and the $\overline{\text{BREQO}}$ signal is output, $\overline{\text{BREQO}}$ may go low before the $\overline{\text{BACK}}$ signal.

This will occur if the next external access request or CBR refresh request occurs while internal bus arbitration is in progress after the chip samples a low level of $\overline{\text{BREQ}}$.

4.10 Bus Arbitration

4.10.1 Overview

The H8S/2678 Series has a bus arbiter that arbitrates bus master operations.

There are four bus masters—the CPU, DTC, DMAC, and EXDMAC—that perform read/write operations when they have possession of the bus. Each bus master requests the bus by means of a bus request signal. The bus arbiter determines priorities at the prescribed timing, and permits use of the bus by means of a bus request acknowledge signal. The selected bus master then takes possession of the bus and begins its operation.

4.10.2 Operation

The bus arbiter monitors the bus masters' bus request signals, and if the bus is requested, sends a bus request acknowledge signal to the bus master making the request. If there are bus requests from more than one bus master, the bus request acknowledge signal is sent to the one with the highest priority. When a bus master receives the bus request acknowledge signal, it takes possession of the bus until that signal is canceled.

The order of priority of the bus masters is as follows:

(High) EXDMAC > DMAC > DTC > CPU (Low)

An external access by an internal bus master (except the EXDMAC) and (1) external bus release, (2) a refresh when the CBRM bit is 0, and (3) an external bus access by the EXDMAC can be executed in parallel.

If an external bus release request, a refresh request, and an external access by an internal bus master occur simultaneously, the order of priority is as follows:

(High) Refresh > EXDMAC > External bus release (Low)

(High) External bus release > External access by internal bus master except EXDMAC (Low)

As a refresh when the CBRM bit is 0 and an external access other than to DRAM space by an internal bus master can be executed simultaneously, there is no relative order of priority for these two operations.

4.10.3 Bus Transfer Timing

Even if a bus request is received from a bus master with a higher priority than that of the bus master that has acquired the bus and is currently operating, the bus is not necessarily transferred immediately. There are specific times at which each bus master can relinquish the bus.

CPU: The CPU is the lowest-priority bus master, and if a bus request is received from the DTC, DMAC, or EXDMAC, the bus arbiter transfers the bus to the bus master that issued the request. The timing for transfer of the bus is as follows:

- The bus is transferred at a break between bus cycles. However, if a bus cycle is executed in discrete operations, as in the case of a longword-size access, the bus is not transferred between the component operations.
- With bit manipulation instructions such as BSET and BCLR, the sequence of operations is: data read (read), relevant bit manipulation operation (modify), write-back (write). The bus is not transferred during this read-modify-write cycle, which is executed as a series of bus cycles.
- If the CPU is in sleep mode, the bus is transferred immediately.

DTC: The DTC sends the bus arbiter a request for the bus when an activation request is generated.

The DTC can release the bus after a vector read, a register information read (3 states), a single data transfer, or a register information write (3 states). It does not release the bus during a register information read (3 states), a single data transfer, or a register information write (3 states).

DMAC: The DMAC sends the bus arbiter a request for the bus when an activation request is generated.

In the case of an external request in short address mode or normal mode, and in cycle steal mode, the DMAC releases the bus after a single transfer.

In block transfer mode, it releases the bus after transfer of one block, and in burst mode, after completion of the transfer. However, in the event of an EXDMAC or external bus release request, which have a higher priority than the DMAC, the bus may be transferred to the bus master even if burst transfer is in progress.

EXDMAC: The EXDMAC sends the bus arbiter a request for the bus when an activation request is generated.

As the EXDMAC is used exclusively for transfers to and from the external bus, if the bus is transferred to the EXDMAC, internal accesses by other internal bus masters are still executed in parallel.

In normal transfer mode or cycle steal transfer mode, the EXDMAC releases the bus after a single transfer.

In block transfer mode, it releases the bus after transfer of one block, and in burst mode, after completion of the transfer. By setting the BGUP bit to 1 in the EDMDR register, it is possible to specify temporary release of the bus in the event of an external access request from an internal bus master. For details see section 7, EXDMA Controller, in the H8S/2678 Series Hardware Manual.

External Bus Release: When the $\overline{\text{BREQ}}$ pin goes low and an external bus release request is issued while the BRLE bit is set to 1 in the BCR register, a bus request is sent to the bus arbiter.

External bus release can be performed on completion of an external bus cycle.

4.11 Bus Controller Operation in a Reset

In a reset, the chip, including the bus controller, enters the reset state immediately, and any executing bus cycle is aborted.

Section 5 I/O Ports

5.1 Overview

The H8S/2678 Series has fifteen I/O ports (ports 1 to 3, P50 to P53, 6 to 8, and A to H), and two input-only ports (port 4 and P54 to P57).

Table 5.1 summarizes the port functions. The pins of each port also have other functions.

Each port includes a data direction register (DDR) that controls input/output (not provided for the input-only ports), a data register (DR) that stores output data, and a port register (PORT) used to read the pin states.

Ports A to E have a built-in MOS input pull-up function, and in addition to DR and DDR, have a MOS input pull-up control register (PCR) to control the on/off status of MOS input pull-ups.

Ports 3 and A include an open-drain control register (ODR) that controls the on/off status of the output buffer PMOS.

Ports A to H can drive a single TTL load and 50 pF capacitive load, and ports 1, 2, 3, 5 (P50 to P53), 6, 7, and 8 can drive a single TTL load and 30 pF capacitive load.

Ports 1 and 2 have Schmitt-trigger input circuits. Ports 5, 6, 8, F (PF1, PF2), and H (PH2, PH3) are Schmitt-trigger inputs when used as IRQ inputs.

Table 5.1 Port Functions

Port	Description	Pins	Modes 1, 2, 5, 6	Mode 4	Mode 7
Port 1	• 8-bit I/O port • Schmitt-trigger input	P17/PO15/TIOCB2/TCLKD/$\overline{\text{EDRAK3}}$ P16/PO14/TIOCA2/$\overline{\text{EDRAK2}}$	2-bit I/O port also functioning as EXDMA controller output pins ($\overline{\text{EDRAK3}}$, $\overline{\text{EDRAK2}}$), TPU I/O pins (TCLKD, TIOCA2, TIOCB2), and PPG output pins (PO15, PO14)		• When EXPE = 0 (after reset): 2-bit I/O port also functioning as TPU I/O pins (TCLKD, TIOCA2, TIOCB2) and PPG output pins (PO15, PO14) • When EXPE = 1: 2-bit I/O port also functioning as EXDMA controller output pins ($\overline{\text{EDRAK3}}$, $\overline{\text{EDRAK2}}$), TPU I/O pins (TCLKD, TIOCA2, TIOCB2), and PPG output pins (PO15, PO14)
		P15/PO13/TIOCB1/TCLKC P14/PO12/TIOCA1 P13/PO11/TIOCD0/TCLKB P12/PO10/TIOCC0/TCLKA P11/PO9/TIOCB0 P10/PO8/TIOCA0	6-bit I/O port also functioning as TPU I/O pins (TCLKA, TCLKB, TCLKC, TIOCA0, TIOCB0, TIOCC0, TIOCD0, TIOCA1, TIOCB1) and PPG output pins (PO13 to PO8)		
Port 2	• 8-bit I/O port • Schmitt-trigger input	P27/PO7/TIOCB5/$\overline{\text{IRQ15}}$/$\overline{\text{EDRAK1}}$ P26/PO6/TIOCA5/$\overline{\text{IRQ14}}$/$\overline{\text{EDRAK0}}$	2-bit I/O port also functioning as EXDMA controller output pins ($\overline{\text{EDRAK1}}$, $\overline{\text{EDRAK0}}$), TPU I/O pins (TIOCA5, TIOCB5), interrupt input pins ($\overline{\text{IRQ15}}$, $\overline{\text{IRQ14}}$), and PPG output pins (PO7, PO6)		• When EXPE = 0 (after reset): 2-bit I/O port also functioning as TPU I/O pins (TIOCA5, TIOCB5), interrupt input pins ($\overline{\text{IRQ15}}$, $\overline{\text{IRQ14}}$), and PPG output pins (PO7, PO6) • When EXPE = 1: 2-bit I/O port also functioning as EXDMA controller output pins ($\overline{\text{EDRAK1}}$, $\overline{\text{EDRAK0}}$), TPU I/O pins (TIOCA5, TIOCB5), interrupt input pins ($\overline{\text{IRQ15}}$, $\overline{\text{IRQ14}}$), and PPG output pins (PO7, PO6)

Port	Description	Pins	Modes 1, 2, 5, 6	Mode 4	Mode 7
Port 2	• 8-bit I/O port • Schmitt-trigger input	P25/PO5/TIOCB4/$\overline{IRQ13}$ P24/PO4/TIOCA4/$\overline{IRQ12}$ P23/PO3/TIOCD3/$\overline{IRQ11}$ P22/PO2/TIOCC3/$\overline{IRQ10}$ P21/PO1/TIOCB3/$\overline{IRQ9}$ P20/PO0/TIOCA3/$\overline{IRQ8}$	6-bit I/O port also functioning as TPU I/O pins (TIOCA3, TIOCB3, TIOCC3, TIOCD3, TIOCA4, TIOCB4), interrupt input pins ($\overline{IRQ13}$ to $\overline{IRQ8}$), and PPG output pins (PO5 to PO0)		
Port 3	• 6-bit I/O port • Open-drain output capability	P35/SCK1/$\overline{OE}$	• When OEE = 1 and OES =0: $\overline{OE}$ output • Otherwise (after reset): I/O port also functioning as SCI (channel 1) I/O pin (SCK1)		• When EXPE = 0 (after reset): I/O port also functioning as SCI (channel 1) I/O pin (SCK1) • When EXPE = 1: $\overline{OE}$ output when OEE = 1 and OES =0 • Otherwise: I/O port also functioning as SCI (channel 1) I/O pin (SCK1)
		P34/SCK0 P33/RxD1 P32/RxD0/IrRxD P31/TxD1 P30/TxD0/IrTxD	5-bit I/O port also functioning as SCI (channels 0 and 1) I/O pins (SCK0, RxD1, RxD0/IrRxD, TxD1, TxD0/IrTxD)		
Port 4	• 8-bit I/O port	P47/AN7/DA1 P46/AN6/DA0 P45/AN5 P44/AN4 P43/AN3 P42/AN2 P41/AN1 P40/AN0	8-bit input port also functioning as A/D converter analog inputs (AN7 to AN0) and D/A converter analog outputs (DA1, DA0)		

Port	Description	Pins	Modes 1, 2, 5, 6	Mode 4	Mode 7
Port 5	• 4-bit I/O port • 4-bit input port	P57/AN15/DA3/$\overline{\text{IRQ7}}$ P56/AN14/DA2/$\overline{\text{IRQ6}}$ P55/AN13/$\overline{\text{IRQ5}}$ P54/AN12/$\overline{\text{IRQ4}}$	4-bit input port also functioning as A/D converter analog inputs (AN15 to AN12), D/A converter analog outputs (DA3, DA2), and interrupt input pins ($\overline{\text{IRQ7}}$ to $\overline{\text{IRQ4}}$)		
		P53/$\overline{\text{ADTRG}}$/$\overline{\text{IRQ3}}$ P52/SCK2/$\overline{\text{IRQ2}}$ P51/RxD2/$\overline{\text{IRQ1}}$ P50/TxD2/$\overline{\text{IRQ0}}$	4-bit I/O port also functioning as A/D converter input pin ($\overline{\text{ADTRG}}$), SCI (channel 2) I/O pins (TxD2, RxD2, SCK2), and interrupt input pins ($\overline{\text{IRQ3}}$ to $\overline{\text{IRQ0}}$)		
Port 6	• 6-bit I/O port	P65/TMO1/$\overline{\text{DACK1}}$/$\overline{\text{IRQ13}}$ P64/TMO0/$\overline{\text{DACK0}}$/$\overline{\text{IRQ12}}$ P63/TMCI1/$\overline{\text{TEND1}}$/$\overline{\text{IRQ11}}$ P62/TMCI0/$\overline{\text{TEND0}}$/$\overline{\text{IRQ10}}$ P61/TMRI1/$\overline{\text{DREQ1}}$/$\overline{\text{IRQ9}}$ P60/TMRI0/$\overline{\text{DREQ0}}$/$\overline{\text{IRQ8}}$	• When DMACS = 0 (after reset): 6-bit I/O port also functioning as DMA controller I/O pins ($\overline{\text{DACK1}}$, $\overline{\text{DACK0}}$, $\overline{\text{TEND1}}$, $\overline{\text{TEND0}}$, $\overline{\text{DREQ1}}$, $\overline{\text{DREQ0}}$), 8-bit timer (channels 0 and 1) pins (TMO1, TMO0, TMCI1, TMCI0, TMRI1, TMRI0), and interrupt input pins ($\overline{\text{IRQ13}}$ to $\overline{\text{IRQ8}}$) • When DMACS = 1: 6-bit I/O port also functioning as 8-bit timer (channels 0 and 1) pins (TMO1, TMO0, TMCI1, TMCI0, TMRI1, TMRI0) and interrupt input pins ($\overline{\text{IRQ13}}$ to $\overline{\text{IRQ8}}$)		
Port 7	• 6-bit I/O port	P75/$\overline{\text{DACK1}}$/$\overline{\text{EDACK1}}$ P74/$\overline{\text{DACK0}}$/$\overline{\text{EDACK0}}$ P73/$\overline{\text{TEND1}}$/$\overline{\text{ETEND1}}$ P72/$\overline{\text{TEND0}}$/$\overline{\text{ETEND0}}$ P71/$\overline{\text{DREQ1}}$/$\overline{\text{EDREQ1}}$ P70/$\overline{\text{DREQ0}}$/$\overline{\text{EDREQ0}}$	• When DMACS = 0 (after reset): 6-bit I/O port also functioning as EXDMA controller I/O pins ($\overline{\text{EDACK1}}$, $\overline{\text{EDACK0}}$, $\overline{\text{ETEND1}}$, $\overline{\text{ETEND0}}$, $\overline{\text{EDREQ1}}$, $\overline{\text{EDREQ0}}$) • When DMACS = 1: 6-bit I/O port also functioning as EXDMA controller I/O pins ($\overline{\text{EDACK1}}$, $\overline{\text{EDACK0}}$, $\overline{\text{ETEND1}}$, $\overline{\text{ETEND0}}$, $\overline{\text{EDREQ1}}$, $\overline{\text{EDREQ0}}$) and DMA controller I/O pins ($\overline{\text{DACK1}}$, $\overline{\text{DACK0}}$, $\overline{\text{TEND1}}$, $\overline{\text{TEND0}}$, $\overline{\text{DREQ1}}$, $\overline{\text{DREQ0}}$)	• When EXPE = 0 and DMACS = 0 (after reset): 6-bit I/O port • When EXPE = 0 and DMACS = 1: 6-bit I/O port also functioning as DMA controller I/O pins ($\overline{\text{DACK1}}$, $\overline{\text{DACK0}}$, $\overline{\text{TEND1}}$, $\overline{\text{TEND0}}$, $\overline{\text{DREQ1}}$, $\overline{\text{DREQ0}}$) • When EXPE = 1 and DMACS = 0: 6-bit I/O port also functioning as EXDMA controller I/O pins ($\overline{\text{EDACK1}}$, $\overline{\text{EDACK0}}$, $\overline{\text{ETEND1}}$, $\overline{\text{ETEND0}}$, $\overline{\text{EDREQ1}}$, $\overline{\text{EDREQ0}}$) • When EXPE = 1 and DMACS = 1: 6-bit I/O port also functioning as EXDMA controller I/O pins ($\overline{\text{EDACK1}}$, $\overline{\text{EDACK0}}$, $\overline{\text{ETEND1}}$, $\overline{\text{ETEND0}}$, $\overline{\text{EDREQ1}}$, $\overline{\text{EDREQ0}}$) and DMA controller I/O pins ($\overline{\text{DACK1}}$, $\overline{\text{DACK0}}$, $\overline{\text{TEND1}}$, $\overline{\text{TEND0}}$, $\overline{\text{DREQ1}}$, $\overline{\text{DREQ0}}$)

Port	Description	Pins	Modes 1, 2, 5, 6	Mode 4	Mode 7
Port 8	• 6-bit I/O port	P85/EDACK3/IRQ5 P84/ EDACK2/IRQ4 P83/ETEND3/IRQ3 P82/ETEND2/IRQ2 P81/EDREQ3/IRQ1 P80/EDREQ2/IRQ0	6-bit I/O port also functioning as EXDMA controller I/O pins (EDACK3, EDACK2, ETEND3, ETEND2, EDREQ3, EDREQ2) and interrupt input pins (IRQ5 to IRQ0)		• When EXPE = 0 (after reset): 6-bit I/O port also functioning as interrupt input pins (IRQ5 to IRQ0) • When EXPE = 1: 6-bit I/O port also functioning as EXDMA controller I/O pins (EDACK3, EDACK2, ETEND3, ETEND2, EDREQ3, EDREQ2) and interrupt input pins (IRQ5 to IRQ0)
Port A	• 8-bit I/O port • Built-in MOS input pull-up • Open-drain output capability	PA7/A23 PA6/A22 PA5/A21	When A23E to A21E = 1 and DDR = 0 (after reset): Input port When A23E to A21E = 0: I/O port When A23E to A21E = 1 and DDR = 1: Address output		When EXPE = 0 (after reset), or when EXPE = 1 and A23E to A16E = 0: I/O port When EXPE = 1, A23E to A16E = 1, and DDR = 0: Input port When EXPE = 1, A23E to A16E = 1, and DDR = 1: Address output
		PA4/A20–PA0/A16	Address output	When A20E to A16E = 1 and DDR = 0 (after reset): Input port When A20E to A16E = 0: I/O port When A20E to A16E = 1 and DDR = 1 (after reset): Address output	
Port B	• 8-bit I/O port • Built-in MOS input pull-up	PB7/A15–PB0/A8	Address output	When DDR = 0 (after reset): Input port When DDR = 1: Address output	When EXPE = 0 (after reset): I/O port When EXPE = 1 and DDR = 0 (after reset): Input port When EXPE = 1 and DDR = 1: Address output
Port C	• 8-bit I/O port • Built-in MOS input pull-up	PC7/A7–PC0/A0	Address output	When DDR = 0 (after reset): Input port When DDR = 1: Address output	When EXPE = 0 (after reset): I/O port When EXPE = 1 and DDR = 0: Input port When EXPE = 1 and DDR = 1: Address output

Port	Description	Pins	Modes 1, 2, 5, 6	Mode 4	Mode 7
Port D	• 8-bit I/O port • Built-in MOS input pull-up	PD7/D15–PD0/D8	Data bus input/output		When EXPE = 0 (after reset): I/O port When EXPE = 1: Data bus input/output
Port E	• 8-bit I/O port • Built-in MOS input pull-up	PE7/D7–PE0/D0	In 8-bit bus mode: I/O port In 16-bit bus mode: Data bus input/output		When EXPE = 0 (after reset): I/O port When EXPE = 1 in 8-bit bus mode: I/O port When EXPE = 1 in 16-bit bus mode: Data bus input/output
Port F	• 8-bit I/O port	PF7/ø	When DDR = 1 (after reset): ø output When DDR = 0: Input port		When DDR = 0: Input port (after reset) When DDR = 1: ø output
		PF6/$\overline{AS}$	When ASOE = 1 (after reset): $\overline{AS}$ output When ASOE = 0: I/O port		When EXPE = 0 (after reset), or when EXPE = 1 and ASOE = 0: I/O port When EXPE = 1 and ASOE = 1: $\overline{AS}$ output
		PF5/$\overline{RD}$ PF4/$\overline{HWR}$	$\overline{RD}$, $\overline{HWR}$ output		When EXPE = 0 (after reset): I/O port When EXPE = 1: $\overline{RD}$, $\overline{HWR}$ output
		PF3/$\overline{LWR}$	When LWROE = 1 (after reset): $\overline{LWR}$ output When LWROE = 0: I/O port		When EXPE = 0 (after reset), or when EXPE = 1 and LWROE = 0: I/O port When EXPE = 1 and LWROE = 1: $\overline{LWR}$ output
		PF2/$\overline{LCAS}$/$\overline{IRQ15}$	When areas 2 to 5 are all normal space (after reset), or when DRAM space areas are all in 8-bit bus mode: I/O port also functioning as $\overline{IRQ15}$ interrupt input When any DRAM space is in 16-bit bus mode: Dual function as $\overline{IRQ15}$ interrupt input and $\overline{LCAS}$ output		When EXPE = 0 (after reset), or when EXPE = 1 and areas 2 to 5 are all normal space, or when EXPE = 1 and DRAM space areas are all in 8-bit bus mode: I/O port also functioning as $\overline{IRQ15}$ interrupt input When EXPE = 1 and any DRAM space is in 16-bit bus mode: Dual function as $\overline{IRQ15}$ interrupt input and $\overline{LCAS}$ output

Port	Description	Pins	Modes 1, 2, 5, 6	Mode 4	Mode 7
Port F	• 8-bit I/O port	PF1/$\overline{\text{UCAS}}$/$\overline{\text{IRQ14}}$	When areas 2 to 5 are all normal space (after reset): I/O port also functioning as $\overline{\text{IRQ14}}$ interrupt input When any of areas 2 to 5 is DRAM space: Dual function as $\overline{\text{IRQ14}}$ interrupt input and $\overline{\text{UCAS}}$ output		When EXPE = 0 (after reset), or when EXPE = 1 and areas 2 to 5 are all normal space: I/O port also functioning as $\overline{\text{IRQ14}}$ interrupt input When EXPE = 1 and any of areas 2 to 5 is DRAM space: Dual function as $\overline{\text{IRQ14}}$ interrupt input and $\overline{\text{UCAS}}$ output
		PF0/$\overline{\text{WAIT}}$	When WAITE = 0 (after reset): I/O port When WAITE = 1: $\overline{\text{WAIT}}$ input		When EXPE = 0 (after reset), or when EXPE = 1 and WAITE = 0: I/O port When EXPE = 1 and WAITE = 1: $\overline{\text{WAIT}}$ input
Port G	• 7-bit I/O port	PG6/$\overline{\text{BREQ}}$	When BRLE = 0 (after reset): I/O port When BRLE = 1: $\overline{\text{BREQ}}$ input		When EXPE = 0 (after reset), or when EXPE = 1 and BRLE = 0: I/O port When EXPE = 1 and BRLE = 1: $\overline{\text{BREQ}}$ input
		PG5/$\overline{\text{BACK}}$	When BRLE = 0 (after reset): I/O port When BRLE = 1: $\overline{\text{BACK}}$ output		When EXPE = 0 (after reset), or when EXPE = 1 and BRLE = 0: I/O port When EXPE = 1 and BRLE = 1: $\overline{\text{BACK}}$ output
		PG4/$\overline{\text{BREQO}}$	When BRLE = 0 (after reset), or when BRLE = 1 and BREQOE = 0: I/O port When BRLE = 1 and BREQOE = 1: $\overline{\text{BREQO}}$ output		When EXPE = 0 (after reset), or when EXPE1 = 1 and BRLE = 0, or when EXPE = 1, BRLE = 1, and BREQOE = 0: I/O port When EXPE = 1, BRLE = 1, and BREQOE = 1: $\overline{\text{BREQO}}$ output
		PG3/$\overline{\text{CS3}}$	When CS3E = 0 (after reset): I/O port When CS3E = 1 and DDR = 0: Input port When CS3E = 1 and DDR = 1: $\overline{\text{CS3}}$ output		When EXPE = 0 (after reset), or when EXPE1 = 1 and CS3E = 0: I/O port When EXPE = 1, CS3E = 1, and DDR = 0: Input port When EXPE = 1, CS3E = 1, and DDR = 1: $\overline{\text{CS3}}$ output

Port	Description	Pins	Modes 1, 2, 5, 6	Mode 4	Mode 7
Port G	• 7-bit I/O port	PG2/$\overline{CS2}$	When CS2E = 0 (after reset): I/O port When CS2E = 1 and DDR = 0: Input port When CS2E = 1 and DDR = 1: $\overline{CS2}$ output		When EXPE = 0 (after reset), or when EXPE1 = 1 and CS2E = 0: I/O port When EXPE = 1, CS2E = 1, and DDR = 0: Input port When EXPE = 1, CS2E = 1, and DDR = 1: $\overline{CS2}$ output
		PG1/$\overline{CS1}$	When CS1E = 0 (after reset): I/O port When CS1E = 1 and DDR = 0: Input port When CS1E = 1 and DDR = 1: $\overline{CS1}$ output		When EXPE = 0 (after reset), or when EXPE1 = 1 and CS1E = 0: I/O port When EXPE = 1, CS1E = 1, and DDR = 0: Input port When EXPE = 1, CS1E = 1, and DDR = 1: $\overline{CS1}$ output
		PG0/$\overline{CS0}$	When CS0E = 1 and DDR = 1 (after reset): $\overline{CS0}$ output When CS0E = 0: I/O port When CS0E = 1 and DDR = 0: Input port	When CS0E = 1 and DDR = 0 (after reset): Input port When CS0E = 0: I/O port When CS0E = 1 and DDR = 1: $\overline{CS0}$ output	When EXPE = 0 (after reset), or when EXPE1 = 1 and CS0E = 0: I/O port When EXPE = 1, CS0E = 1, and DDR = 0: Input port When EXPE = 1, CS0E = 1, and DDR = 1: $\overline{CS0}$ output
Port H	• 4-bit I/O port	PH3/$\overline{CS7}$/$\overline{OE}$/$\overline{IRQ7}$	When OEE = 0 and CS7E = 0 (after reset), or when OEE = 1, OES = 0, and CS7E = 0: I/O port also functioning as $\overline{IRQ7}$ interrupt input When OEE = 0, CS7E = 1, and DDR = 0, or when OEE = 1, OES = 0, CS7E = 1, and DDR = 0: Input port also functioning as $\overline{IRQ7}$ interrupt input When OEE = 0, CS7E = 1, and DDR = 1, or when OEE = 1, OES = 0, CS7E = 1, and DDR = 1: Dual function as $\overline{IRQ7}$ interrupt input and $\overline{CS7}$ output When OEE = 1 and OES = 1: Dual function as $\overline{IRQ7}$ interrupt input and $\overline{OE}$ output		When EXPE = 0 (after reset), or when EXPE = 1, OEE = 0, and CS7E = 0, or when EXPE = 1, OEE = 1, OES = 0, and CS7E = 0: I/O port also functioning as $\overline{IRQ7}$ interrupt input When EXPE = 1, OEE = 0, CS7E = 1, and DDR = 0, or when EXPE = 1, OEE = 1, OES = 0, CS7E = 1, and DDR = 0: Input port also functioning as $\overline{IRQ7}$ interrupt input When EXPE = 1, OEE = 0, CS7E = 1, and DDR = 1, or when OEE = 1, OES = 0, CS7E = 1, and DDR = 1: Dual function as $\overline{IRQ7}$ interrupt input and $\overline{CS7}$ output When EXPE = 1, OEE = 1, and OES = 1: Dual function as $\overline{IRQ7}$ interrupt input and $\overline{OE}$ output

Port	Description	Pins	Modes 1, 2, 5, 6	Mode 4	Mode 7
Port H	• 4-bit I/O port	PH2/$\overline{CS6}$/$\overline{IRQ6}$	When CS6E = 0 (after reset): I/O port also functioning as $\overline{IRQ6}$ interrupt input When CS6E = 1 and DDR = 0: Input port also functioning as $\overline{IRQ6}$ interrupt input When CS6E = 1 and DDR = 1: Dual function as $\overline{IRQ6}$ interrupt input and $\overline{CS6}$ output		When EXPE = 0 (after reset), or when EXPE = 1 and CS6E = 0: I/O port also functioning as $\overline{IRQ6}$ interrupt input When EXPE = 1, CS6E = 1, and DDR = 0: Input port also functioning as $\overline{IRQ6}$ interrupt input When EXPE = 1, CS6E = 1, and DDR = 1: Dual function as $\overline{IRQ6}$ interrupt input and $\overline{CS6}$ output
		PH1/$\overline{CS5}$	When CS5E = 0 (after reset): I/O port When CS5E = 1 and DDR = 0: Input port When CS5E = 1 and DDR = 1: $\overline{CS5}$ output		When EXPE = 0 (after reset), or when EXPE = 1 and CS5E = 0: I/O port When EXPE = 1, CS5E = 1, and DDR = 0: Input port When EXPE = 1, CS5E = 1, and DDR = 1: $\overline{CS5}$ output
		PH0/$\overline{CS4}$	When CS4E = 0 (after reset): I/O port When CS4E = 1 and DDR = 0: Input port When CS4E = 1 and DDR = 1: $\overline{CS4}$ output		When EXPE = 0 (after reset), or when EXPE = 1 and CS4E = 0: I/O port When EXPE = 1, CS4E = 1, and DDR = 0: Input port When EXPE = 1, CS4E = 1, and DDR = 1: $\overline{CS4}$ output

5.2 Port 1

5.2.1 Overview

Port 1 is an 8-bit I/O port. Port 1 pins also function as PPG output pins (PO15 to PO8), TPU I/O pins (TCLKA, TCLKB, TCLKC, TCLKD, TIOCA0, TIOCB0, TIOCC0, TIOCD0, TIOCA1, TIOCB1, TIOCA2, and TIOCB2), and EXDMAC output pins ($\overline{\text{EDRAK2}}$ and $\overline{\text{EDRAK3}}$). The functions of pins P15 to P10 are the same in all operating modes, while the functions of pins P17 and P16 change according to the operating mode. Port 1 has Schmitt-trigger inputs.

Figure 5.1 shows the port 1 pin configuration.

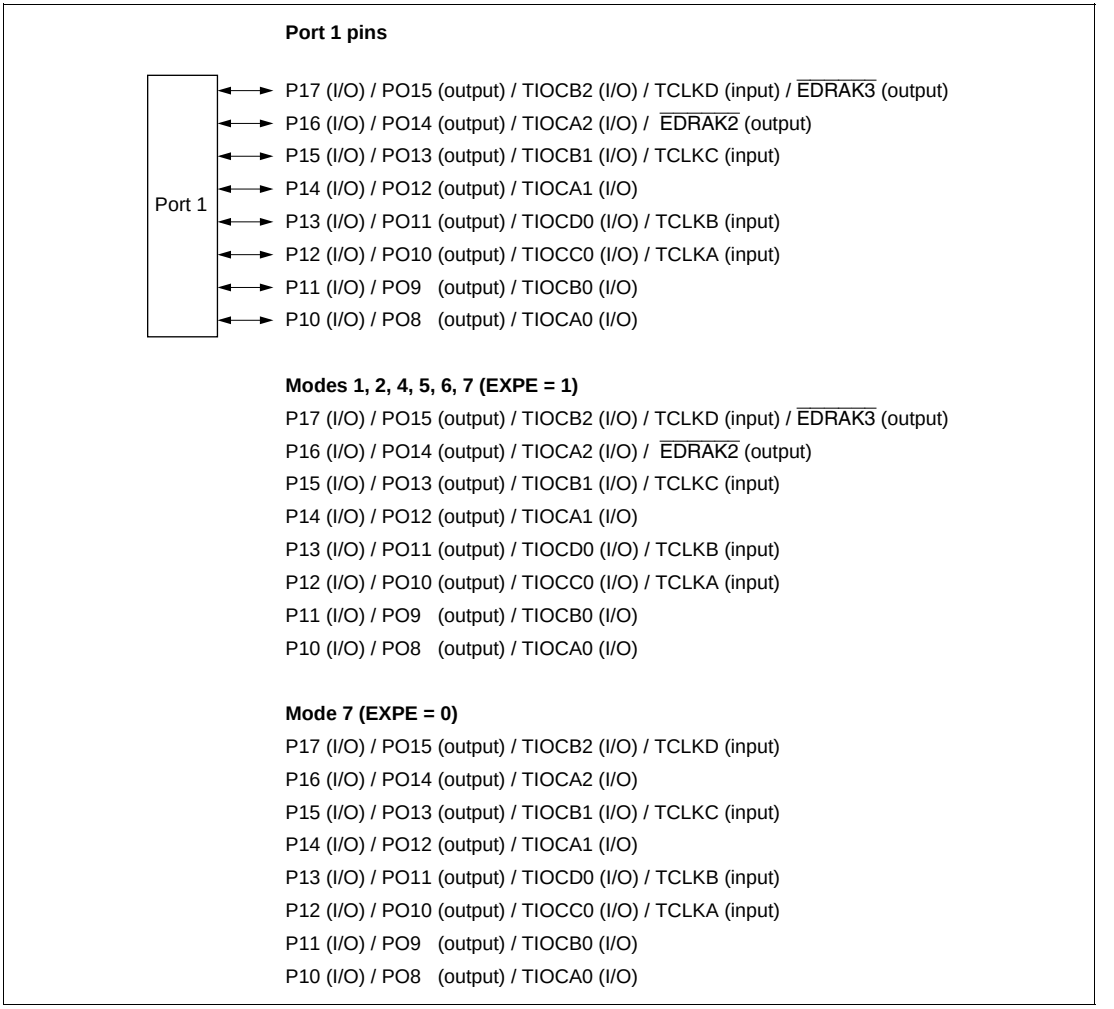


Figure 5.1 Port 1 Pin Functions

5.2.2 Register Configuration

Table 5.2 shows the port 1 register configuration.

Table 5.2 Port 1 Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port 1 data direction register	P1DDR	W	H'00	H'FE20
Port 1 data register	P1DR	R/W	H'00	H'FF60
Port 1 register	PORT1	R	Undefined	H'FF50

Note: * Lower 16 bits of the address.

Port 1 Data Direction Register (P1DDR)

Bit	7	6	5	4	3	2	1	0
	P17DDR	P16DDR	P15DDR	P14DDR	P13DDR	P12DDR	P11DDR	P10DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

P1DDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port 1. P1DDR cannot be read; if it is, an undefined value will be read.

Setting a P1DDR bit to 1 makes the corresponding port 1 pin an output pin, while clearing the bit to 0 makes the pin an input pin.

P1DDR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Port 1 Data Register (P1DR)

Bit	7	6	5	4	3	2	1	0
	P17DR	P16DR	P15DR	P14DR	P13DR	P12DR	P11DR	P10DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P1DR is an 8-bit readable/writable register that stores output data for the port 1 pins (P17 to P10).

P1DR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Port 1 Register (PORT1)

Bit	7	6	5	4	3	2	1	0
	P17	P16	P15	P14	P13	P12	P11	P10
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

Note: * Determined by the state of pins P17 to P10.

PORT1 is an 8-bit read-only register that shows the pin states. PORT1 cannot be written to; writing of output data for the port 1 pins (P17 to P10) must always be performed on P1DR.

If a port 1 read is performed while P1DDR bits are set to 1, the P1DR values are read. If a port 1 read is performed while P1DDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORT1 contents are determined by the pin states, as P1DDR and P1DR are initialized. PORT1 retains its prior state in software standby mode.

5.2.3 Pin Functions

Port 1 pins also function as PPG output pins (PO15 to PO8), TPU I/O pins (TCLKA, TCLKB, TCLKC, TCLKD, TIOCA0, TIOCB0, $\overline{\text{TIOCC0}}$, TIOCD0, TIOCA1, TIOCB1, TIOCA2, and TIOCB2), and EXDMAC output pins ($\overline{\text{EDRAK2}}$ and $\overline{\text{EDRAK3}}$). Port 1 pin functions are shown in table 5.3.

Table 5.3 Port 1 Pin Functions

Pin	Selection Method and Pin Functions
P17/PO15/ TIOCB2/ TCLKD/ $\overline{\text{EDRAK3}}$	The pin function is switched as shown below according to the combination of the TPU channel 2 settings (by bits MD3 to MD0 in TMDR2, bits IOB3 to IOB0 in TIOR2, and bits CCLR1 and CCLR0 in TCR2), bits TPSC2 to TPSC0 in TCR0 and TCR5, bit NDER15 in NDERH, bit EDRAKE in EDMDR3, and bit P17DDR.

Modes 1, 2, 4, 5, 6, 7 (EXPE = 1)

EDRAKE	0				1
TPU channel 2 settings	(1) in table below	(2) in table below			—
P17DDR	—	0	1	1	—
NDER15	—	—	0	1	—
Pin function	TIOCB2 output	P17 input	P17 output	PO15 output	$\overline{\text{EDRAK3}}$ output
		TIOCB2 input*1			
	TCLKD input*2				

Mode 7 (EXPE = 0)

EDRAKE	—			
TPU channel 2 settings	(1) in table below	(2) in table below		
P17DDR	—	0	1	1
NDER15	—	—	0	1
Pin function	TIOCB2 output	P17 input	P17 output	PO15 output
		TIOCB2 input*1		
	TCLKD input*2			

Notes: 1. TIOCB2 input when MD3 to MD0 = B'0000 or B'01xx and IOB3 = 1.

2. TCLKD input when the setting for either TCR0 or TCR5 is TPSC2 to TPSC0 = B'111.
TCLKD input when channels 2 and 4 are set to phase counting mode.

TPU channel 2 settings	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'001x	B'0010	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00		
CCLR1, CCLR0	—	—	—	—	Other than B'10	B'10
Output function	—	Output compare output	—	PWM*2 mode 1 output	PWM mode 2 output	—

x: Don't care

Pin	Selection Method and Pin Functions
P16/PO14/ TIOCA2/ $\overline{\text{EDRAK2}}$	The pin function is switched as shown below according to the combination of the TPU channel 2 settings (by bits MD3 to MD0 in TMDR2, bits IOA3 to IOA0 in TIOR2, and bits CCLR1 and CCLR0 in TCR2), bit NDER14 in NDERH, and bit P16DDR.

Modes 1, 2, 4, 5, 6, 7 (EXPE = 1)

EDRAKE	0				1
TPU channel 2 settings	(1) in table below	(2) in table below			—
P16DDR	—	0	1	1	—
NDER14	—	—	0	1	—
Pin function	TIOCA2 output	P16 input	P16 output	PO14 output	$\overline{\text{EDRAK2}}$ output
		TIOCA2 input*1			

Mode 7 (EXPE = 0)

EDRAKE	—			
TPU channel 2 settings	(1) in table below	(2) in table below		
P16DDR	—	0	1	1
NDER14	—	—	0	1
Pin function	TIOCA2 output	P16 input	P16 output	PO14 output
		TIOCA2 input*1		

Note: 1. TIOCA2 input when MD3 to MD0 = B'0000 or B'01XX and IOA3 = 1.

TPU channel 2 settings	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'001x	B'0010	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00		
CCLR1, CCLR0	—	—	—	—	Other than B'10	B'10
Output function	—	Output compare output	—	PWM*2 mode 1 output	PWM mode 2 output	—

x: Don't care

Note: 2. TIOCB2 output disabled.

Pin	Selection Method and Pin Functions
P15/PO13/ TIOCB1/ TCLKC	The pin function is switched as shown below according to the combination of the TPU channel 1 settings (by bits MD3 to MD0 in TMDR1, bits IOB3 to IOB0 in TIOR1, and bits CCLR1 and CCLR0 in TCR1), bits TPSC2 to TPSC0 in TCR0, TCR2, TCR4, and TCR5, bit NDER13 in NDERH, and bit P15DDR.

TPU channel 1 settings	(1) in table below	(2) in table below		
P15DDR	—	0	1	1
NDER13	—	—	0	1
Pin function	TIOCB1 output	P15 input	P15 output	PO13 output
		TIOCB1 input*1		
	TCLKC input*2			

Notes: 1. TIOCB1 input when MD3 to MD0 = B'0000 or B'01XX and IOB3 to IOB0 = B'10xx.

2. TCLKC input when the setting for either TCR0 or TCR2 is TPSC2 to TPSC0 = B'110, or when the setting for either TCR4 or TCR5 is TPSC2 to TPSC0 = B'101.
TCLKC input when phase counting mode is set for channels 2 and 4.

TPU channel 1 settings	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'0010	B'0011		
IOB3 to IOB0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR1, CCLR0	—	—	—	—	Other than B'10	B'10
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don’t care

Pin	Selection Method and Pin Functions
P14/PO12/ TIOCA1	The pin function is switched as shown below according to the combination of the TPU channel 1 settings (by bits MD3 to MD0 in TMDR1, bits IOA3 to IOA0 in TIOR1, and bits CCLR1 and CCLR0 in TCR1), bit NDER12 in NDERH, and bit P14DDR.

TPU channel 1 settings	(1) in table below	(2) in table below		
P14DDR	—	0	1	1
NDER12	—	—	0	1
Pin function	TIOCA1 output	P14 input	P14 output	PO12 output
		TIOCA1 input*[1]		

Note: 1. TIOCA1 input when MD3 to MD0 = B'0000 or B'01XX and IOA3 to IOA0 = B'10xx.

TPU channel 1 settings	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'001x	B'0010	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00	Other than B'xx00	
CCLR1, CCLR0	—	—	—	—	Other than B'01	B'01
Output function	—	Output compare output	—	PWM*[2] mode 1 output	PWM mode 2 output	—

x: Don't care

Note: 2. TIOCB1 output disabled.

Pin	Selection Method and Pin Functions
P13/PO11/ TIOCD0/ TCLKB	The pin function is switched as shown below according to the combination of the TPU channel 0 settings (by bits MD3 to MD0 in TMDR0, bits IOD3 to IOD0 in TIOR0L, and bits CCLR2 to CCLR0 in TCR0), bits TPSC2 to TPSC0 in TCR0 to TCR2, bit NDER11 in NDERH, and bit P13DDR.

TPU channel 0 settings	(1) in table below	(2) in table below		
P13DDR	—	0	1	1
NDER11	—	—	0	1
Pin function	TIOCD0 output	P13 input	P13 output	PO11 output
		TIOCD0 input*1		
	TCLKB input*2			

Notes: 1. TIOCD0 input when MD3 to MD0 = B'0000 and IOD3 to IOD0 = B'10xx.

2. TCLKB input when the setting for any of TCR0 to TCR2 is TPSC2 to TPSC0 = B'101.
TCLKB input when phase counting mode is set for channels 1 and 5.

TPU channel 0 settings	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000		B'0010	B'0011		
IOD3 to IOD0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR2, CCLR0	—	—	—	—	Other than B'110	B'110
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

Pin	Selection Method and Pin Functions
P12/PO10/ TIOCC0/ TCLKA	The pin function is switched as shown below according to the combination of the TPU channel 0 settings (by bits MD3 to MD0 in TMDR0, bits IOC3 to IOC0 in TIOR0L, and bits CCLR2 to CCLR0 in TCR0), bits TPSC2 to TPSC0 in TCR0 to TCR5, bit NDER10 in NDERH, and bit P12DDR.

TPU channel 0 settings	(1) in table below	(2) in table below		
P12DDR	—	0	1	1
NDER10	—	—	0	1
Pin function	TIOCC0 output	P12 input	P12 output	PO10 output
		TIOCC0 input*1		
	TCLKA input*2			

Notes: 1. TIOCC0 input when MD3 to MD0 = B'0000 and IOC3 to IOC0 = B'10xx.

2. TCLKA input when the setting for any of TCR0 to TCR5 is TPSC2 to TPSC0 = B'100.
TCLKA input when phase counting mode is set for channels 1 and 5.

TPU channel 0 settings	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000		B'001x	B'0010	B'0011	
IOC3 to IOC0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00	Other than B'xx00	
CCLR2, CCLR0	—	—	—	—	Other than B'101	B'101
Output function	—	Output compare output	—	PWM*3 mode 1 output	PWM mode 2 output	—

x: Don't care

Note: 3. TIOCD0 output disabled.
Output disabled and settings (2) effective when BFA = 1 or BFB = 1 in TMDR0.

Pin	Selection Method and Pin Functions
P11/PO9/ TIOCB0	The pin function is switched as shown below according to the combination of the TPU channel 0 settings (by bits MD3 to MD0 in TMDR0 and bits IOB3 to IOB0 in TIOR0H), bit NDER9 in NDERH, and bit P11DDR.

TPU channel 0 settings	(1) in table below	(2) in table below		
P11DDR	—	0	1	1
NDER9	—	—	0	1
Pin function	TIOCB0 output	P11 input	P11 output	PO9 output
		TIOCB0 input*1		

Note: 1. TIOCB0 input when MD3 to MD0 = B'0000 and IOB3 to IOB0 = B'10xx.

TPU channel 0 settings	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000		B'0010	B'0011		
IOB3 to IOB0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR2, CCLR0	—	—	—	—	Other than B'010	B'010
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

Pin	Selection Method and Pin Functions
P10/PO8/ TIOCA0	The pin function is switched as shown below according to the combination of the TPU channel 0 settings (by bits MD3 to MD0 in TMDR0, bits IOA3 to IOA0 in TIOR0H, and bits CCLR2 to CCLR0 in TCR0), bit NDER8 in NDERH, and bit P10DDR.

TPU channel 0 settings	(1) in table below	(2) in table below		
P10DDR	—	0	1	1
NDER8	—	—	0	1
Pin function	TIOCA0 output	P10 input	P10 output	PO8 output
		TIOCA0 input*[1]		

Note: 1. TIOCA0 input when MD3 to MD0 = B'0000 and IOA3 to IOA0 = B'10xx.

TPU channel 0 settings	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000		B'001x	B'0010	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00	Other than B'xx00	
CCLR2, CCLR0	—	—	—	—	Other than B'001	B'001
Output function	—	Output compare output	—	PWM*[2] mode 1 output	PWM mode 2 output	—

x: Don't care

Note: 2. TIOCB0 output disabled.

5.3 Port 2

5.3.1 Overview

Port 2 is an 8-bit I/O port. Port 2 pins also function as PPG output pins (PO7 to PO0), TPU I/O pins (TIOCA3, TIOCB3, TIOCC3, TIOCD3, TIOCA4, TIOCB4, TIOCA5, and TIOCB5), EXDMAC output pins ($\overline{\text{EDRAK0}}$ and $\overline{\text{EDRAK1}}$), and interrupt input pins ($\overline{\text{IRQ15}}$ to $\overline{\text{IRQ8}}$). The functions of pins P25 to P20 are the same in all operating modes, while the functions of pins P27 and P26 change according to the operating mode. Port 2 has Schmitt-trigger inputs.

Figure 5.2 shows the port 2 pin configuration.

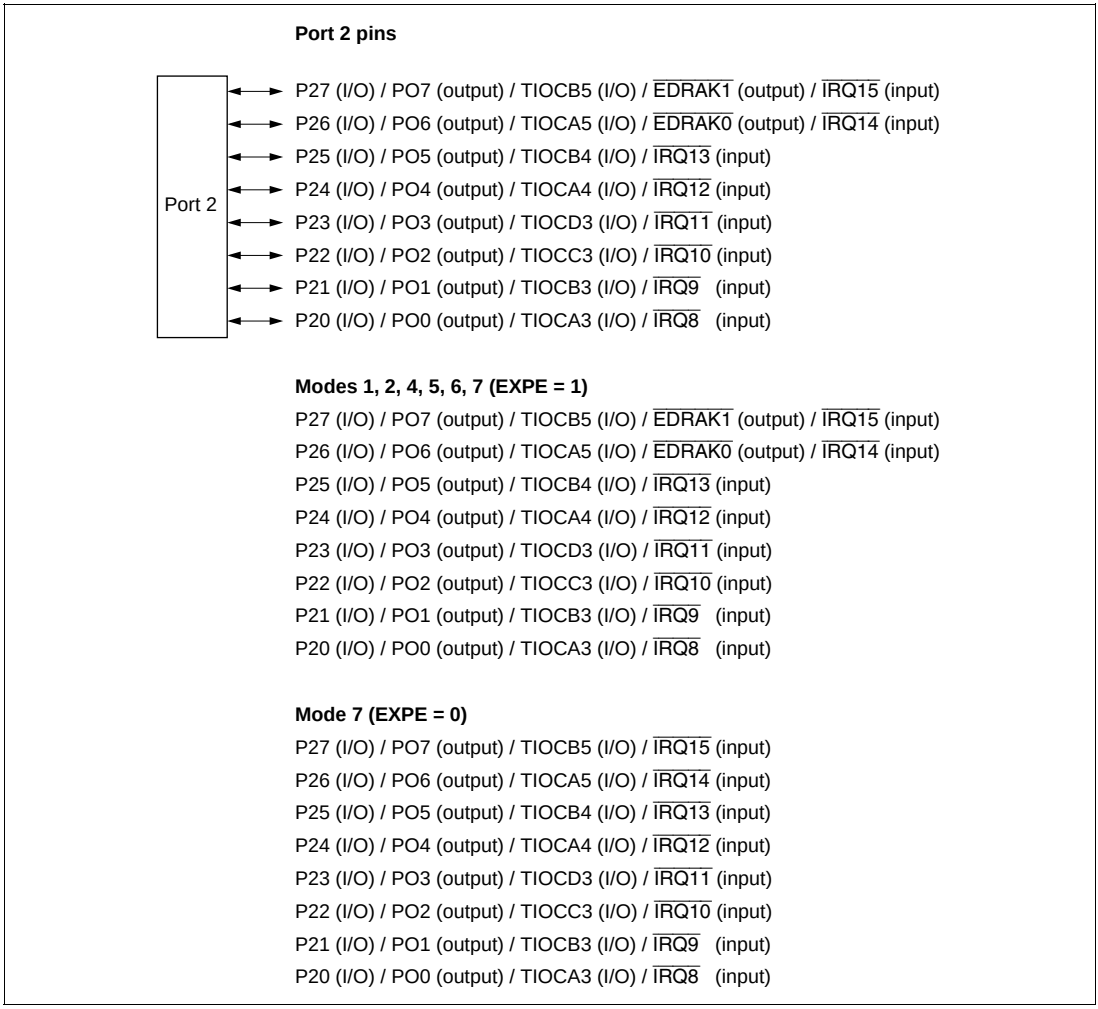


Figure 5.2 Port 2 Pin Functions

5.3.2 Register Configuration

Table 5.4 shows the port 2 register configuration.

Table 5.4 Port 2 Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port 2 data direction register	P2DDR	W	H'00	H'FE21
Port 2 data register	P2DR	R/W	H'00	H'FF61
Port 2 register	PORT2	R	Undefined	H'FF51

Note: * Lower 16 bits of the address.

Port 2 Data Direction Register (P2DDR)

Bit	7	6	5	4	3	2	1	0
	P27DDR	P26DDR	P25DDR	P24DDR	P23DDR	P22DDR	P21DDR	P20DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

P2DDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port 2. P2DDR cannot be read; if it is, an undefined value will be read.

Setting a P2DDR bit to 1 makes the corresponding port 2 pin an output pin, while clearing the bit to 0 makes the pin an input pin.

P2DDR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Port 2 Data Register (P2DR)

Bit	7	6	5	4	3	2	1	0
	P27DR	P26DR	P25DR	P24DR	P23DR	P22DR	P21DR	P20DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P2DR is an 8-bit readable/writable register that stores output data for the port 2 pins (P27 to P20).

P2DR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Port 2 Register (PORT2)

Bit	7	6	5	4	3	2	1	0
	P27	P26	P25	P24	P23	P22	P21	P20
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

Note: * Determined by the state of pins P27 to P20.

PORT2 is an 8-bit read-only register that shows the pin states. PORT2 cannot be written to; writing of output data for the port 2 pins (P27 to P20) must always be performed on P2DR.

If a port 2 read is performed while P2DDR bits are set to 1, the P2DR values are read. If a port 2 read is performed while P2DDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORT2 contents are determined by the pin states, as P2DDR and P2DR are initialized. PORT2 retains its prior state in software standby mode.

5.3.3 Pin Functions

Port 2 pins also function as PPG output pins (PO7 to PO0), TPU I/O pins (TIOCA3, TIOCB3, TIOCC3, TIOCD3, TIOCA4, TIOCB4, TIOCA5, and TIOCB5), interrupt input pins ($\overline{\text{IRQ15}}$ to $\overline{\text{IRQ8}}$), and EXDMAC output pins ($\overline{\text{EDRAK0}}$ and $\overline{\text{EDRAK1}}$). Port 2 pin functions are shown in table 5.5.

Table 5.5 Port 2 Pin Functions

Pin	Selection Method and Pin Functions
P27/PO7/ TIOCB5/ $\overline{\text{IRQ15}}$/ $\overline{\text{EDRAK1}}$	The pin function is switched as shown below according to the combination of the TPU channel 5 settings (by bits MD3 to MD0 in TMDR5, bits IOB3 to IOB0 in TIOR5, and bits CCLR1 and CCLR0 in TCR5), bit NDER7 in NDERL, bit EDRAKE in EDMDR1, bit P27DDR, and bit ITS15 in ITSR.

Modes 1, 2, 4, 5, 6, 7 (EXPE = 1)

EDRAKE	0				1
TPU channel 5 settings	(1) in table below	(2) in table below			—
P27DDR	—	0	1	1	—
NDER7	—	—	0	1	—
Pin function	TIOCB5 output	P27 input	P27 output	PO7 output	$\overline{\text{EDRAK1}}$ output
		TIOCB5 input*1			
	$\overline{\text{IRQ15}}$ interrupt input pin*2				

Mode 7 (EXPE = 0)

EDRAKE	—			
TPU channel 5 settings	(1) in table below	(2) in table below		
P27DDR	—	0	1	1
NDER7	—	—	0	1
Pin function	TIOCB5 output	P27 input	P27 output	PO7 output
		TIOCB5 input*1		
	$\overline{\text{IRQ15}}$ interrupt input pin*2			

Notes: 1. TIOCB5 input when MD3 to MD0 = B'0000 or B'01xx and IOB3 = 1.
2. $\overline{\text{IRQ15}}$ input when ITS15 = 1.

TPU channel 5 settings	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000 to B'0011		B'0010	B'0011		
IOB3 to IOB0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR1, CCLR0	—	—	—	—	Other than B'10	B'10
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

Pin	Selection Method and Pin Functions
P26/PO6/ TIOCA5/ $\overline{\text{IRQ14}}$/ $\overline{\text{EDRAK0}}$	The pin function is switched as shown below according to the combination of the TPU channel 5 settings (by bits MD3 to MD0 in TMDR5, bits IOA3 to IOA0 in TIOR5, and bits CCLR1 and CCLR0 in TCR5), bit NDER6 in NDERL, bit EDRAKE in EDMDR0, bit P26DDR, and bit ITS14 in ITSR.

Modes 1, 2, 4, 5, 6, 7 (EXPE = 1)

EDRAKE	0				1
TPU channel 5 settings	(1) in table below	(2) in table below			—
P26DDR	—	0	1	1	—
NDER6	—	—	0	1	—
Pin function	TIOCA5 output	P26 input	P26 output	PO6 output	$\overline{\text{EDRAK0}}$ output
		TIOCA5 input*1			
	$\overline{\text{IRQ14}}$ interrupt input pin*2				

Mode 7 (EXPE = 0)

EDRAKE	—			
TPU channel 5 settings	(1) in table below	(2) in table below		
P26DDR	—	0	1	1
NDER6	—	—	0	1
Pin function	TIOCA5 output	P26 input	P26 output	PO6 output
		TIOCA5 input*1		
	$\overline{\text{IRQ14}}$ interrupt input pin*2			

Notes: 1. TIOCA5 input when MD3 to MD0 = B'0000 or B'01xx and IOA3 = 1.
2. $\overline{\text{IRQ14}}$ input when ITS14 = 1.

TPU channel 5 settings	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000 to B'0011		B'0010	B'0010	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00	Other than B'xx00	
CCLR1, CCLR0	—	—	—	—	Other than B'10	B'10
Output function	—	Output compare output	—	PWM*3 mode 1 output	PWM mode 2 output	—

x: Don't care

Note: 3. TIOCB5 output disabled.

Pin	Selection Method and Pin Functions
P25/PO5/ TIOCB4/ $\overline{\text{IRQ13}}$	The pin function is switched as shown below according to the combination of the TPU channel 4 settings (by bits MD3 to MD0 in TMDR4, bits IOB3 to IOB0 in TIOR4, and bits CCLR1 and CCLR0 in TCR4), bit NDER5 in NDERL, bit P25DDR, and bit ITS13 in ITSR.

TPU channel 4 settings	(1) in table below	(2) in table below		
P25DDR	—	0	1	1
NDER5	—	—	0	1
Pin function	TIOCB4 output	P25 input	P25 output	PO5 output
		TIOCB4 input*1		
	$\overline{\text{IRQ13}}$ interrupt input pin*2			

Notes: 1. TIOCB4 input when MD3 to MD0 = B'0000 or B'01xx and IOB3 to IOB0 = B'10xx.

2. $\overline{\text{IRQ13}}$ input when ITS13 = 1.

TPU channel 5 settings	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000 to B'0011		B'0010	B'0011		
IOB3 to IOB0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR1, CCLR0	—	—	—	—	Other than B'10	B'10
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

Pin	Selection Method and Pin Functions
P24/PO4/ TIOCA4/ $\overline{\text{IRQ12}}$	The pin function is switched as shown below according to the combination of the TPU channel 4 settings (by bits MD3 to MD0 in TMDR4 and bits IOA3 to IOA0 in TIOR4), bit NDER4 in NDERL, bit P24DDR, and bit ITS12 in ITSR.

TPU channel 4 settings	(1) in table below	(2) in table below		
P24DDR	—	0	1	1
NDER4	—	—	0	1
Pin function	TIOCA4 output	P24 input	P24 output	PO4 output
		TIOCA4 input*[1]		
	$\overline{\text{IRQ12}}$ interrupt input pin*[2]			

Notes: 1. TIOCA4 input when MD3 to MD0 = B'0000 or B'01xx and IOA3 to IOA0 = B'10xx.

2. $\overline{\text{IRQ12}}$ input when ITS12 = 1.

TPU channel 4 settings	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0001 to B'01xx		B'001x	B'0010	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00	Other than B'xx00	
CCLR1, CCLR0	—	—	—	—	Other than B'10	B'10
Output function	—	Output compare output	—	PWM*[3] mode 1 output	PWM mode 2 output	—

x: Don't care

Note: 3. TIOCB4 output disabled.

Pin	Selection Method and Pin Functions
P23/PO3/ TIOCD3/ $\overline{\text{IRQ11}}$	The pin function is switched as shown below according to the combination of the TPU channel 3 settings (by bits MD3 to MD0 in TMDR3, bits IOD3 to IOD0 in TIOR3L, and bits CCLR2 to CCLR0 in TCR3), bit NDER3 in NDERL, bit P23DDR, and bit ITS11 in ITSR.

TPU channel 3 settings	(1) in table below	(2) in table below		
P23DDR	—	0	1	1
NDER3	—	—	0	1
Pin function	TIOCD3 output	P23 input	P23 output	PO3 output
		TIOCD3 input*[1]		
	$\overline{\text{IRQ11}}$ interrupt input pin*[2]			

Notes: 1. TIOCD3 input when MD3 to MD0 = B'0000 and IOD3 to IOD0 = B'10xx.

2. $\overline{\text{IRQ11}}$ input when ITS11 = 1.

TPU channel 3 settings	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0001 to B'0011		B'0010	B'0011		
IOD3 to IOD0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR2 to CCLR0	—	—	—	—	Other than B'110	B'110
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

Pin	Selection Method and Pin Functions
P22/PO2/ TIOCC3/ $\overline{\text{IRQ10}}$	The pin function is switched as shown below according to the combination of the TPU channel 3 settings (by bits MD3 to MD0 in TMDR3, bits IOC3 to IOC0 in TIOR3L, and bits CCLR2 to CCLR0 in TCR3), bit NDER2 in NDERL, bit P22DDR, and bit ITS10 in ITSR.

TPU channel 3 settings	(1) in table below	(2) in table below		
P22DDR	—	0	1	1
NDER2	—	—	0	1
Pin function	TIOCC3 output	P22 input	P22 output	PO2 output
		TIOCC3 input*1		
	$\overline{\text{IRQ10}}$ interrupt input pin*2			

Notes: 1. TIOCC3 input when MD3 to MD0 = B'0000 and IOC3 to IOC0 = B'10xx.
2. $\overline{\text{IRQ10}}$ input when ITS10 = 1.

TPU channel 3 settings	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0001 to B'01xx		B'001x	B'0010	B'0011	
IOC3 to IOC0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00	Other than B'xx00	
CCLR2 to CCLR0	—	—	—	—	Other than B'101	B'101
Output function	—	Output compare output	—	PWM*3 mode 1 output	PWM mode 2 output	—

x: Don't care

Note: 3. TIOCD3 output disabled.
Output disabled and settings (2) effective when BFA = 1 or BFB = 1 in TMDR3.

Pin	Selection Method and Pin Functions
P21/PO1/ TIOCB3/$\overline{\text{IRQ9}}$	The pin function is switched as shown below according to the combination of the TPU channel 3 settings (by bits MD3 to MD0 in TMDR3, bits IOB3 to IOB0 in TIOR3H, and bits CCLR2 to CCLR0 in TCR3), bit NDER1 in NDERL, bit P21DDR, and bit ITS9 in ITSR.

TPU channel 3 settings	(1) in table below	(2) in table below		
P21DDR	—	0	1	1
NDER1	—	—	0	1
Pin function	TIOCB3 output	P21 input	P21 output	PO1 output
		TIOCB3 input*1		
	$\overline{\text{IRQ9}}$ interrupt input pin*2			

Notes: 1. TIOCB3 input when MD3 to MD0 = B'0000 and IOB3 to IOB0 = B'10xx.

2. $\overline{\text{IRQ9}}$ input when ITS9 = 1.

TPU channel 3 settings	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0001 to B'0011		B'0010	B'0011		
IOB3 to IOB0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR2 to CCLR0	—	—	—	—	Other than B'010	B'010
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

Pin	Selection Method and Pin Functions
P20/PO0/ TIOCA3/$\overline{\text{IRQ8}}$	The pin function is switched as shown below according to the combination of the TPU channel 3 settings (by bits MD3 to MD0 in TMDR3, bits IOA3 to IOA0 in TIOR3H, and bits CCLR2 to CCLR0 in TCR3), bit NDER0 in NDERL, bit P20DDR, and bit ITS8 in ITSR.

TPU channel 3 settings	(1) in table below	(2) in table below		
P20DDR	—	0	1	1
NDER0	—	—	0	1
Pin function	TIOCA3 output	P20 input	P20 output	PO0 output
		TIOCA3 input*1		
	$\overline{\text{IRQ8}}$ interrupt input pin*2			

Notes: 1. TIOCA3 input when MD3 to MD0 = B'0000 and IOA3 to IOA0 = B'10xx.

2. $\overline{\text{IRQ8}}$ input when ITS8 = 1.

TPU channel 3 settings	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0001 to B'01xx		B'001x	B'0010	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00	Other than B'xx00	
CCLR2 to CCLR0	—	—	—	—	Other than B'001	B'001
Output function	—	Output compare output	—	PWM*3 mode 1 output	PWM mode 2 output	—

x: Don't care

Note: 3. TIOCB3 output disabled.

5.4 Port 3

5.4.1 Overview

Port 3 is a 6-bit I/O port. Port 3 pins also function as SCI input/output pins (TxD0/IrTxD, RxD0/IrRxD, SCK0, TxD1, RxD1, and SCK1), and a bus control signal output pin ($\overline{OE}$). The functions of pins P34 to P30 are the same in all operating modes, while the function of pin P35 changes according to the operating mode.

Figure 5.3 shows the port 3 pin configuration.

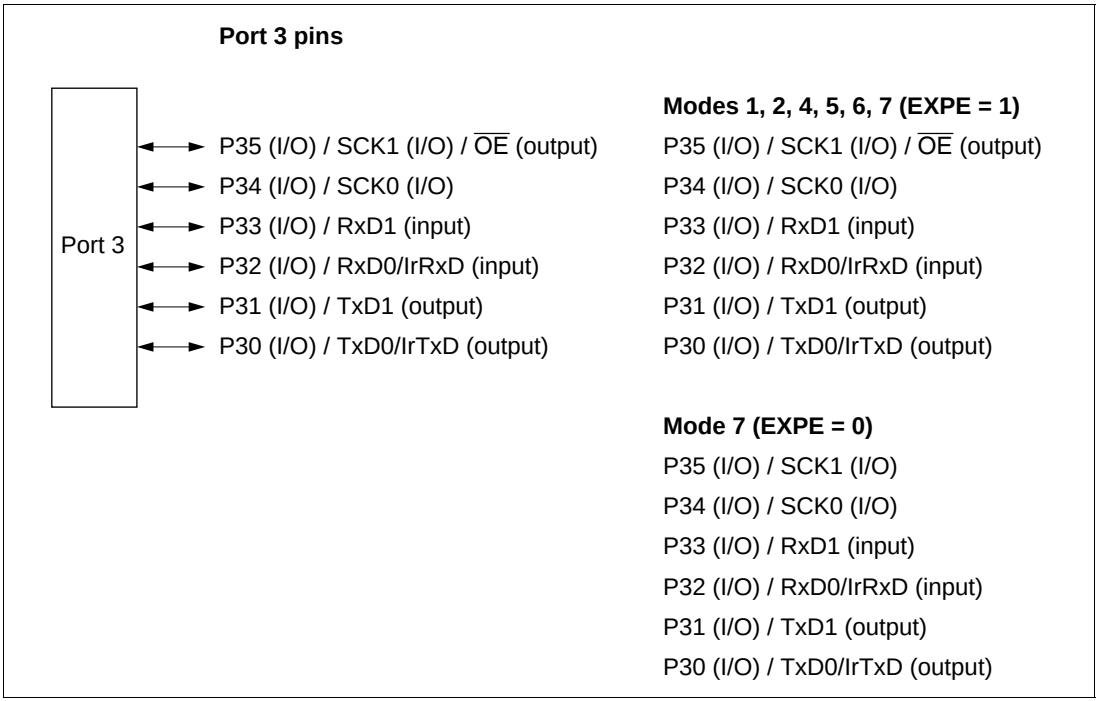


Figure 5.3 Port 3 Pin Functions

5.4.2 Register Configuration

Table 5.6 shows the port 3 register configuration.

Table 5.6 Port 3 Registers

Name	Abbreviation	R/W	Initial Value*[2]	Address*[1]
Port 3 data direction register	P3DDR	W	H'00	H'FE22
Port 3 data register	P3DR	R/W	H'00	H'FF62
Port 3 register	PORT3	R	Undefined	H'FF52
Port 3 open drain control register	P3ODR	R/W	H'00	H'FE3C
Port function control register 2	PFCR2	R/W	H'0E	H'FE34

Notes: 1. Lower 16 bits of the address.
2. Value of bits 5 to 0.

Port 3 Data Direction Register (P3DDR)

Bit	7	6	5	4	3	2	1	0
	—	—	P35DDR	P34DDR	P33DDR	P32DDR	P31DDR	P30DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	W	W	W	W	W	W

P3DDR is a 6-bit write-only register, the individual bits of which specify input or output for the pins of port 3. P3DDR cannot be read; if it is, an undefined value will be read. Bits 7 and 6 are reserved.

Setting a P3DDR bit to 1 makes the corresponding port 3 pin an output pin, while clearing the bit to 0 makes the pin an input pin.

P3DDR is initialized to H'00 (bits 5 to 0) by a reset and in hardware standby mode. It retains its prior state in software standby mode. As the SCI is initialized, the pin states are determined by the P3DDR and P3DR specifications.

Port 3 Data Register (P3DR)

Bit	7	6	5	4	3	2	1	0
	—	—	P35DR	P34DR	P33DR	P32DR	P31DR	P30DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

P3DR is a 6-bit readable/writable register that stores output data for the port 3 pins (P35 to P30).

Bits 7 and 6 are reserved; they are always read as 0 and cannot be modified.

P3DR is initialized to H'00 (bits 5 to 0) by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Port 3 Register (PORT3)

Bit	7	6	5	4	3	2	1	0
	—	—	P35	P34	P33	P32	P31	P30
Initial value	Undefined	Undefined	—*	—*	—*	—*	—*	—*
Read/Write	—	—	R	R	R	R	R	R

Note: * Determined by the state of pins P35 to P30.

PORT3 is a 6-bit read-only register that shows the pin states. PORT3 cannot be written to; writing of output data for the port 3 pins (P35 to P30) must always be performed on P3DR.

Bits 7 and 6 are reserved; if read they will return an undefined value.

If a port 3 read is performed while P3DDR bits are set to 1, the P3DR values are read. If a port 3 read is performed while P3DDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORT3 contents are determined by the pin states, as P3DDR and P3DR are initialized. PORT3 retains its prior state in software standby mode.

Port 3 Open Drain Control Register (P3ODR)

Bit	7	6	5	4	3	2	1	0
	—	—	P35ODR	P34ODR	P33ODR	P32ODR	P31ODR	P30ODR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

P3ODR is a 6-bit readable/writable register that controls the PMOS on/off status for each port 3 pin (P35 to P30).

Bits 7 and 6 are reserved; they are always read as 0 and cannot be modified.

Setting a P3ODR bit to 1 makes the corresponding port 3 pin an NMOS open-drain output pin, while clearing the bit to 0 makes the pin a CMOS output pin.

P3ODR is initialized to H'00 (bits 5 to 0) by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Port Function Control Register 2 (PFCR2)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	ASOE	LWROE	OES	DMACS
Initial value	0	0	0	0	1	1	1	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

PFCR2 is an 8-bit readable/writable register that performs I/O port control. PFCR2 is initialized to H'0E by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Bits 7 to 4—Reserved: These bits are always read as 0, and should only be written with 0.

Bit 1—OE Output Select (OES): Selects the $\overline{OE}$ output pin port when the OEE bit is set to 1 in DRAMCR (enabling $\overline{OE}$ output).

Bit 1 OES	Description	
0	P35 is designated as $\overline{OE}$ output pin	
1	PH3 is designated as $\overline{OE}$ output pin	(Initial value)

5.4.3 Pin Functions

Port 3 pins also function as SCI input/output pins (TxD0/IrTxD, RxD0/IrRxD, SCK0, TxD1, RxD1, and SCK1), and a bus control signal output pin ($\overline{OE}$). Port 3 pin functions are shown in table 5.7.

Table 5.7 Port 3 Pin Functions

Pin	Selection Method and Pin Functions
P35/SCK1/$\overline{OE}$	The pin function is switched as shown below according to the combination of the C/$\overline{A}$ bit in SMR of SCI1, bits CKE0 and CKE1 and RMTS2 to RMTS0 in SCR, bit OES in PFCR2, and bit P35DDR.

Modes 1, 2, 4, 5, 6, 7 (EXPE = 1)

OEE	0					1					
OES	—					1					0
CKE1	0				1	0				1	—
C/$\overline{A}$	0			1	—	0			1	—	—
CKE0	0		1	—	—	0		1	—	—	—
P35DDR	0	1	—	—	—	0	1	—	—	—	—
Pin function	P35 input pin	P35 output pin*	SCK1 output pin*	SCK1 output pin*	SCK1 input pin	P35 input pin	P35 output pin*	SCK1 output pin*	SCK1 output pin*	SCK1 input pin	$\overline{OE}$ output

Mode 7 (EXPE = 0)

OEE	—				
OES	—				
CKE1	0				—
C/$\overline{A}$	0			1	—
CKE0	0		1	—	—
P35DDR	0	1	—	—	—
Pin function	P35 input pin	P35 output pin*	SCK1 output pin*	SCK1 output pin*	SCK1 input pin

Note: * NMOS open-drain output when P35ODR = 1.

P34/SCK0 — The pin function is switched as shown below according to the combination of bit C/$\overline{A}$ in SMR of SCI0, bits CKE0 and CKE1 in SCR, and bit P34DDR.

CKE1	0				1
C/$\overline{A}$	0			1	—
CKE0	0		1	—	—
P34DDR	0	1	—	—	—
Pin function	P34 input pin	P34 output pin*	SCK0 output pin*	SCK0 output pin*	SCK0 input pin

Note: * NMOS open-drain output when P34ODR = 1.

Pin	Selection Method and Pin Functions
P33/RxD1	The pin function is switched as shown below according to the combination of bit RE in SCR of SCI1 and bit P33DDR.

RE	0		1
P33DDR	0	1	—
Pin function	P33 input pin	P33 output pin*	RxD1 input pin

Note: * NMOS open-drain output when P33ODR = 1.

P32/RxD0/ IrRxD — The pin function is switched as shown below according to the combination of bit RE in SCR of SCI0 and bit P32DDR.

RE	0		1
P32DDR	0	1	—
Pin function	P32 input pin	P32 output pin*	RxD0/IrRxD input pin

Note: * NMOS open-drain output when P32ODR = 1.

P31/TxD1 — The pin function is switched as shown below according to the combination of bit TE in SCR of SCI1 and bit P31DDR.

TE	0		1
P31DDR	0	1	—
Pin function	P31 input pin	P31 output pin*	TxD1 output pin*

Note: * NMOS open-drain output when P31ODR = 1.

P30/TxD0/ IrTxD — The pin function is switched as shown below according to the combination of bit TE in SCR of SCI0 and bit P30DDR.

TE	0		1
P30DDR	0	1	—
Pin function	P30 input pin	P30 output pin*	TxD0/IrTxD output pin*

Note: * NMOS open-drain output when P30ODR = 1.

5.5 Port 4

5.5.1 Overview

Port 4 is an 8-bit input-only port. Port 4 pins also function as A/D converter analog input pins (AN0 to AN7) and D/A converter analog output pins (DA0 and DA1). Port 4 pin functions are the same in all operating modes.

Figure 5.4 shows the port 4 pin configuration.

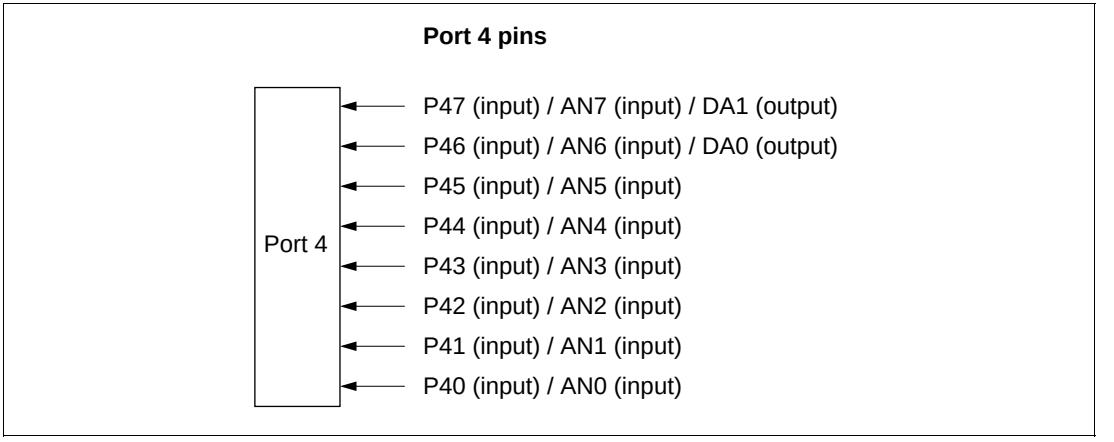


Figure 5.4 Port 4 Pin Functions

5.5.2 Register Configuration

Table 5.8 shows the port 4 register configuration. Port 4 is an input-only register, and does not have a data direction register or data register.

Table 5.8 Port 4 Register

Name	Abbreviation	R/W	Initial Value	Address*
Port 4 register	PORT4	R	Undefined	H'FF53

Note: * Lower 16 bits of the address.

Port 4 Register (PORT4)

The pin states are always read when a port 4 read is performed.

Bit	7	6	5	4	3	2	1	0
	P47	P46	P45	P44	P43	P42	P41	P40
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

Note: * Determined by the state of pins P47 to P40.

5.5.3 Pin Functions

Port 4 pins also function as A/D converter analog input pins (AN0 to AN7) and D/A converter analog output pins (DA0 and DA1).

5.6 Port 5

5.6.1 Overview

Port 5 comprises a 4-bit I/O port (P53 to P50) and a 4-bit input-only port (P57 to P54). Port 5 pins also function as SCI input/output pins (TxD2, RxD2, and SCK2), the A/D converter input pin ($\overline{\text{ADTRG}}$), A/D converter analog input pins (AN12 to AN15), D/A converter analog output pins (DA2 and DA3), and interrupt input pins ($\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$). Port 5 pin functions are the same in all operating modes.

Figure 5.5 shows the port 5 pin configuration.

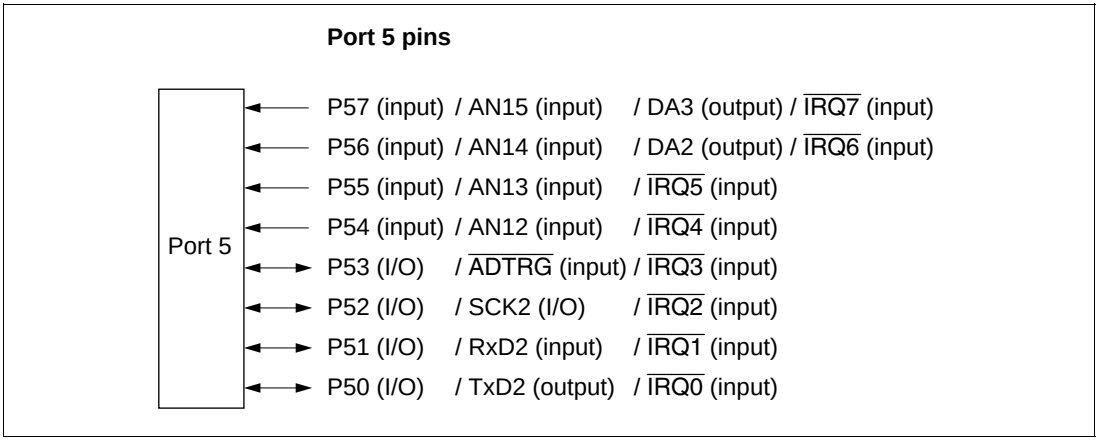


Figure 5.5 Port 5 Pin Functions

5.6.2 Register Configuration

Table 5.9 shows the port 5 register configuration. Bits 7 to 4 of port 5 are input-only ports, and do not have corresponding data direction register or data register bits.

Table 5.9 Port 5 Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port 5 data direction register	P5DDR	W	H'00	H'FE24
Port 5 data register	P5DR	R/W	H'00	H'FF64
Port 5 register	PORT5	R	Undefined	H'FF54

Note: * Lower 16 bits of the address.

Port 5 Data Direction Register (P5DDR)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	P53DDR	P52DDR	P51DDR	P50DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	W	W	W	W

P5DDR is a 4-bit write-only register, the individual bits of which specify input or output for the pins of port 5. P5DDR cannot be read; if it is, an undefined value will be read. Bits 7 to 4 are reserved.

Setting a P5DDR bit to 1 makes the corresponding port 5 pin an output pin, while clearing the bit to 0 makes the pin an input pin.

P5DDR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode. As the SCI is initialized, the pin states are determined by the P5DDR and P5DR specifications.

Port 5 Data Register (P5DR)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	P53DR	P52DR	P51DR	P50DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

P5DR is a 4-bit readable/writable register that stores output data for the port 5 pins (P53 to P50).

Bits 7 to 4 are reserved; they are always read as 0 and cannot be modified.

P5DR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Port 5 Register (PORT5)

Bit	7	6	5	4	3	2	1	0
	P57	P56	P55	P54	P53	P52	P51	P50
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

Note: * Determined by the state of pins P57 to P50.

PORT5 is an 8-bit read-only register that shows the pin states. PORT5 cannot be written to; writing of output data for the port 5 pins (P53 to P50) must always be performed on P5DR.

When a port 5 read is performed, the pin states are always read from bits 7 to 4 regardless of the P5DDR settings.

If a port 5 read is performed while P5DDR bits are set to 1, the P5DR values are read. If a port 5 read is performed while P5DDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORT5 contents are determined by the pin states, as P5DDR and P5DR are initialized. PORT5 retains its prior state in software standby mode.

5.6.3 Pin Functions

Port 5 pins also function as SCI input/output pins (TxD2, RxD2, and SCK2), the A/D converter input pin ($\overline{\text{ADTRG}}$), A/D converter analog input pins (AN15 to AN12), D/A converter analog output pins (DA3 and DA2), and interrupt input pins ($\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$). Port 5 pin functions are shown in table 5.10.

Table 5.10 Port 5 Pin Functions

Pin	Selection Method and Pin Functions
P57/AN15/ DA3/$\overline{\text{IRQ7}}$	The pin function is switched as shown below according to bit ITS7 in ITSR.

Pin function	$\overline{\text{IRQ7}}$ interrupt input pin*
	AN15 input
	DA3 output

Note: * $\overline{\text{IRQ7}}$ input when ITS7 = 0.

P56/AN14/ DA2/$\overline{\text{IRQ6}}$	The pin function is switched as shown below according to bit ITS6 in ITSR.

Pin function	$\overline{\text{IRQ6}}$ interrupt input pin*
	AN14 input
	DA2 output

Note: * $\overline{\text{IRQ6}}$ input when ITS6 = 0.

P55/AN13/ $\overline{\text{IRQ5}}$	The pin function is switched as shown below according to bit ITS5 in ITSR.

Pin function	$\overline{\text{IRQ5}}$ interrupt input pin*
	AN13 input

Note: * $\overline{\text{IRQ5}}$ input when ITS5 = 0.

P54/AN12/ $\overline{\text{IRQ4}}$	The pin function is switched as shown below according to bit ITS4 in ITSR.

Pin function	$\overline{\text{IRQ4}}$ interrupt input pin*
	AN12 input

Note: * $\overline{\text{IRQ4}}$ input when ITS4 = 0.

P53/$\overline{\text{ADTRG}}$/ $\overline{\text{IRQ3}}$	The pin function is switched as shown below according to the combination of bits TRGS1 and TRGS0 in the A/D control register (ADCR), bit ITS3 in ITSR, and bit P53DDR.

P53DDR	0	1
Pin function	P53 input pin	P53 output pin
	$\overline{\text{ADTRG}}$ input pin*[1]	
	$\overline{\text{IRQ3}}$ interrupt input pin*[2]	

Notes: 1. $\overline{\text{ADTRG}}$ input when TRGS1 = TRGS0 = 0.
2. $\overline{\text{IRQ3}}$ input when ITS3 = 0.

Pin	Selection Method and Pin Functions

P52/SCK2/$\overline{\text{IRQ2}}$

The pin function is switched as shown below according to the combination of bit C/$\overline{\text{A}}$ in SMR of SCI2, bits CKE0 and CKE1 in SCR, bit ITS2 in ITSR, and bit P52DDR.

CKE1	0				1
C/$\overline{\text{A}}$	0			1	—
CKE0	0		1	—	—
P52DDR	0	1	—	—	—
Pin function	P52 input pin	P52 output pin	SCK2 output pin	SCK2 output pin	SCK2 input pin
	$\overline{\text{IRQ2}}$ interrupt input pin*				

Note: * $\overline{\text{IRQ2}}$ input when ITS2 = 0.

P51/RxD2/$\overline{\text{IRQ1}}$

The pin function is switched as shown below according to the combination of bit RE in SCR of SCI2, bit ITS1 in ITSR, and bit P51DDR.

RE	0		1
P51DDR	0	1	—
Pin function	P51 input pin	P51 output pin	RxD2 input pin
	$\overline{\text{IRQ1}}$ interrupt input pin*		

Note: * $\overline{\text{IRQ1}}$ input when ITS1 = 0.

P50/TxD2/$\overline{\text{IRQ0}}$

The pin function is switched as shown below according to the combination of bit TE in SCR of SCI2, bit ITS0 in ITSR, and bit P50DDR.

TE	0		1
P50DDR	0	1	—
Pin function	P50 input pin	P50 output pin	TxD2 input pin
	$\overline{\text{IRQ0}}$ interrupt input pin*		

Note: * $\overline{\text{IRQ0}}$ input when ITS0 = 0.

5.7 Port 6

5.7.1 Overview

Port 6 is a 6-bit I/O port. Port 6 pins also function as 8-bit timer input/output pins (TMRI0, TMCI0, TMO0, TMRI1, TMCI1, and TMO1), interrupt input pins ($\overline{\text{IRQ13}}$ to $\overline{\text{IRQ8}}$), and DMAC input/output pins ($\overline{\text{DREQ0}}$, $\overline{\text{TEND0}}$, $\overline{\text{DACK0}}$, $\overline{\text{DREQ1}}$, $\overline{\text{TEND1}}$, and $\overline{\text{DACK1}}$). Port 6 pin functions are the same in all operating modes.

DMAC input/output pins can be switched to port 7 by setting the DMACS bit in PFCR2. When pins P65 to P60 are used for IRQ input, they are Schmitt-trigger inputs.

Figure 5.6 shows the port 6 pin configuration.

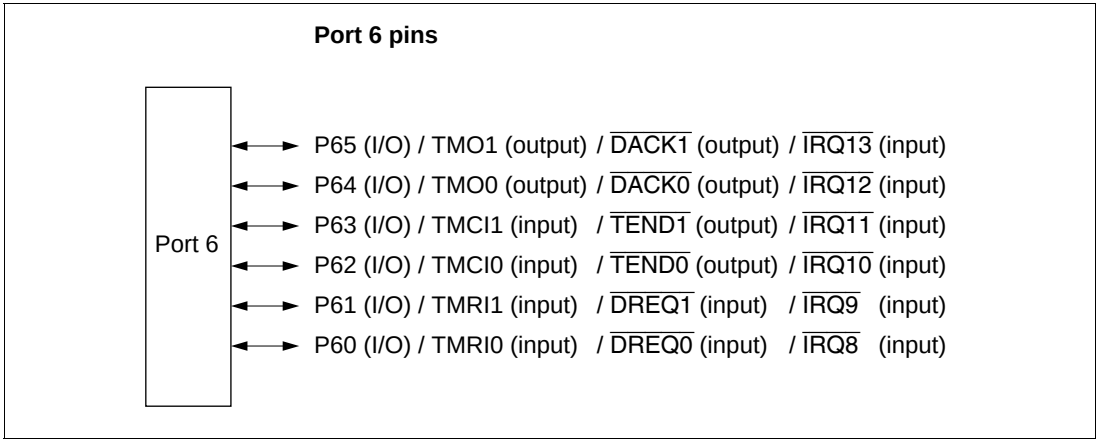


Figure 5.6 Port 6 Pin Functions

5.7.2 Register Configuration

Table 5.11 shows the port 6 register configuration.

Table 5.11 Port 6 Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port 6 data direction register	P6DDR	W	H'00	H'FE25
Port 6 data register	P6DR	R/W	H'00	H'FF65
Port 6 register	PORT6	R	Undefined	H'FF55
Port function control register 2	PFCR2	R/W	H'0E	H'FE34

Note: * Lower 16 bits of the address.

Port 6 Data Direction Register (P6DDR)

Bit	7	6	5	4	3	2	1	0
	—	—	P65DDR	P64DDR	P63DDR	P62DDR	P61DDR	P60DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	W	W	W	W	W	W

P6DDR is a 6-bit write-only register, the individual bits of which specify input or output for the pins of port 6. P6DDR cannot be read; if it is, an undefined value will be read. Bits 7 and 6 are reserved.

Setting a P6DDR bit to 1 makes the corresponding port 6 pin an output pin, while clearing the bit to 0 makes the pin an input pin.

P6DDR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Port 6 Data Register (P6DR)

Bit	7	6	5	4	3	2	1	0
	—	—	P65DR	P64DR	P63DR	P62DR	P61DR	P60DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

P6DR is a 6-bit readable/writable register that stores output data for the port 6 pins (P65 to P60).

Bits 7 and 6 are reserved; they are always read as 0 and cannot be modified.

P6DR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Port 6 Register (PORT6)

Bit	7	6	5	4	3	2	1	0
	—	—	P65	P64	P63	P62	P61	P60
Initial value	Undefined	Undefined	—*	—*	—*	—*	—*	—*
Read/Write	—	—	R	R	R	R	R	R

Note: * Determined by the state of pins P65 to P60.

PORT6 is a 6-bit read-only register that shows the pin states. PORT6 cannot be written to; writing of output data for the port 6 pins (P65 to P60) must always be performed on P6DR.

Bits 7 and 6 are reserved; if read they will return an undefined value.

If a port 6 read is performed while P6DDR bits are set to 1, the P6DR values are read. If a port 6 read is performed while P6DDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORT6 contents are determined by the pin states, as P6DDR and P6DR are initialized. PORT6 retains its prior state in software standby mode.

Port Function Control Register 2 (PFCR2)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	ASOE	LWROE	OES	DMACS
Initial value	0	0	0	0	1	1	1	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

PFCR2 is an 8-bit readable/writable register that performs I/O port control. PFCR2 is initialized to H'0E by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Bits 7 to 4—Reserved: These bits are always read as 0, and should only be written with 0.

Bit 0—DMAC Control Pin Select (DMACS): Selects the DMAC control port.

Bit 0 DMACS	Description	
0	P65 to P60 are designated as DMAC control pins	(Initial value)
1	P75 to P70 are designated as DMAC control pins	

5.7.3 Pin Functions

Port 6 pins also function as 8-bit timer input/output pins (TMRI0, TMCI0, TMO0, TMRI1, TMCI1, and TMO1), interrupt input pins ($\overline{\text{IRQ13}}$ to $\overline{\text{IRQ8}}$), and DMAC input/output pins ($\overline{\text{DREQ0}}$, $\overline{\text{TEND0}}$, $\overline{\text{DACK0}}$, $\overline{\text{DREQ1}}$, $\overline{\text{TEND1}}$, and $\overline{\text{DACK1}}$). Port 6 pin functions are shown in table 5.12.

Table 5.12 Port 6 Pin Functions

Pin	Selection Method and Pin Functions
P65/TMO1/$\overline{\text{DACK1}}$/$\overline{\text{IRQ13}}$	The pin function is switched as shown below according to the combination of bit DMACS in PFCR2, bit SAE1 in DMABCRH, bits OS3 to OS0 in TCSR1 of the 8-bit timer, bit P65DDR, and bit ITS13 in ITSR.

SAE1	0			1			
DMACS	—			1			0
OS3 to OS0	All 0		Not all 0	All 0		Not all 0	—
P65DDR	0	1	—	0	1	—	—
Pin function	P65 input pin	P65 output pin	TMO1 output pin	P65 input pin	P65 output pin	TMO1 output pin	$\overline{\text{DACK1}}$ output pin
	$\overline{\text{IRQ13}}$ interrupt input pin*						

Note: * $\overline{\text{IRQ13}}$ interrupt input when ITS13 = 0.

P64/TMO0/$\overline{\text{DACK0}}$/$\overline{\text{IRQ12}}$	The pin function is switched as shown below according to the combination of bit DMACS in PFCR2, bit SAE1 in DMABCRH, bits OS3 to OS0 in TCSR1 of the 8-bit timer, bit P64DDR, and bit ITS12 in ITSR.

SAE0	0			1			
DMACS	—			1			0
OS3 to OS0	All 0		Not all 0	All 0		Not all 0	—
P64DDR	0	1	—	0	1	—	—
Pin function	P64 input pin	P64 output pin	TMO0 output pin	P64 input pin	P64 output pin	TMO0 output pin	$\overline{\text{DACK0}}$ output pin
	$\overline{\text{IRQ12}}$ interrupt input pin*						

Note: * $\overline{\text{IRQ12}}$ interrupt input when ITS12 = 0.

Pin	Selection Method and Pin Functions
P63/TMCI1/ $\overline{\text{TEND1}}$/$\overline{\text{IRQ11}}$	The pin function is switched as shown below according to the combination of bit DMACS in PFCR2, bit TEE1 in DMATCR of the DMAC, bit P63DDR, and bit ITS11 in ITSR.

TEE1	0		1		
DMACS	—		1		0
P63DDR	0	1	0	1	—
Pin function	P63 input pin	P63 output pin	P63 input pin	P63 output pin	$\overline{\text{TEND1}}$ output pin
	$\overline{\text{IRQ11}}$ interrupt input pin*				

Note: * $\overline{\text{IRQ11}}$ interrupt input when ITS11 = 0.

P62/TMCI0/ $\overline{\text{TEND0}}$/$\overline{\text{IRQ10}}$	The pin function is switched as shown below according to the combination of bit DMACS in PFCR2, bit TEE0 in DMATCR of the DMAC, bit P62DDR, and bit ITS10 in ITSR.

TEE0	0		1		
DMACS	—		1		0
P62DDR	0	1	0	1	—
Pin function	P62 input pin	P62 output pin	P62 input pin	P62 output pin	$\overline{\text{TEND0}}$ output pin
	$\overline{\text{IRQ10}}$ interrupt input pin*				

Note: * $\overline{\text{IRQ10}}$ interrupt input when ITS10 = 0.

P61/TMRI1/ $\overline{\text{DREQ1}}$/$\overline{\text{IRQ9}}$	The pin function is switched as shown below according to the combination of bit P61DDR and bit ITS9 in ITSR.

P61DDR	0	1
Pin function	P61 input pin	P61 output pin
	TMRI1 input pin	
	$\overline{\text{DREQ1}}$ input pin*[1]	
	$\overline{\text{IRQ9}}$ interrupt input pin*[2]	

Notes: 1. $\overline{\text{DREQ1}}$ input when DMAKS = 0.
2. $\overline{\text{IRQ9}}$ interrupt input when ITS9 = 0.

Pin	Selection Method and Pin Functions
P60/TMRI0/ $\overline{\text{DREQ0}}$/$\overline{\text{IRQ8}}$	The pin function is switched as shown below according to the combination of bit P60DDR and bit ITS8 in ITSR.

P60DDR	0	1
Pin function	P60 input pin	P60 output pin
	TMRI0 input pin	
	$\overline{\text{DREQ0}}$ input pin*[1]	
	$\overline{\text{IRQ8}}$ interrupt input pin*[2]	

Notes: 1. $\overline{\text{DREQ0}}$ input when DMAKS = 0.
2. $\overline{\text{IRQ8}}$ interrupt input when ITS8 = 0.

5.8 Port 7

5.8.1 Overview

Port 7 is a 6-bit I/O port. Port 7 pins also function as DMAC input/output pins ($\overline{\text{DREQ0}}$, $\overline{\text{TEND0}}$, $\overline{\text{DACK0}}$, $\overline{\text{DREQ1}}$, $\overline{\text{TEND1}}$, and $\overline{\text{DACK1}}$) and EXDMAC input/output pins ($\overline{\text{EDREQ0}}$, $\overline{\text{ETEND0}}$, $\overline{\text{EDACK0}}$, $\overline{\text{EDREQ1}}$, $\overline{\text{ETEND1}}$, and $\overline{\text{EDACK1}}$). The functions of pins P75 to P70 change according to the operating mode.

DMAC input/output pins can be switched to port 6 by setting the DMACS bit in PFCR2.

Figure 5.7 shows the port 7 pin configuration.

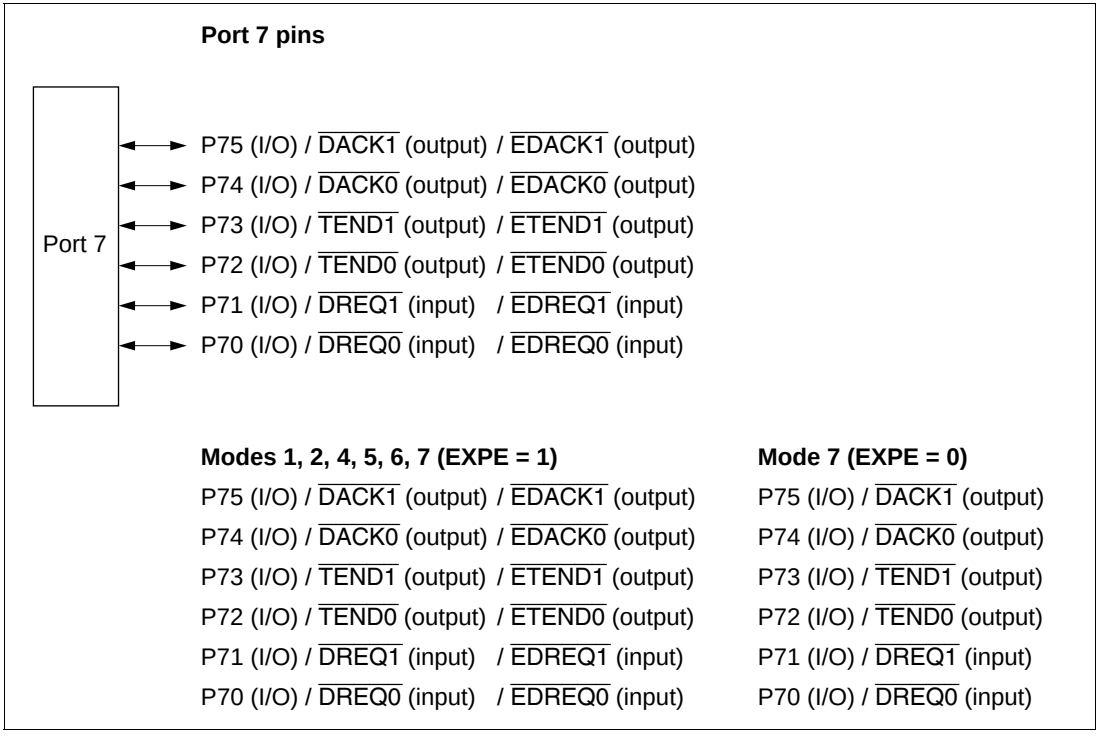


Figure 5.7 Port 7 Pin Functions

5.8.2 Register Configuration

Table 5.13 shows the port 7 register configuration.

Table 5.13 Port 7 Registers

Name	Abbreviation	R/W	Initial Value	Address*[1]
Port 7 data direction register	P7DDR	W	H'00*[2]	H'FE26
Port 7 data register	P7DR	R/W	H'00*[2]	H'FF66
Port 7 register	PORT7	R	Undefined	H'FF56
Port function control register 2	PFCR2	R/W	H'0E	H'FE34

Notes: 1. Lower 16 bits of the address.
2. Value of bits 5 to 0.

Port 7 Data Direction Register (P7DDR)

Bit	7	6	5	4	3	2	1	0
	—	—	P75DDR	P74DDR	P73DDR	P72DDR	P71DDR	P70DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	W	W	W	W	W	W

P7DDR is a 6-bit write-only register, the individual bits of which specify input or output for the pins of port 7. P7DDR cannot be read; if it is, an undefined value will be read. Bits 7 and 6 are reserved.

Setting a P7DDR bit to 1 makes the corresponding port 7 pin an output pin, while clearing the bit to 0 makes the pin an input pin.

P7DDR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Port 7 Data Register (P7DR)

Bit	7	6	5	4	3	2	1	0
	—	—	P75DR	P74DR	P73DR	P72DR	P71DR	P70DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

P7DR is a 6-bit readable/writable register that stores output data for the port 7 pins (P75 to P70).

Bits 7 and 6 are reserved; they are always read as 0 and cannot be modified.

P7DR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Port 7 Register (PORT7)

Bit	7	6	5	4	3	2	1	0
	—	—	P75	P74	P73	P72	P71	P70
Initial value	Undefined	Undefined	—*	—*	—*	—*	—*	—*
Read/Write	—	—	R	R	R	R	R	R

Note: * Determined by the state of pins P75 to P70.

PORT7 is a 6-bit read-only register that shows the pin states. PORT7 cannot be written to; writing of output data for the port 7 pins (P75 to P70) must always be performed on P7DR.

Bits 7 and 6 are reserved; if read they will return an undefined value.

If a port 7 read is performed while P7DDR bits are set to 1, the P7DR values are read. If a port 7 read is performed while P7DDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORT7 contents are determined by the pin states, as P7DDR and P7DR are initialized. PORT7 retains its prior state in software standby mode.

Port Function Control Register 2 (PFCR2)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	ASOE	LWROE	OES	DMACS
Initial value	0	0	0	0	1	1	1	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

PFCR2 is an 8-bit readable/writable register that performs I/O port control. PFCR2 is initialized to H'0E by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Bits 7 to 4—Reserved: These bits are always read as 0, and should only be written with 0.

Bit 0—DMAC Control Pin Select (DMACS): Selects the DMAC control port.

Bit 0 DMACS	Description	
0	P65 to P60 are designated as DMAC control pins	(Initial value)
1	P75 to P70 are designated as DMAC control pins	

5.8.3 Pin Functions

Port 7 pins also function as DMAC input/output pins ($\overline{\text{DREQ0}}$, $\overline{\text{TEND0}}$, $\overline{\text{DACK0}}$, $\overline{\text{DREQ1}}$, $\overline{\text{TEND1}}$, and $\overline{\text{DACK1}}$) and EXDMAC input/output pins ($\overline{\text{EDREQ0}}$, $\overline{\text{ETEND0}}$, $\overline{\text{EDACK0}}$, $\overline{\text{EDREQ1}}$, $\overline{\text{ETEND1}}$, and $\overline{\text{EDACK1}}$). Port 7 pin functions are shown in table 5.14.

Table 5.14 Port 7 Pin Functions

Pin | **Selection Method and Pin Functions**

P75/$\overline{\text{DACK1}}$/ $\overline{\text{EDACK1}}$

The pin function is switched as shown below according to the combination of bit DMACS in PFCR2, bit SAE1 in DMABCRH, bit AMS in EDMDR1, and bit P75DDR.

Modes 1, 2, 4, 5, 6, 7 (EXPE = 1)

AMS	0					1
SAE1	0		1			—
DMACS	—		0		1	—
P75DDR	0	1	0	1	—	—
Pin function	P75 input pin	P75 output pin	P75 input pin	P75 output pin	$\overline{\text{DACK1}}$ output pin	$\overline{\text{EDACK1}}$ output pin

Mode 7 (EXPE = 0)

AMS	—				
SAE1	0		1		
DMACS	—		0		1
P75DDR	0	1	0	1	—
Pin function	P75 input pin	P75 output pin	P75 input pin	P75 output pin	$\overline{\text{DACK1}}$ output pin

Pin	Selection Method and Pin Functions
P74/$\overline{\text{DACK0}}$/ $\overline{\text{EDACK0}}$	The pin function is switched as shown below according to the combination of bit DMACS in PFCR2, bit SAE0 in DMABCRH, bit AMS in EDMDR0, and bit P74DDR.

Modes 1, 2, 4, 5, 6, 7 (EXPE = 1)

AMS	0					1
SAE0	0		1			—
DMACS	—		0		1	—
P74DDR	0	1	0	1	—	—
Pin function	P74 input pin	P74 output pin	P74 input pin	P74 output pin	$\overline{\text{DACK0}}$ output pin	$\overline{\text{EDACK0}}$ output pin

Mode 7 (EXPE = 0)

AMS	—				
SAE0	0		1		
DMACS	—		0		1
P74DDR	0	1	0	1	—
Pin function	P74 input pin	P74 output pin	P74 input pin	P74 output pin	$\overline{\text{DACK0}}$ output pin

Pin	Selection Method and Pin Functions
P73/$\overline{\text{TEND1}}$/ $\overline{\text{ETEND1}}$	The pin function is switched as shown below according to the combination of bit DMACS in PFCR2, bit TEE1 in DMATCR of the DMAC, bit ETENDE in EDMDR1 of the EXDMAC, and bit P73DDR.

Modes 1, 2, 4, 5, 6, 7 (EXPE = 1)

ETENDE	0					1
TEE1	0		1			—
DMACS	—		0		1	—
P73DDR	0	1	0	1	—	—
Pin function	P73 input pin	P73 output pin	P73 input pin	P73 output pin	$\overline{\text{TEND1}}$ output pin	$\overline{\text{ETEND1}}$ output pin

Mode 7 (EXPE = 0)

ETENDE	—				
TEE1	0		1		
DMACS	—		0		1
P73DDR	0	1	0	1	—
Pin function	P73 input pin	P73 output pin	P73 input pin	P73 output pin	$\overline{\text{TEND1}}$ output pin

Pin	Selection Method and Pin Functions

P72/$\overline{\text{TEND0}}$/$\overline{\text{ETEND0}}$

The pin function is switched as shown below according to the combination of bit DMACS in PFCR2, bit TEE0 in DMATCR of the DMAC, bit ETENDE in EDMDR0 of the EXDMAC, and bit P72DDR.

Modes 1, 2, 4, 5, 6, 7 (EXPE = 1)

ETENDE	0					1
TEE0	0		1			—
DMACS	—		0		1	—
P72DDR	0	1	0	1	—	—
Pin function	P72 input pin	P72 output pin	P72 input pin	P72 output pin	$\overline{\text{TEND0}}$ output pin	$\overline{\text{ETEND0}}$ output pin

Mode 7 (EXPE = 0)

ETENDE	—				
TEE0	0		1		
DMACS	—		0		1
P72DDR	0	1	0	1	—
Pin function	P72 input pin	P72 output pin	P72 input pin	P72 output pin	$\overline{\text{TEND0}}$ output pin

P71/$\overline{\text{DREQ1}}$/$\overline{\text{EDREQ1}}$

The pin function is switched as shown below according to bit P71DDR.

P71DDR	0	1
Pin function	P71 input pin	P71 output pin
	$\overline{\text{DREQ1}}$ input*	
	$\overline{\text{EDREQ1}}$ input	

Note: * $\overline{\text{DREQ1}}$ input when DMACS = 1.

P70/$\overline{\text{DREQ0}}$/$\overline{\text{EDREQ0}}$

The pin function is switched as shown below according to bit P70DDR.

P70DDR	0	1
Pin function	P70 input pin	P70 output pin
	$\overline{\text{DREQ0}}$ input*	
	$\overline{\text{EDREQ0}}$ input	

Note: * $\overline{\text{DREQ0}}$ input when DMACS = 1.

5.9 Port 8

5.9.1 Overview

Port 8 is a 6-bit I/O port. Port 8 pins also function as interrupt input pins ($\overline{IRQ0}$ to $\overline{IRQ5}$) and EXDMAC input/output pins ($\overline{EDREQ2}$, $\overline{ETEND2}$, $\overline{EDACK2}$, $\overline{EDREQ3}$, $\overline{ETEND3}$, and $\overline{EDACK3}$). The functions of pins P85 to P80 change according to the operating mode.

The interrupt input pins ($\overline{IRQ0}$ to $\overline{IRQ5}$) can be switched by making a setting in ITSR.

When pins P85 to P80 are used for IRQ input, they are Schmitt-trigger inputs.

Figure 5.8 shows the port 8 pin configuration.

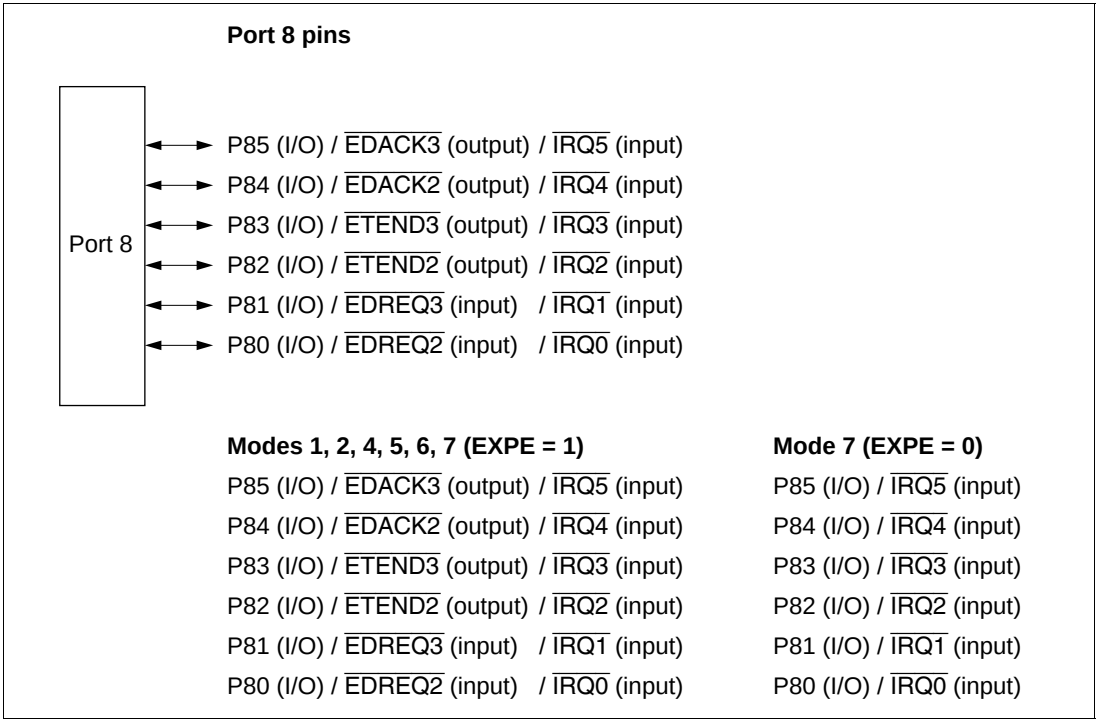


Figure 5.8 Port 8 Pin Functions

5.9.2 Register Configuration

Table 5.15 shows the port 8 register configuration.

Table 5.15 Port 8 Registers

Name	Abbreviation	R/W	Initial Value	Address*[1]
Port 8 data direction register	P8DDR	W	H'00*[2]	H'FE27
Port 8 data register	P8DR	R/W	H'00*[2]	H'FF67
Port 8 register	PORT8	R	Undefined	H'FF57

Notes: 1. Lower 16 bits of the address.
2. Value of bits 5 to 0.

Port 8 Data Direction Register (P8DDR)

Bit	7	6	5	4	3	2	1	0
	—	—	P85DDR	P84DDR	P83DDR	P82DDR	P81DDR	P80DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	W	W	W	W	W	W

P8DDR is a 6-bit write-only register, the individual bits of which specify input or output for the pins of port 8. P8DDR cannot be read; if it is, an undefined value will be read. Bits 7 and 6 are reserved.

Setting a P8DDR bit to 1 makes the corresponding port 8 pin an output pin, while clearing the bit to 0 makes the pin an input pin.

P8DDR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Port 8 Data Register (P8DR)

Bit	7	6	5	4	3	2	1	0
	—	—	P85DR	P84DR	P83DR	P82DR	P81DR	P80DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

P8DR is a 6-bit readable/writable register that stores output data for the port 8 pins (P85 to P80).

Bits 7 and 6 are reserved; they are always read as 0 and cannot be modified.

P8DR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Port 8 Register (PORT8)

Bit	7	6	5	4	3	2	1	0
	—	—	P85	P84	P83	P82	P81	P80
Initial value	Undefined	Undefined	—*	—*	—*	—*	—*	—*
Read/Write	—	—	R	R	R	R	R	R

Note: * Determined by the state of pins P85 to P80.

PORT8 is a 6-bit read-only register that shows the pin states. PORT8 cannot be written to; writing of output data for the port 8 pins (P85 to P80) must always be performed on P8DR.

Bits 7 and 6 are reserved; if read they will return an undefined value.

If a port 8 read is performed while P8DDR bits are set to 1, the P8DR values are read. If a port 8 read is performed while P8DDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORT8 contents are determined by the pin states, as P8DDR and P8DR are initialized. PORT8 retains its prior state in software standby mode.

5.9.3 Pin Functions

Port 8 pins also function as interrupt input pins ($\overline{\text{IRQ0}}$ to $\overline{\text{IRQ5}}$) and EXDMAC input/output pins ($\overline{\text{EDREQ2}}$, $\overline{\text{ETEND2}}$, $\overline{\text{EDACK2}}$, $\overline{\text{EDREQ3}}$, $\overline{\text{ETEND3}}$, and $\overline{\text{EDACK3}}$). Port 8 pin functions are shown in table 5.16.

Table 5.16 Port 8 Pin Functions

Pin	Selection Method and Pin Functions
P85/$\overline{\text{IRQ5}}$/ $\overline{\text{EDACK3}}$	The pin function is switched as shown below according to the combination of bit AMS in EDMDR3 of the EXDMAC, bit P85DDR, and bit ITS5 in ITSR.

Modes 1, 2, 4, 5, 6, 7 (EXPE = 1)

AMS	0		1
P85DDR	0	1	—
Pin function	P85 input pin	P85 output pin	$\overline{\text{EDACK3}}$ output
	$\overline{\text{IRQ5}}$ interrupt input*		

Mode 7 (EXPE = 0)

AMS	—	
P85DDR	0	1
Pin function	P85 input pin	P85 output pin
	$\overline{\text{IRQ5}}$ interrupt input*	

Note: * $\overline{\text{IRQ5}}$ input when ITS5 = 1.

P84/$\overline{\text{IRQ4}}$/ $\overline{\text{EDACK2}}$	The pin function is switched as shown below according to the combination of bit AMS in EDMDR2 of the EXDMAC, bit P84DDR, and bit ITS4 in ITSR.

Modes 1, 2, 4, 5, 6, 7 (EXPE = 1)

AMS	0		1
P84DDR	0	1	—
Pin function	P84 input pin	P84 input/output	$\overline{\text{EDACK2}}$ output
	$\overline{\text{IRQ4}}$ interrupt input*		

Mode 7 (EXPE = 0)

AMS	—	
P84DDR	0	1
Pin function	P84 input pin	P84 output pin
	$\overline{\text{IRQ4}}$ interrupt input*	

Note: * $\overline{\text{IRQ4}}$ input when ITS4 = 1.

Pin	Selection Method and Pin Functions
P83/$\overline{\text{IRQ3}}$/ $\overline{\text{ETEND3}}$	The pin function is switched as shown below according to the combination of bit ETENDE in EDMDR3 of the EXDMAC, bit P83DDR, and bit ITS3 in ITSR.

Modes 1, 2, 4, 5, 6, 7 (EXPE = 1)

ETENDE	0		1
P83DDR	0	1	—
Pin function	P83 input pin	P83 output pin	$\overline{\text{ETEND3}}$ output
	$\overline{\text{IRQ3}}$ interrupt input*		

Mode 7 (EXPE = 0)

ETENDE	—	
P83DDR	0	1
Pin function	P83 input pin	P83 output pin
	$\overline{\text{IRQ3}}$ interrupt input*	

Note: * $\overline{\text{IRQ3}}$ input when ITS3 = 1.

P82/$\overline{\text{IRQ2}}$/ $\overline{\text{ETEND2}}$	The pin function is switched as shown below according to the combination of bit ETENDE in EDMDR2 of the EXDMAC, bit P82DDR, and bit ITS2 in ITSR.

Modes 1, 2, 4, 5, 6, 7 (EXPE = 1)

ETENDE	0		1
P82DDR	0	1	—
Pin function	P82 input pin	P82 output pin	$\overline{\text{ETEND2}}$ output
	$\overline{\text{IRQ2}}$ interrupt input*		

Mode 7 (EXPE = 0)

ETENDE	—	
P82DDR	0	1
Pin function	P82 input pin	P82 output pin
	$\overline{\text{IRQ2}}$ interrupt input*	

Note: * $\overline{\text{IRQ2}}$ input when ITS2 = 1.

Pin	Selection Method and Pin Functions
P81/$\overline{\text{IRQ1}}$/ $\overline{\text{EDREQ3}}$	The pin function is switched as shown below according to the combination of bit P81DDR and bit ITS1 in ITSR.

P81DDR	0	1
Pin function	P81 input pin	P81 output pin
	$\overline{\text{EDREQ3}}$ input pin	
	$\overline{\text{IRQ1}}$ interrupt input*	

Note: * $\overline{\text{IRQ1}}$ input when ITS1 = 1.

P80/$\overline{\text{IRQ0}}$/ $\overline{\text{EDREQ2}}$	The pin function is switched as shown below according to the combination of bit P80DDR and bit ITS0 in ITSR.

P80DDR	0	1
Pin function	P80 input pin	P80 output pin
	$\overline{\text{EDREQ2}}$ input pin	
	$\overline{\text{IRQ0}}$ interrupt input*	

Note: * $\overline{\text{IRQ0}}$ input when ITS0 = 1.

5.10 Port A

5.10.1 Overview

Port A is an 8-bit I/O port. Port A pins also function as address bus outputs. The pin functions change according to the operating mode. Address output or port output can be selected with bits A23E to A16E in PFCR1.

Port A has a built-in MOS input pull-up function that can be controlled by software.

Figure 5.9 shows the port A pin configuration.

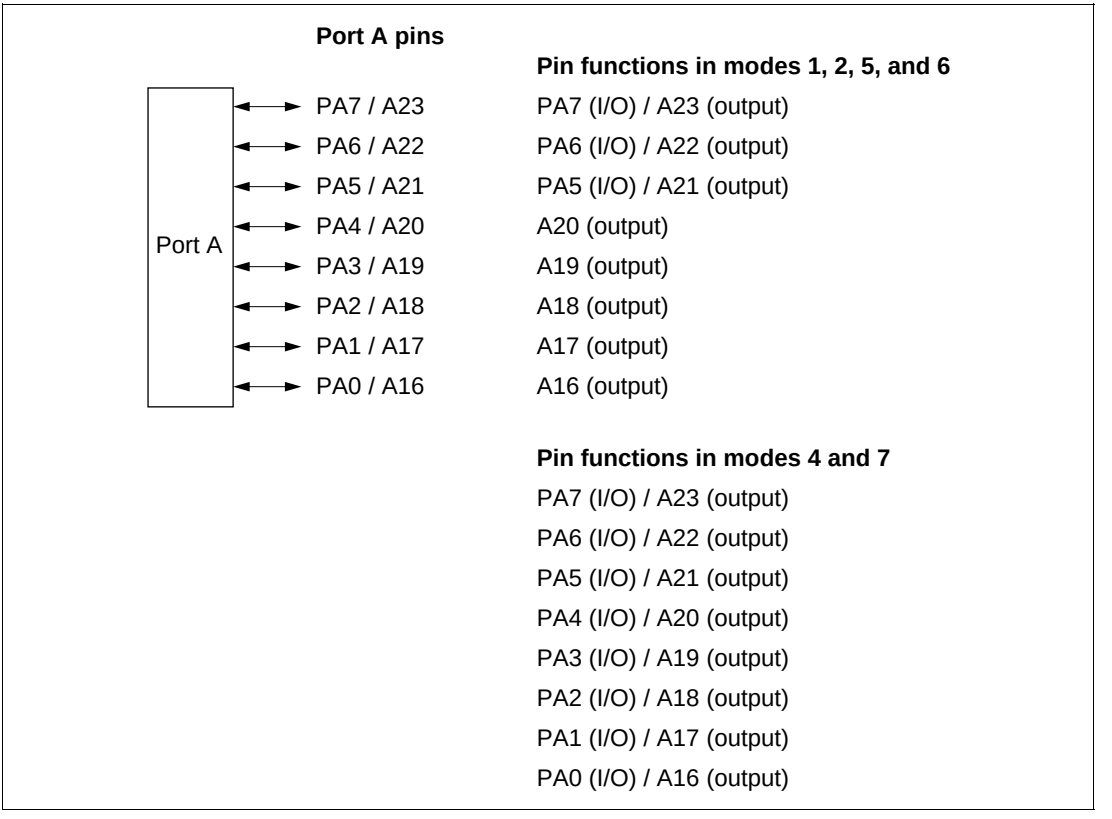


Figure 5.9 Port A Pin Functions

5.10.2 Register Configuration

Table 5.17 shows the port A register configuration.

Table 5.17 Port A Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port A data direction register	PADDR	W	H'00	H'FE29
Port A data register	PADR	R/W	H'00	H'FF69
Port A register	PORTA	R	Undefined	H'FF59
Port A MOS pull-up control register	PAPCR	R/W	H'00	H'FE36
Port A open-drain control register	PAODR	R/W	H'00	H'FE3D
Port function control register 1	PFCR1	R/W	H'FF	H'FE33

Note: * Lower 16 bits of the address.

Port A Data Direction Register (PADDR)

Bit	7	6	5	4	3	2	1	0
	PA7DDR	PA6DDR	PA5DDR	PA4DDR	PA3DDR	PA2DDR	PA1DDR	PA0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

PADDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port A. PADDR cannot be read; if it is, an undefined value will be read.

PADDR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode. The OPE bit in SBYCR is used to select whether the address output pins retain their output state or become high-impedance when a transition is made to software standby mode.

- Modes 1, 2, 5, and 6

  Pins PA4 to PA0 are address outputs regardless of the PADDR settings.

  For pins PA7 to PA5, when the corresponding bit of A23E to A21E is set to 1, setting a PADDR bit to 1 makes the corresponding port A pin an address output, while clearing the bit to 0 makes the pin an input port. Clearing one of bits A23E to A21E to 0 makes the corresponding port A pin an I/O port, and its function can be switched with PADDR.

- Mode 4

  When the corresponding bit of A23E to A16E is set to 1, setting a PADDR bit to 1 makes the corresponding port A pin an address output, while clearing the bit to 0 makes the pin an input port. Clearing one of bits A23E to A16 to 0 makes the corresponding port A pin an I/O port, and its function can be switched with PADDR.

- Mode 7 (when bit EXPE is set to 1 in SYSCR)

  When the corresponding bit of A23E to A16E is set to 1, setting a PADDR bit to 1 makes the corresponding port A pin an address output, while clearing the bit to 0 makes the pin an input port. Clearing one of bits A23E to A16E to 0 makes the corresponding port A pin an I/O port; setting the corresponding PADDR bit to 1 makes the pin an output port, while clearing the bit to 0 makes the pin an input port.

- Mode 7 (when bit EXPE is cleared to 0 in SYSCR)

  Port A is an I/O port, and its pin functions can be switched with PADDR.

Port A Data Register (PADR)

Bit	7	6	5	4	3	2	1	0
	PA7DR	PA6DR	PA5DR	PA4DR	PA3DR	PA2DR	PA1DR	PA0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PADR is an 8-bit readable/writable register that stores output data for the port A pins (PA7 to PA0).

PADR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Port A Register (PORTA)

Bit	7	6	5	4	3	2	1	0
	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

Note: * Determined by the state of pins PA7 to PA0.

PORTA is an 8-bit read-only register that shows the pin states. PORTA cannot be written to; writing of output data for the port A pins (PA7 to PA0) must always be performed on PADR.

If a port A read is performed while PADDR bits are set to 1, the PADR values are read. If a port A read is performed while PADDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORTA contents are determined by the pin states, as PADDR and PADR are initialized. PORTA retains its prior state in software standby mode.

Port A MOS Pull-Up Control Register (PAPCR)

Bit	7	6	5	4	3	2	1	0
	PA7PCR	PA6PCR	PA5PCR	PA4PCR	PA3PCR	PA2PCR	PA1PCR	PA0PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PAPCR is an 8-bit readable/writable register that controls the MOS input pull-up function incorporated into port A on a bit-by-bit basis.

All the bits are valid in modes 4 and 7, and bits 7 to 5 are valid in modes 1, 2, 5, and 6. When a PADDR bit is cleared to 0 (input port setting), setting the corresponding PAPCR bit to 1 turns on the MOS input pull-up for the corresponding pin.

PAPCR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Port A Open Drain Control Register (PAODR)

Bit	7	6	5	4	3	2	1	0
	PA7ODR	PA6ODR	PA5ODR	PA4ODR	PA3ODR	PA2ODR	PA1ODR	PA0ODR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PAODR is an 8-bit readable/writable register that controls whether PMOS is on or off for each port A pin (PA7 to PA0).

Setting a PAODR bit to 1 makes the corresponding port A pin an NMOS open-drain output, while clearing the bit to 0 makes the pin a CMOS output.

PAODR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Port Function Control Register 1 (PFCR1)

Bit	7	6	5	4	3	2	1	0
	A23E	A22E	A21E	A20E	A19E	A18E	A17E	A16E
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PFCR1 is an 8-bit readable/writable register that performs I/O port control. All the bits are valid in modes 4 and 7, and bits 7 to 5 are valid in modes 1, 2, 5, and 6. PFCR1 is initialized to H'FF by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Bit 7—Address 23 Enable (A23E): Enables or disables output for address output 23 (A23).

Bit 7 A23E	Description	
0	DR output when PA7DDR = 1	
1	A23 output when PA7DDR = 1	(Initial value)

Bit 6—Address 22 Enable (A22E): Enables or disables output for address output 22 (A22).

Bit 6 A22E	Description	
0	DR output when PA6DDR = 1	
1	A22 output when PA6DDR = 1	(Initial value)

Bit 5—Address 21 Enable (A21E): Enables or disables output for address output 21 (A21).

Bit 5 A21E	Description	
0	DR output when PA5DDR = 1	
1	A21 output when PA5DDR = 1	(Initial value)

Bit 4—Address 20 Enable (A20E): Enables or disables output for address output 20 (A20). Valid only in modes 4 and 7.

Bit 4 A20E	Description	
0	DR output when PA4DDR = 1	
1	A20 output when PA4DDR = 1	(Initial value)

Bit 3—Address 19 Enable (A19E): Enables or disables output for address output 19 (A19). Valid only in modes 4 and 7.

Bit 3 A19E	Description	
0	DR output when PA3DDR = 1	
1	A19 output when PA3DDR = 1	(Initial value)

Bit 2—Address 18 Enable (A18E): Enables or disables output for address output 18 (A18). Valid only in modes 4 and 7.

Bit 2 A18E	Description	
0	DR output when PA2DDR = 1	
1	A18 output when PA2DDR = 1	(Initial value)

Bit 1—Address 17 Enable (A17E): Enables or disables output for address output 17 (A17). Valid only in modes 4 and 7.

Bit 1 A17E	Description	
0	DR output when PA1DDR = 1	
1	A17 output when PA1DDR = 1	(Initial value)

Bit 0—Address 16 Enable (A16E): Enables or disables output for address output 16 (A16). Valid only in modes 4 and 7.

Bit 0 A16E	Description	
0	DR output when PA0DDR = 1	
1	A16 output when PA0DDR = 1	(Initial value)

5.10.3 Pin Functions

Port A pins also function as address outputs. Port A pin functions are shown in table 5.18.

Table 5.18 Port A Pin Functions

Pin — **Selection Method and Pin Functions**

PA7/A23
PA6/A22
PA5/A21

The pin function is switched as shown below according to the operating mode, bit EXPE, bits A23E to A21E, and bit PADDR.

Operating mode	1, 2, 4, 5, 6				7					
EXPE	—				0		1			
AxxE	0		1		—		0		1	
PADDR	0	1	0	1	0	1	0	1	0	1
Pin function	PA input pin	PA output pin	PA input pin	Address output pin	PA input pin	PA output pin	PA input pin	PA output pin	PA input pin	Address output pin

PA4/A20
PA3/A19
PA2/A18
PA1/A17
PA0/A16

The pin function is switched as shown below according to the operating mode, bit EXPE, bits A20E to A16E, and bit PADDR.

Operating mode	1, 2, 5, 6	4				7					
EXPE	—	—				0		1			
AxxE	—	0		1		—		0		1	
PADDR	—	0	1	0	1	0	1	0	1	0	1
Pin function	Address output pin	PA input pin	PA output pin	PA input pin	Address output pin	PA input pin	PA output pin	PA input pin	PA output pin	PA input pin	Address output pin

5.10.4 MOS Input Pull-Up Function

Port A has a built-in MOS input pull-up function that can be controlled by software. This MOS input pull-up function can be used by pins PA7 to PA5 in modes 1, 2, 5, and 6, and by all pins in modes 4 and 7. MOS input pull-up can be specified as on or off on a bit-by-bit basis.

When a PADDR bit is cleared to 0, setting the corresponding PAPCR bit to 1 turns on the MOS input pull-up for that pin.

The MOS input pull-up function is in the off state after a reset and in hardware standby mode. The prior state is retained in software standby mode.

Table 5.19 summarizes the MOS input pull-up states.

Table 5.19 MOS Input Pull-Up States (Port A)

Mode		Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
4, 7	PA7 to PA0	Off	Off	On/Off	On/Off
1, 2, 5, 6	PA7 to PA5			On/Off	On/Off
	PA4 to PA0			Off	Off

Legend:
Off: MOS input pull-up is always off.
On/Off: On when PADDR = 0 and PAPCR = 1; otherwise off.

5.11 Port B

5.11.1 Overview

Port B is an 8-bit I/O port. Port B pins also function as address bus outputs. The pin functions change according to the operating mode.

Port B has a built-in MOS input pull-up function that can be controlled by software.

Figure 5.10 shows the port B pin configuration.

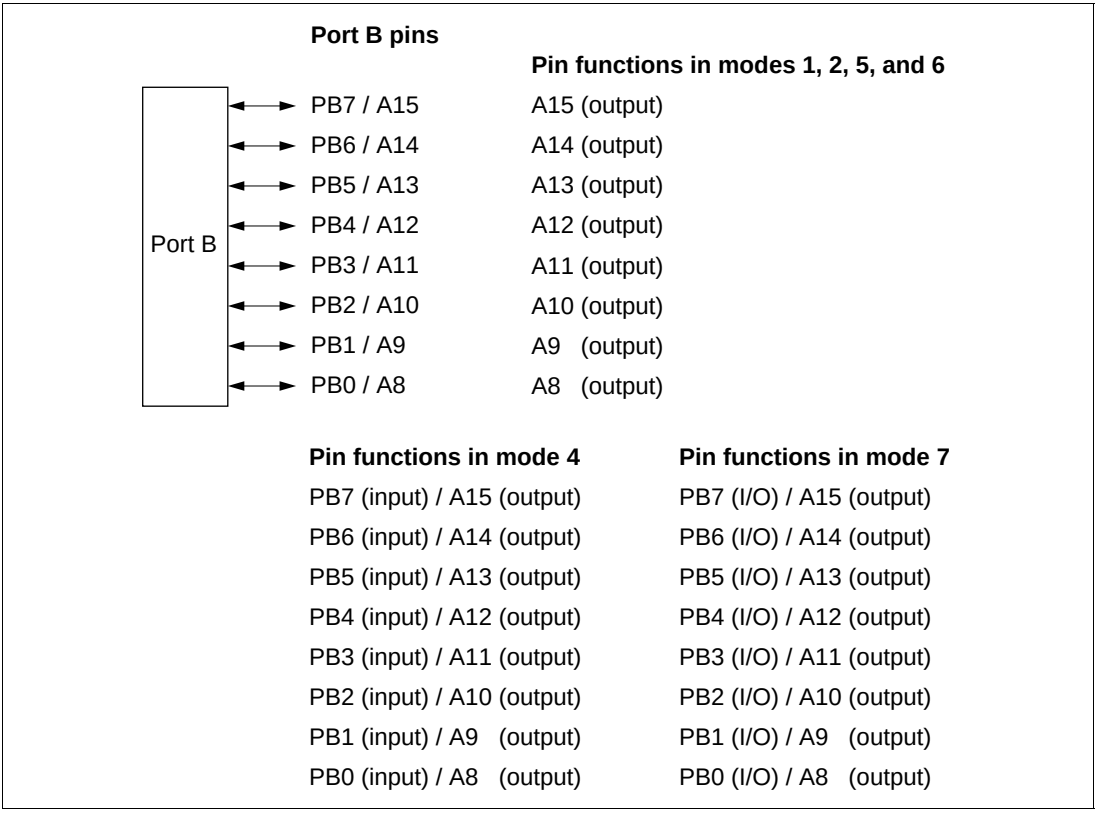


Figure 5.10 Port B Pin Functions

5.11.2 Register Configuration

Table 5.20 shows the port B register configuration.

Table 5.20 Port B Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port B data direction register	PBDDR	W	H'00	H'FE2A
Port B data register	PBDR	R/W	H'00	H'FF6A
Port B register	PORTB	R	Undefined	H'FF5A
Port B MOS pull-up control register	PBPCR	R/W	H'00	H'FE37

Note: * Lower 16 bits of the address.

Port B Data Direction Register (PBDDR)

Bit	7	6	5	4	3	2	1	0
	PB7DDR	PB6DDR	PB5DDR	PB4DDR	PB3DDR	PB2DDR	PB1DDR	PB0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

PBDDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port B. PBDDR cannot be read; if it is, an undefined value will be read.

PBDDR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode. The OPE bit in SBYCR is used to select whether the address output pins retain their output state or become high-impedance when a transition is made to software standby mode.

- Modes 1, 2, 5, and 6
  Port B pins are address outputs regardless of the PBDDR settings.
- Mode 4
  Setting a PBDDR bit to 1 makes the corresponding port B pin an address output, while clearing the bit to 0 makes the pin an input port.
- Mode 7 (when bit EXPE is set to 1 in SYSCR)
  Setting a PBDDR bit to 1 makes the corresponding port B pin an address output, while clearing the bit to 0 makes the pin an input port.
- Mode 7 (when bit EXPE is cleared to 0 in SYSCR)
  Port B is an I/O port, and its pin functions can be switched with PBDDR.

Port B Data Register (PBDR)

Bit	7	6	5	4	3	2	1	0
	PB7DR	PB6DR	PB5DR	PB4DR	PB3DR	PB2DR	PB1DR	PB0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PBDR is an 8-bit readable/writable register that stores output data for the port B pins (PB7 to PB0).

PBDR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Port B Register (PORTB)

Bit	7	6	5	4	3	2	1	0
	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

Note: * Determined by the state of pins PB7 to PB0.

PORTB is an 8-bit read-only register that shows the pin states. PORTB cannot be written to; writing of output data for the port B pins (PB7 to PB0) must always be performed on PBDR.

If a port B read is performed while PBDDR bits are set to 1, the PBDR values are read. If a port B read is performed while PBDDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORTB contents are determined by the pin states, as PBDDR and PBDR are initialized. PORTB retains its prior state in software standby mode.

Port B MOS Pull-Up Control Register (PBPCR)

Bit	7	6	5	4	3	2	1	0
	PB7PCR	PB6PCR	PB5PCR	PB4PCR	PB3PCR	PB2PCR	PB1PCR	PB0PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PBPCR is an 8-bit readable/writable register that controls the MOS input pull-up function incorporated into port B on a bit-by-bit basis.

In modes 4 and 7, when a PBDDR bit is cleared to 0 (input port setting), setting the corresponding PBPCR bit to 1 turns on the MOS input pull-up for the corresponding pin.

PBPCR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

5.11.3 Pin Functions

Port B pins also function as address outputs. Port B pin functions are shown in table 5.21.

Table 5.21 Port B Pin Functions

Pin	Selection Method and Pin Functions
PB7/A15 PB6/A14 PB5/A13 PB4/A12 PB3/A11 PB2/A10 PB1/A9 PB0/A8	The pin function is switched as shown below according to the operating mode, bit EXPE, and bit PBDDR.

Operating mode	1, 2, 5, 6	4		7			
EXPE	—	—		0		1	
PBDDR	—	0	1	0	1	0	1
Pin function	Address output pin	PB input pin	Address output pin	PB input pin	PB output pin	PB input pin	Address output pin

5.11.4 MOS Input Pull-Up Function

Port B has a built-in MOS input pull-up function that can be controlled by software. This MOS input pull-up function can be used in modes 4 and 7. MOS input pull-up can be specified as on or off on a bit-by-bit basis.

In modes 4 and 7, when a PBDDR bit is cleared to 0, setting the corresponding PBPCR bit to 1 turns on the MOS input pull-up for that pin.

The MOS input pull-up function is in the off state after a reset and in hardware standby mode. The prior state is retained in software standby mode.

Table 5.22 summarizes the MOS input pull-up states.

Table 5.22 MOS Input Pull-Up States (Port B)

Mode	Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
1, 2, 5, 6	Off	Off	Off	Off
4, 7			On/Off	On/Off

Legend:
Off: MOS input pull-up is always off.
On/Off: On when PBDDR = 0 and PBPCR = 1; otherwise off.

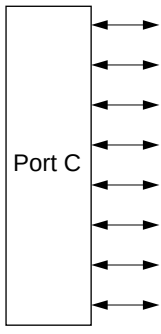
5.12 Port C

5.12.1 Overview

Port C is an 8-bit I/O port. Port C pins also function as address bus outputs. The pin functions change according to the operating mode.

Port C has a built-in MOS input pull-up function that can be controlled by software.

Figure 5.11 shows the port C pin configuration.



Port C pins	Pin functions in modes 1, 2, 5, and 6
PC7 / A7	A7 (output)
PC6 / A6	A6 (output)
PC5 / A5	A5 (output)
PC4 / A4	A4 (output)
PC3 / A3	A3 (output)
PC2 / A2	A2 (output)
PC1 / A1	A1 (output)
PC0 / A0	A0 (output)

Pin functions in mode 4	Pin functions in mode 7
PC7 (input) / A7 (output)	PC7 (I/O) / A7 (output)
PC6 (input) / A6 (output)	PC6 (I/O) / A6 (output)
PC5 (input) / A5 (output)	PC5 (I/O) / A5 (output)
PC4 (input) / A4 (output)	PC4 (I/O) / A4 (output)
PC3 (input) / A3 (output)	PC3 (I/O) / A3 (output)
PC2 (input) / A2 (output)	PC2 (I/O) / A2 (output)
PC1 (input) / A1 (output)	PC1 (I/O) / A1 (output)
PC0 (input) / A0 (output)	PC0 (I/O) / A0 (output)

Figure 5.11 Port C Pin Functions

5.12.2 Register Configuration

Table 5.23 shows the port C register configuration.

Table 5.23 Port C Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port C data direction register	PCDDR	W	H'00	H'FE2B
Port C data register	PCDR	R/W	H'00	H'FF6B
Port C register	PORTC	R	Undefined	H'FF5B
Port C MOS pull-up control register	PCPCR	R/W	H'00	H'FE38

Note: * Lower 16 bits of the address.

Port C Data Direction Register (PCDDR)

Bit	7	6	5	4	3	2	1	0
	PC7DDR	PC6DDR	PC5DDR	PC4DDR	PC3DDR	PC2DDR	PC1DDR	PC0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

PCDDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port C. PCDDR cannot be read; if it is, an undefined value will be read.

PCDDR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode. The OPE bit in SBYCR is used to select whether the address output pins retain their output state or become high-impedance when a transition is made to software standby mode.

- Modes 1, 2, 5, and 6
  Port C pins are address outputs regardless of the PCDDR settings.
- Mode 4
  Setting a PCDDR bit to 1 makes the corresponding port C pin an address output, while clearing the bit to 0 makes the pin an input port.
- Mode 7 (when bit EXPE is set to 1 in SYSCR)
  Setting a PCDDR bit to 1 makes the corresponding port C pin an address output, while clearing the bit to 0 makes the pin an input port.
- Mode 7 (when bit EXPE is cleared to 0 in SYSCR)
  Port C is an I/O port, and its pin functions can be switched with PCDDR.

Port C Data Register (PCDR)

Bit	7	6	5	4	3	2	1	0
	PC7DR	PC6DR	PC5DR	PC4DR	PC3DR	PC2DR	PC1DR	PC0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PCDR is an 8-bit readable/writable register that stores output data for the port C pins (PC7 to PC0).

PCDR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Port C Register (PORTC)

Bit	7	6	5	4	3	2	1	0
	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

Note: * Determined by the state of pins PC7 to PC0.

PORTC is an 8-bit read-only register that shows the pin states. PORTC cannot be written to; writing of output data for the port C pins (PC7 to PC0) must always be performed on PCDR.

If a port C read is performed while PCDDR bits are set to 1, the PCDR values are read. If a port C read is performed while PCDDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORTC contents are determined by the pin states, as PCDDR and PCDR are initialized. PORTC retains its prior state in software standby mode.

Port C MOS Pull-Up Control Register (PCPCR)

Bit	7	6	5	4	3	2	1	0
	PC7PCR	PC6PCR	PC5PCR	PC4PCR	PC3PCR	PC2PCR	PC1PCR	PC0PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PCPCR is an 8-bit readable/writable register that controls the MOS input pull-up function incorporated into port C on a bit-by-bit basis.

In modes 4 and 7, when a PCDDR bit is cleared to 0 (input port setting), setting the corresponding PCPCR bit to 1 turns on the MOS input pull-up for the corresponding pin.

PCPCR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

5.12.3 Pin Functions

Port C pins also function as address outputs. Port C pin functions are shown in table 5.24.

Table 5.24 Port C Pin Functions

Pin	Selection Method and Pin Functions
PC7/A7 PC6/A6 PC5/A5 PC4/A4 PC3/A3 PC2/A2 PC1/A1 PC0/A0	The pin function is switched as shown below according to the operating mode, bit EXPE, and bit PCDDR.

Operating mode	1, 2, 5, 6	4		7			
EXPE	—	—		0		1	
PCDDR	—	0	1	0	1	0	1
Pin function	Address output pin	PC input pin	Address output pin	PC input pin	PC output pin	PC input pin	Address output pin

5.12.4 MOS Input Pull-Up Function

Port C has a built-in MOS input pull-up function that can be controlled by software. This MOS input pull-up function can be used in modes 4 and 7. MOS input pull-up can be specified as on or off on a bit-by-bit basis.

In modes 4 and 7, when a PCDDR bit is cleared to 0, setting the corresponding PCPCR bit to 1 turns on the MOS input pull-up for that pin.

The MOS input pull-up function is in the off state after a reset and in hardware standby mode. The prior state is retained in software standby mode.

Table 5.25 summarizes the MOS input pull-up states.

Table 5.25 MOS Input Pull-Up States (Port C)

Mode	Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
1, 2, 5, 6	Off	Off	Off	Off
4, 7			On/Off	On/Off

Legend:
Off: MOS input pull-up is always off.
On/Off: On when PCDDR = 0 and PCPCR = 1; otherwise off.

5.13 Port D

5.13.1 Overview

Port D is an 8-bit I/O port. Port D pins also function as data bus input/output pins. The pin functions change according to the operating mode.

Port D has a built-in MOS input pull-up function that can be controlled by software.

Figure 5.12 shows the port D pin configuration.

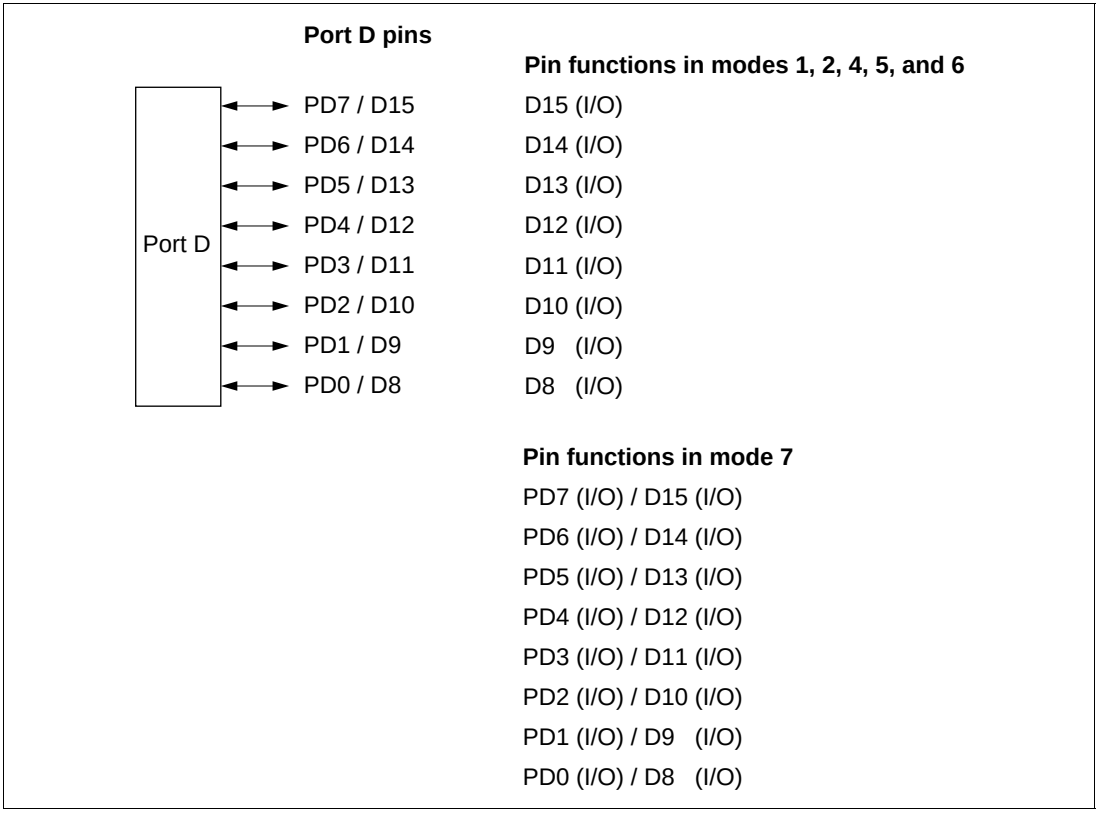


Figure 5.12 Port D Pin Functions

5.13.2 Register Configuration

Table 5.26 shows the port D register configuration.

Table 5.26 Port D Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port D data direction register	PDDDR	W	H'00	H'FE2C
Port D data register	PDDR	R/W	H'00	H'FF6C
Port D register	PORTD	R	Undefined	H'FF5C
Port D MOS pull-up control register	PDPCR	R/W	H'00	H'FE39

Note: * Lower 16 bits of the address.

Port D Data Direction Register (PDDDR)

Bit	7	6	5	4	3	2	1	0
	PD7DDR	PD6DDR	PD5DDR	PD4DDR	PD3DDR	PD2DDR	PD1DDR	PD0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

PDDDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port D. PDDDR cannot be read; if it is, an undefined value will be read.

PDDDR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

- Modes 1, 2, 4, 5, and 6

  The input/output direction specification by PDDDR is ignored, and port D is automatically designated for data input/output.

- Mode 7 (when bit EXPE is set to 1 in SYSCR)

  The input/output direction specification by PDDDR is ignored, and port D is automatically designated for data input/output.

- Mode 7 (when bit EXPE is cleared to 0 in SYSCR)

  Port D is an I/O port, and its pin functions can be switched with PDDDR.

Port D Data Register (PDDR)

Bit	7	6	5	4	3	2	1	0
	PD7DR	PD6DR	PD5DR	PD4DR	PD3DR	PD2DR	PD1DR	PD0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDDR is an 8-bit readable/writable register that stores output data for the port D pins (PD7 to PD0).

PDDR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Port D Register (PORTD)

Bit	7	6	5	4	3	2	1	0
	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

Note: * Determined by the state of pins PD7 to PD0.

PORTD is an 8-bit read-only register that shows the pin states. PORTD cannot be written to; writing of output data for the port D pins (PD7 to PD0) must always be performed on PDDR.

If a port D read is performed while PDDDR bits are set to 1, the PDDR values are read. If a port D read is performed while PDDDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORTD contents are determined by the pin states, as PDDDR and PDDR are initialized. PORTD retains its prior state in software standby mode.

Port D MOS Pull-Up Control Register (PDPCR)

Bit	7	6	5	4	3	2	1	0
	PD7PCR	PD6PCR	PD5PCR	PD4PCR	PD3PCR	PD2PCR	PD1PCR	PD0PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDPCR is an 8-bit readable/writable register that controls the MOS input pull-up function incorporated into port D on a bit-by-bit basis.

In mode 7, when a PDDDR bit is cleared to 0 (input port setting), setting the corresponding PDPCR bit to 1 turns on the MOS input pull-up for the corresponding pin.

PDPCR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

5.13.3 Pin Functions

Port D pins also function as data input/output pins. Port D pin functions are shown in table 5.27.

Table 5.27 Port D Pin Functions

<table>
<tr><th>Pin</th><th>Selection Method and Pin Functions</th></tr>
<tr><td>PD7/D15
PD6/D14
PD5/D13
PD4/D12
PD3/D11
PD2/D10
PD1/D9
PD0/D8</td><td>The pin function is switched as shown below according to the operating mode, bit EXPE, and bit PDDDR.
<table>
<tr><td>Operating mode</td><td>1, 2, 4, 5, 6</td><td colspan="3">7</td></tr>
<tr><td>EXPE</td><td>—</td><td colspan="2">0</td><td>1</td></tr>
<tr><td>PDDDR</td><td>—</td><td>0</td><td>1</td><td>—</td></tr>
<tr><td>Pin function</td><td>Data I/O pin</td><td>PD input pin</td><td>PD output pin</td><td>Data I/O pin</td></tr>
</table></td></tr>
</table>

5.13.4 MOS Input Pull-Up Function

Port D has a built-in MOS input pull-up function that can be controlled by software. This MOS input pull-up function can be used in mode 7. MOS input pull-up can be specified as on or off on a bit-by-bit basis.

In mode 7, when a PDDDR bit is cleared to 0, setting the corresponding PDPCR bit to 1 turns on the MOS input pull-up for that pin.

The MOS input pull-up function is in the off state after a reset and in hardware standby mode. The prior state is retained in software standby mode.

Table 5.28 summarizes the MOS input pull-up states.

Table 5.28 MOS Input Pull-Up States (Port D)

Mode	Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
1, 2, 4, 5, 6	Off	Off	Off	Off
7			On/Off	On/Off

Legend:
OFF: MOS input pull-up is always off.
On/Off: On when PDDDR = 0 and PDPCR = 1; otherwise off.

5.14 Port E

5.14.1 Overview

Port E is an 8-bit I/O port. Port E pins also function as data bus input/output pins. The pin functions change according to the operating mode and the bus mode (8-bit or 16-bit).

Port E has a built-in MOS input pull-up function that can be controlled by software.

Figure 5.13 shows the port E pin configuration.

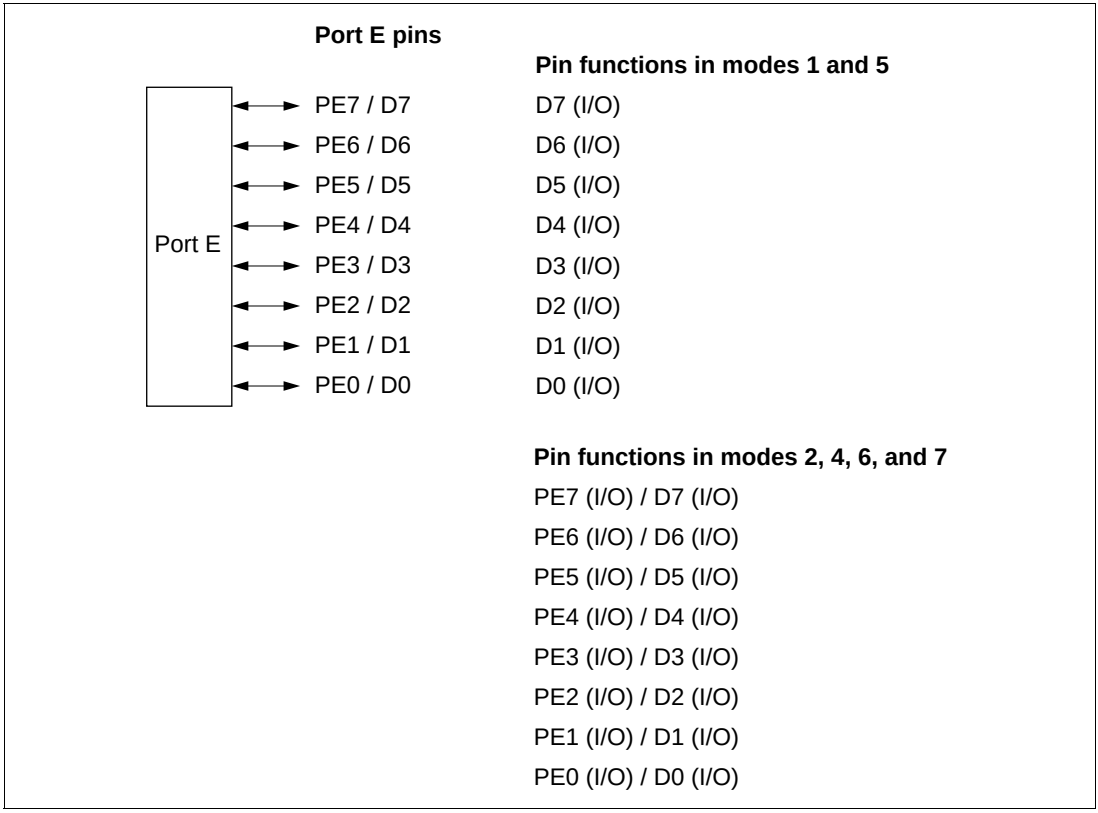


Figure 5.13 Port E Pin Functions

5.14.2 Register Configuration

Table 5.29 shows the port E register configuration.

Table 5.29 Port E Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port E data direction register	PEDDR	W	H'00	H'FE2D
Port E data register	PEDR	R/W	H'00	H'FF6D
Port E register	PORTE	R	Undefined	H'FF5D
Port E MOS pull-up control register	PEPCR	R/W	H'00	H'FE3A

Note: * Lower 16 bits of the address.

Port E Data Direction Register (PEDDR)

Bit	7	6	5	4	3	2	1	0
	PE7DDR	PE6DDR	PE5DDR	PE4DDR	PE3DDR	PE2DDR	PE1DDR	PE0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

PEDDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port E. PEDDR cannot be read; if it is, an undefined value will be read.

PEDDR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

- Modes 1, 2, 4, 5, and 6

  When 8-bit bus mode is selected, port E functions as an I/O port. The pin states can be changed with PEDDR. When 16-bit bus mode is selected, the input/output direction specification by PEDDR is ignored and port E is designated for data input/output.

  For details of 8-bit and 16-bit bus modes, see section 4, Bus Controller.

- Mode 7 (when bit EXPE is set to 1 in SYSCR)

  When 8-bit bus mode is selected, port E functions as an I/O port. Setting a PEDDR bit to 1 makes the corresponding port E pin an output port, while clearing the bit to 0 makes the pin an input port. When 16-bit bus mode is selected, the input/output direction specification by PEDDR is ignored and port E is designated for data input/output.

- Mode 7 (when bit EXPE is cleared to 0 in SYSCR)

  Port E is an I/O port, and its pin functions can be switched with PEDDR.

Port E Data Register (PEDR)

Bit	7	6	5	4	3	2	1	0
	PE7DR	PE6DR	PE5DR	PE4DR	PE3DR	PE2DR	PE1DR	PE0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PEDR is an 8-bit readable/writable register that stores output data for the port E pins (PE7 to PE0).

PEDR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Port E Register (PORTE)

Bit	7	6	5	4	3	2	1	0
	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

Note: * Determined by the state of pins PE7 to PE0.

PORTE is an 8-bit read-only register that shows the pin states. PORTE cannot be written to; writing of output data for the port E pins (PE7 to PE0) must always be performed on PEDR.

If a port E read is performed while PEDDR bits are set to 1, the PEDR values are read. If a port E read is performed while PEDDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORTE contents are determined by the pin states, as PEDDR and PEDR are initialized. PORTE retains its prior state in software standby mode.

Port E MOS Pull-Up Control Register (PEPCR)

Bit	7	6	5	4	3	2	1	0
	PE7PCR	PE6PCR	PE5PCR	PE4PCR	PE3PCR	PE2PCR	PE1PCR	PE0PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PEPCR is an 8-bit readable/writable register that controls the MOS input pull-up function incorporated into port E on a bit-by-bit basis.

In 8-bit bus mode, when a PEDDR bit is cleared to 0 (input port setting), setting the corresponding PEPCR bit to 1 turns on the MOS input pull-up for the corresponding pin.

PEPCR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

5.14.3 Pin Functions

Port E pins also function as data input/output pins. Port E pin functions are shown in table 5.30.

Table 5.30 Port E Pin Functions

Pin	Selection Method and Pin Functions
PE7/D7 PE6/D6 PE5/D5 PE4/D4 PE3/D3 PE2/D2 PE1/D1 PE0/D0	The pin function is switched as shown below according to the operating mode, the bus mode, bit EXPE, and bit PEDDR.

Operating mode	1, 2, 4, 5, 6			7				
Bus mode	All areas 8-bit space		At least one area 16-bit space	—		All areas 8-bit space		At least one area 16-bit space
EXPE	—		—	0		1		1
PEDDR	0	1	—	0	1	0	1	—
Pin function	PE input pin	PE output pin	Data I/O pin	PE input pin	PE output pin	PE input pin	PE output pin	Data I/O pin

5.14.4 MOS Input Pull-Up Function

Port E has a built-in MOS input pull-up function that can be controlled by software. This MOS input pull-up function can be used in 8-bit bus mode. MOS input pull-up can be specified as on or off on a bit-by-bit basis.

In 8-bit bus mode, when a PEDDR bit is cleared to 0, setting the corresponding PEPCR bit to 1 turns on the MOS input pull-up for that pin.

The MOS input pull-up function is in the off state after a reset and in hardware standby mode. The prior state is retained in software standby mode.

Table 5.31 summarizes the MOS input pull-up states.

Table 5.31 MOS Input Pull-Up States (Port E)

Mode		Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
1, 2, 4 to 7	8-bit bus	Off	Off	On/Off	On/Off
	16-bit bus			Off	Off

Legend:
Off: MOS input pull-up is always off.
On/Off: On when PEDDR = 0 and PEPCR = 1; otherwise off.

5.15 Port F

5.15.1 Overview

Port F is an 8-bit I/O port. Port F pins also function as interrupt input pins ($\overline{\text{IRQ14}}$ and $\overline{\text{IRQ15}}$), bus control signal input/output pins ($\overline{\text{AS}}$, $\overline{\text{RD}}$, $\overline{\text{HWR}}$, $\overline{\text{LWR}}$, $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$, and $\overline{\text{WAIT}}$), and the system clock (ø) output pin. The $\overline{\text{AS}}$ and $\overline{\text{LWR}}$ output pins can be switched by making a setting in PFCR2.

Figure 5.14 shows the port F pin configuration.

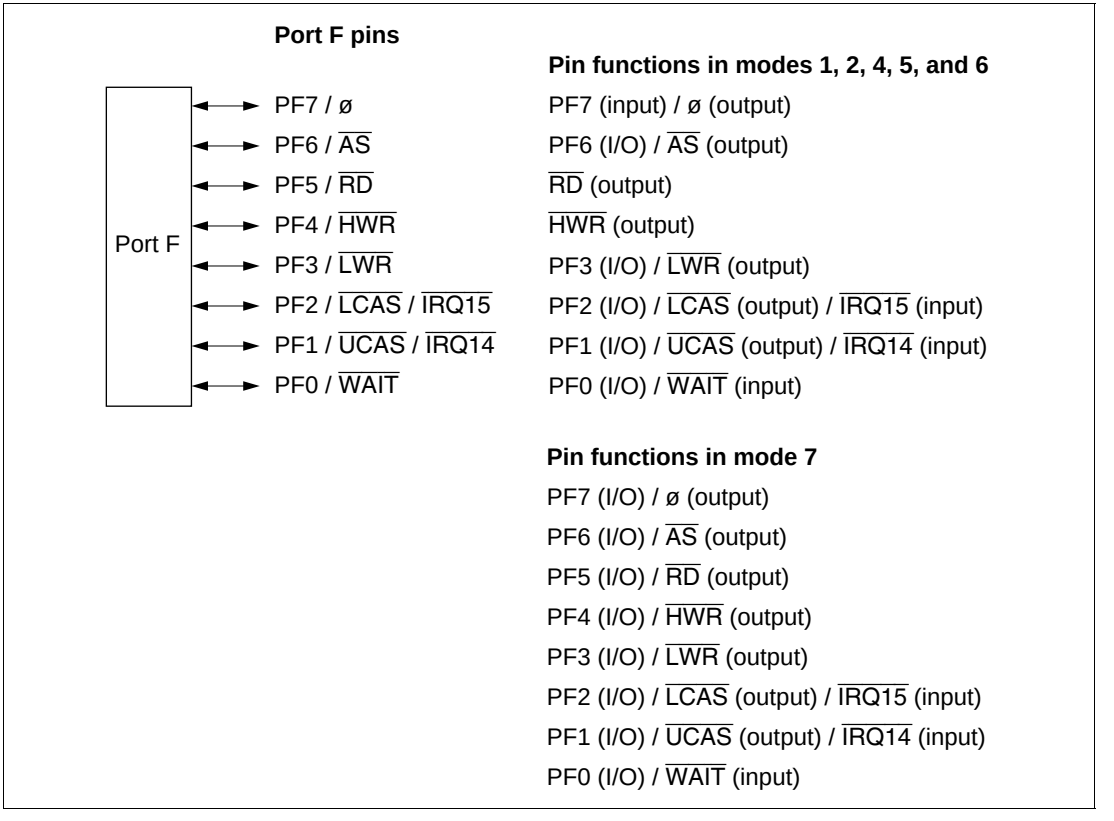


Figure 5.14 Port F Pin Functions

5.15.2 Register Configuration

Table 5.32 shows the port F register configuration.

Table 5.32 Port F Registers

Name	Abbreviation	R/W	Initial Value	Address*[1]
Port F data direction register	PFDDR	W	H'80/H'00*[2]	H'FE2E
Port F data register	PFDR	R/W	H'00	H'FF6E
Port F register	PORTF	R	Undefined	H'FF5E
Port function control register 2	PFCR2	R/W	H'0E	H'FE34

Notes: 1. Lower 16 bits of the address.
2. Initial value depends on the mode.

Port F Data Direction Register (PFDDR)

Bit	7	6	5	4	3	2	1	0
	PF7DDR	PF6DDR	PF5DDR	PF4DDR	PF3DDR	PF2DDR	PF1DDR	PF0DDR
Modes 1, 2, 4, 5, 6								
Initial value	1	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Mode 7								
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

PFDDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port F. PFDDR cannot be read; if it is, an undefined value will be read.

PFDDR is initialized by a reset and in hardware standby mode, to H'80 in modes 1, 2, 4, 5, and 6, and to H'00 in mode 7. It retains its prior state in software standby mode. The OPE bit in SBYCR is used to select whether the bus control output pins retain their output state or become high-impedance when a transition is made to software standby mode.

- Modes 1, 2, 4, 5, and 6

  Pin PF7 functions as the ø output pin when the corresponding PFDDR bit is set to 1, and as an input port when the bit is cleared to 0.

  Pin PF6 functions as the $\overline{AS}$ output pin when ASOE is set to 1. When ASOE is cleared to 0, pin PF6 is an I/O port and its function can be switched with PF6DDR.

  The input/output direction specification in PFDDR is ignored for pins PF5 and PF4, which are automatically designated as bus control outputs ($\overline{RD}$ and $\overline{HWR}$).

Pin PF3 functions as the $\overline{LWR}$ output pin when LWROE is set to 1. When LWROE is cleared to 0, pin PF3 is an I/O port and its function can be switched with PF3DDR.

Pins PF2 to PF0 function as bus control input/output pins ($\overline{LCAS}$, $\overline{UCAS}$, and $\overline{WAIT}$) when the appropriate bus controller settings are made. Otherwise, these pins are output ports when the corresponding PFDDR bit is set to 1, and input ports when the bit is cleared to 0.

- Mode 7 (when bit EXPE is set to 1 in SYSCR)

  Pin PF7 functions as the ø output pin when the corresponding PFDDR bit is set to 1, and as an input port when the bit is cleared to 0.

  Pin PF6 functions as the $\overline{AS}$ output pin when ASOE is set to 1. When ASOE is cleared to 0, pin PF6 is an I/O port and its function can be switched with PF6DDR.

  The input/output direction specification in PFDDR is ignored for pins PF5 and PF4, which are automatically designated as bus control outputs ($\overline{RD}$ and $\overline{HWR}$).

  Pin PF3 functions as the $\overline{LWR}$ output pin when LWROE is set to 1. When LWROE is cleared to 0, pin PF3 is an I/O port and its function can be switched with PF3DDR.

  Pins PF2 to PF0 function as bus control input/output pins ($\overline{LCAS}$, $\overline{UCAS}$, and $\overline{WAIT}$) when the appropriate PFCR2 settings are made. Otherwise, these pins are I/O ports, and their functions can be switched with PFDDR.

- Mode 7 (when bit EXPE is cleared to 0 in SYSCR)

  Pin PF7 functions as the ø output pin when the corresponding PFDDR bit is set to 1, and as an input port when the bit is cleared to 0.

  Pins PF6 to PF0 are I/O ports, and their functions can be switched with PFDDR.

Port F Data Register (PFDR)

Bit	7	6	5	4	3	2	1	0
	PF7DR	PF6DR	PF5DR	PF4DR	PF3DR	PF2DR	PF1DR	PF0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PFDR is an 8-bit readable/writable register that stores output data for the port F pins (PF7 to PF0).

PFDR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Port F Register (PORTF)

Bit	7	6	5	4	3	2	1	0
	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

Note: * Determined by the state of pins PF7 to PF0.

PORTF is an 8-bit read-only register that shows the pin states. PORTF cannot be written to; writing of output data for the port F pins (PF7 to PF0) must always be performed on PFDR.

If a port F read is performed while PFDDR bits are set to 1, the PFDR values are read. If a port F read is performed while PFDDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORTF contents are determined by the pin states, as PFDDR and PFDR are initialized. PORTF retains its prior state in software standby mode.

Port Function Control Register 2 (PFCR2)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	ASOE	LWROE	OES	DMACS
Initial value	0	0	0	0	1	1	1	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

PFCR2 is an 8-bit readable/writable register that performs I/O port control. PFCR2 is initialized to H'0E by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Bits 7 to 4—Reserved: These bits are always read as 0, and should only be written with 0.

Bit 3—AS Output Enable (ASOE): Enables or disables $\overline{AS}$ output.

Bit 3 ASOE	Description
0	PF6 is designated as I/O port and does not function as $\overline{AS}$ output pin
1	PF6 is designated as $\overline{AS}$ output pin (Initial value)

Bit 2—LWR Output Enable (LWROE): Enables or disables $\overline{\text{LWR}}$ output.

Bit 2 LWROE	Description	
0	PF3 is designated as I/O port and does not function as $\overline{\text{LWR}}$ output pin	
1	PF3 is designated as $\overline{\text{LWR}}$ output pin	(Initial value)

Bit 1—OE Output Select (OES): Selects the $\overline{\text{OE}}$ output pin port when the OEE bit is set to 1 in DRAMCR (enabling $\overline{\text{OE}}$ output).

Bit 1 OES	Description	
0	P35 is designated as $\overline{\text{OE}}$ output pin	
1	PH3 is designated as $\overline{\text{OE}}$ output pin	(Initial value)

Bit 0—DMAC Control Pin Select (DMACS): Selects the DMAC control I/O port.

Bit 0 DMACS	Description	
0	P65 to P60 are designated as DMAC control pins	(Initial value)
1	P75 to P70 are designated as DMAC control pins	

5.15.3 Pin Functions

Port F pins also function as interrupt input pins ($\overline{\text{IRQ14}}$ and $\overline{\text{IRQ15}}$), bus control signal input/output pins ($\overline{\text{AS}}$, $\overline{\text{RD}}$, $\overline{\text{HWR}}$, $\overline{\text{LWR}}$, $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$, and $\overline{\text{WAIT}}$), and the system clock (ø) output pin. Port F pin functions are shown in table 5.33.

Table 5.33 Port F Pin Functions

Pin	Selection Method and Pin Functions

PF7/ø — The pin function is switched as shown below according to bit PF7DDR.

Operating mode	1, 2, 4, 5, 6, 7	
PFDDR	0	1
Pin function	PF7 input pin	ø output pin

PF6/$\overline{AS}$ — The pin function is switched as shown below according to the operating mode, bit EXPE, bit PF6DDR, and bit ASOE.

Operating mode	1, 2, 4, 5, 6			7				
EXPE	—			0		1		
ASOE	1	0		—		1	0	
PF6DDR	—	0	1	0	1	—	0	1
Pin function	$\overline{AS}$ output pin	PF6 input pin	PF6 output pin	PF6 input pin	PF6 output pin	$\overline{AS}$ output pin	PF6 input pin	PF6 output pin

PF5/$\overline{RD}$ — The pin function is switched as shown below according to the operating mode, bit EXPE, and bit PF5DDR.

Operating mode	1, 2, 4, 5, 6	7		
EXPE	—	0		1
PF5DDR	—	0	1	—
Pin function	$\overline{RD}$ output pin	PF5 input pin	PF5 output pin	$\overline{RD}$ output pin

PF4/$\overline{HWR}$ — The pin function is switched as shown below according to the operating mode, bit EXPE, and bit PF4DDR.

Operating mode	1, 2, 4, 5, 6	7		
EXPE	—	0		1
PF4DDR	—	0	1	—
Pin function	$\overline{HWR}$ output pin	PF4 input pin	PF4 output pin	$\overline{HWR}$ output pin

Pin	Selection Method and Pin Functions

PF3/$\overline{\text{LWR}}$

The pin function is switched as shown below according to the operating mode, bit EXPE, bit PF3DDR, and bit LWROE.

Operating mode	1, 2, 4, 5, 6			7				
EXPE	—			0		1		
LWROD	1	0		—		1	0	
PF3DDR	—	0	1	0	1	—	0	1
Pin function	$\overline{\text{LWR}}$ output pin	PF3 input pin	PF3 output pin	PF3 input pin	PF3 output pin	$\overline{\text{LWR}}$ output pin	PF3 input pin	PF3 output pin

PF2/$\overline{\text{LCAS}}$/$\overline{\text{IRQ15}}$

The pin function is switched as shown below according to the combination of the operating mode, bit EXPE, bits RMTS2 to RMTS0 in DRAMCR, bits ABW5 to ABW2 in ABWCR, and bit PF2DDR.

Operating mode	1, 2, 4, 5, 6			7				
EXPE	—			0		1		
Areas 2 to 5	Any DRAM space area is 16-bit bus space	All DRAM space areas are 8-bit bus space, or areas 2 to 5 are all normal space		—		Any DRAM space area is 16-bit bus space	All DRAM space areas are 8-bit bus space, or areas 2 to 5 are all normal space	
PF2DDR	—	0	1	0	1	—	0	1
Pin function	$\overline{\text{LCAS}}$ output pin	PF2 input pin	PF2 output pin	PF2 input pin	PF2 output pin	$\overline{\text{LCAS}}$ output pin	PF2 input pin	PF2 output pin
	$\overline{\text{IRQ15}}$ interrupt input pin*							

Note: * $\overline{\text{IRQ15}}$ interrupt input pin when bit ITS15 is cleared to 0 in ITSR.

Pin	Selection Method and Pin Functions

PF1/$\overline{\text{UCAS}}$/$\overline{\text{IRQ14}}$

The pin function is switched as shown below according to the combination of the operating mode, bit EXPE, bits RMTS2 to RMTS0 in DRAMCR, and bit PF1DDR.

Operating mode	1, 2, 4, 5, 6			7				
EXPE	—			0		1		
Areas 2 to 5	Any of areas 2 to 5 is DRAM space	Areas 2 to 5 are all normal space		—		Any of areas 2 to 5 is DRAM space	Areas 2 to 5 are all normal space	
PF1DDR	—	0	1	0	1	—	0	1
Pin function	$\overline{\text{UCAS}}$ output pin	PF1 input pin	PF1 output pin	PF1 input pin	PF1 output pin	$\overline{\text{UCAS}}$ output pin	PF1 input pin	PF1 output pin
	$\overline{\text{IRQ14}}$ interrupt pin*							

Note: * $\overline{\text{IRQ14}}$ interrupt input pin when bit ITS14 is cleared to 0 in ITSR.

PF0/$\overline{\text{WAIT}}$

The pin function is switched as shown below according to the operating mode, bit EXPE, bit WAITE, and bit PF0DDR.

Operating mode	1, 2, 4, 5, 6			7				
EXPE	—			0		1		
WAITE	0		1	—		0		1
PF0DDR	0	1	—	0	1	0	1	—
Pin function	PF0 input pin	PF0 output pin	$\overline{\text{WAIT}}$ input pin	PF0 input pin	PF0 output pin	PF0 input pin	PF0 output pin	$\overline{\text{WAIT}}$ input pin

5.16 Port G

5.16.1 Overview

Port G is a 7-bit I/O port. Port G pins also function as bus control signal output pins ($\overline{\text{BREQ}}$, $\overline{\text{BACK}}$, $\overline{\text{BREQO}}$, and $\overline{\text{CS3}}$ to $\overline{\text{CS0}}$). $\overline{\text{CS3}}$ to $\overline{\text{CS0}}$ output can be enabled or disabled by making a setting in PFCR0.

Figure 5.15 shows the port G pin configuration.

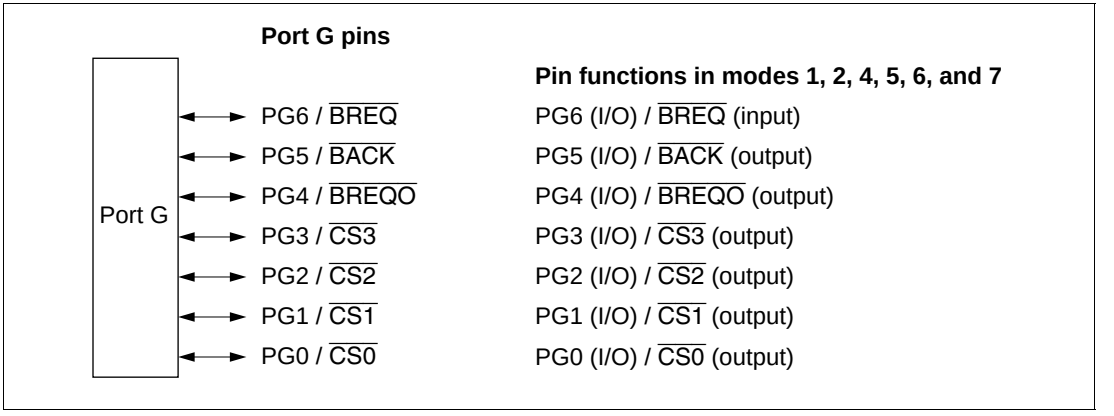


Figure 5.15 Port G Pin Functions

5.16.2 Register Configuration

Table 5.34 shows the port G register configuration.

Table 5.34 Port G Registers

Name	Abbreviation	R/W	Initial Value	Address*[1]
Port G data direction register	PGDDR	W	H'01/H'00*[2]	H'FE2F
Port G data register	PGDR	R/W	H'00	H'FF6F
Port G register	PORTG	R	Undefined	H'FF5F
Port function control register 0	PFCR0	R/W	H'FF	H'FE32

Notes: 1. Lower 16 bits of the address.
2. Initial value depends on the mode.

Port G Data Direction Register (PGDDR)

Bit	7	6	5	4	3	2	1	0
	—	PG6DDR	PG5DDR	PG4DDR	PG3DDR	PG2DDR	PG1DDR	PG0DDR
Modes 1, 2, 5, 6								
Initial value	0	0	0	0	0	0	0	1
Read/Write	—	W	W	W	W	W	W	W
Modes 4 and 7								
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	W	W	W	W	W	W	W

PGDDR is a 7-bit write-only register, the individual bits of which specify input or output for the pins of port G. PGDDR cannot be read. Bit 7 is reserved.

PGDDR is initialized by a reset and in hardware standby mode, to H'01 in modes 1, 2, 5, and 6, and to H'00 in modes 4 and 7. It retains its prior state in software standby mode. The OPE bit in SBYCR is used to select whether the bus control output pins retain their output state or become high-impedance when a transition is made to software standby mode.

- Modes 1, 2, 4, 5, and 6

  When the $\overline{CS}$ output enable bits (CS3E to CS0E) are set to 1, pins PG3 to PG0 function as $\overline{CS}$ output pins when the corresponding PGDDR bit is set to 1, and as input ports when the bit is cleared to 0. When CS3E to CS0E are cleared to 0, pins PG3 to PG0 are I/O ports, and their functions can be switched with PGDDR.

  Pins PG6 to PG4 function as bus control input/output pins ($\overline{BREQO}$, $\overline{BACK}$, and $\overline{BREQ}$) when the appropriate bus controller settings are made. Otherwise, these pins are I/O ports, and their functions can be switched with PGDDR.

- Mode 7 (when bit EXPE is set to 1 in SYSCR)

  When the $\overline{CS}$ output enable bits (CS3E to CS0E) are set to 1, pins PG3 to PG0 function as $\overline{CS}$ output pins when the corresponding PGDDR bit is set to 1, and as input ports when the bit is cleared to 0. When CS3E to CS0E are cleared to 0, pins PG3 to PG0 are I/O ports, and their functions can be switched with PGDDR.

  Pins PG6 to PG4 function as bus control input/output pins ($\overline{BREQO}$, $\overline{BACK}$, and $\overline{BREQ}$) when the appropriate bus controller settings are made. Otherwise, these pins are output ports when the corresponding PGDDR bit is set to 1, and as input ports when the bit is cleared to 0.

- Mode 7 (when bit EXPE is cleared to 0 in SYSCR)

  Pins PG6 to PG0 are I/O ports, and their functions can be switched with PGDDR.

Port G Data Register (PGDR)

Bit	7	6	5	4	3	2	1	0
	—	PG6DR	PG5DR	PG4DR	PG3DR	PG2DR	PG1DR	PG0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PGDR is a 7-bit readable/writable register that stores output data for the port G pins (PG6 to PG0).

Bit 7 is reserved; it is always read as 0, and cannot be modified.

PGDR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Port G Register (PORTG)

Bit	7	6	5	4	3	2	1	0
	—	PG6	PG5	PG4	PG3	PG2	PG1	PG0
Initial value	Undefined	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

Note: * Determined by the state of pins PG6 to PG0.

PORTG is a 7-bit read-only register that shows the pin states. PORTG cannot be written to; writing of output data for the port G pins (PG6 to PG0) must always be performed on PGDR.

Bit 7 is reserved; if read it will return an undefined value.

If a port G read is performed while PGDDR bits are set to 1, the PGDR values are read. If a port G read is performed while PGDDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORTG contents are determined by the pin states, as PGDDR and PGDR are initialized. PORTG retains its prior state in software standby mode.

Port Function Control Register 0 (PFCR0)

Bit	7	6	5	4	3	2	1	0
	CS7E	CS6E	CS5E	CS4E	CS3E	CS2E	CS1E	CS0E
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PFCR0 is an 8-bit readable/writable register that performs I/O port control. PFCR0 is initialized to H'FF by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Bits 7 to 0—CS7 to CS0 Enable (CS7E to CS0E): These bits enable or disable the corresponding $\overline{\text{CSn}}$ output.

Bit n CSnE	Description	
0	Pin is designated as I/O port and does not function as $\overline{\text{CSn}}$ output pin	
1	Pin is designated as $\overline{\text{CSn}}$ output pin	(Initial value)

(n = 7 to 0)

5.16.3 Pin Functions

Port G pins also function as bus control signal output pins ($\overline{\text{BREQ}}$, $\overline{\text{BACK}}$, $\overline{\text{BREQO}}$, and $\overline{\text{CS3}}$ to $\overline{\text{CS0}}$). Port G pin functions are shown in table 5.35.

Table 5.35 Port G Pin Functions

Pin — **Selection Method and Pin Functions**

PG6/$\overline{\text{BREQ}}$ The pin function is switched as shown below according to the operating mode, bit EXPE, bit BRLE, and bit PG6DDR.

Operating mode	1, 2, 4, 5, 6			7				
EXPE	—			0		1		
BRLE	0		1	—		0		1
PG6DDR	0	1	—	0	1	0	1	—
Pin function	PG6 input pin	PG6 output pin	$\overline{\text{BREQ}}$ input pin	PG6 input pin	PG6 output pin	PG6 input pin	PG6 output pin	$\overline{\text{BREQ}}$ input pin

PG5/$\overline{\text{BACK}}$ The pin function is switched as shown below according to the operating mode, bit EXPE, bit BRLE, and bit PG5DDR.

Operating mode	1, 2, 4, 5, 6			7				
EXPE	—			0		1		
BRLE	0		1	—		0		1
PG5DDR	0	1	—	0	1	0	1	—
Pin function	PG5 input pin	PG5 output pin	$\overline{\text{BACK}}$ output pin	PG5 input pin	PG5 output pin	PG5 input pin	PG5 output pin	$\overline{\text{BACK}}$ output pin

Pin	Selection Method and Pin Functions

PG4/$\overline{\text{BREQO}}$

The pin function is switched as shown below according to the operating mode, bit EXPE, bit BRLE, bit BREQOE, and bit PG4DDR.

Operating mode	1, 2, 4, 5, 6					7						
EXPE	—					0		1				
BRLE	0		1			—		0		1		
BREQOE	—		0		1	—		—		0		1
PG4DDR	0	1	0	1	—	0	1	0	1	0	1	—
Pin function	PG4 input pin	PG4 output pin	PG4 input pin	PG4 output pin	$\overline{\text{BREQO}}$ output pin	PG4 input pin	PG4 output pin	PG4 input pin	PG4 output pin	PG4 input pin	PG4 output pin	$\overline{\text{BREQO}}$ output pin

PG3/$\overline{\text{CS3}}$
PG2/$\overline{\text{CS2}}$
PG1/$\overline{\text{CS1}}$
PG0/$\overline{\text{CS0}}$

The pin function is switched as shown below according to the operating mode, bit PGnDDR, and bit CSnE.

Operating mode	1, 2, 4, 5, 6				7					
EXPE	—				0		1			
CSnE	0		1		—		0		1	
PGnDDR	0	1	0	1	0	1	0	1	0	1
Pin function	PGn input pin	PGn output pin	PGn input pin	$\overline{\text{CSn}}$ output pin	PGn input pin	PGn output pin	PGn input pin	PGn output pin	PGn input pin	$\overline{\text{CSn}}$ output pin

(n = 3 to 0)

5.17 Port H

5.17.1 Overview

Port H is a 4-bit I/O port. Port H pins also function as bus control signal output pins ($\overline{CS7}$ to $\overline{CS4}$ and $\overline{OE}$) and interrupt signal input pins ($\overline{IRQ7}$ and $\overline{IRQ6}$).

Figure 5.16 shows the port H pin configuration.

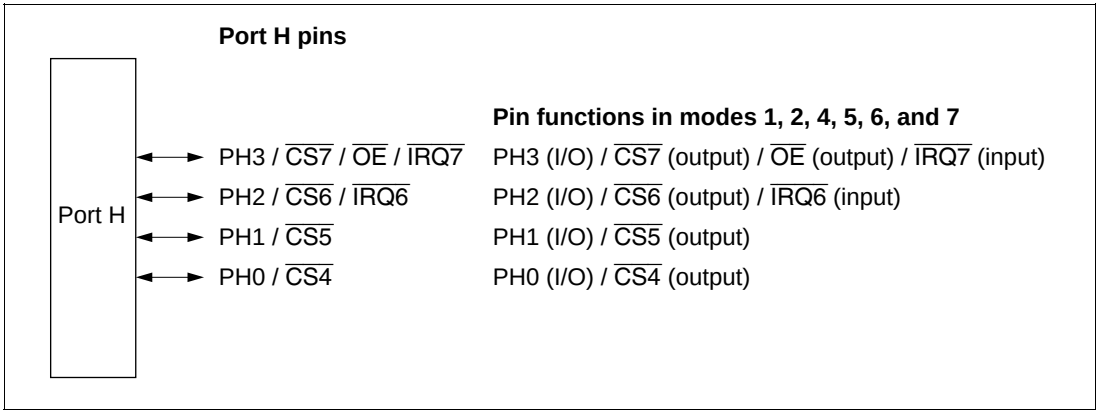


Figure 5.16 Port H Pin Functions

5.17.2 Register Configuration

Table 5.36 shows the port H register configuration.

Table 5.36 Port H Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port H data direction register	PHDDR	W	H'00	H'FF74
Port H data register	PHDR	R/W	H'00	H'FF72
Port H register	PORTH	R	Undefined	H'FF70
Port function control register 0	PFCR0	R/W	H'FF	H'FE32
Port function control register 2	PFCR2	R/W	H'0E	H'FE34

Note: * Lower 16 bits of the address.

Port H Data Direction Register (PHDDR)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	PH3DDR	PH2DDR	PH1DDR	PH0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	W	W	W	W

PHDDR is a 4-bit write-only register, the individual bits of which specify input or output for the pins of port H. PHDDR cannot be read; if it is, an undefined value will be read.

PHDDR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode. The OPE bit in SBYCR is used to select whether the bus control output pins retain their output state or become high-impedance when a transition is made to software standby mode.

- Modes 1, 2, 4, 5, and 6

  When the $\overline{OE}$ output enable bit (OEE) and $\overline{OE}$ output select bit (OES) are set to 1, pin PH3 functions as the $\overline{OE}$ output pin. Otherwise, when bit CS7E is set to 1, pin PH3 functions as a $\overline{CS}$ output pin when the corresponding PHDDR bit is set to 1, and as an input port when the bit is cleared to 0. When bit CS7E is cleared to 0, pin PH3 is an I/O port, and its function can be switched with PHDDR.

  When the $\overline{CS}$ output enable bits (CS6E to CS4E) are set to 1, pins PH2 to PH0 function as $\overline{CS}$ output pins when the corresponding PHDDR bit is set to 1, and as I/O ports when the bit is cleared to 0. When CS6E to CS4E are cleared to 0, pins PH2 to PH0 are I/O ports, and their functions can be switched with PHDDR.

- Mode 7 (when bit EXPE is set to 1 in SYSCR)

  When the $\overline{OE}$ output enable bit (OEE) and $\overline{OE}$ output select bit (OES) are set to 1, pin PH3 functions as the $\overline{OE}$ output pin. Otherwise, when bit CS7E is set to 1, pin PH3 functions as a $\overline{CS}$ output pin when the corresponding PHDDR bit is set to 1, and as an input port when the bit is cleared to 0. When bit CS7E is cleared to 0, pin PH3 is an I/O port, and their functions can be switched with PHDDR.

  When the $\overline{CS}$ output enable bits (CS6E to CS4E) are set to 1, pins PH2 to PH0 function as $\overline{CS}$ output pins when the corresponding PHDDR bit is set to 1, and as input ports when the bit is cleared to 0. When CS6E to CS4E are cleared to 0, pins PH2 to PH0 are I/O ports, and their functions can be switched with PHDDR.

- Mode 7 (when bit EXPE is cleared to 0 in SYSCR)

  Pins PH3 to PH0 are I/O ports, and their functions can be switched with PHDDR.

Port H Data Register (PHDR)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	PH3DR	PH2DR	PH1DR	PH0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

PHDR is a 4-bit readable/writable register that stores output data for the port H pins (PH3 to PH0).

Bits 7 to 4 are reserved; they are always read as 0 and cannot be modified.

PHDR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Port H Register (PORTH)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	PH3	PH2	PH1	PH0
Initial value	Undefined	Undefined	Undefined	Undefined	—*	—*	—*	—*
Read/Write	—	—	—	—	R	R	R	R

Note: * Determined by the state of pins PH3 to PH0.

PORTH is a 4-bit read-only register that shows the pin states. PORTH cannot be written to; writing of output data for the port H pins (PH3 to PH0) must always be performed on PHDR.

Bits 7 to 4 are reserved; if read they will return an undefined value.

If a port H read is performed while PHDDR bits are set to 1, the PHDR values are read. If a port H read is performed while PHDDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORTH contents are determined by the pin states, as PHDDR and PHDR are initialized. PORTH retains its prior state in software standby mode.

Port Function Control Register 0 (PFCR0)

Bit	7	6	5	4	3	2	1	0
	CS7E	CS6E	CS5E	CS4E	CS3E	CS2E	CS1E	CS0E
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PFCR0 is an 8-bit readable/writable register that performs I/O port control. PFCR0 is initialized to H'FF by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Bits 7 to 0—CS7 to CS0 Enable (CS7E to CS0E): These bits enable or disable the corresponding $\overline{\text{CSn}}$ output.

Bit n CSnE	Description	
0	Pin is designated as I/O port and does not function as $\overline{\text{CSn}}$ output pin	
1	Pin is designated as $\overline{\text{CSn}}$ output pin	(Initial value)

(n = 7 to 0)

Port Function Control Register 2 (PFCR2)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	ASOE	LWROE	OES	DMACS
Initial value	0	0	0	0	1	1	1	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

PFCR2 is an 8-bit readable/writable register that performs I/O port control. PFCR2 is initialized to H'0E by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Bits 7 to 4—Reserved: These bits are always read as 0, and should only be written with 0.

Bit 1—OE Output Select (OES): Selects the $\overline{\text{OE}}$ output pin port when the OEE bit is set to 1 in DRAMCR (enabling $\overline{\text{OE}}$ output).

Bit 1 OES	Description	
0	P35 is designated as $\overline{\text{OE}}$ output pin	
1	PH5 is designated as $\overline{\text{OE}}$ output pin	(Initial value)

5.17.3 Pin Functions

Port H pins also function as bus control signal output pins ($\overline{\text{CS7}}$ to $\overline{\text{CS4}}$ and $\overline{\text{OE}}$) and interrupt signal input pins ($\overline{\text{IRQ7}}$ and $\overline{\text{IRQ6}}$). Port H pin functions are shown in table 5.37.

Table 5.37 Port H Pin Functions

Pin	Selection Method and Pin Functions
PH3/$\overline{CS7}$/ $\overline{OE}$/$\overline{IRQ7}$	The pin function is switched as shown below according to the operating mode, bit EXPE, bit OEE, bit OES, bit CS7E, and bit PH3DDR.

Operating mode	1, 2, 4, 5, 6									7									
EXPE	—									0		1							
OEE	0				1					—		0			1				
OES	—				0				1	—		—			0				1
CS7E	0		1		0		1		—	—		0		1		0		1		—
PH3DDR	0	1	0	1	0	1	0	1	—	0	1	0	1	0	1	0	1	0	1	—
Pin function	PH3 input pin	PH3 output pin	PH3 input pin	$\overline{CS7}$ output pin	PH3 input pin	PH3 output pin	PH3 input pin	$\overline{CS7}$ output pin	$\overline{OE}$ output pin	PH3 input pin	PH3 output pin	PH3 input pin	PH3 output pin	PH3 input pin	$\overline{CS7}$ output pin	PH3 input pin	PH3 output pin	PH3 input pin	$\overline{CS7}$ output pin	$\overline{OE}$ output pin
	$\overline{IRQ7}$ interrupt input pin*																			

Note: * $\overline{IRQ7}$ interrupt input pin when bit ITS7 is set to 1 in ITSR.

PH2/$\overline{CS6}$/ $\overline{IRQ6}$	The pin function is switched as shown below according to the operating mode, bit CS6E, and bit PH2DDR.

Operating mode	1, 2, 4, 5, 6				7					
EXPE	—				0		1			
CS6E	0		1		—		0		1	
PH2DDR	0	1	0	1	0	1	0	1	0	1
Pin function	PH2 input pin	PH2 output pin	PH2 input pin	$\overline{CS6}$ output pin	PH2 input pin	PH2 output pin	PH2 input pin	PH2 output pin	PH2 input pin	$\overline{CS6}$ output pin
	$\overline{IRQ6}$ interrupt input pin*									

Note: * $\overline{IRQ6}$ interrupt input pin when bit ITS6 is set to 1 in ITSR.

PH1/$\overline{CS5}$ PH0/$\overline{CS4}$	The pin function is switched as shown below according to the operating mode, bits CS5E and CS4E, and bit PHmDDR.

Operating mode	1, 2, 4, 5, 6				7					
EXPE	—				0		1			
CSnE	0		1		—		0		1	
PHmDDR	0	1	0	1	0	1	0	1	0	1
Pin function	PHm input pin	PHm output pin	PHm input pin	$\overline{CSn}$ output pin	PHm input pin	PHm output pin	PHm input pin	PHm output pin	PHm input pin	$\overline{CSn}$ output pin

(m = 1 or 0, n = 5 or 4)

5.18 Pin Functions

5.18.1 Port States in Each Processing State

Table 5.38 I/O Port States in Each Processing State

Port Name Pin Name	MCU Operating Mode	Reset	Hardware Standby Mode	Software Standby Mode	Bus-Released State	Program Execution State Sleep Mode
Port 1	1, 2, 4 to 7	T	T	keep	keep	I/O port
Port 2	1, 2, 4 to 7	T	T	keep	keep	I/O port
P34 to P30	1, 2, 4 to 7	T	T	keep	keep	I/O port
P35	1, 2, 4 to 7	T	T	[$\overline{OE}$ output, OPE = 0] T [$\overline{OE}$ output, OPE = 1] H [Otherwise] keep	[$\overline{OE}$ output] T [Otherwise] keep	[$\overline{OE}$ output] $\overline{OE}$ [Otherwise] I/O port
P47/DA1	1, 2, 4 to 7	T	T	[DAOE1 = 1] keep [DAOE1 = 0] T	keep	Input port
P46/DA0	1, 2, 4 to 7	T	T	[DAOE0 = 1] keep [DAOE0 = 0] T	keep	Input port
P45 to P40	1, 2, 4 to 7	T	T	T	T	Input port
P57/DA3	1, 2, 4 to 7	T	T	[DAOE3 = 1] keep [DAOE3 = 0] T	keep	Input port
P56/DA2	1, 2, 4 to 7	T	T	[DAOE2 = 1] keep [DAOE2 = 0] T	keep	Input port
P55, P54	1, 2, 4 to 7	T	T	T	T	Input port
P53 to P50	1, 2, 4 to 7	T	T	keep	keep	I/O port
Port 6	1, 2, 4 to 7	T	T	keep	keep	I/O port
Port 7	1, 2, 4 to 7	T	T	keep	keep	I/O port
Port 8	1, 2, 4 to 7	T	T	keep	keep	I/O port

Port Name Pin Name	MCU Operating Mode	Reset	Hardware Standby Mode	Software Standby Mode	Bus-Released State	Program Execution State Sleep Mode
PA7/A23 PA6/A22 PA5/A21	1, 2, 4 to 7	T	T	[Address output, OPE = 0] T [Address output, OPE = 1] keep [Otherwise] keep	[Address output] T [Otherwise] keep	[Address output] A23 to A21 [Otherwise] I/O port
PA4/A20 PA3/A19 PA2/A18 PA1/A17	1, 2, 5, 6	L	T	[OPE = 0] T [OPE = 1] keep	T	Address output A20 to A16
PA0/A16	4, 7	T	T	[Address output, OPE = 0] T [Address output, OPE = 1] keep [Otherwise] keep	[Address output] T [Otherwise] keep	[Address output] A20 to A16 [Otherwise] I/O port
Port B	1, 2, 5, 6	L	T	[OPE = 0] T [OPE = 1] keep	T	Address output A15 to A8
	4	T	T	[Address output, OPE = 0] T [Address output, OPE = 1] keep [Otherwise] keep	[Address output] T [Otherwise] keep	[Address output] A15 to A8 [Otherwise] I/O port
	7	T	T	[Address output, OPE = 0] T [Address output, OPE = 1] keep [Otherwise] keep	[Address output] T [Otherwise] keep	[Address output] A15 to A8 [Otherwise] I/O port

Port Name Pin Name	MCU Operating Mode		Reset	Hardware Standby Mode	Software Standby Mode	Bus-Released State	Program Execution State Sleep Mode
Port C	1, 2, 5, 6		L	T	[OPE = 0] T [OPE = 1] keep	T	Address output A7 to A0
	4		T	T	[Address output, OPE = 0] T [Address output, OPE = 1] keep [Otherwise] keep	[Address output] T [Otherwise] keep	[Address output] A7 to A0 [Otherwise] I/O port
	7		T	T	[Address output, OPE = 0] T [Address output, OPE = 1] keep [Otherwise] keep	[Address output] T [Otherwise] keep	[Address output] A7 to A0 [Otherwise] I/O port
Port D	1, 2, 4 to 6		T	T	T	T	D15 to D8
	7		T	T	[Data bus] T [Otherwise] keep	[Data bus] T [Otherwise] keep	[Data bus] D15 to D8 [Otherwise] I/O port
Port E	1, 2, 4 to 6	8-bit bus	T	T	keep	keep	I/O port
		16-bit bus	T	T	T	T	D7 to D0
	7	8-bit bus	T	T	keep	keep	I/O port
		16-bit bus	T	T	[Data bus] T [Otherwise] keep	[Data bus] T [Otherwise] keep	[Data bus] D7 to D0 [Otherwise] I/O port
PF7/ø	1, 2, 4 to 6		Clock output	T	[Clock output] H	[Clock output] Clock output	[Clock output] Clock output
	7		T		[Otherwise] keep	[Otherwise] keep	[Otherwise] Input port
PF6/$\overline{AS}$	1, 2, 4 to 6		H	T	[$\overline{AS}$ output, OPE = 0] T	[$\overline{AS}$ output] T	[$\overline{AS}$ output] $\overline{AS}$
	7		T		[$\overline{AS}$ output, OPE = 1] H [Otherwise] keep	[Otherwise] keep	[Otherwise] I/O port

Port Name Pin Name	MCU Operating Mode	Reset	Hardware Standby Mode	Software Standby Mode	Bus-Released State	Program Execution State Sleep Mode
PF5/$\overline{RD}$ PF4/$\overline{HWR}$	1, 2, 4 to 6	H	T	[OPE = 0] T [OPE = 1] H	T	$\overline{RD}$, $\overline{HWR}$
	7	T		[$\overline{RD}$, $\overline{HWR}$ output, OPE = 0] T [$\overline{RD}$, $\overline{HWR}$ output, OPE = 1] H [Otherwise] keep	[$\overline{RD}$, $\overline{HWR}$ output] T [Otherwise] keep	[$\overline{RD}$, $\overline{HWR}$ output] $\overline{RD}$, $\overline{HWR}$ [Otherwise] I/O port
PF3/$\overline{LWR}$	1, 2, 4 to 6	H	T	[$\overline{LWR}$ output, OPE = 0] T	[$\overline{LWR}$ output] T	[$\overline{LWR}$ output] $\overline{LWR}$
	7	T		[$\overline{LWR}$ output, OPE = 1] H [Otherwise] keep	[Otherwise] keep	[Otherwise] I/O port
PF2/$\overline{LCAS}$	1, 2, 4 to 7	T	T	[$\overline{LCAS}$ output, OPE = 0] T [$\overline{LCAS}$ output, OPE = 1] H [Otherwise] keep	[$\overline{LCAS}$ output] T [Otherwise] keep	[$\overline{LCAS}$ output] $\overline{LCAS}$ [Otherwise] I/O port
PF1/$\overline{UCAS}$	1, 2, 4 to 7	T	T	[$\overline{UCAS}$ output, OPE = 0] T [$\overline{UCAS}$ output, OPE = 1] H [Otherwise] keep	[$\overline{UCAS}$ output] T [Otherwise] keep	[$\overline{UCAS}$ output] $\overline{UCAS}$ [Otherwise] I/O port
PF0/$\overline{WAIT}$	1, 2, 4 to 7	T	T	[$\overline{WAIT}$ input] T [Otherwise] keep	[$\overline{WAIT}$ input] T [Otherwise] keep	[$\overline{WAIT}$ input] $\overline{WAIT}$ [Otherwise] I/O port
PG6/$\overline{BREQ}$	1, 2, 4 to 7	T	T	[$\overline{BREQ}$ input] T [Otherwise] keep	$\overline{BREQ}$ input $\overline{BREQ}$	[$\overline{BREQ}$ input] $\overline{BREQ}$ [Otherwise] I/O port
PG5/$\overline{BACK}$	1, 2, 4 to 7	T	T	[$\overline{BACK}$ output] T [Otherwise] keep	$\overline{BACK}$ output $\overline{BACK}$	[BACK output] BACK [Otherwise] I/O port

Port Name Pin Name	MCU Operating Mode	Reset	Hardware Standby Mode	Software Standby Mode	Bus-Released State	Program Execution State Sleep Mode
PG4/$\overline{\text{BREQO}}$	1, 2, 4 to 7	T	T	[$\overline{\text{BREQO}}$ output] T	$\overline{\text{BREQO}}$ output $\overline{\text{BREQO}}$	[$\overline{\text{BREQO}}$ output] $\overline{\text{BREQO}}$
				[Otherwise] keep	[Otherwise] keep	[Otherwise] I/O port
PG3/$\overline{\text{CS3}}$ PG2/$\overline{\text{CS2}}$ PG1/$\overline{\text{CS1}}$	1, 2, 4 to 7	T	T	[$\overline{\text{CS}}$ output, OPE = 0] T	[$\overline{\text{CS}}$ output] T	[$\overline{\text{CS}}$ output] $\overline{\text{CS}}$
				[$\overline{\text{CS}}$ output, OPE = 1] H	[Otherwise] keep	[Otherwise] I/O port
				[Otherwise] keep		
PG0/$\overline{\text{CS0}}$	1, 2, 5, 6	H	T	[$\overline{\text{CS}}$ output, OPE = 0] T	[$\overline{\text{CS}}$ output] T	[$\overline{\text{CS}}$ output] $\overline{\text{CS}}$
	4, 7	T		[$\overline{\text{CS}}$ output, OPE = 1] H	[Otherwise] keep	[Otherwise] I/O port
				[Otherwise] keep		
PH3/$\overline{\text{OE}}$/$\overline{\text{CS7}}$	1, 2, 4 to 7	T	T	[$\overline{\text{OE}}$ output, OPE = 0] T	[$\overline{\text{OE}}$ output] T	[$\overline{\text{OE}}$ output] $\overline{\text{OE}}$
				[$\overline{\text{OE}}$ output, OPE = 1] H	[$\overline{\text{CS}}$ output] T	[$\overline{\text{CS}}$ output] $\overline{\text{CS}}$
				[$\overline{\text{CS}}$ output, OPE = 0] T	[Otherwise] keep	[Otherwise] I/O port
				[$\overline{\text{CS}}$ output, OPE = 1] H		
				[Otherwise] keep		
PH2/$\overline{\text{CS6}}$ PH1/$\overline{\text{CS5}}$ PH0/$\overline{\text{CS4}}$	1, 2, 4 to 7	T	T	[$\overline{\text{CS}}$ output, OPE = 0] T	[$\overline{\text{CS}}$ output] T	[$\overline{\text{CS}}$ output] $\overline{\text{CS}}$
				[$\overline{\text{CS}}$ output, OPE = 1] H	[Otherwise] keep	[Otherwise] I/O port
				[Otherwise] keep		

Legend

L: Low level

keep: Input port becomes high-impedance, output port retains state

OPE: Output port enable

H: High level

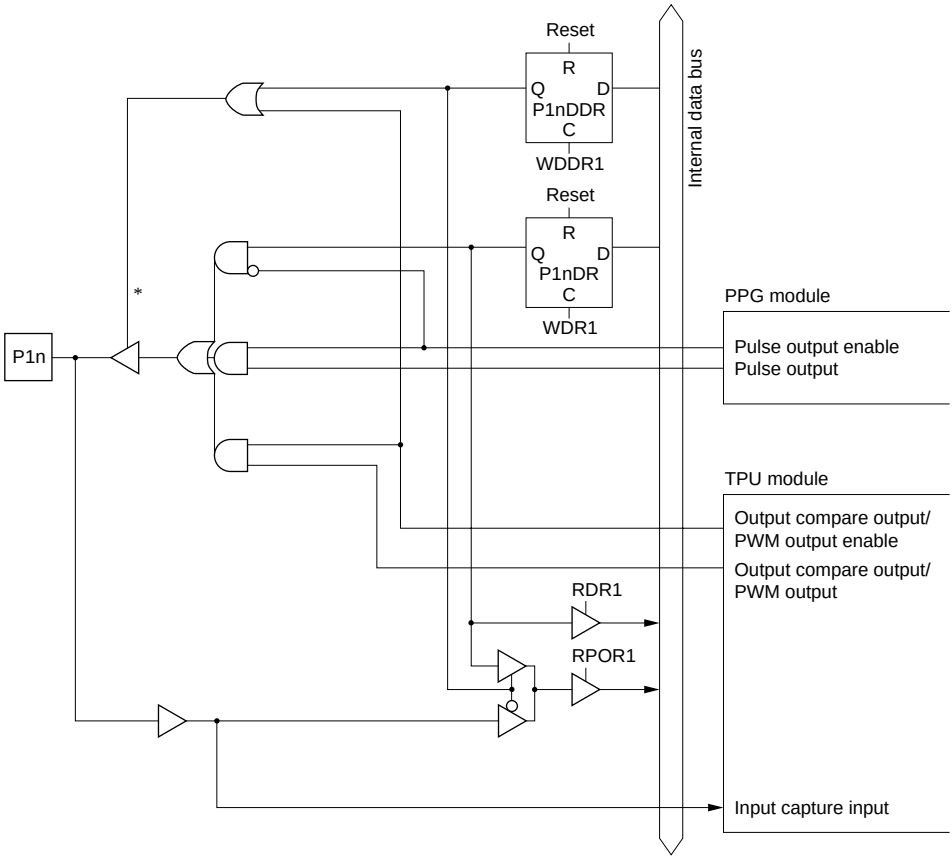
T: High impedance

DDR Data direction register

Note: * Shows the state after completion of the executing bus cycle.

5.19 I/O Port Block Diagrams

5.19.1 Port 1



WDDR1: Write to P1DDR
WDR1: Write to P1DR
RPOR1: Read port 1
RDR1: Read P1DR
n = 0, 1, 4

Note: * Output enable signal
Priority order: TPU > PPG > DR

Figure 5.17 Port 1 Block Diagram (a) (Pins P10, P11, and P14)

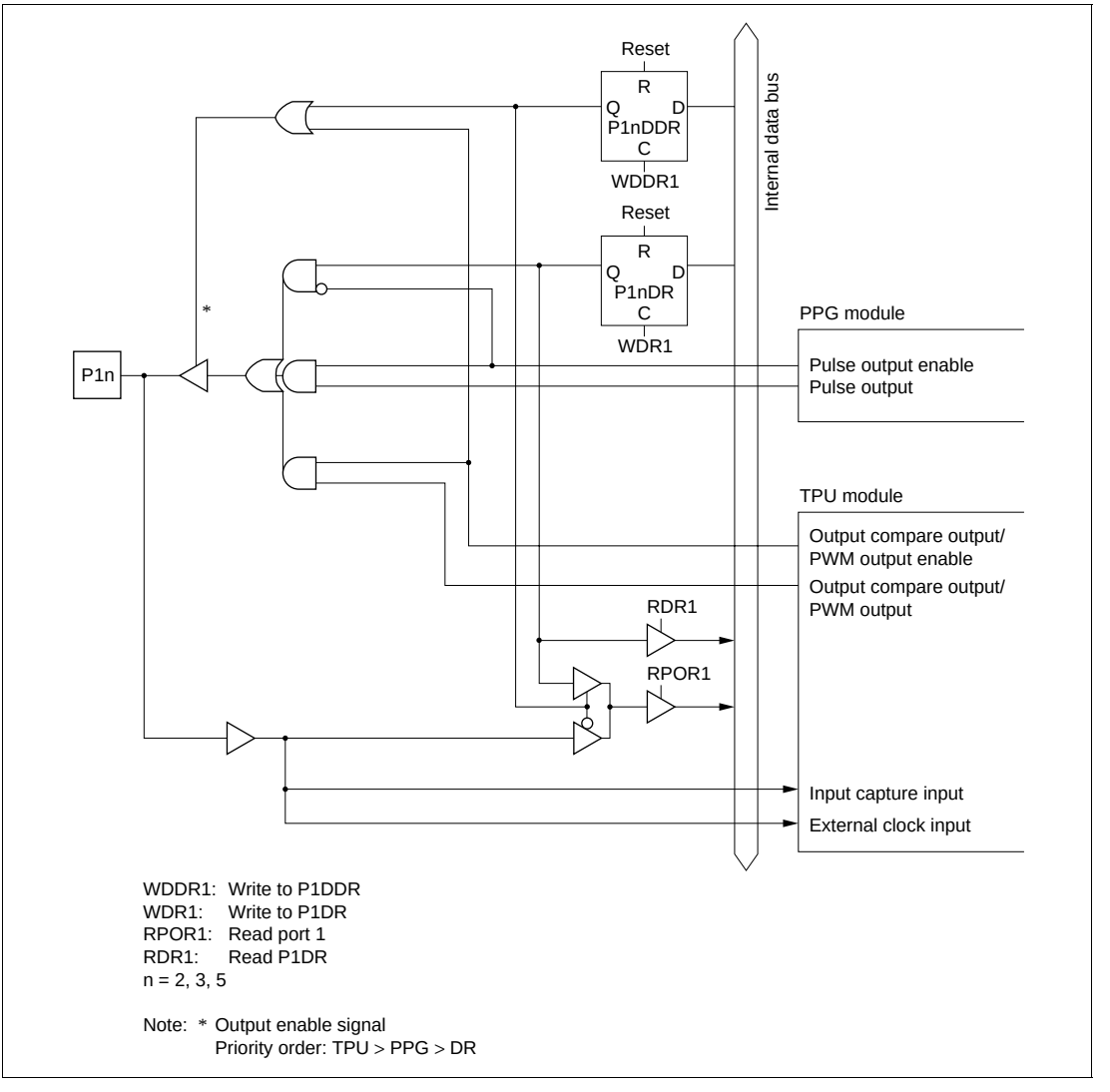


Figure 5.18 Port 1 Block Diagram (b) (Pins P12, P13, and P15)

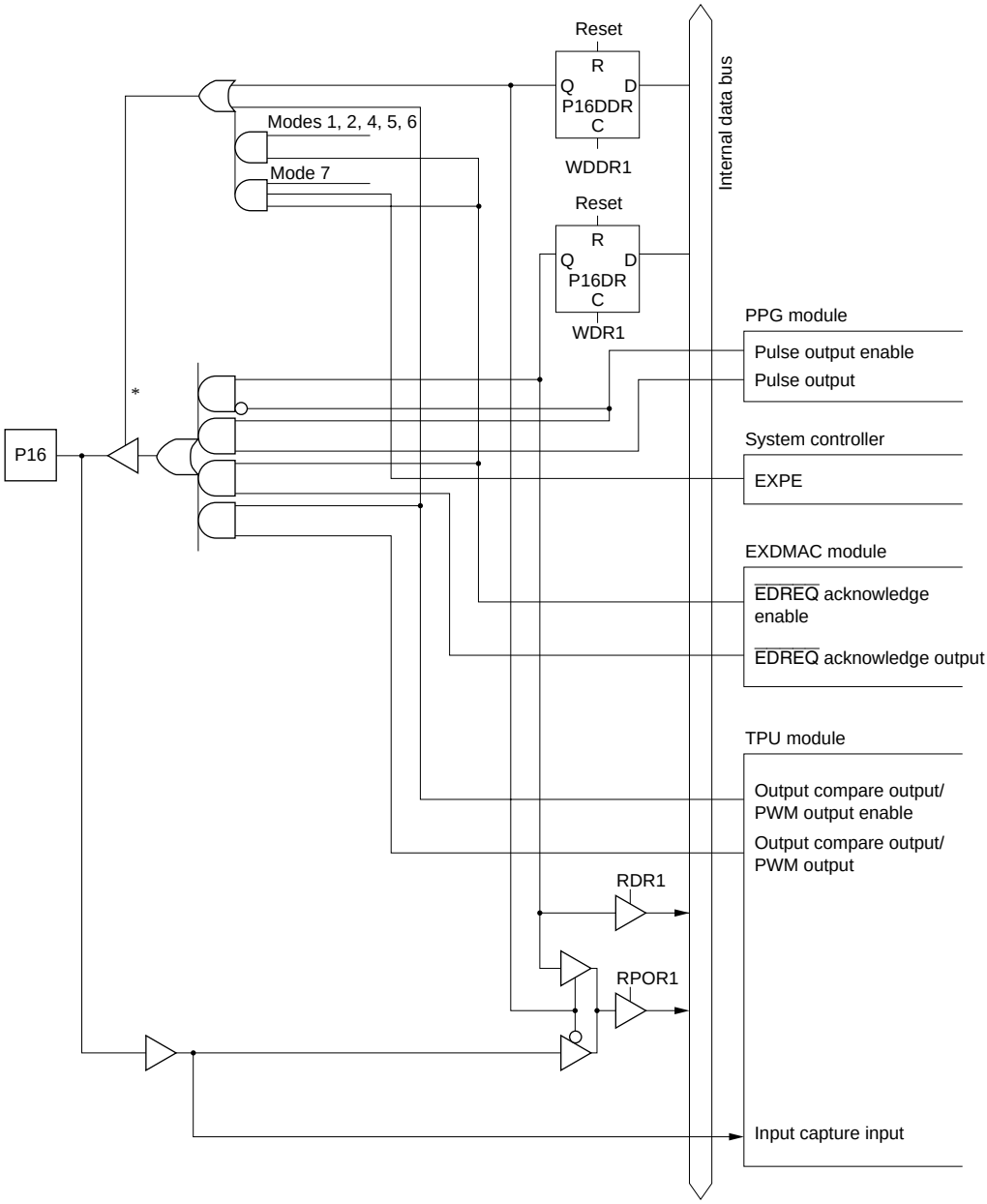


Figure 5.19 Port 1 Block Diagram (c) (Pin P16)

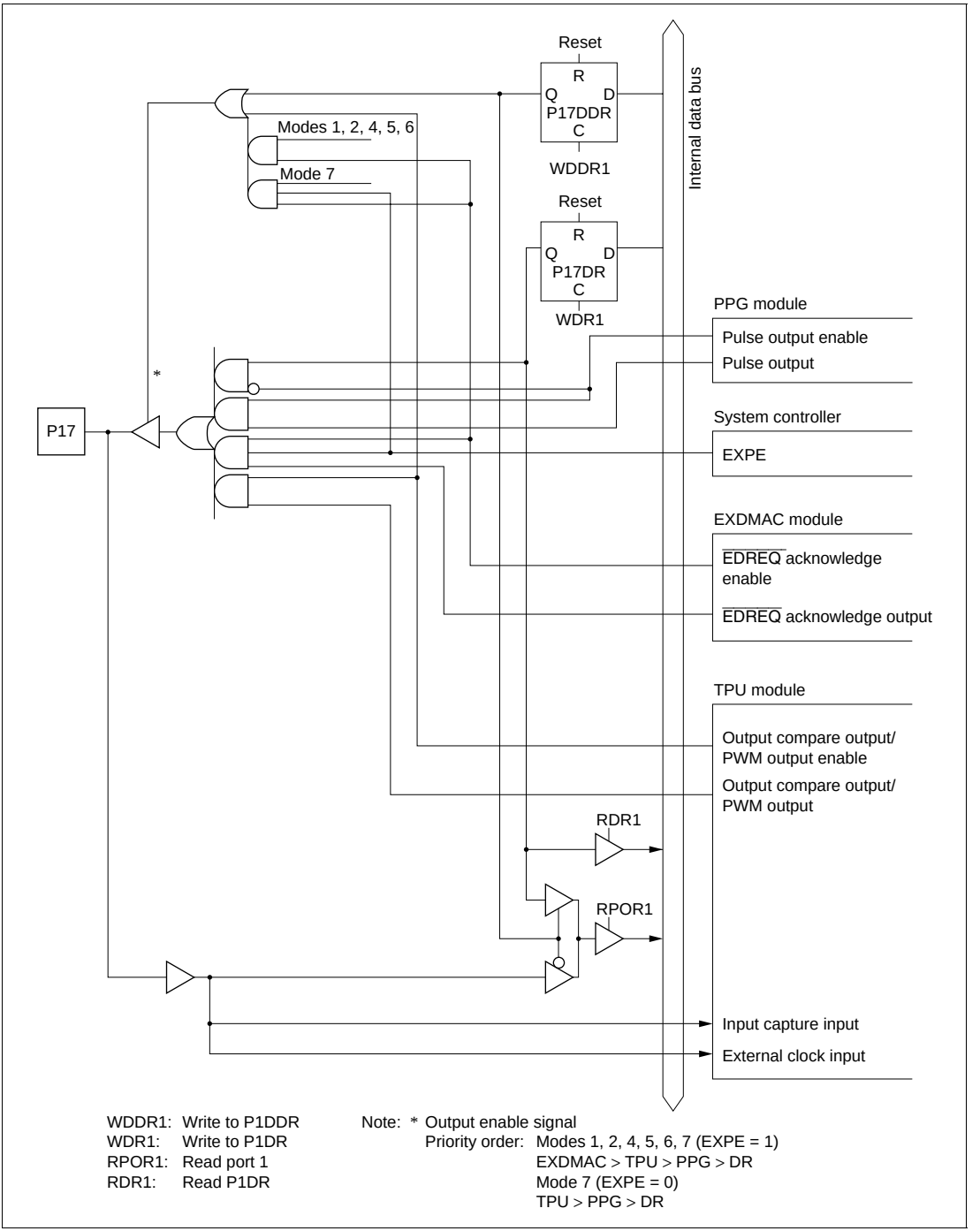


Figure 5.20 Port 1 Block Diagram (d) (Pin P17)

5.19.2 Port 2

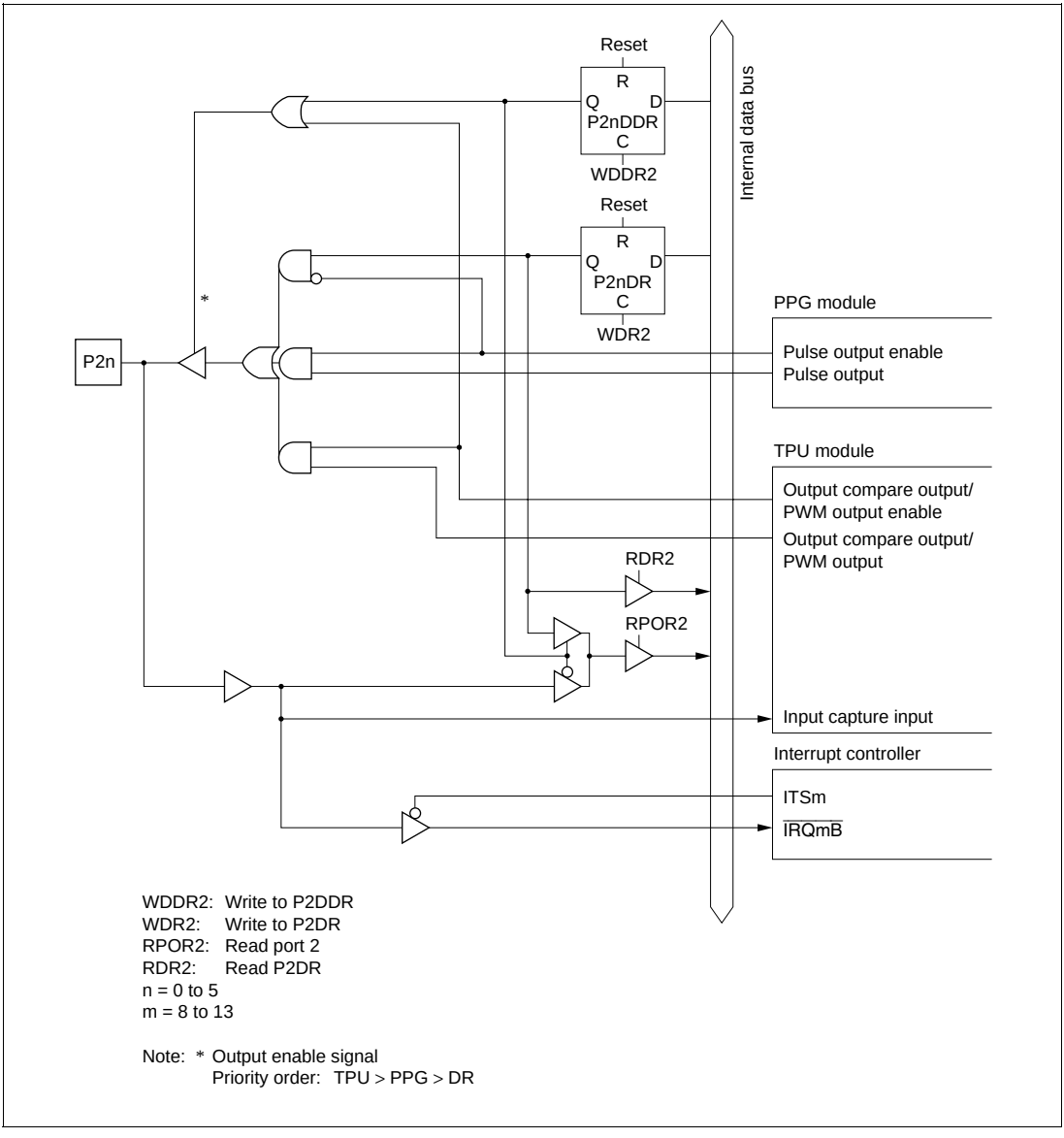


Figure 5.21 Port 2 Block Diagram (a) (Pins P20 to P25)

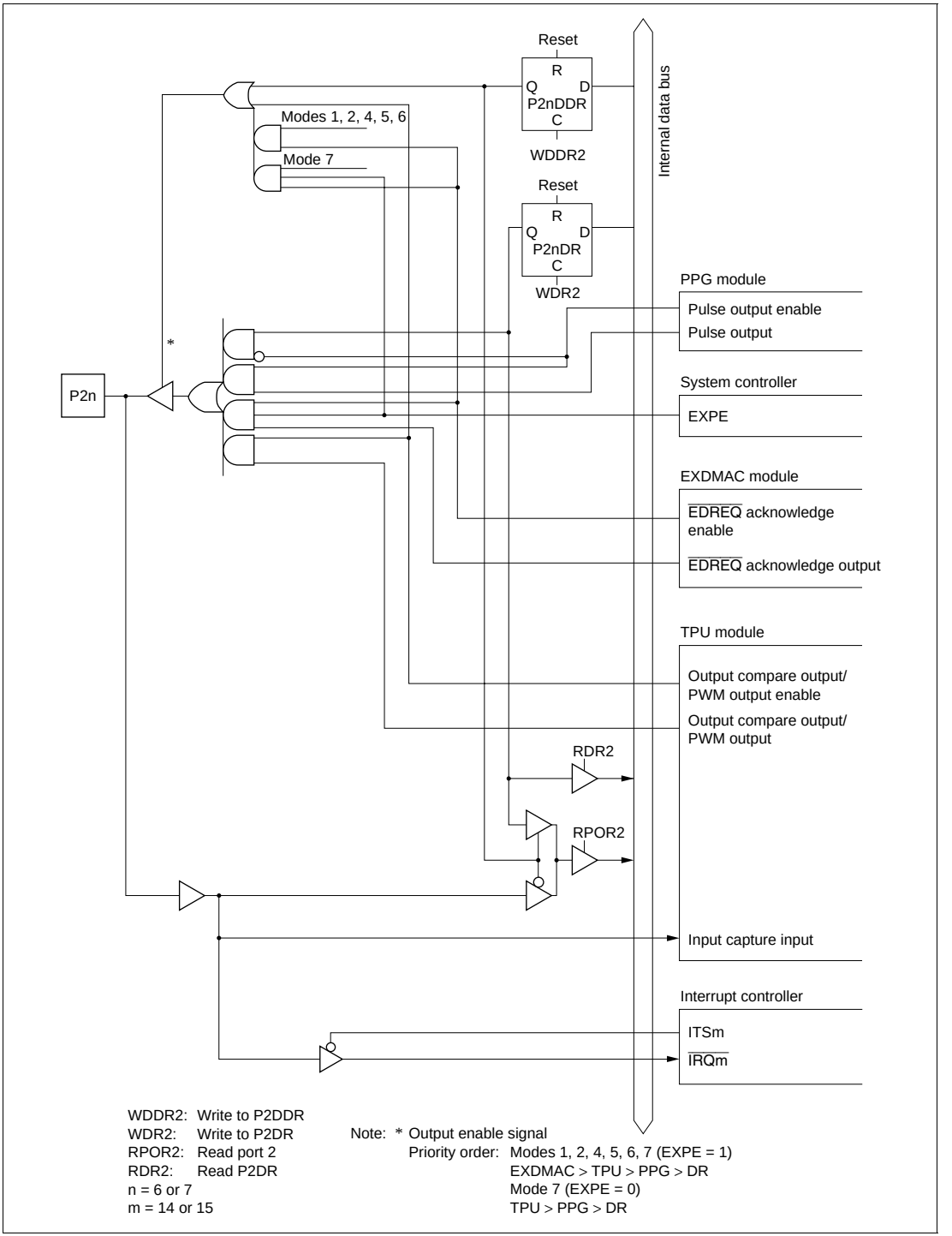
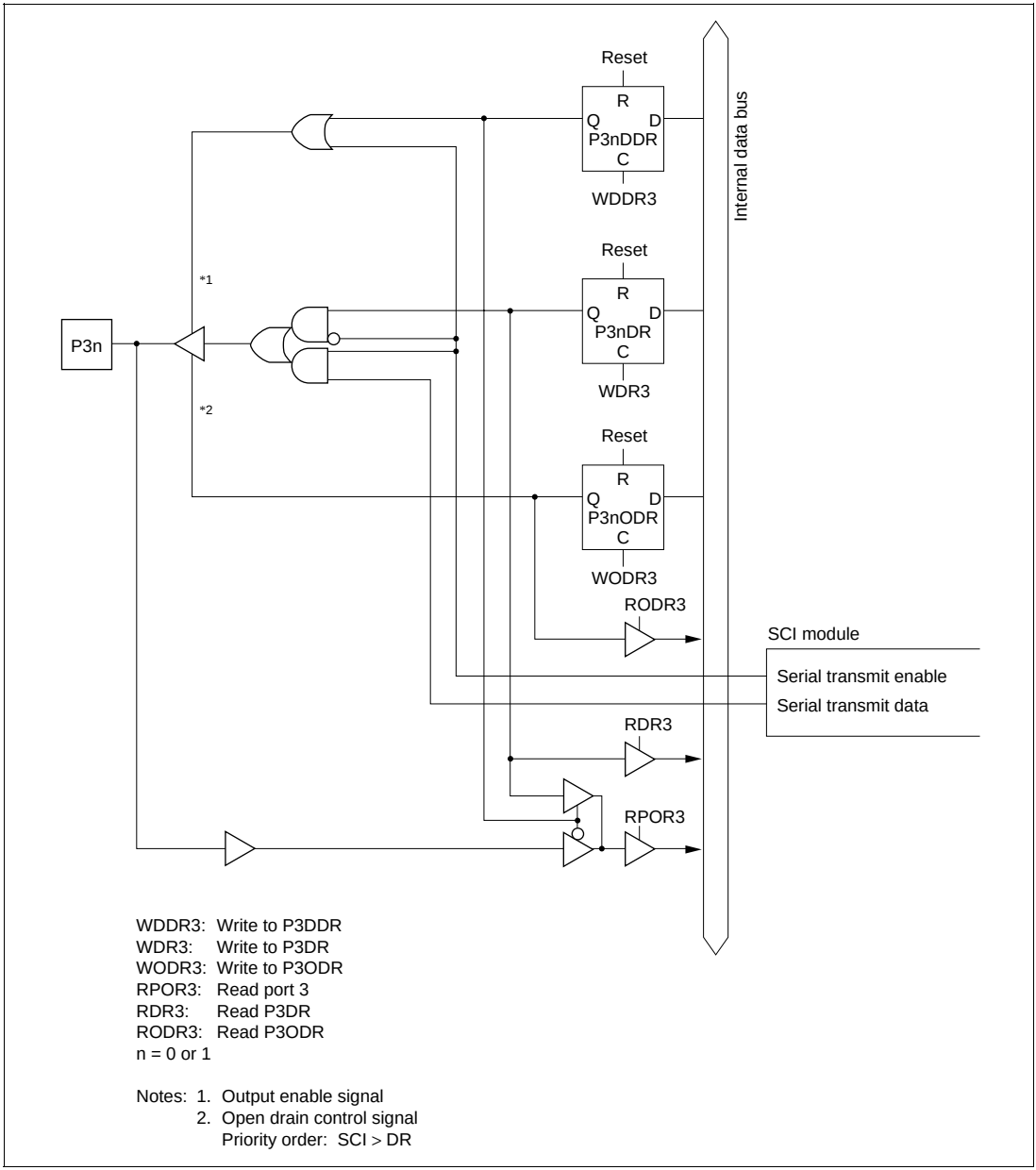


Figure 5.22 Port 2 Block Diagram (b) (Pins P26 and P27)

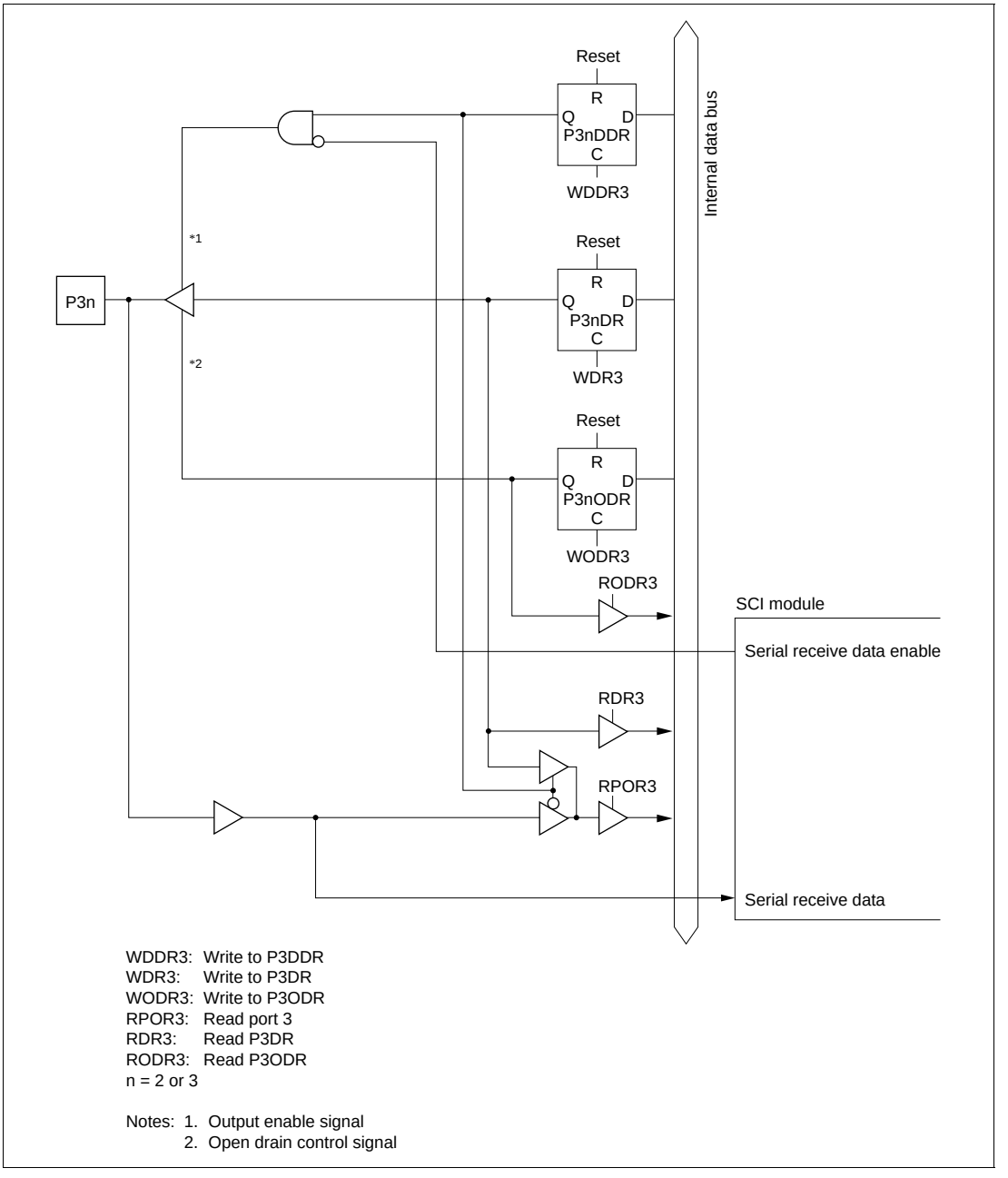
5.19.3 Port 3



WDDR3: Write to P3DDR
WDR3: Write to P3DR
WODR3: Write to P3ODR
RPOR3: Read port 3
RDR3: Read P3DR
RODR3: Read P3ODR
n = 0 or 1

Notes: 1. Output enable signal
2. Open drain control signal
Priority order: SCI > DR

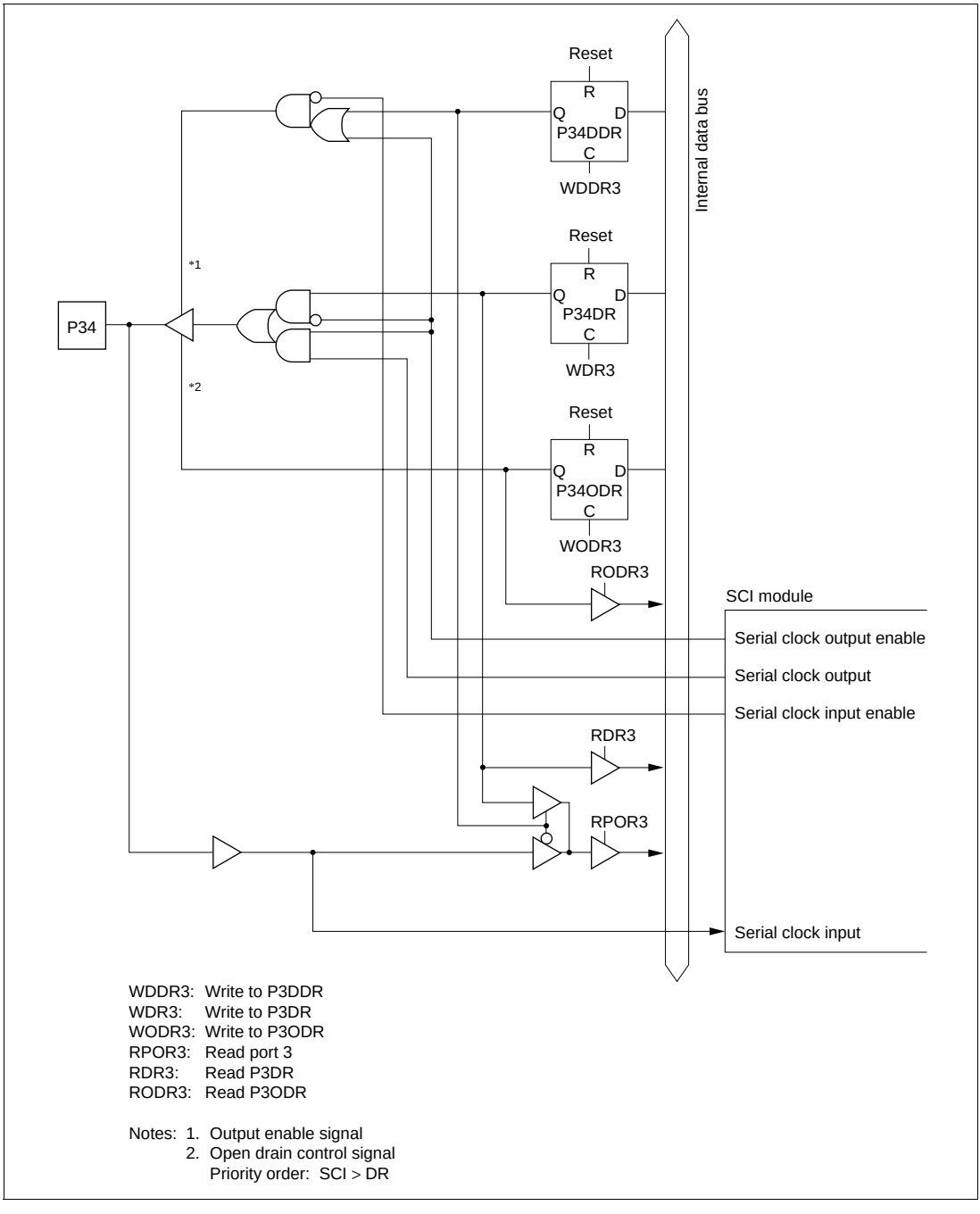
Figure 5.23 Port 3 Block Diagram (a) (Pins P30 and P31)



WDDR3: Write to P3DDR
WDR3: Write to P3DR
WODR3: Write to P3ODR
RPOR3: Read port 3
RDR3: Read P3DR
RODR3: Read P3ODR
n = 2 or 3

Notes: 1. Output enable signal
2. Open drain control signal

Figure 5.24 Port 3 Block Diagram (b) (Pins P32 and P33)



WDDR3: Write to P3DDR
WDR3: Write to P3DR
WODR3: Write to P3ODR
RPOR3: Read port 3
RDR3: Read P3DR
RODR3: Read P3ODR

Notes: 1. Output enable signal
2. Open drain control signal
Priority order: SCI > DR

Figure 5.25 Port 3 Block Diagram (c) (Pin P34)

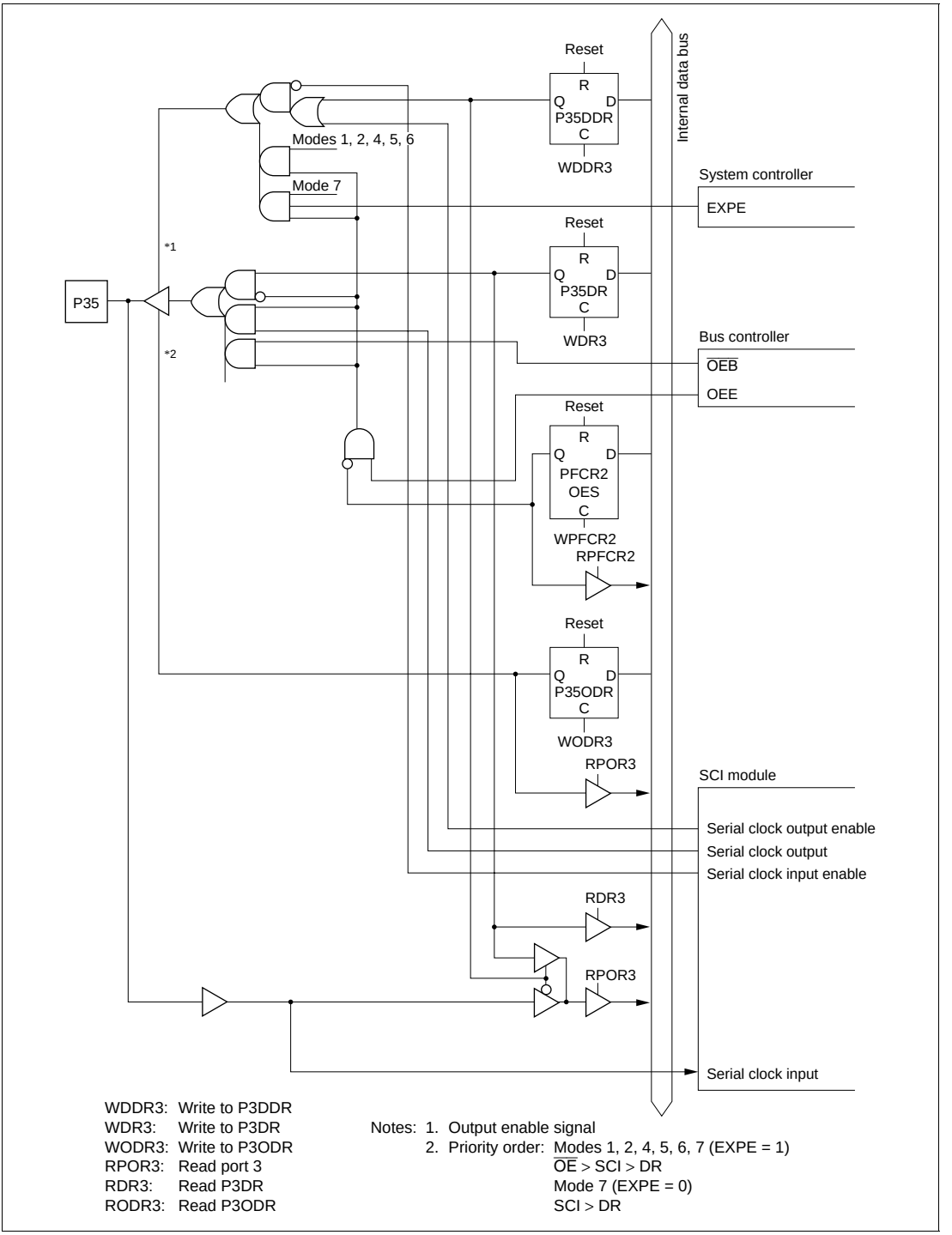


Figure 5.26 Port 3 Block Diagram (d) (Pin P35)

5.19.4 Port 4

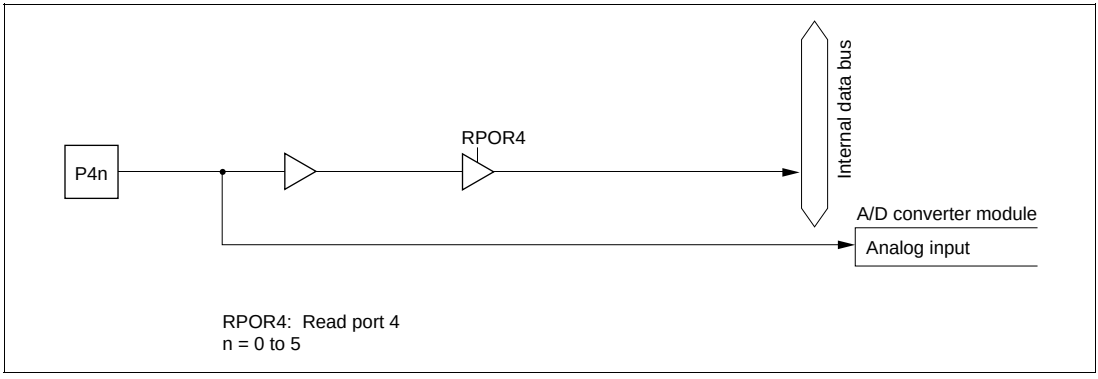


Figure 5.27 Port 4 Block Diagram (a) (Pins P40 to P45)

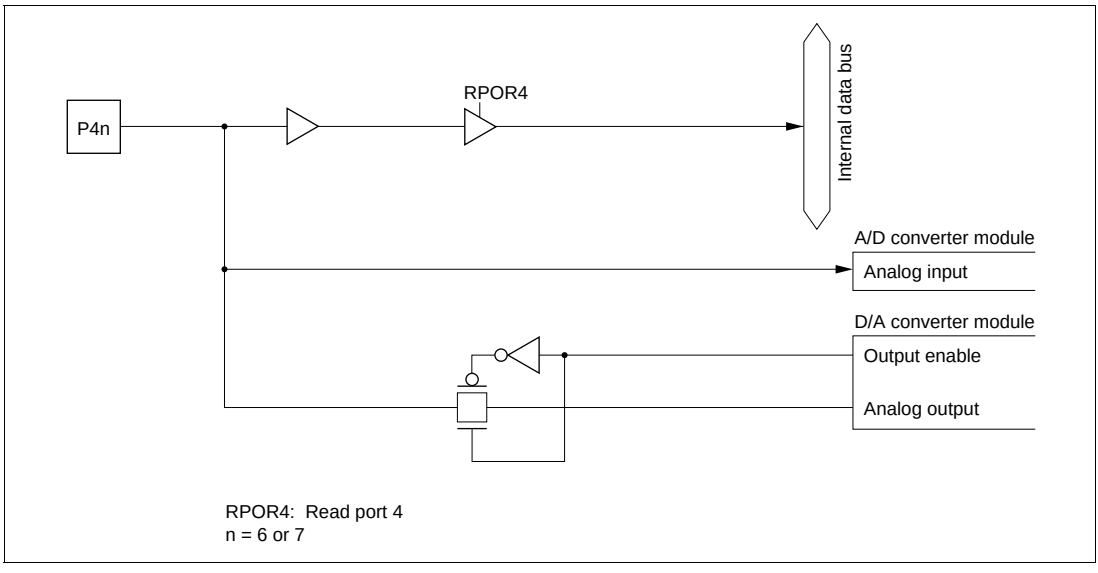


Figure 5.28 Port 4 Block Diagram (b) (Pins P46 and P47)

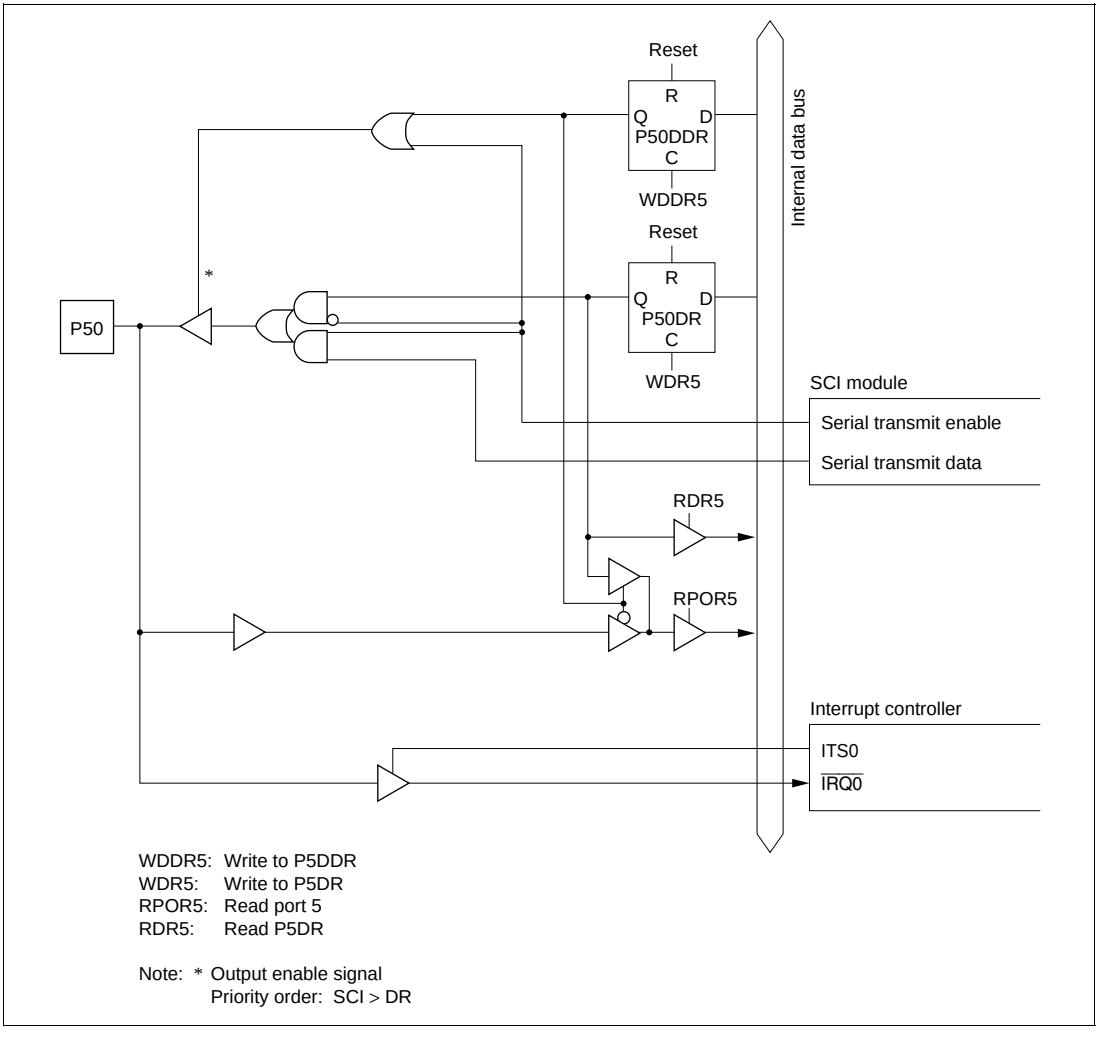


Figure 5.29 Port 5 Block Diagram (a) (Pin P50)

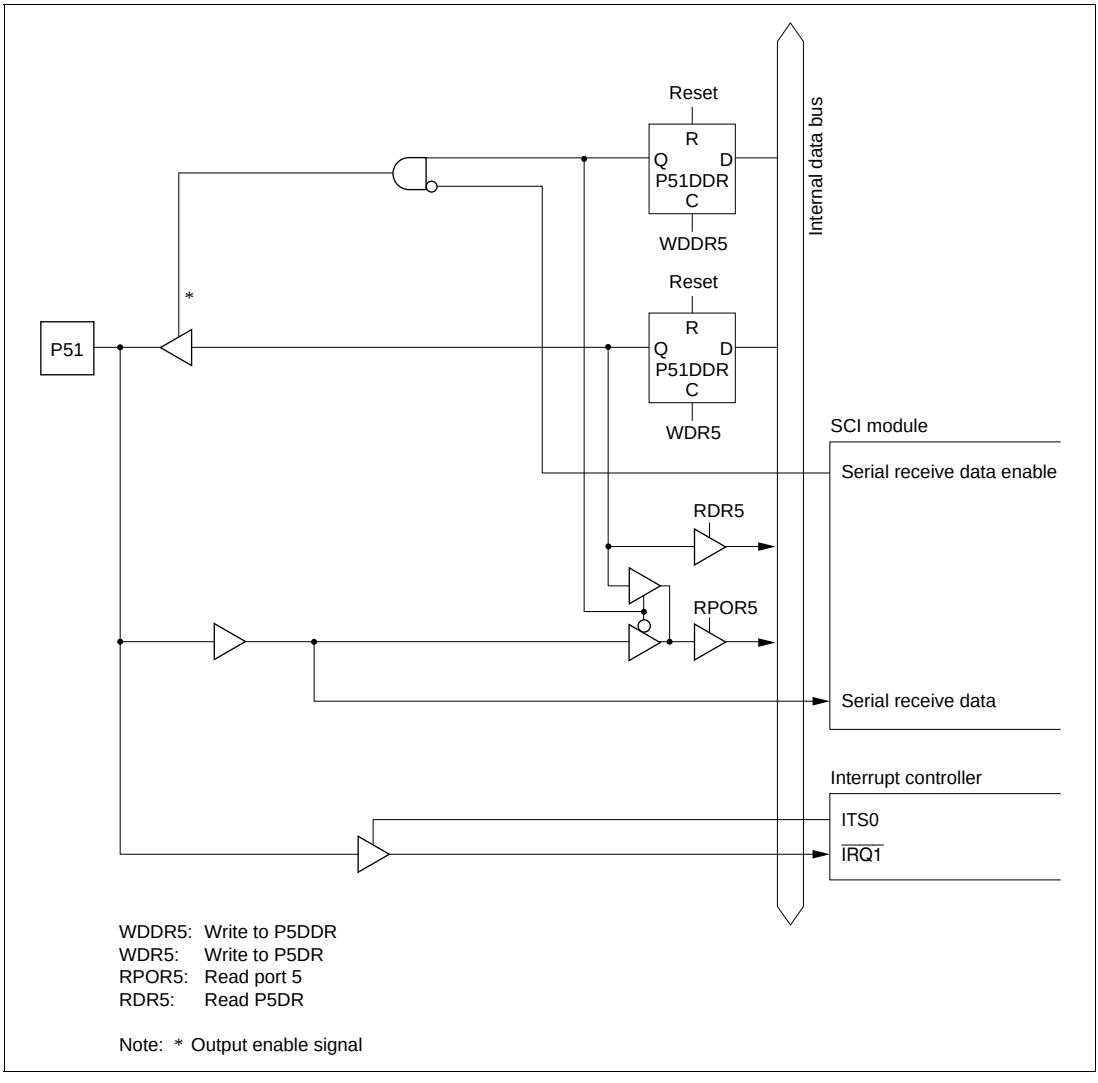


Figure 5.30 Port 5 Block Diagram (b) (Pin P51)

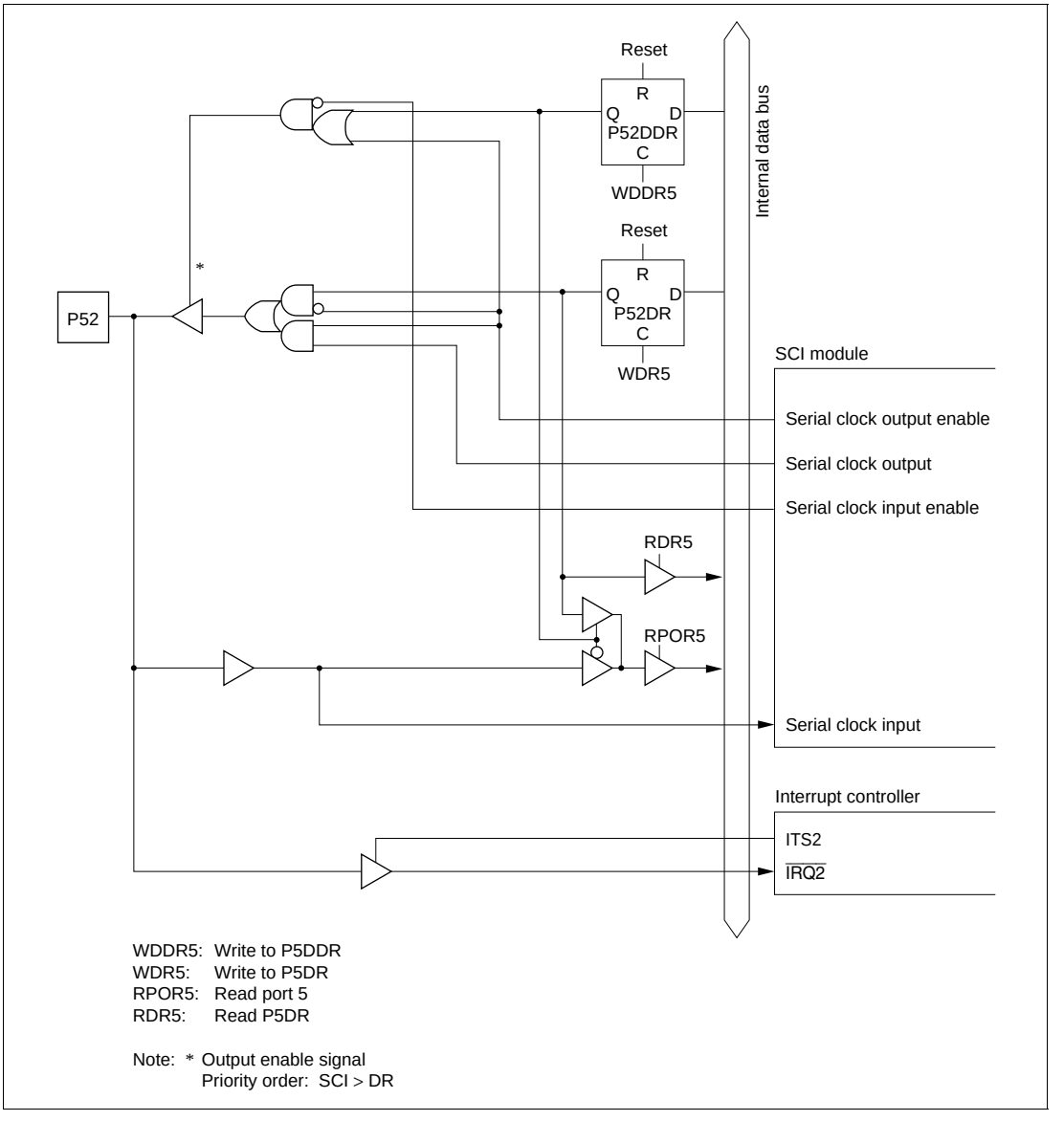


Figure 5.31 Port 5 Block Diagram (c) (Pin P52)

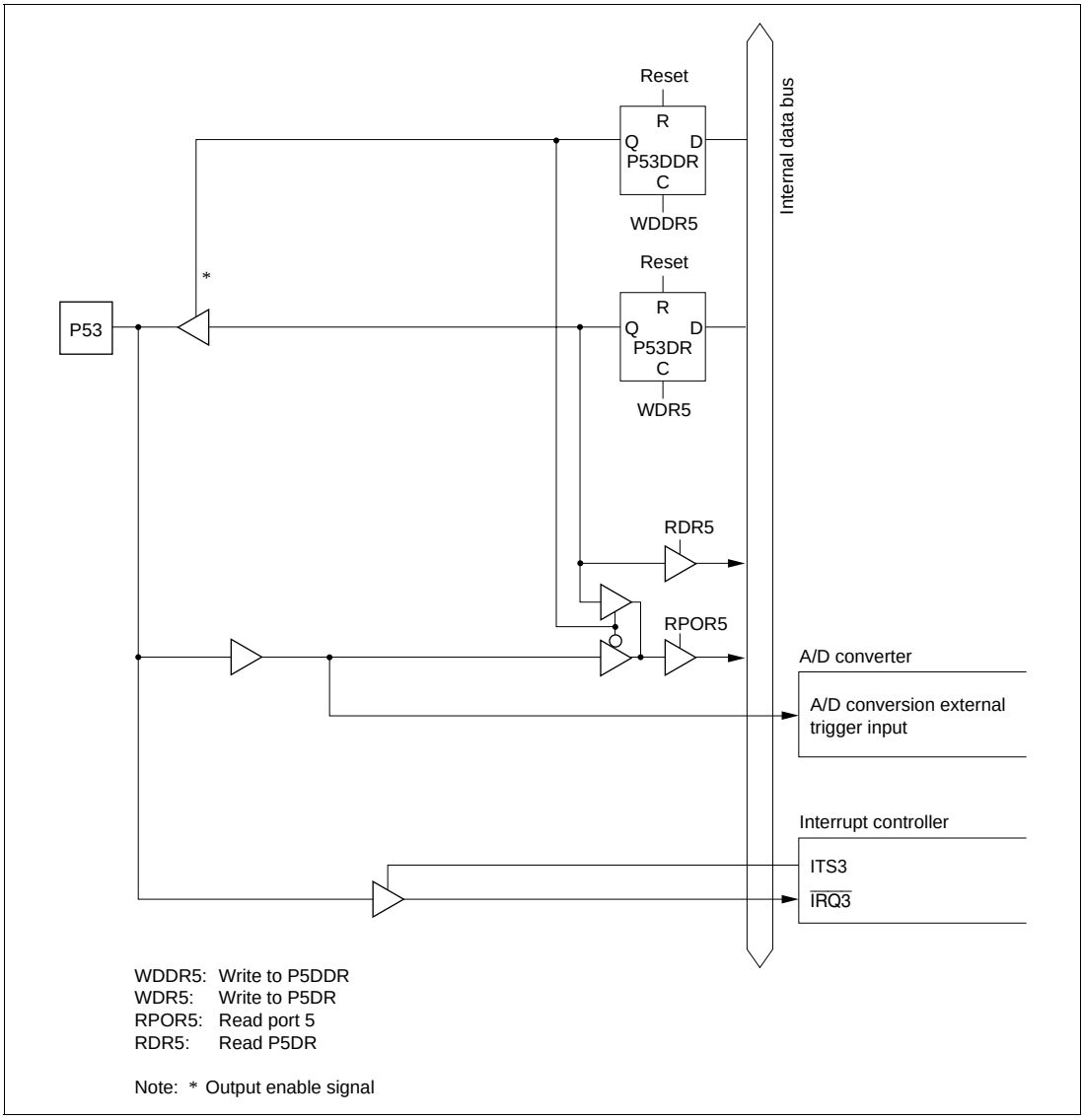


Figure 5.32 Port 5 Block Diagram (d) (Pin P53)

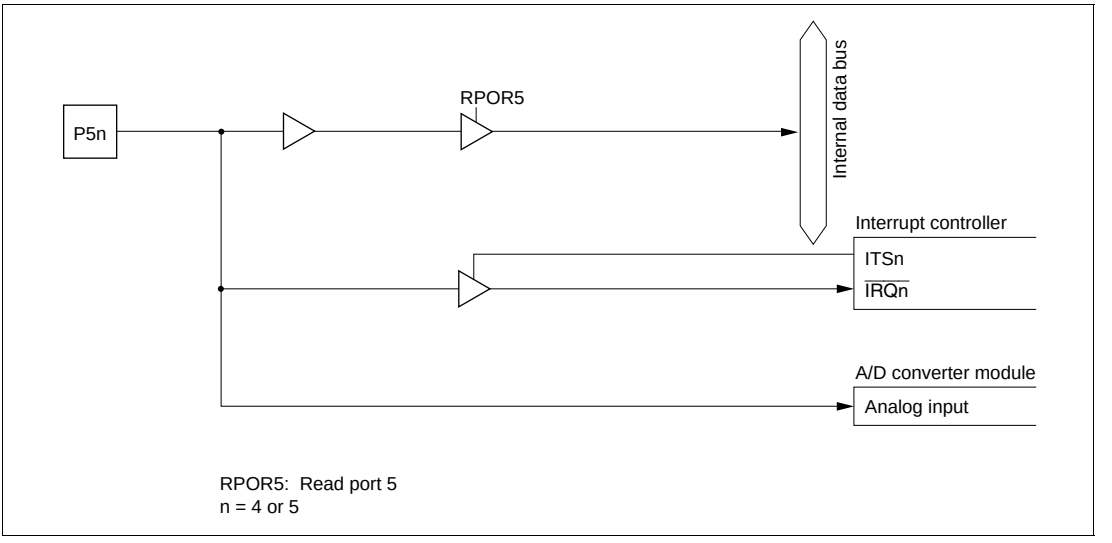


Figure 5.33 Port 5 Block Diagram (e) (Pins P54 and P55)

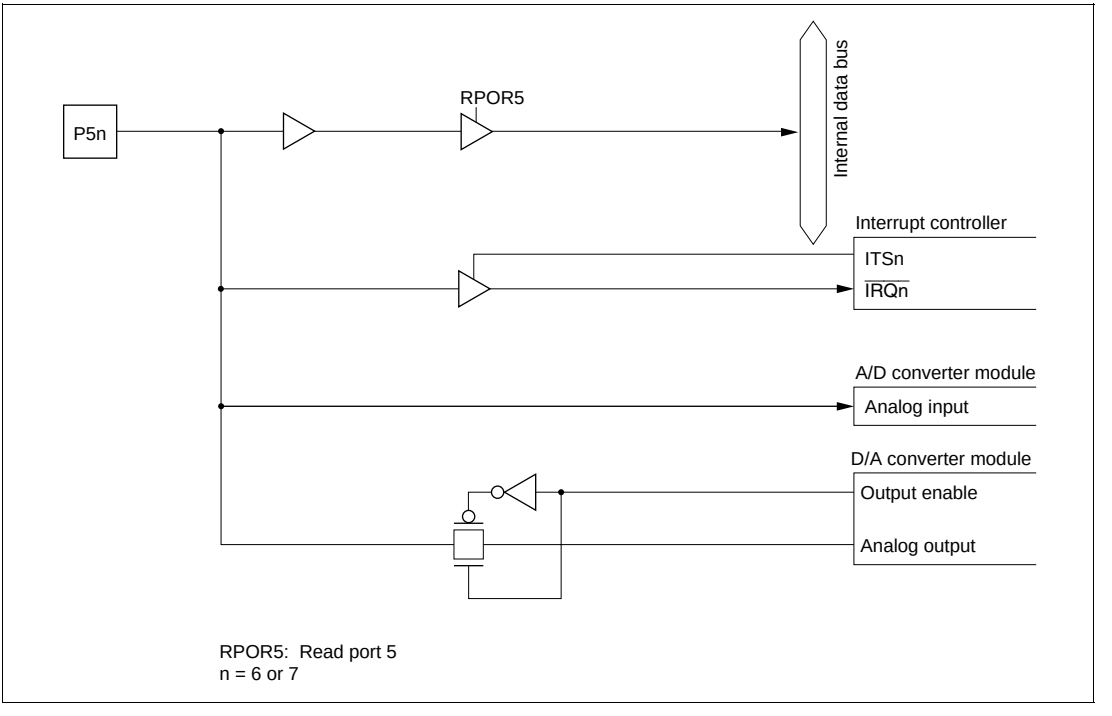


Figure 5.34 Port 5 Block Diagram (f) (Pins P56 and P57)

5.19.6 Port 6

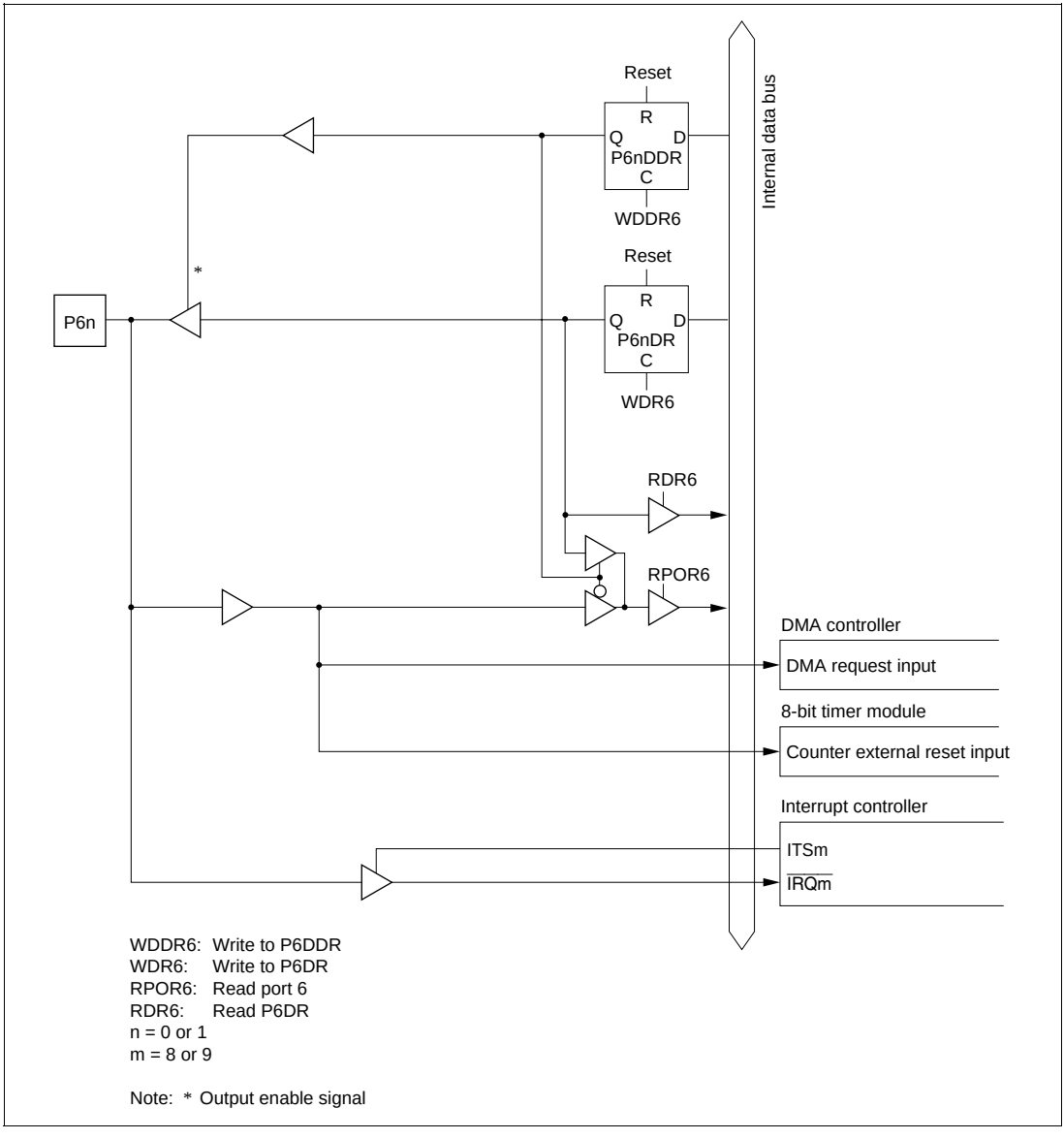


Figure 5.35 Port 6 Block Diagram (a) (Pins P60 and P61)

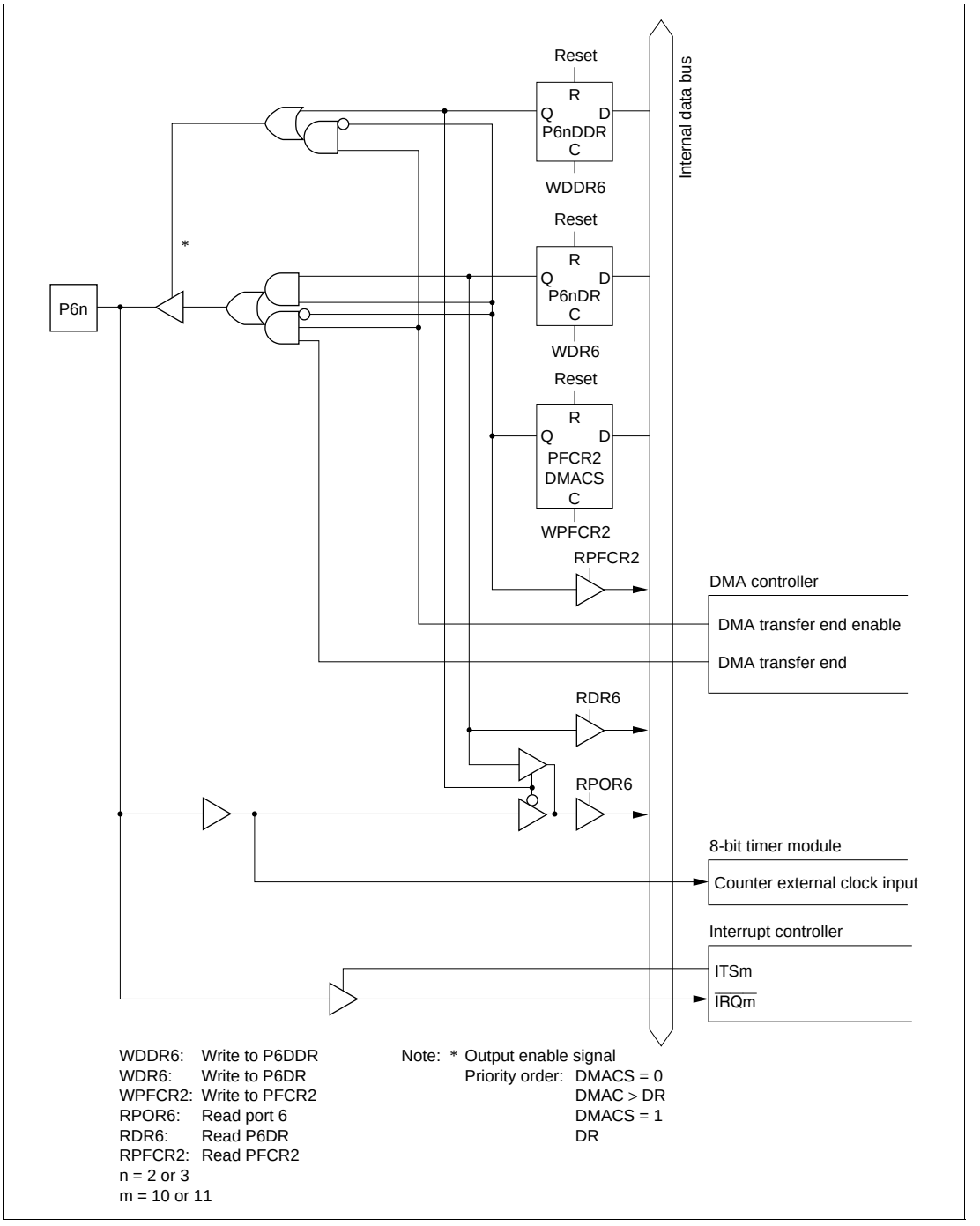


Figure 5.36 Port 6 Block Diagram (b) (Pins P62 and P63)

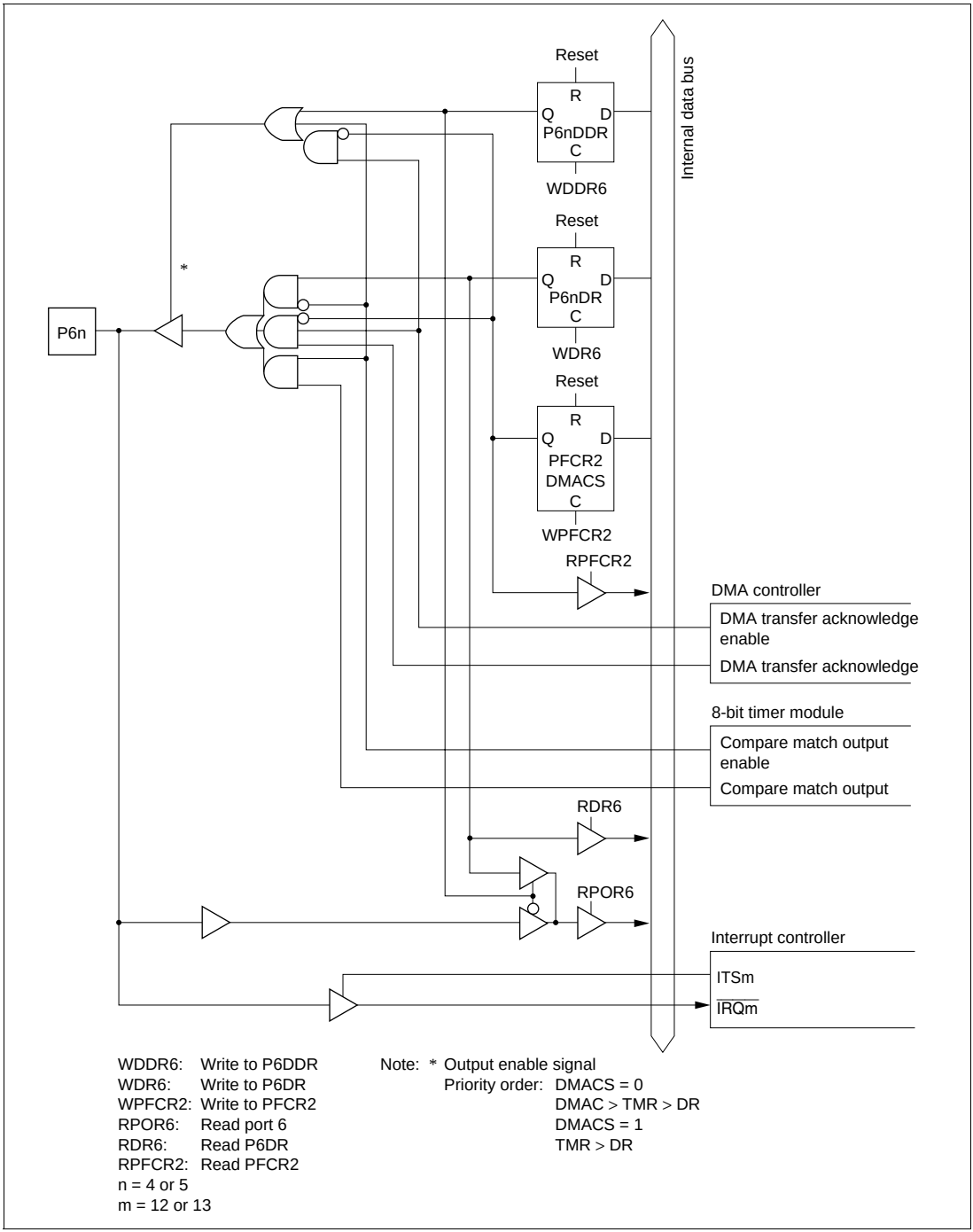


Figure 5.37 Port 6 Block Diagram (c) (Pins P64 and P65)

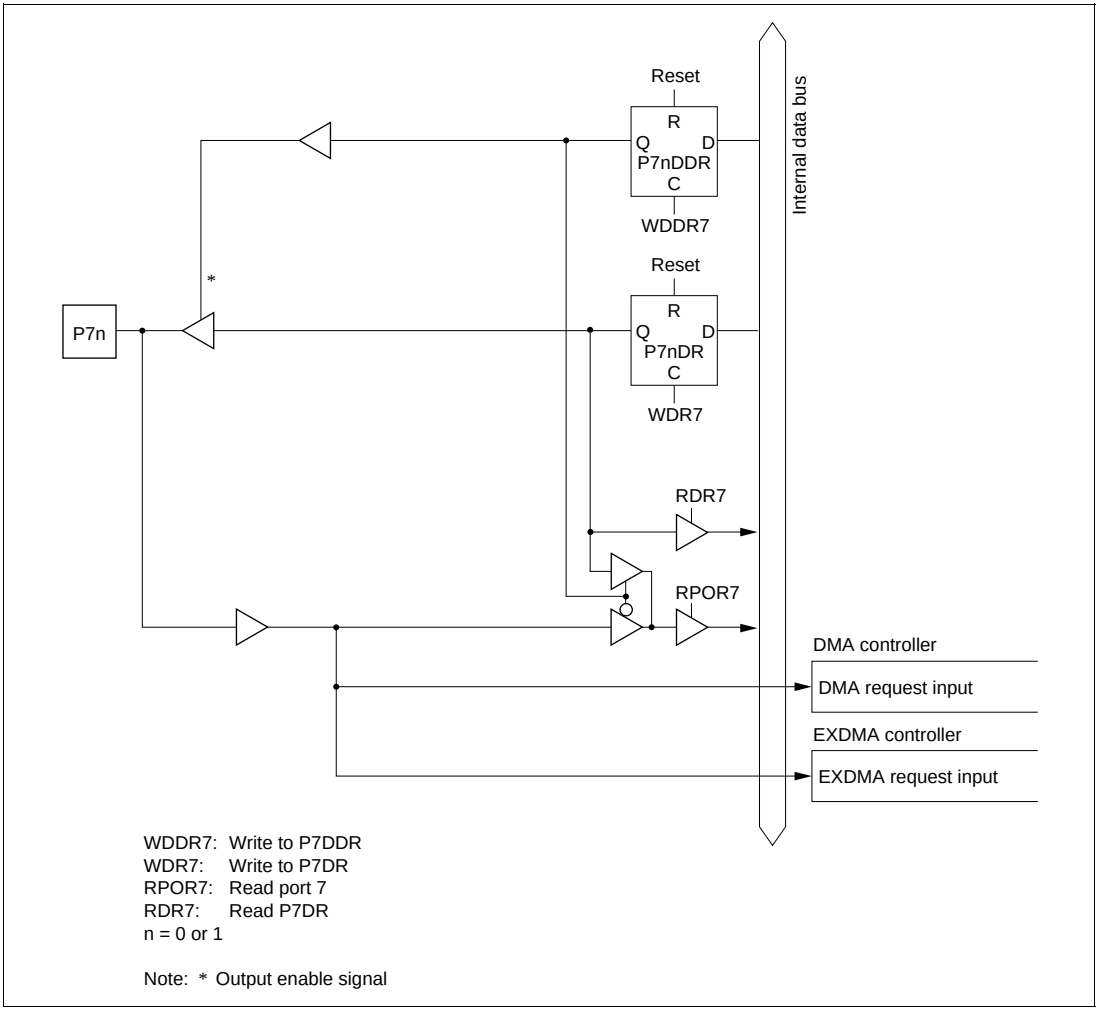
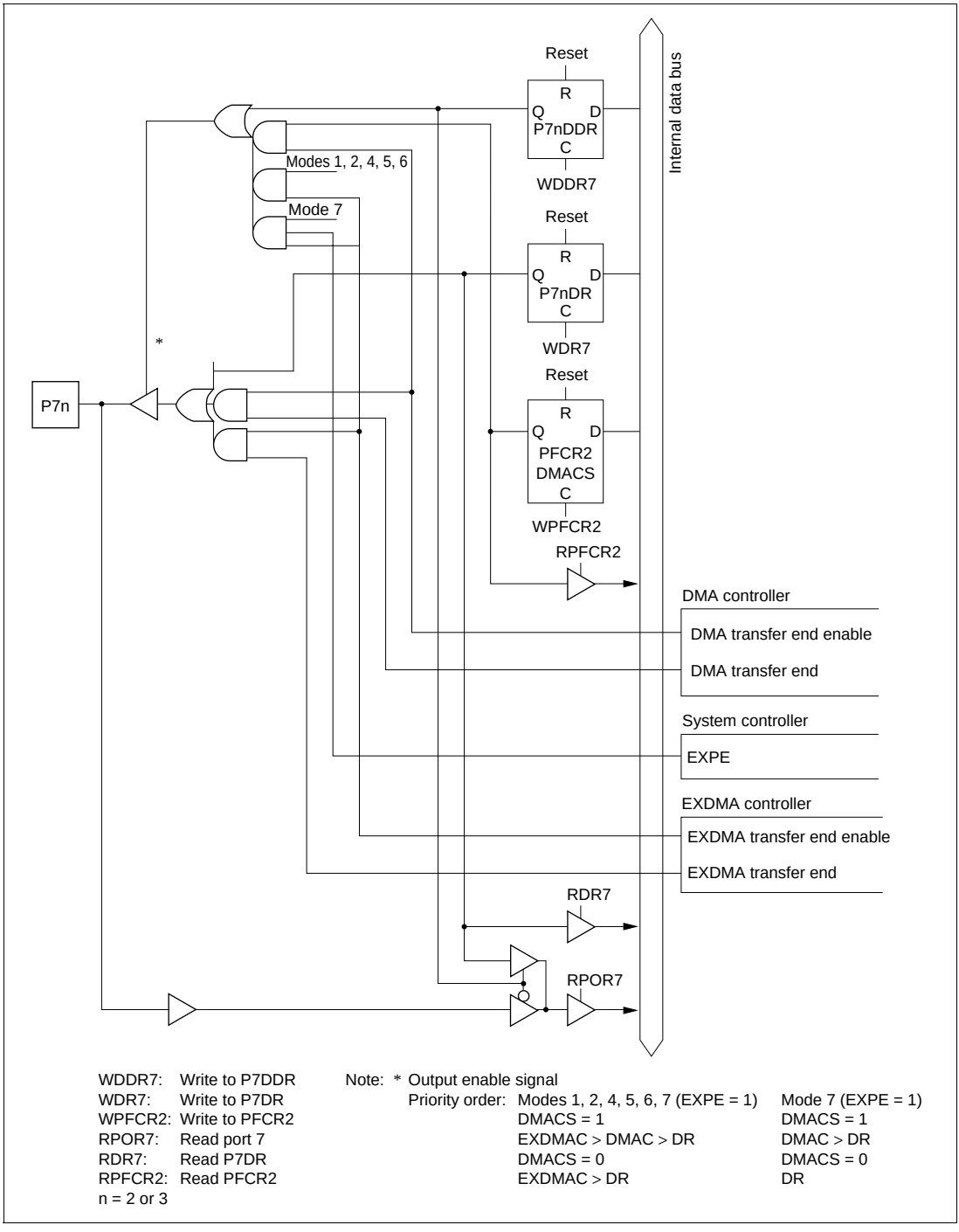


Figure 5.38 Port 7 Block Diagram (a) (Pins P70 and P71)

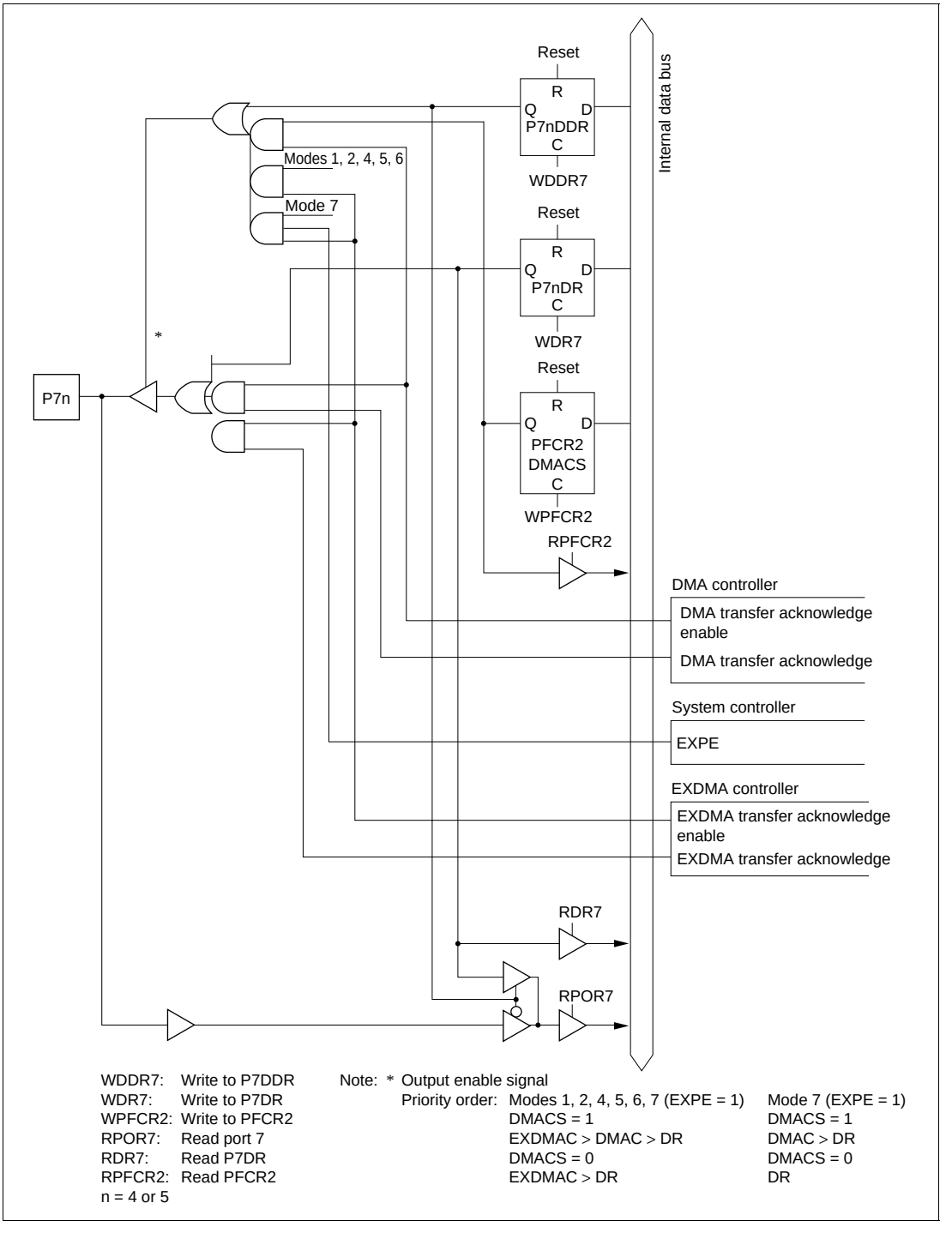


WDDR7: Write to P7DDR
WDR7: Write to P7DR
WPFCR2: Write to PFCR2
RPOR7: Read port 7
RDR7: Read P7DR
RPFCR2: Read PFCR2
n = 2 or 3

Note: * Output enable signal

Priority order:	Modes 1, 2, 4, 5, 6, 7 (EXPE = 1)	Mode 7 (EXPE = 1)
	DMACS = 1	DMACS = 1
	EXDMAC > DMAC > DR	DMAC > DR
	DMACS = 0	DMACS = 0
	EXDMAC > DR	DR

Figure 5.39 Port 7 Block Diagram (b) (Pins P72 and P73)



WDDR7: Write to P7DDR
WDR7: Write to P7DR
WPFCR2: Write to PFCR2
RPOR7: Read port 7
RDR7: Read P7DR
RPFCR2: Read PFCR2
n = 4 or 5

Note: * Output enable signal

Priority order:

Modes 1, 2, 4, 5, 6, 7 (EXPE = 1)	Mode 7 (EXPE = 1)
DMACS = 1	DMACS = 1
EXDMAC > DMAC > DR	DMAC > DR
DMACS = 0	DMACS = 0
EXDMAC > DR	DR

Figure 5.40 Port 7 Block Diagram (c) (Pins P74 and P75)

5.19.8 Port 8

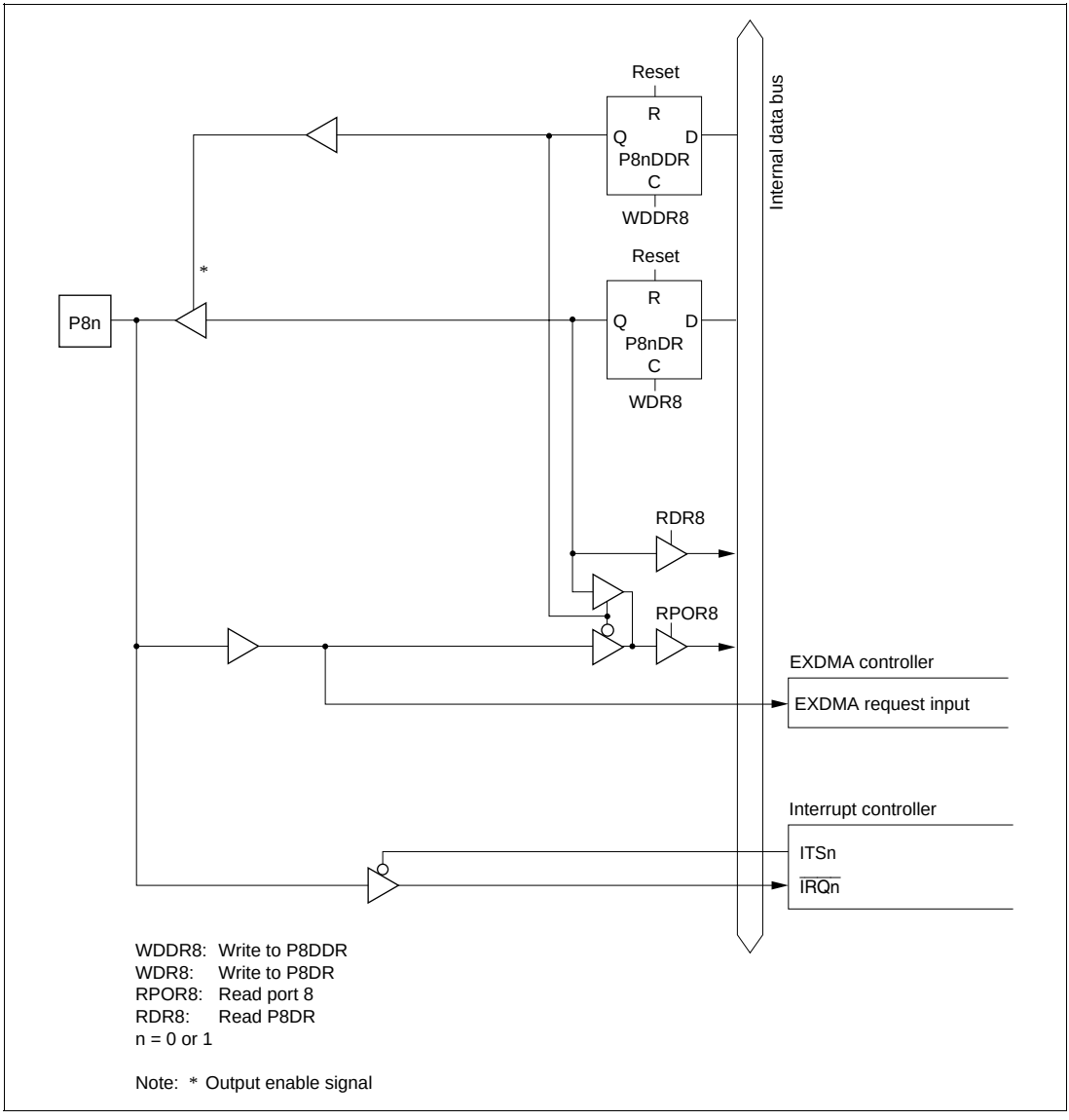


Figure 5.41 Port 8 Block Diagram (a) (Pins P80 and P81)

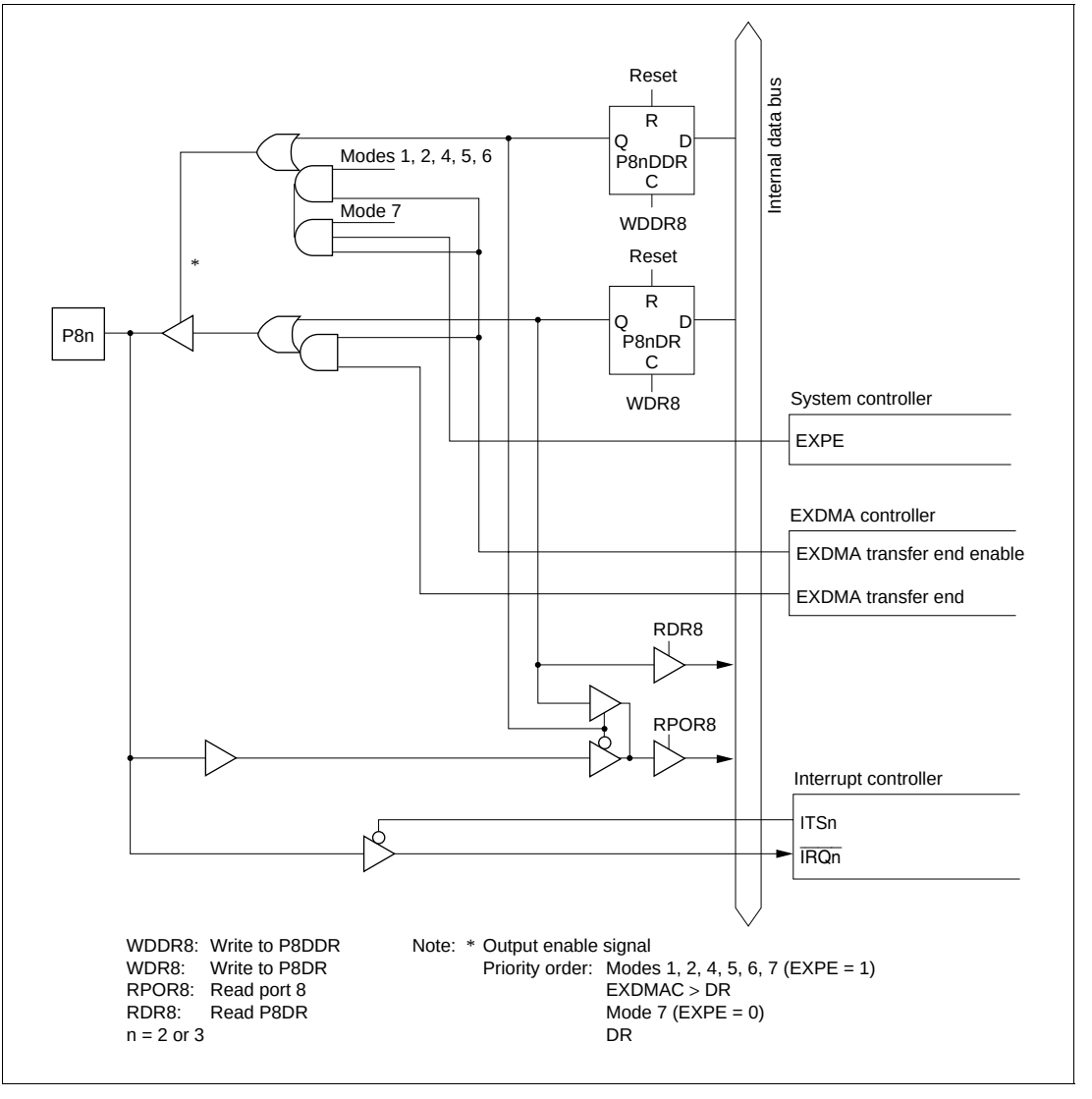


Figure 5.42 Port 8 Block Diagram (b) (Pins P82 and P83)

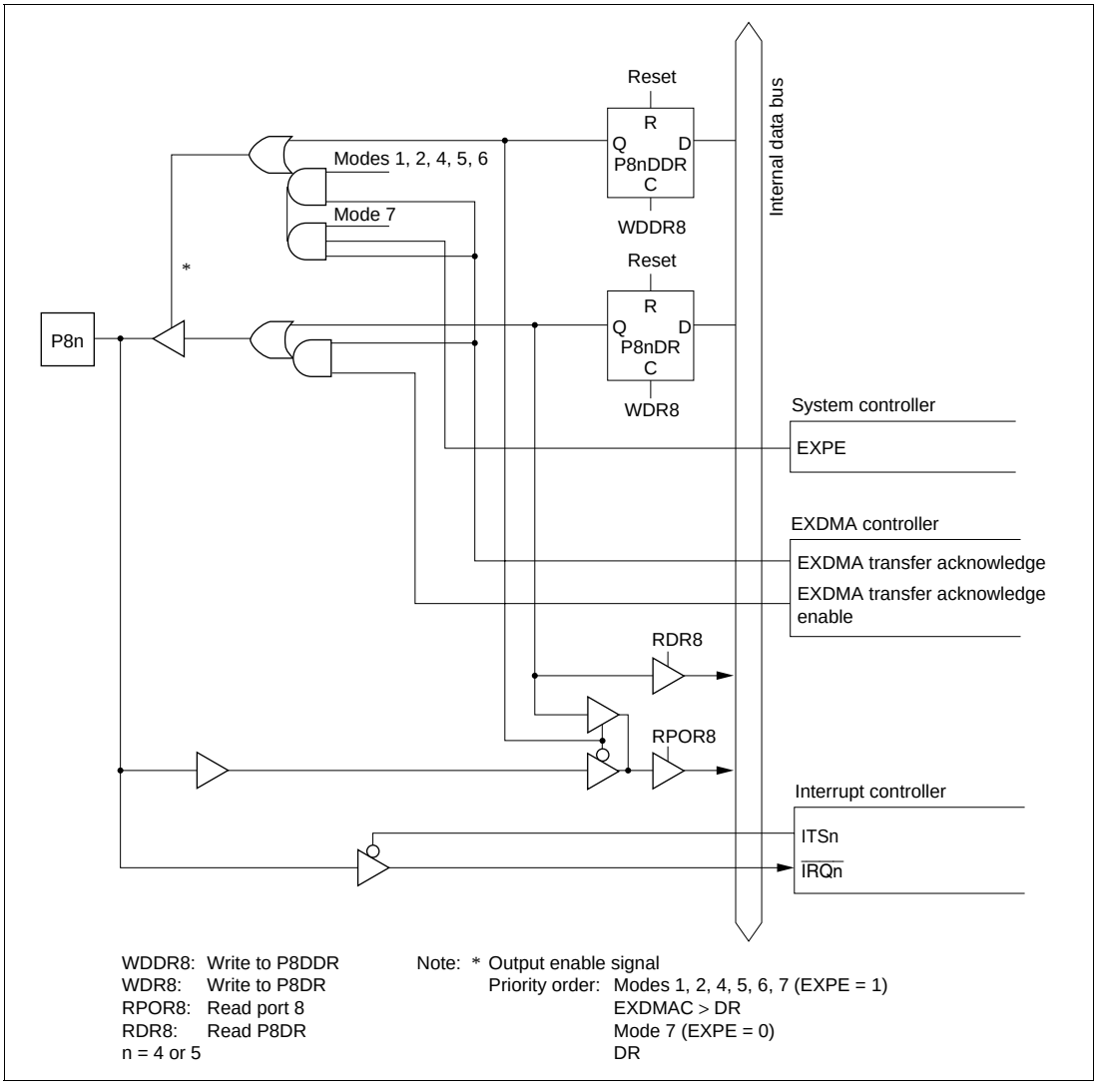
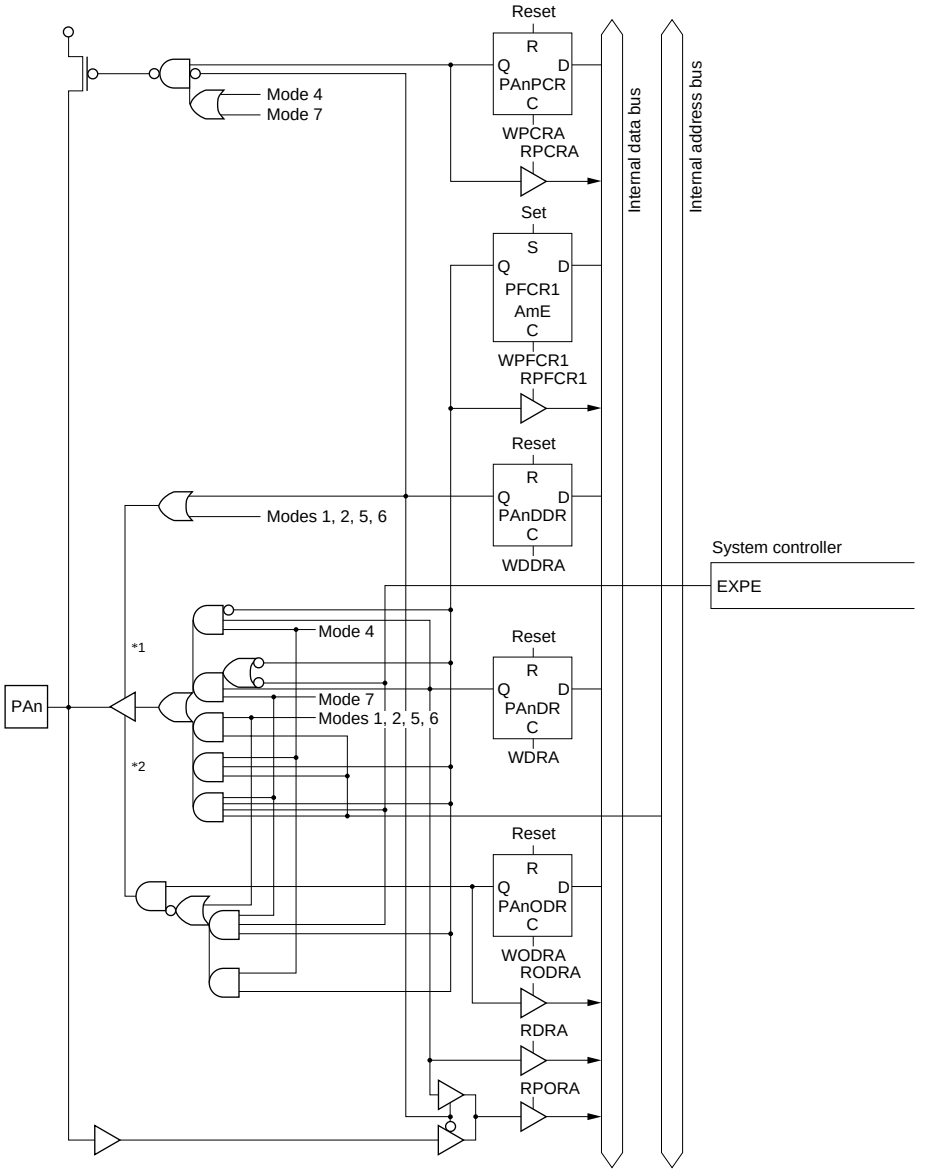


Figure 5.43 Port 8 Block Diagram (c) (Pins P84 and P85)

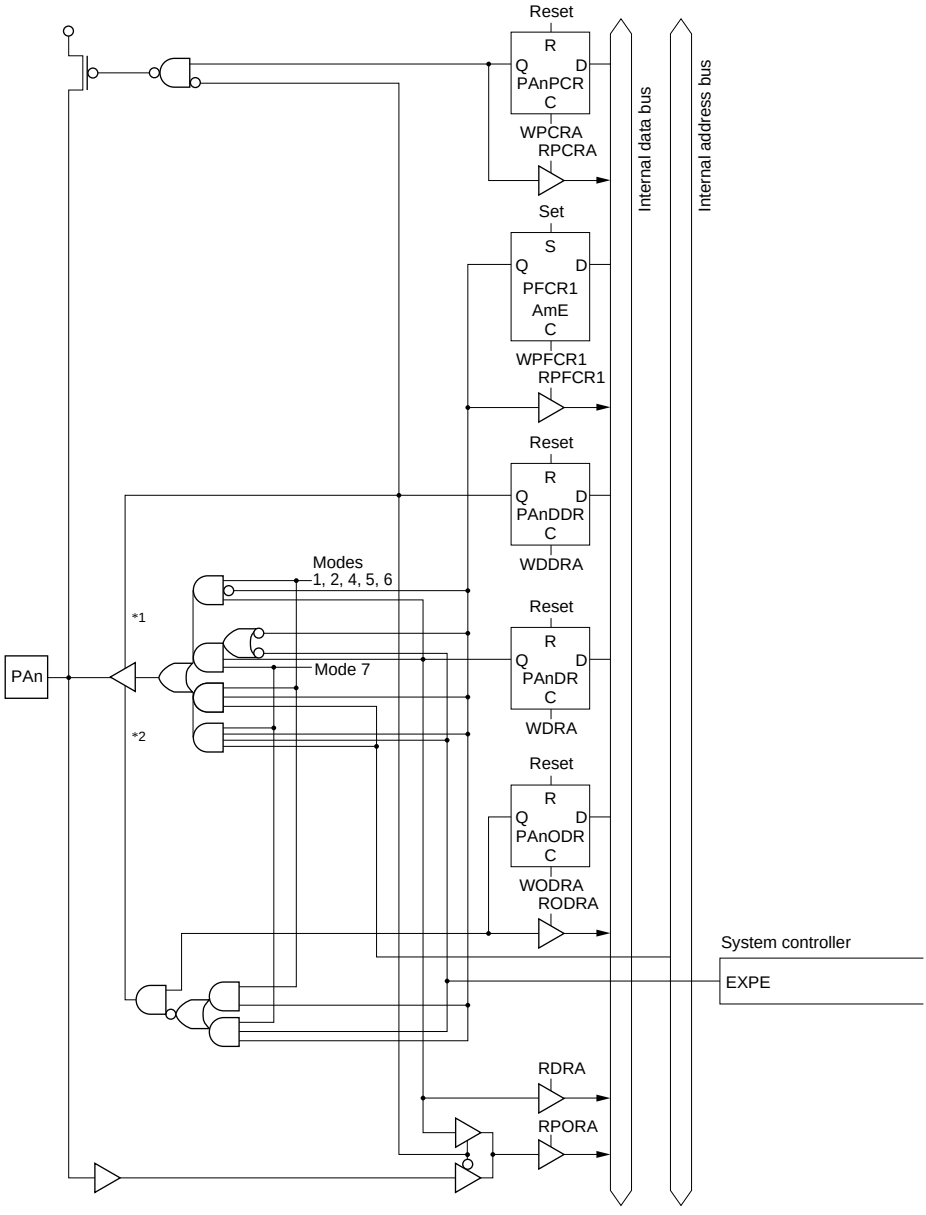


WDDRA: Write to PADDR
WDRA: Write to PADR
WODRA: Write to PAODR
WPCRA: Write to PAPCR
WPFCR1: Write to PFCR1
n = 0, 1, 2, 3, 4
m = 16, 17, 18, 19, 20

RPORA: Read port A
RDRA: Read PADR
RODRA: Read PAODR
RPCRA: Read PAPCR
RPFCR1: Read PFCR1

Notes: 1. Output enable signal
2. Open drain control signal

Figure 5.44 Port A Block Diagram (a) (Pins PA0 to PA4)

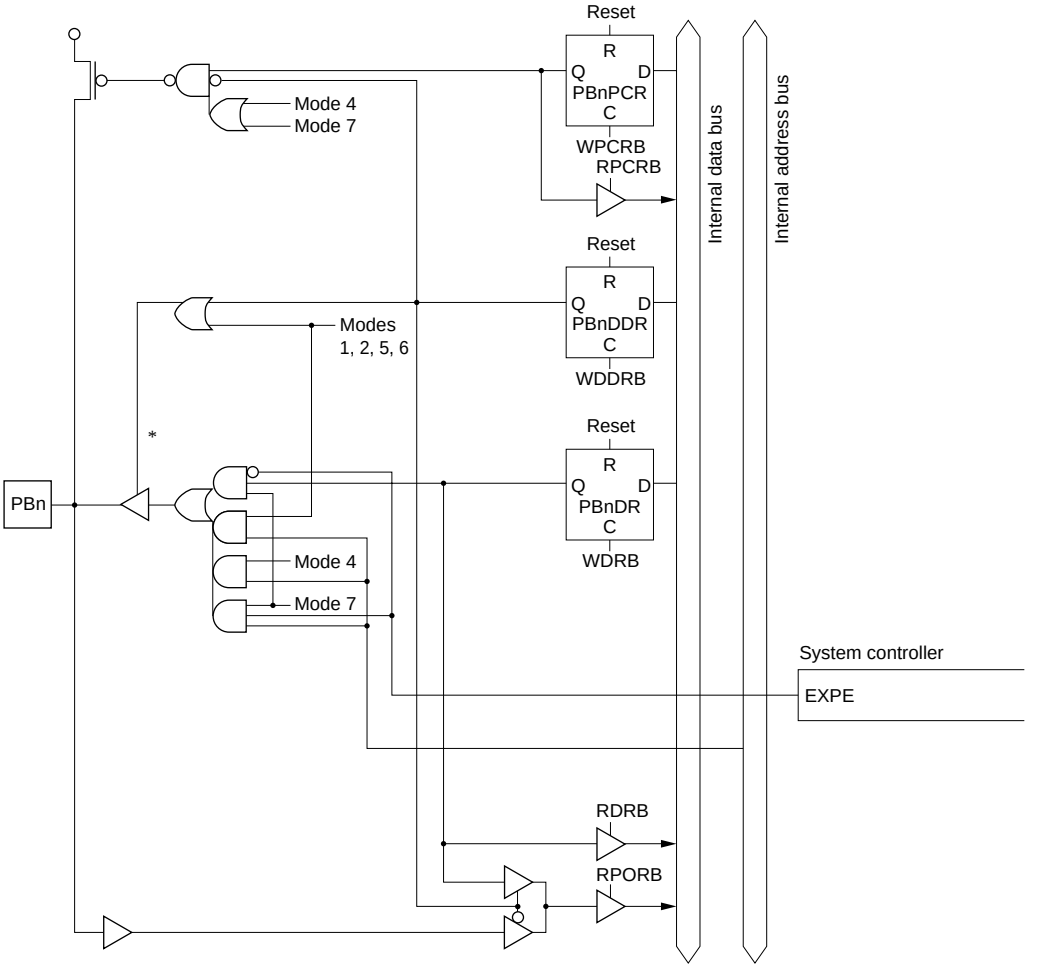


WDDRA: Write to PADDR
WDRA: Write to PADR
WODRA: Write to PAODR
WPCRA: Write to PAPCR
WPFCR1: Write to PFCR1
n = 5, 6, 7
m = 21, 22, 23

RPORA: Read port A
RDRA: Read PADR
RODRA: Read PAODR
RPCRA: Read PAPCR
RPFCR1: Read PFCR1

Notes: 1. Output enable signal
2. Open drain control signal

Figure 5.45 Port A Block Diagram (b) (Pins PA5 to PA7)

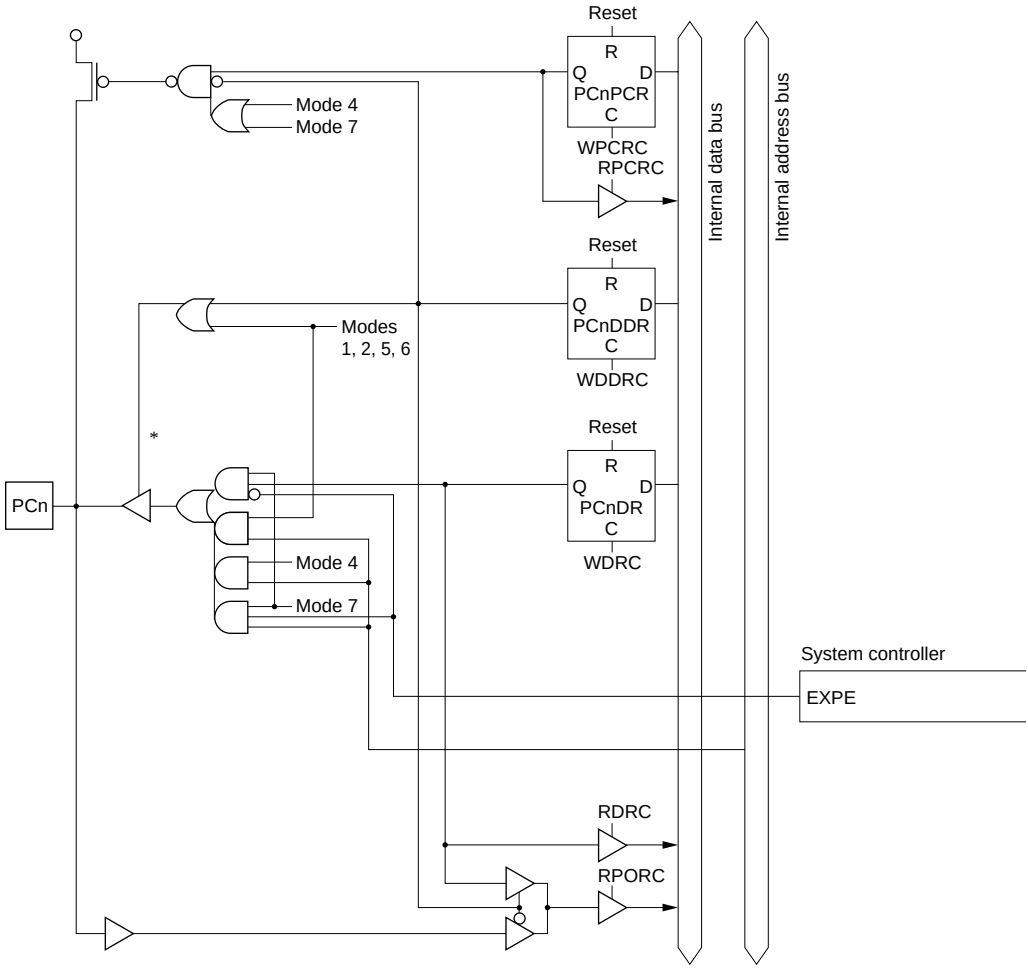


WDDRB: Write to PBDDR
WDRB: Write to PBDR
WPCRB: Write to PBPCR
RPORB: Read port B
RDRB: Read PBDR
RPCRB: Read PBPCR
n = 0 to 7

Note: * Output enable signal

Figure 5.46 Port B Block Diagram (Pins PBn)

5.19.11 Port C



WDDRC: Write to PCDDR
WDRC: Write to PCDR
WPCRC: Write to PCPCR
RPORC: Read port C
RDRC: Read PCDR
RPCRC: Read PCPCR
n = 0 to 7

Note: * Output enable signal

Figure 5.47 Port C Block Diagram (Pins PCn)

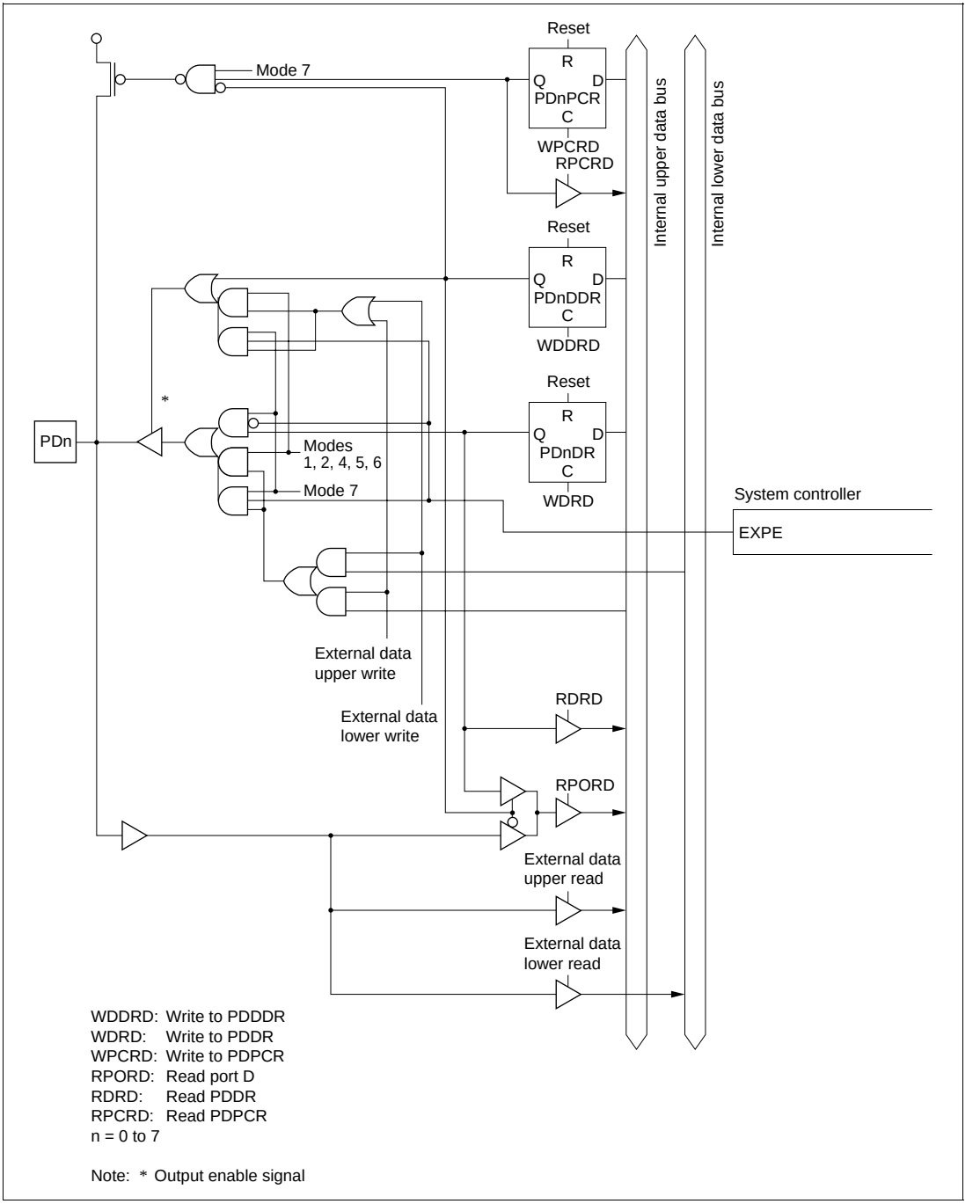


Figure 5.48 Port D Block Diagram (Pins PDn)

5.19.13 Port E

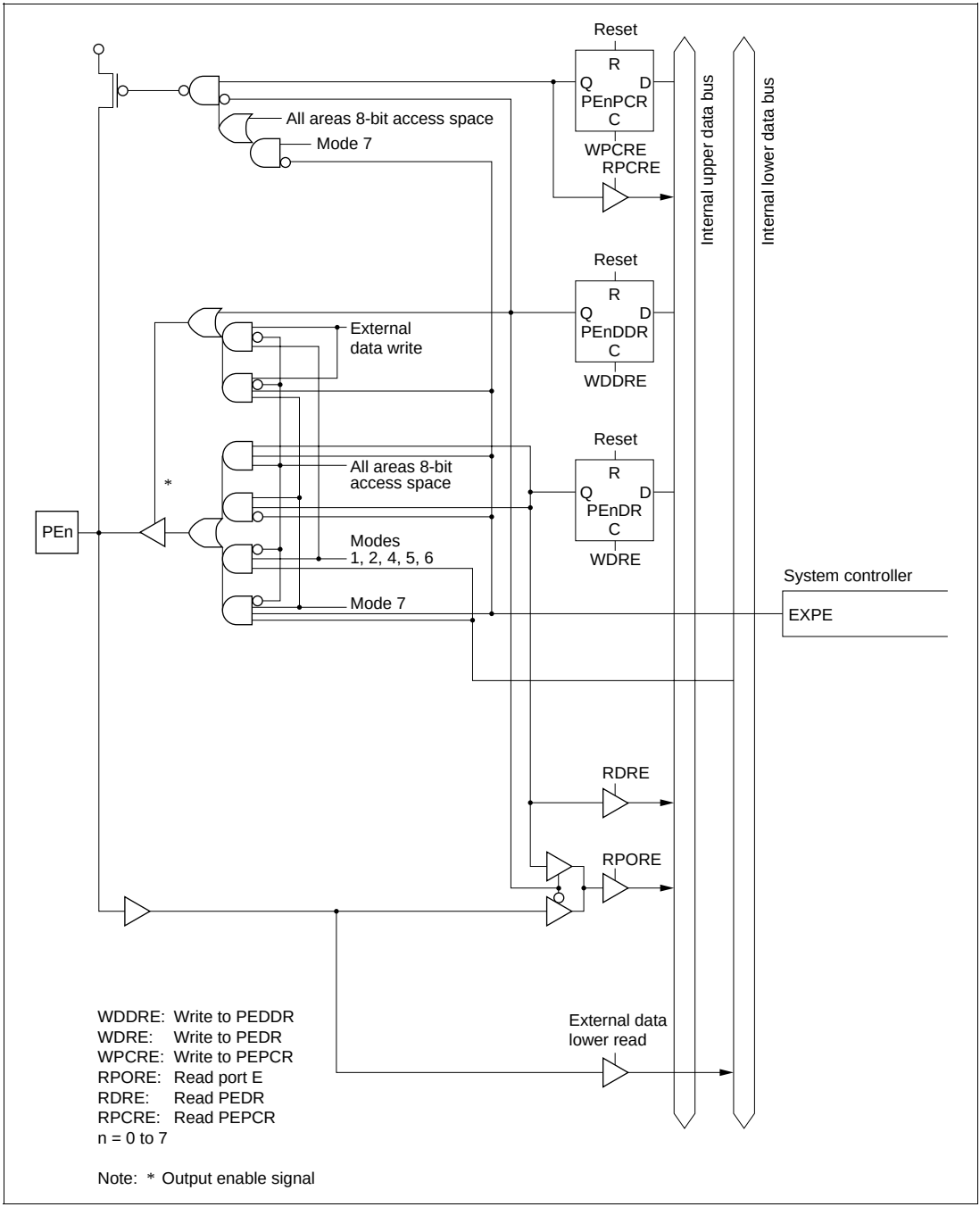


Figure 5.49 Port E Block Diagram (Pins PEn)

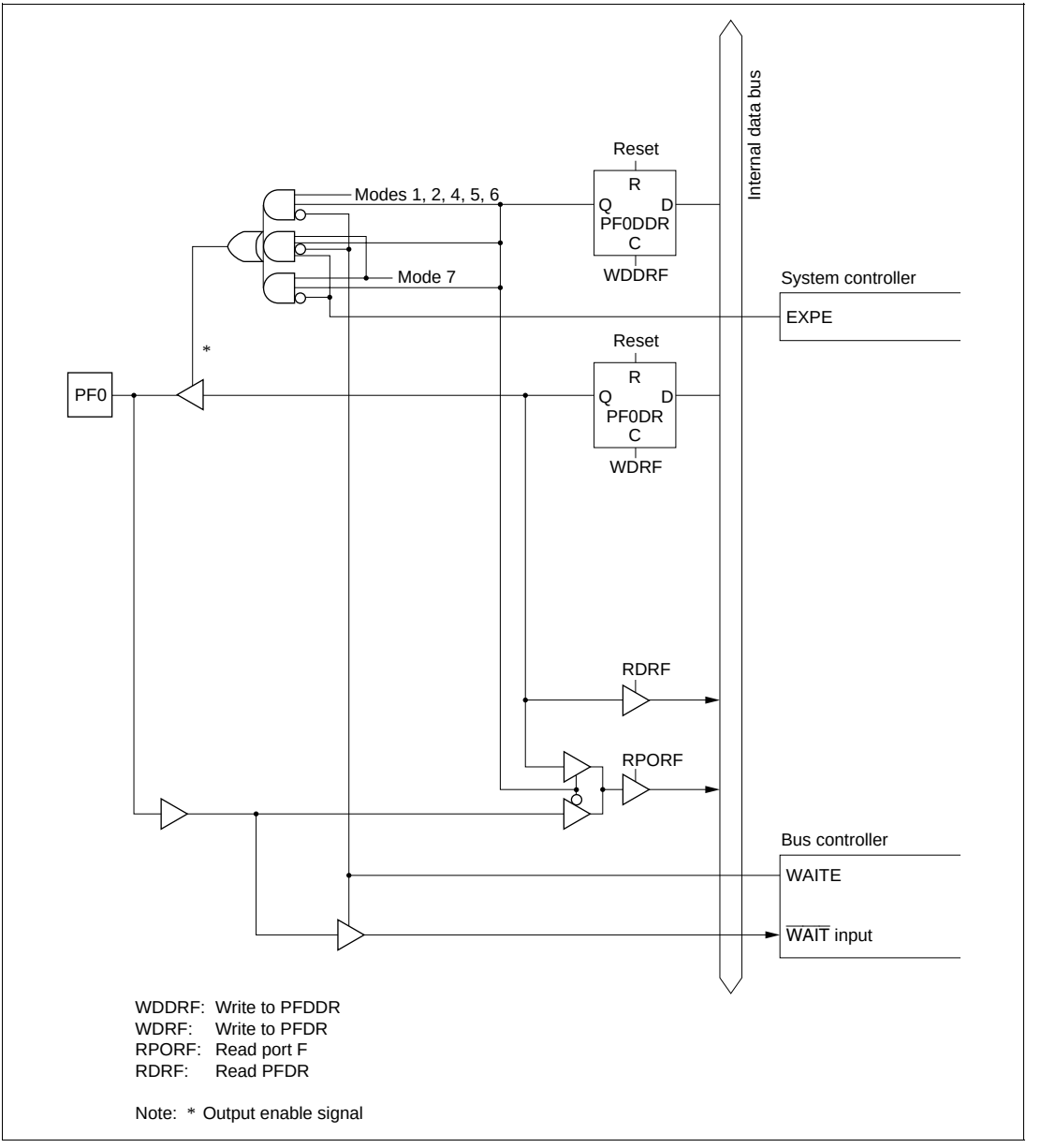


Figure 5.50 Port F Block Diagram (a) (Pin PF0)

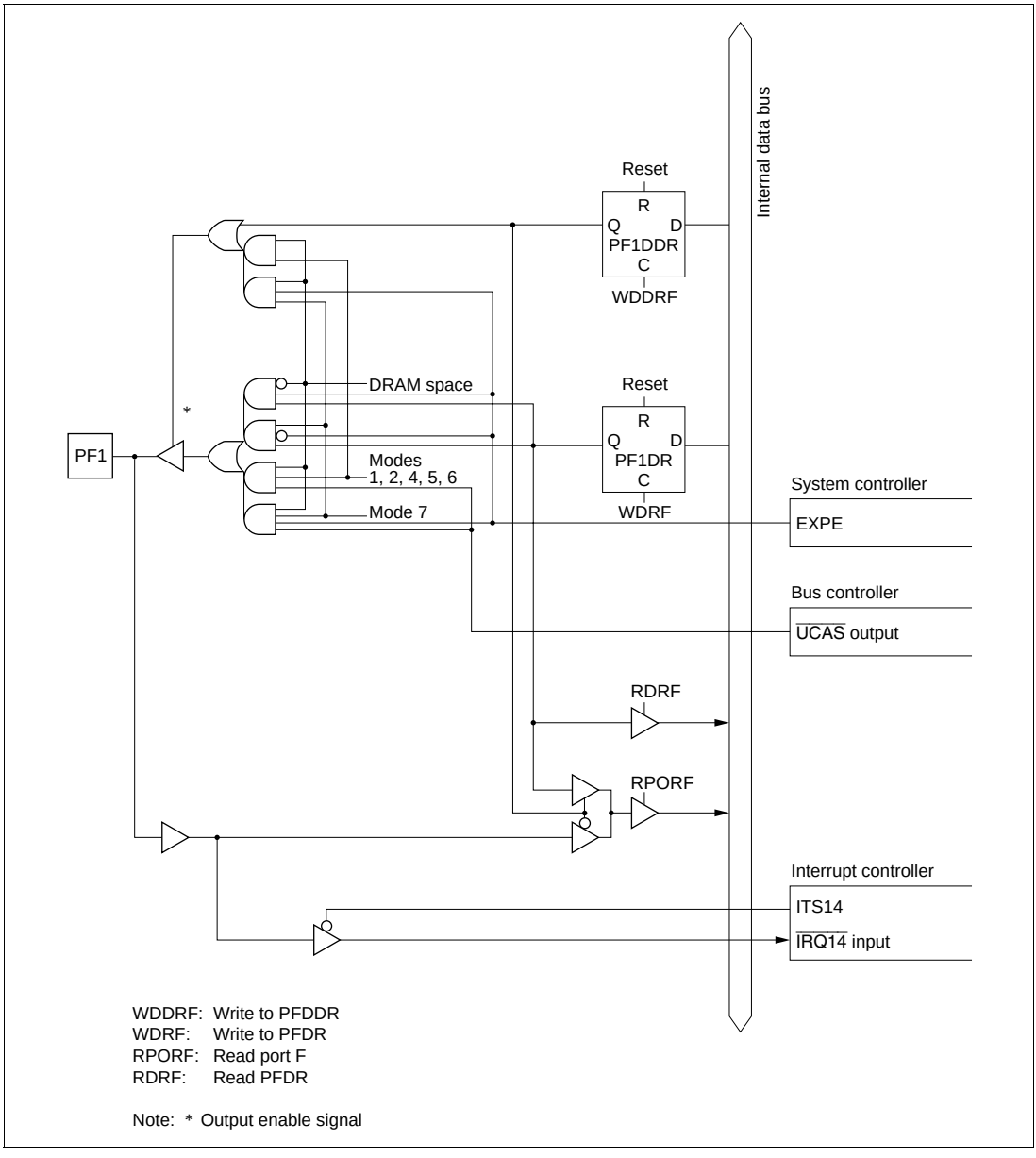


Figure 5.51 Port F Block Diagram (b) (Pin PF1)

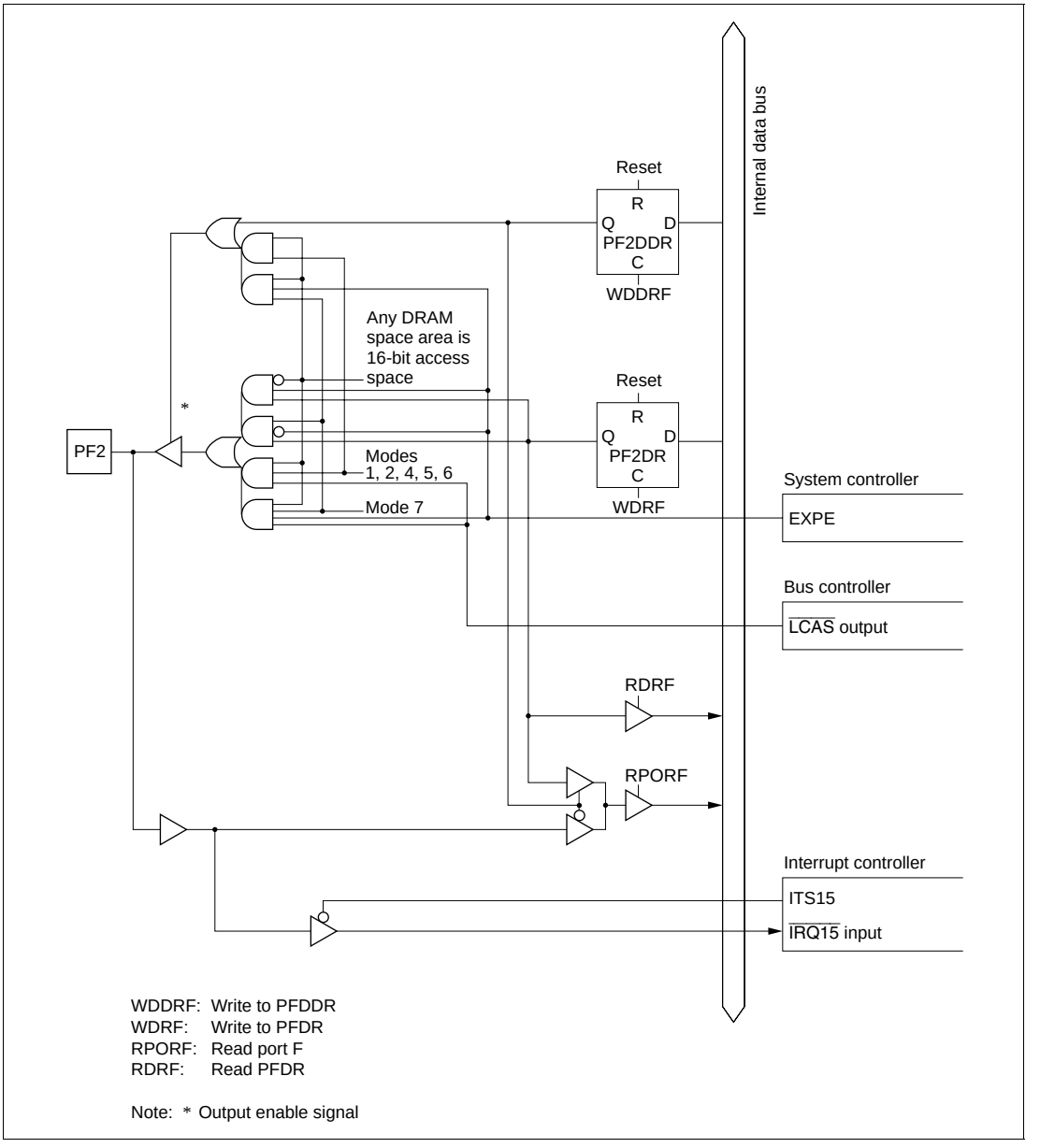


Figure 5.52 Port F Block Diagram (c) (Pin PF2)

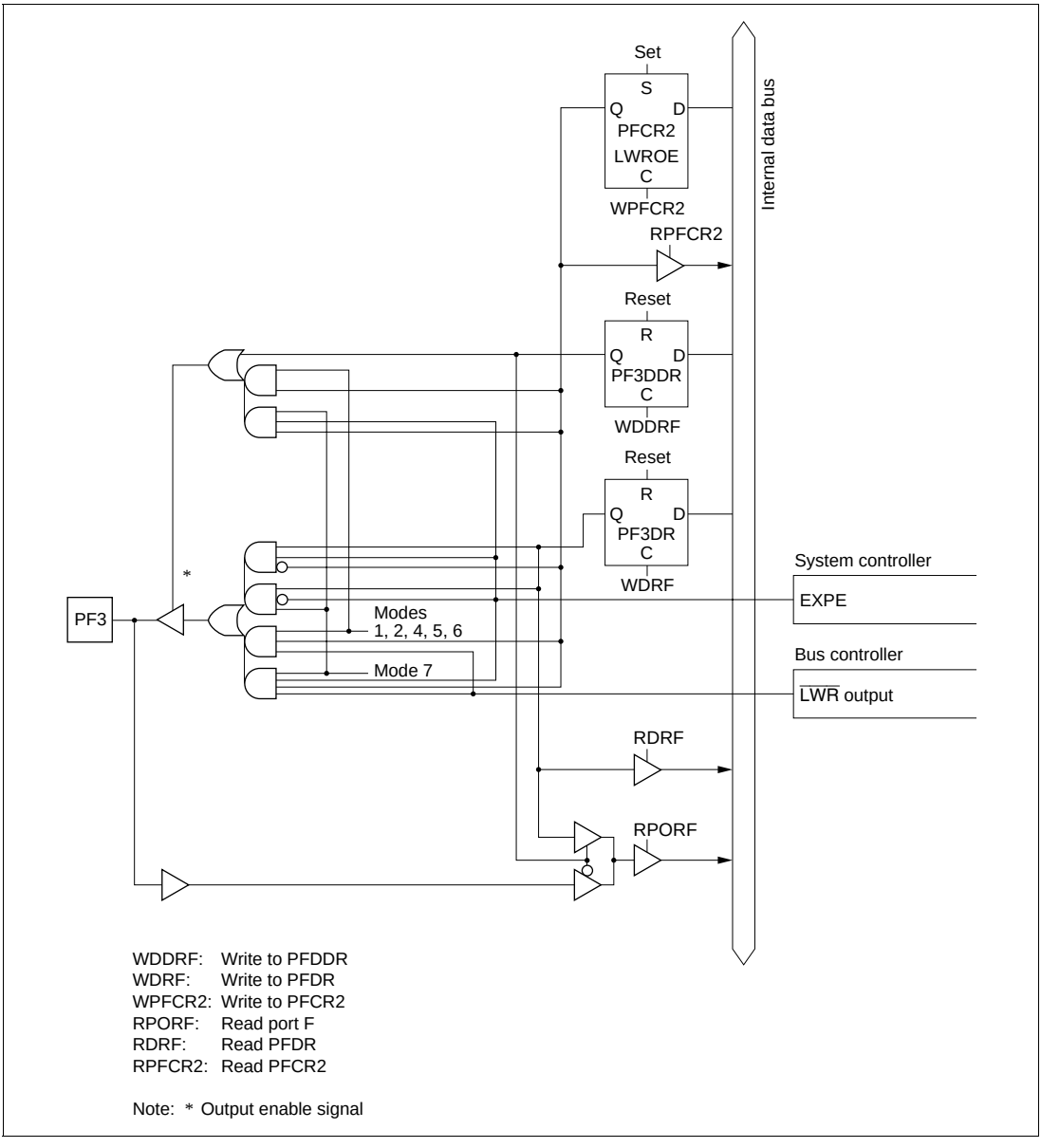


Figure 5.53 Port F Block Diagram (d) (Pin PF3)

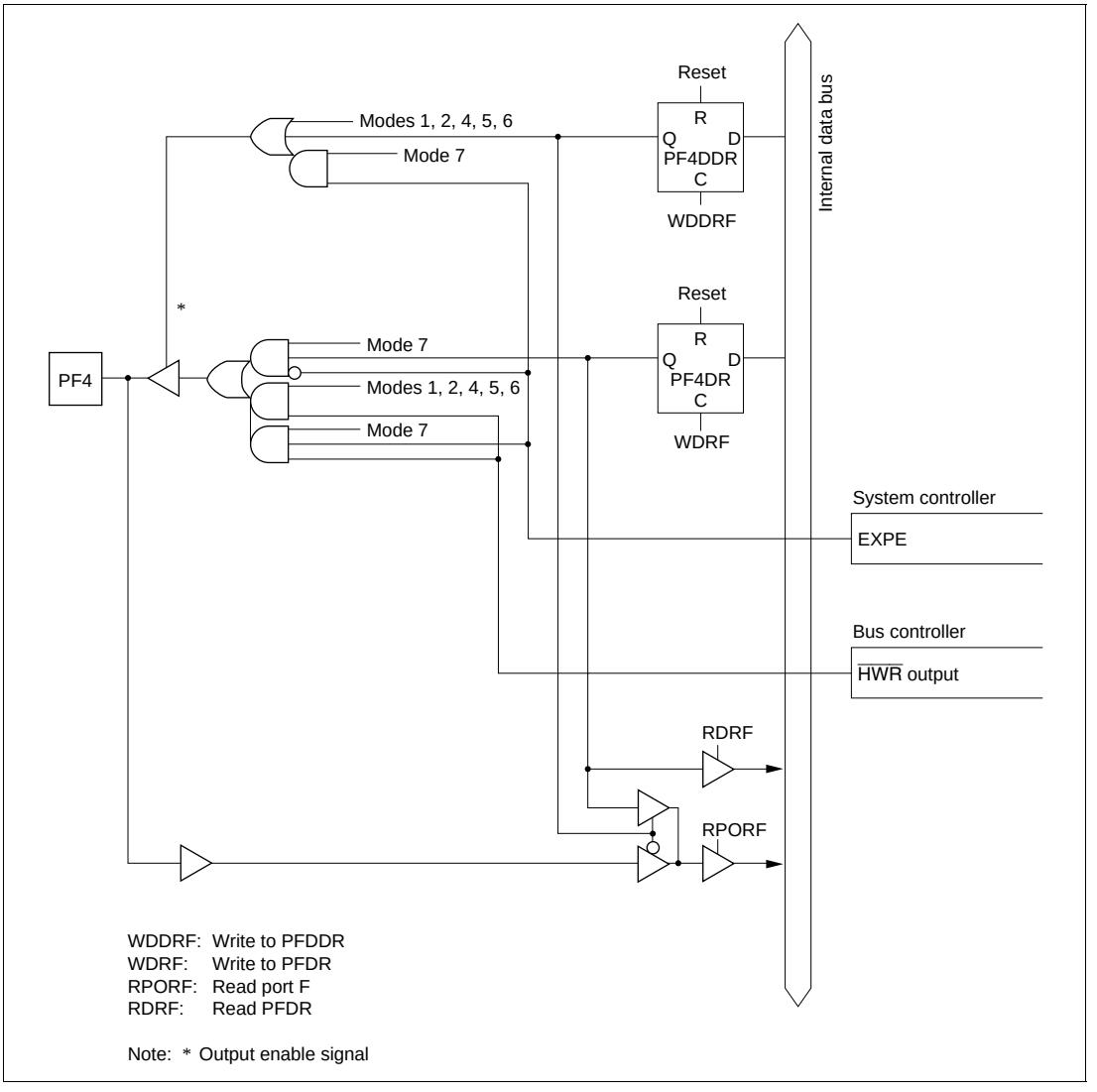


Figure 5.54 Port F Block Diagram (e) (Pin PF4)

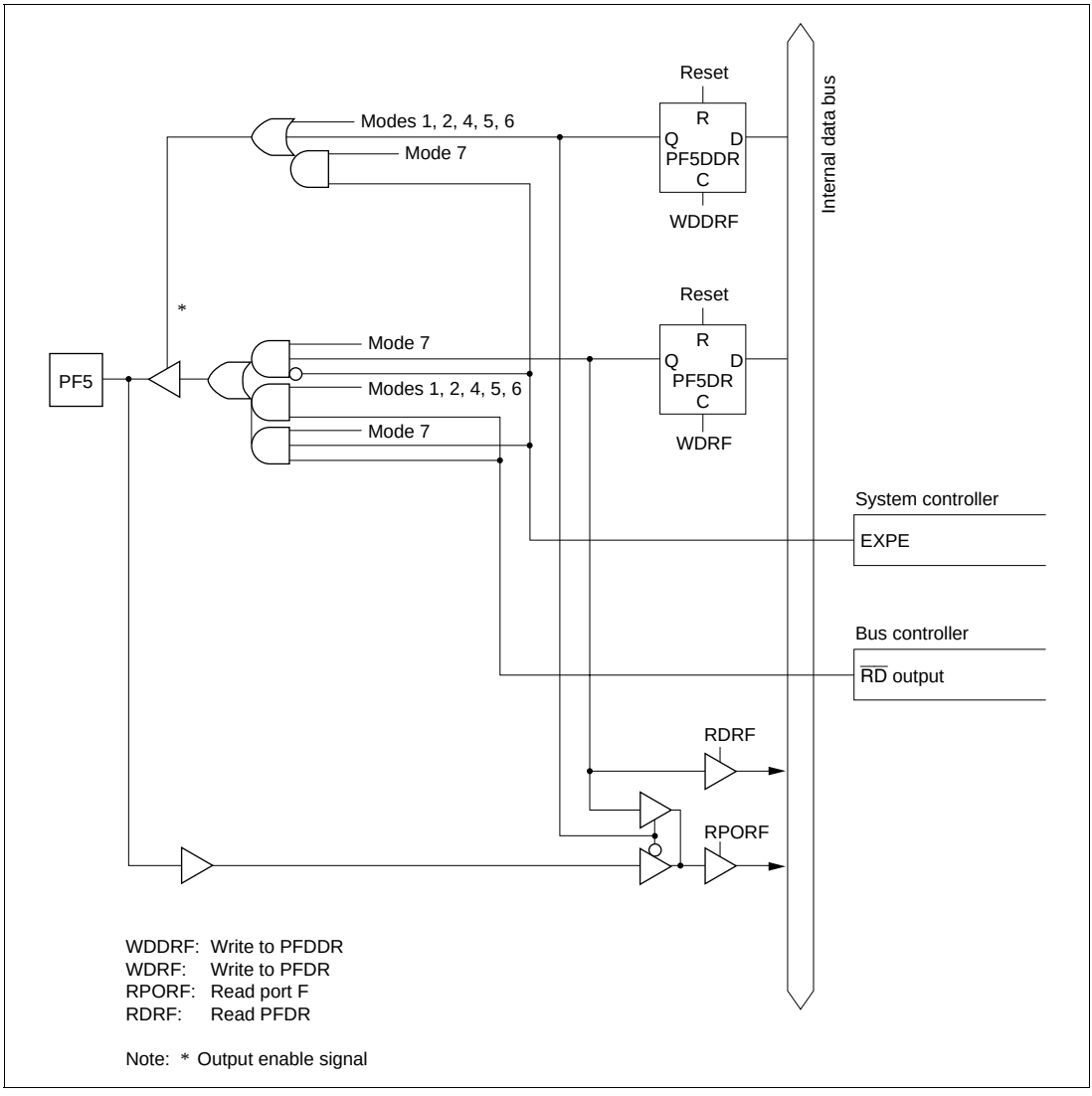


Figure 5.55 Port F Block Diagram (f) (Pin PF5)

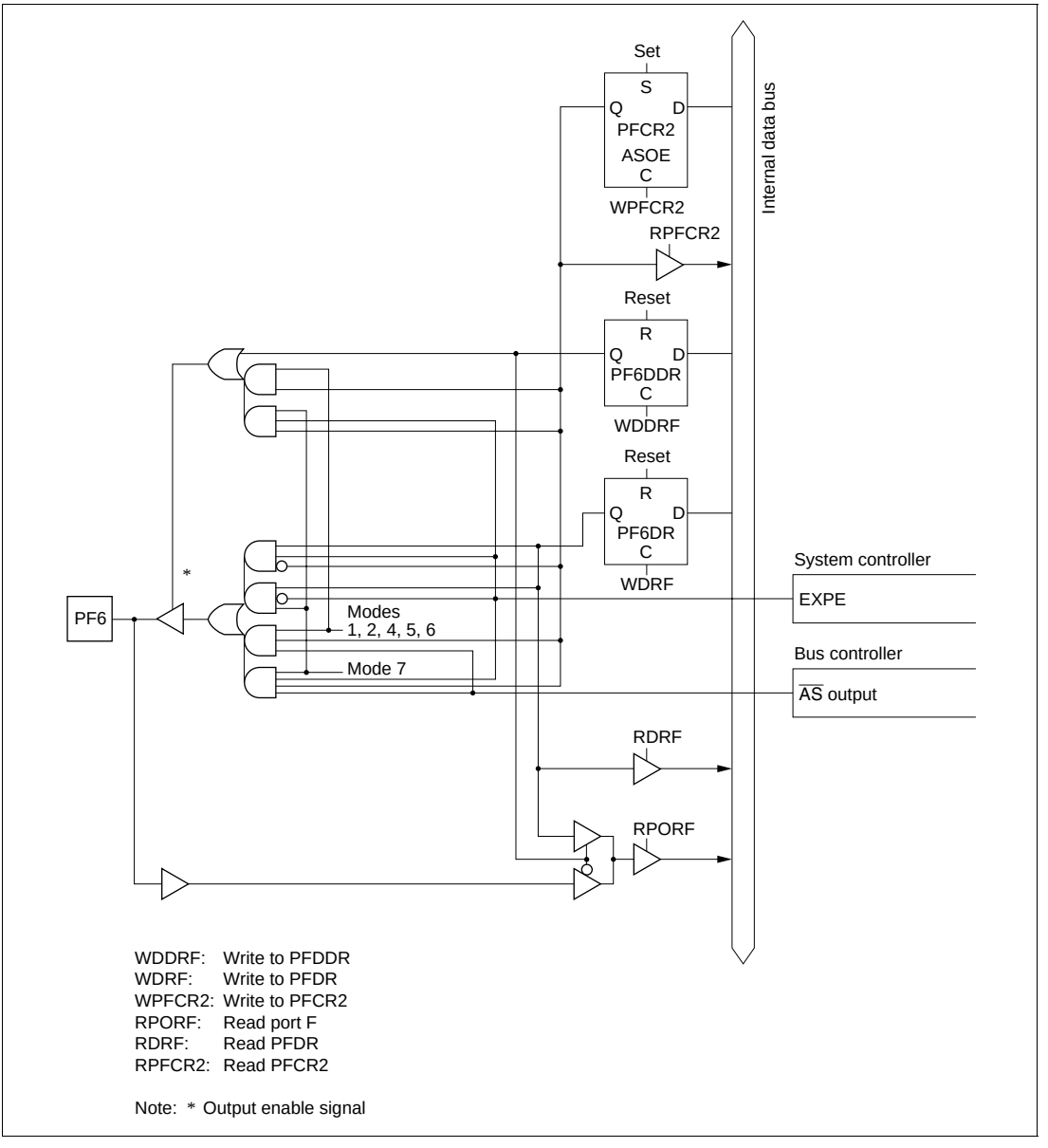


Figure 5.56 Port F Block Diagram (g) (Pin PF6)

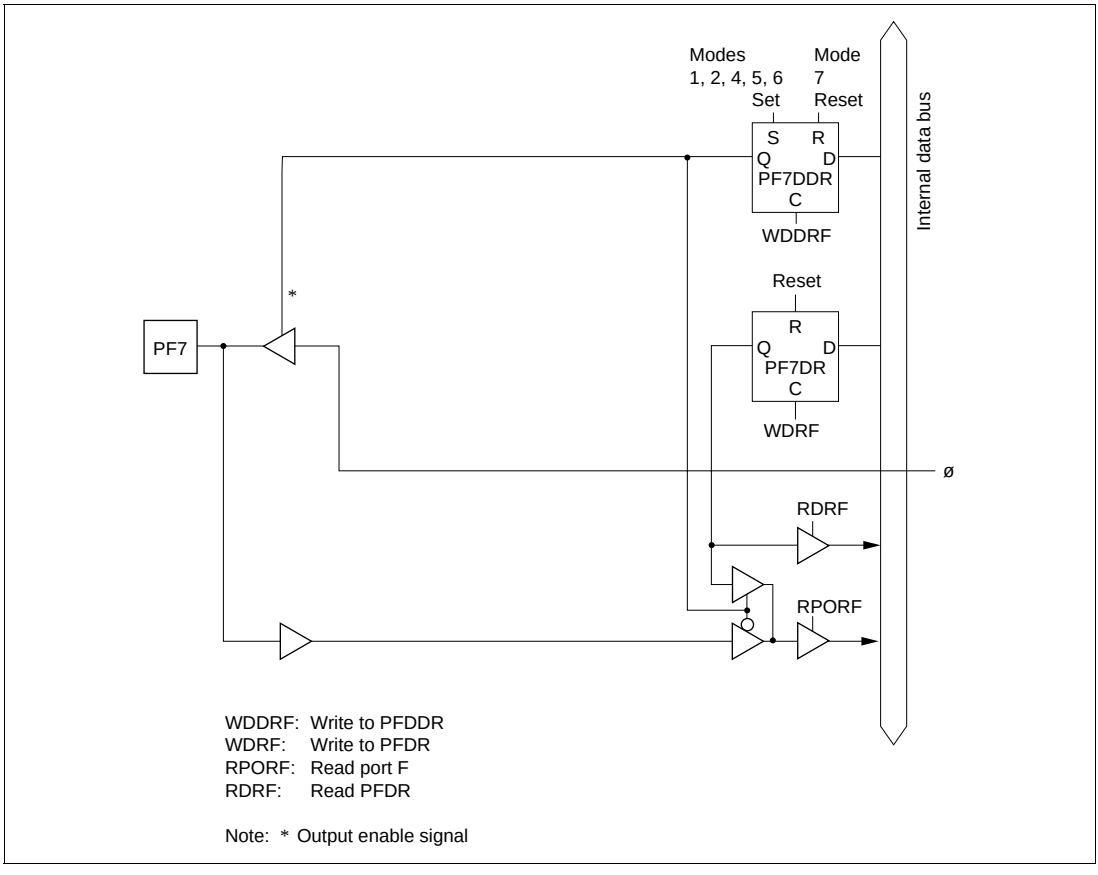


Figure 5.57 Port F Block Diagram (h) (Pin PF7)

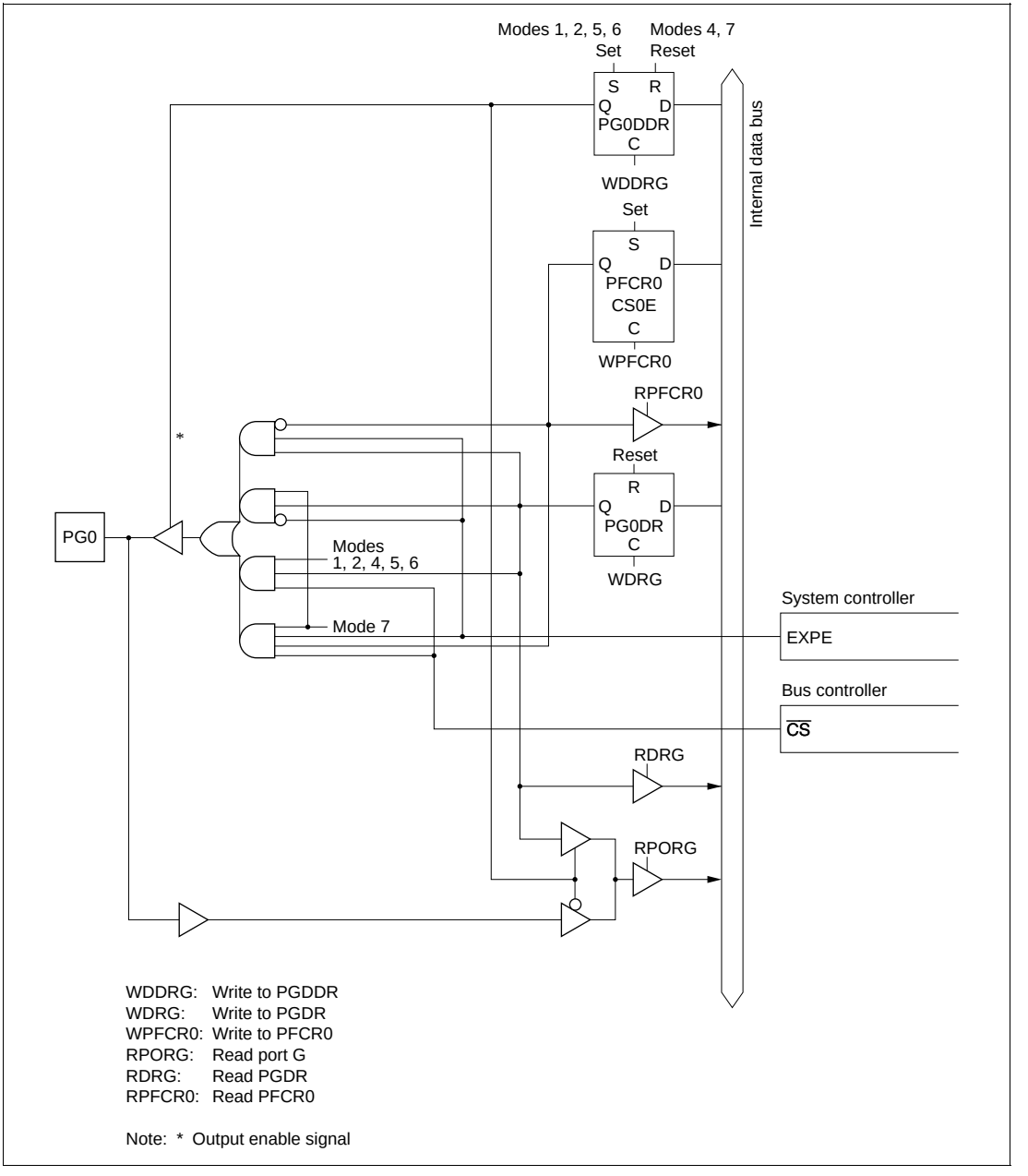
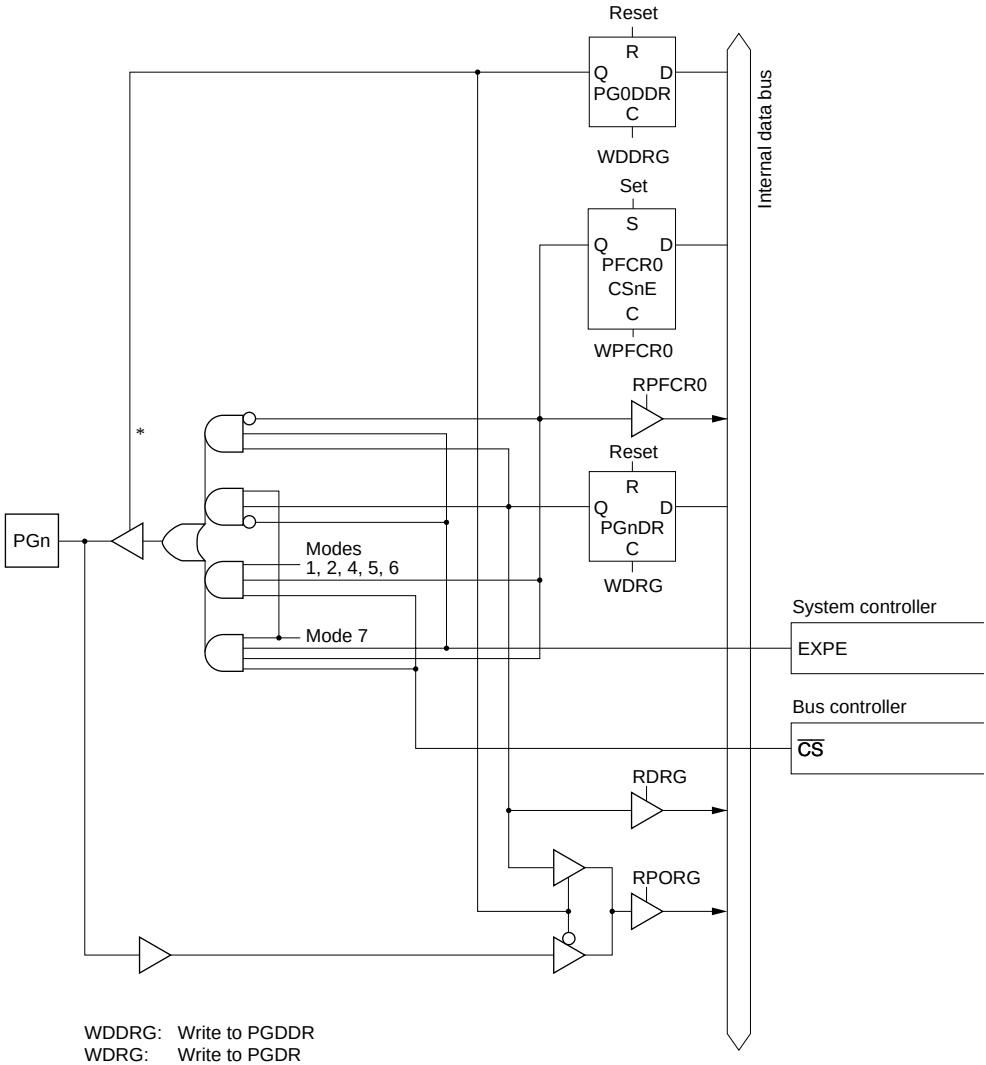


Figure 5.58 Port G Block Diagram (a) (Pin PG0)



WDDRG: Write to PGDDR
WDRG: Write to PGDR
WPFCR0: Write to PFCR0
RPORG: Read port G
RDRG: Read PGDR
RPFCR0: Read PFCR0
n = 1 to 3

Note: * Output enable signal

Figure 5.59 Port G Block Diagram (b) (Pins PG1 to PG3)

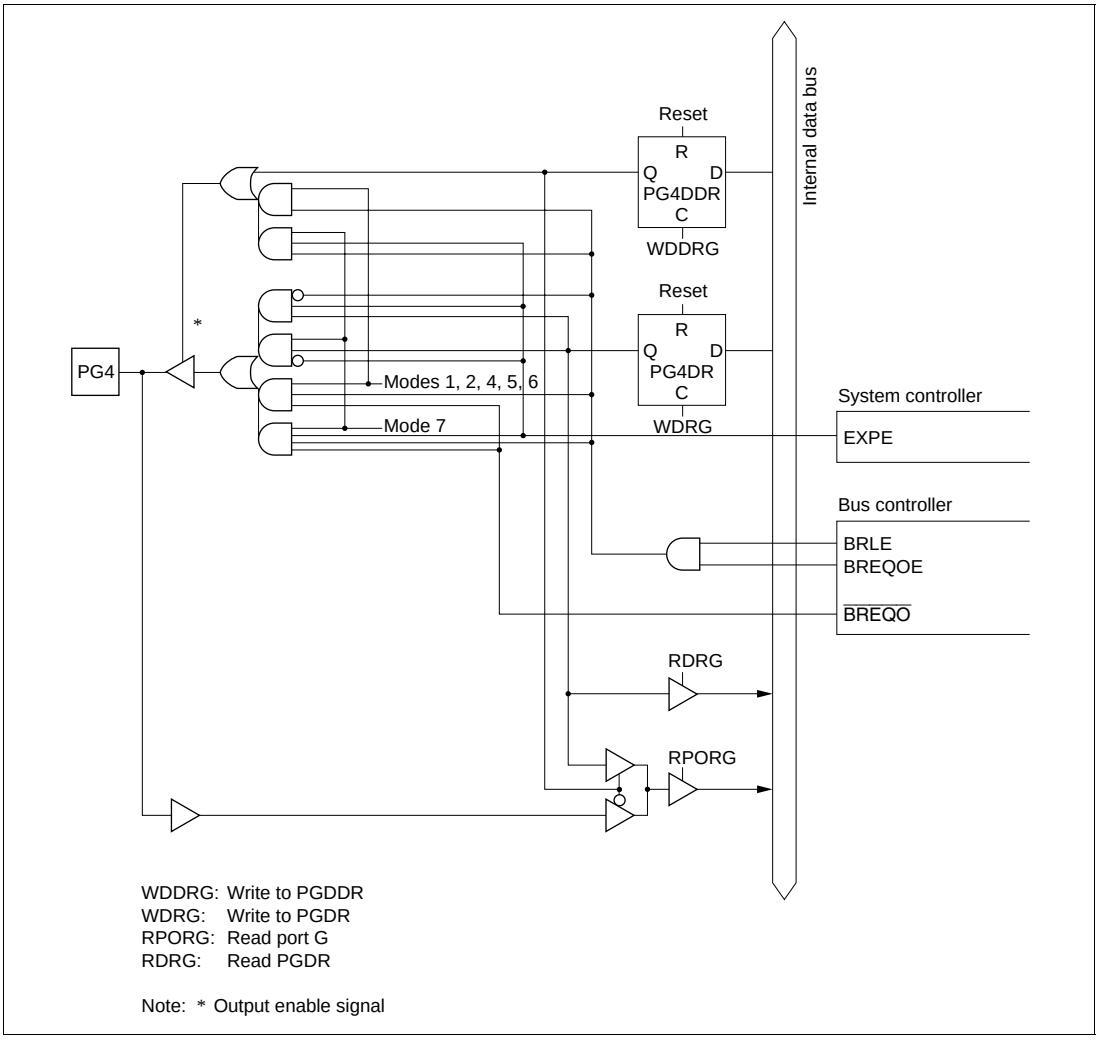


Figure 5.60 Port G Block Diagram (c) (Pin PG4)

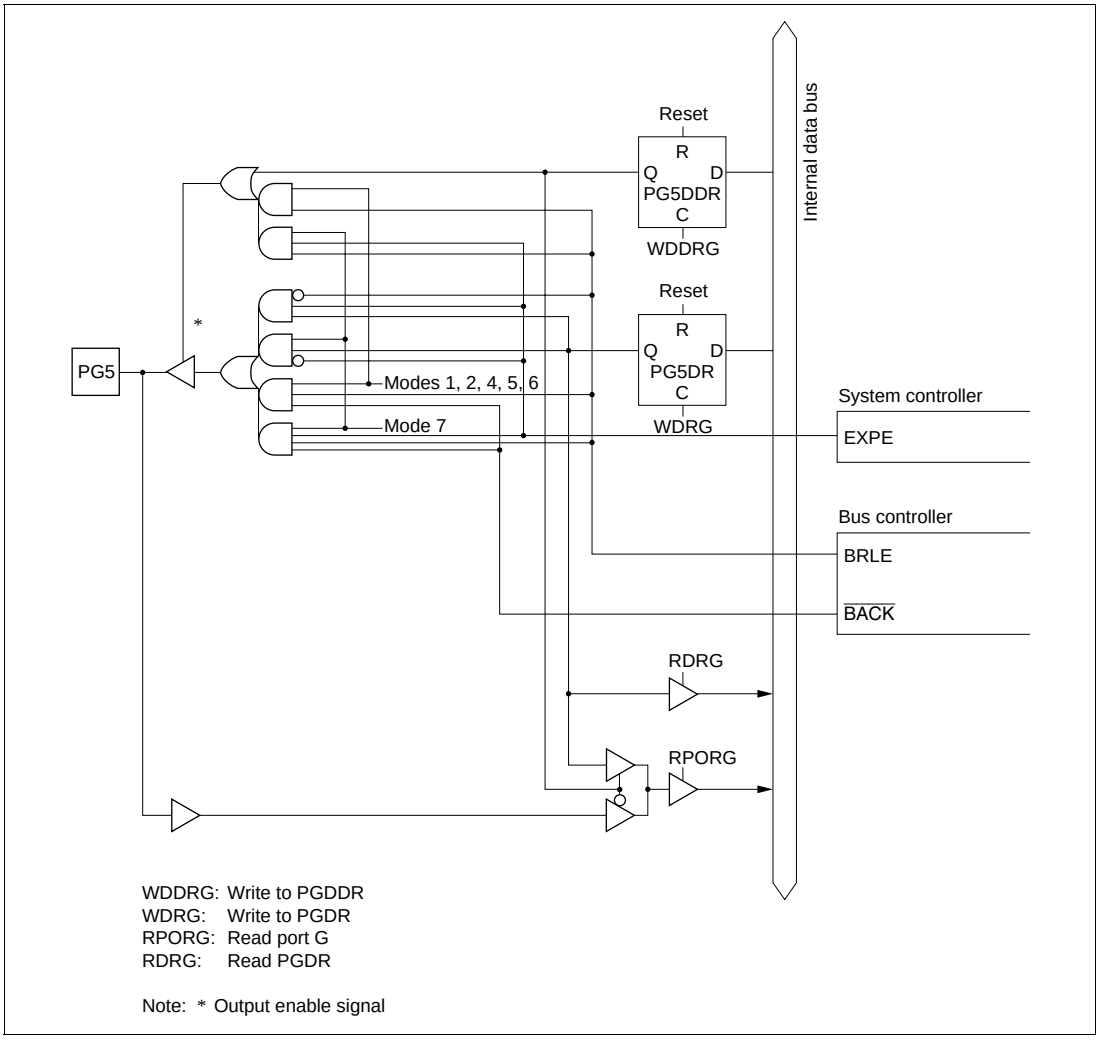


Figure 5.61 Port G Block Diagram (d) (Pin PG5)

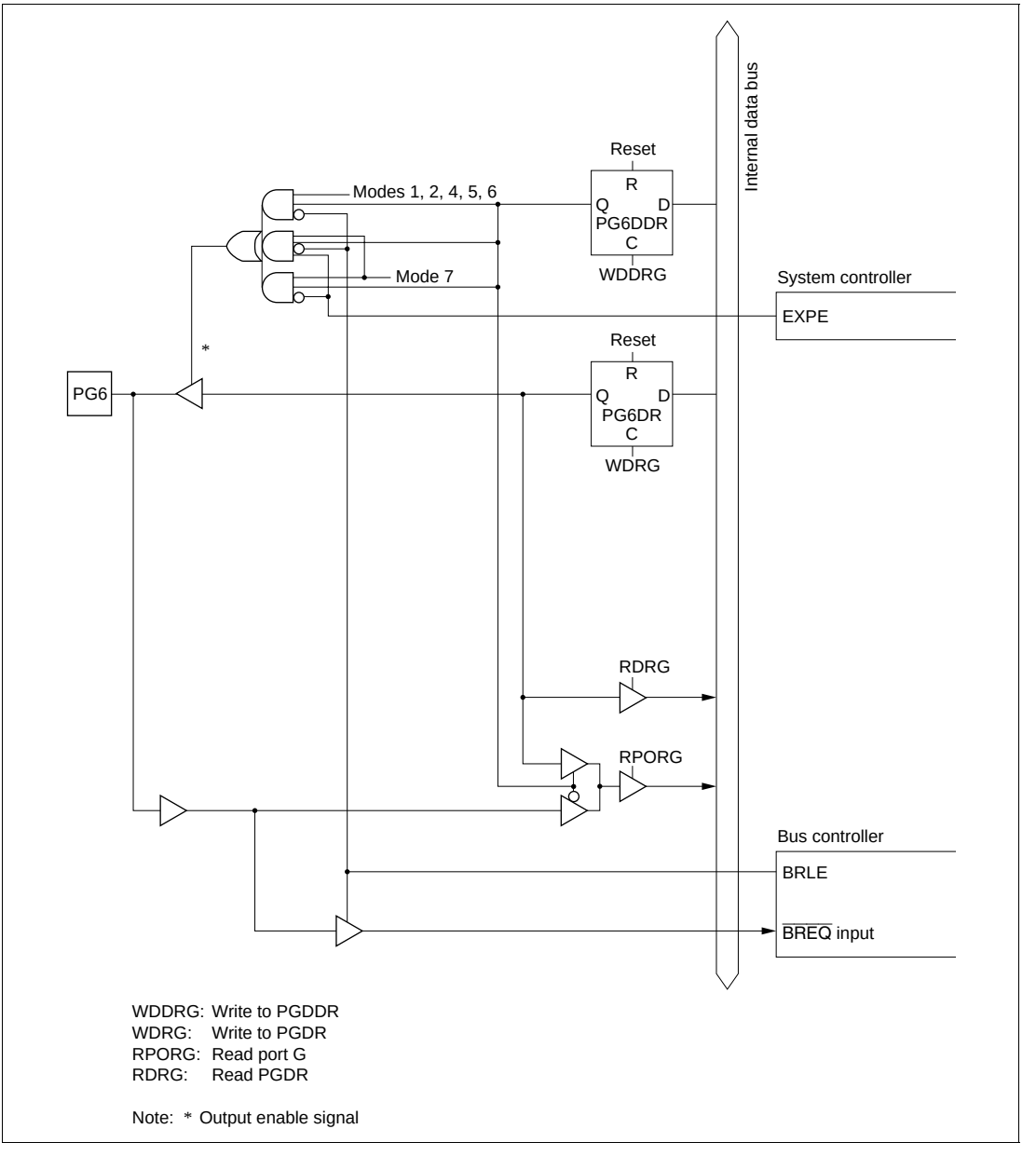


Figure 5.62 Port G Block Diagram (e) (Pin PG6)

5.19.16 Port H

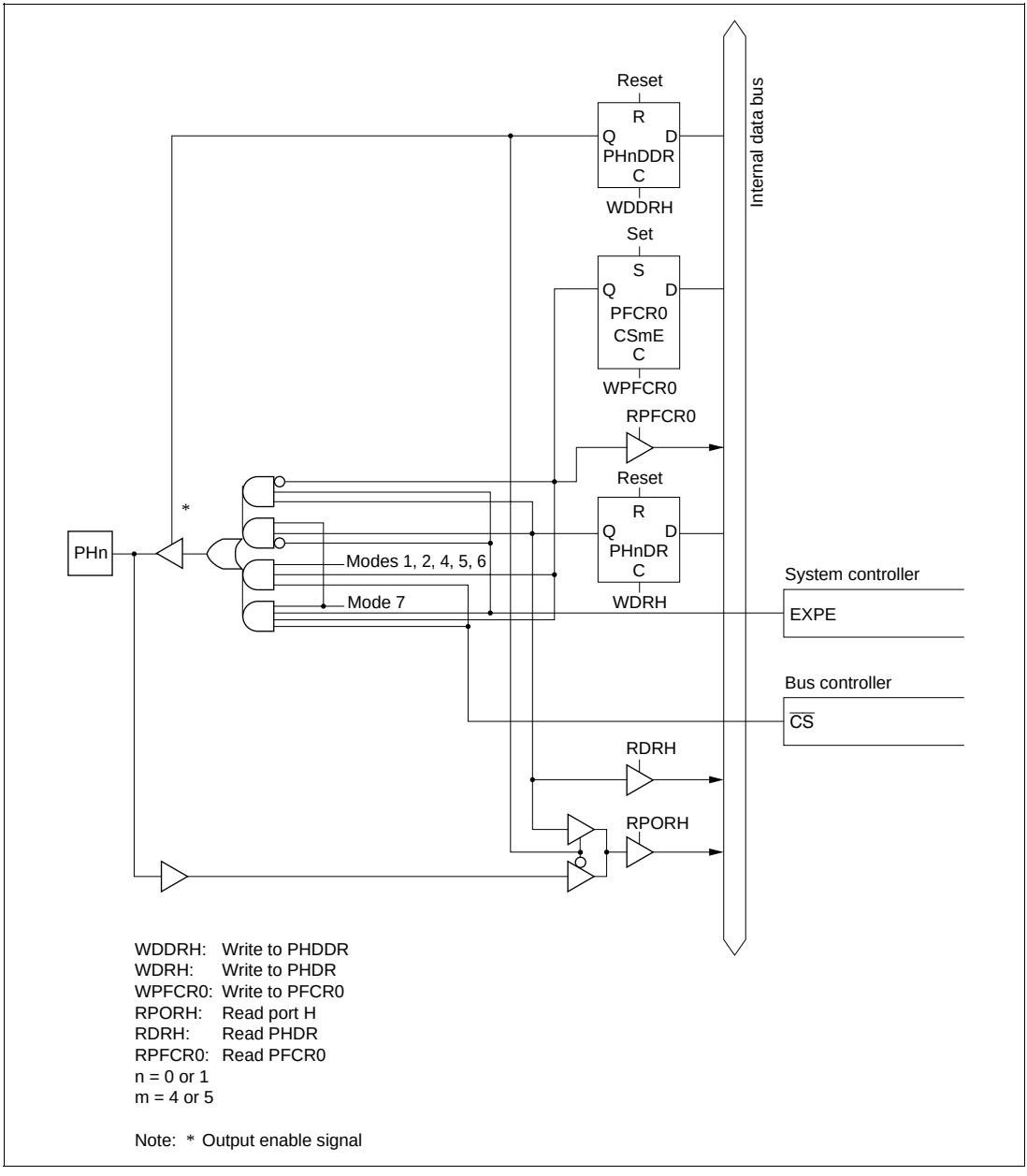


Figure 5.63 Port H Block Diagram (a) (Pins PH0 and PH1)

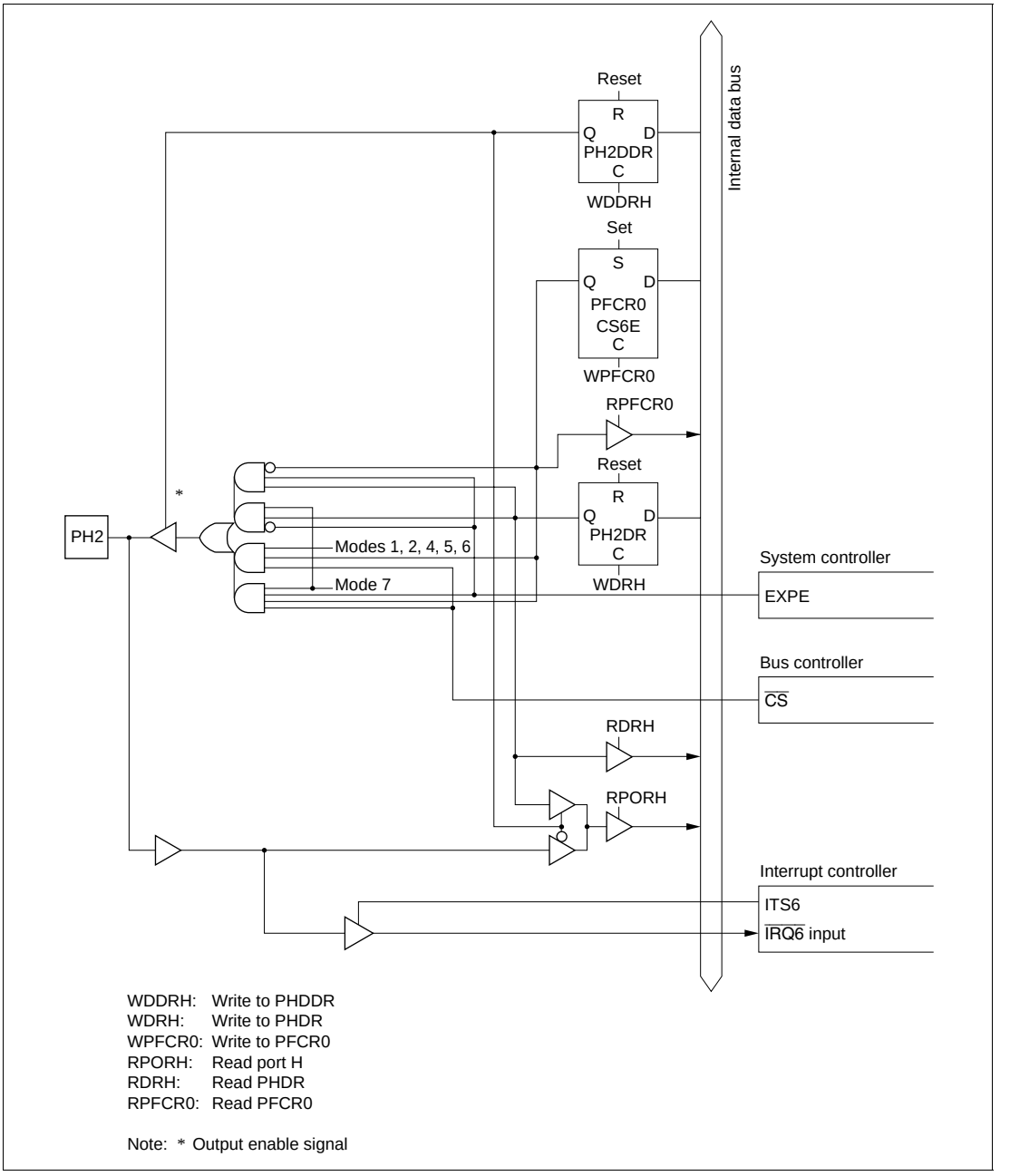


Figure 5.64 Port H Block Diagram (b) (Pin PH2)

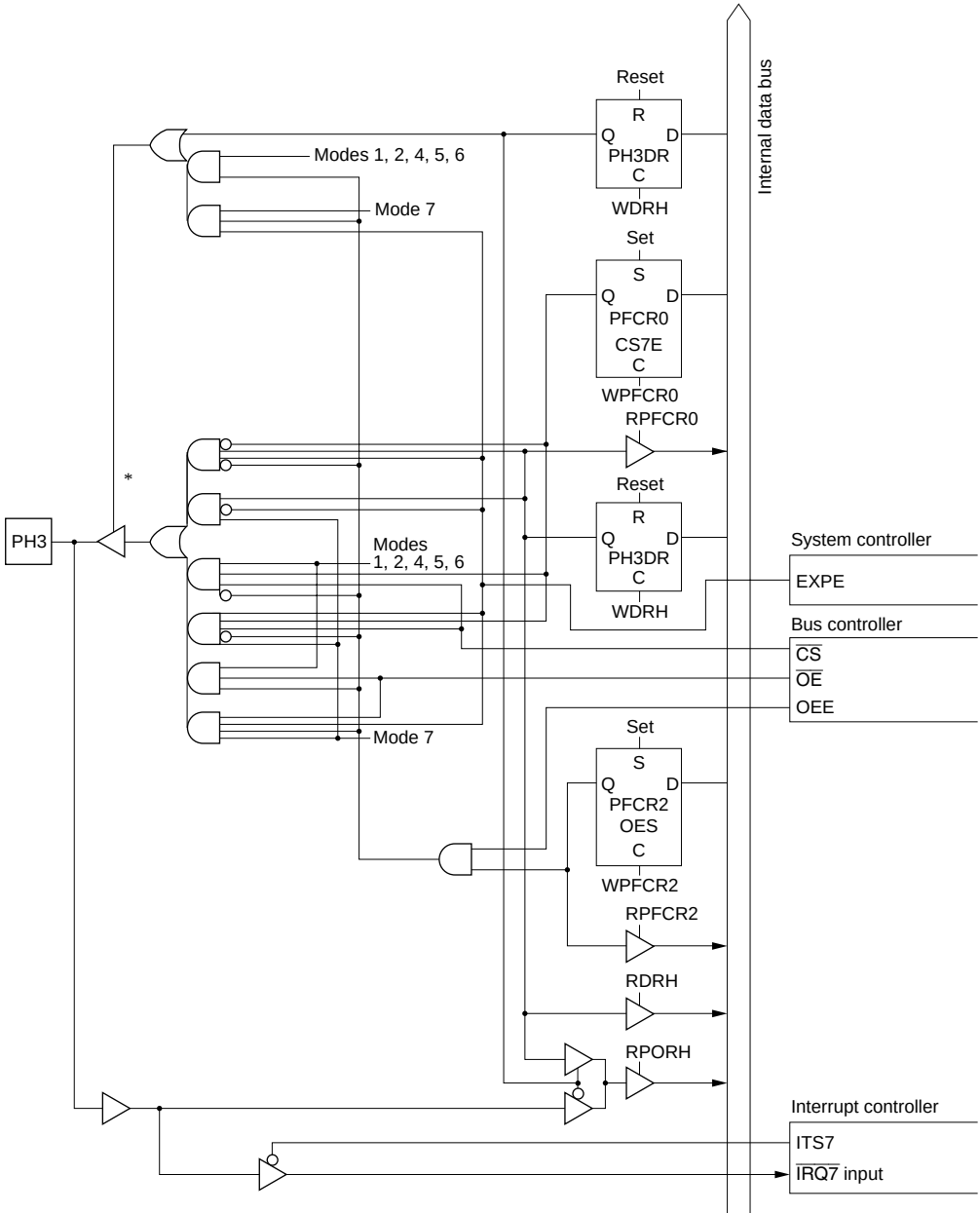


Figure 5.65 Port H Block Diagram (c) (Pin PH3)

Section 6 Supporting Module Block Diagrams

6.1 Interrupt Controller

6.1.1 Features

- Selection of two interrupt control modes
- Eight priority levels can be set for each module with IPR
- Independent vector addresses
- 17 external interrupt pins (NMI, $\overline{\text{IRQ15}}$ to $\overline{\text{IRQ0}}$)
- DTC and DMAC activation control

6.1.2 Block Diagram

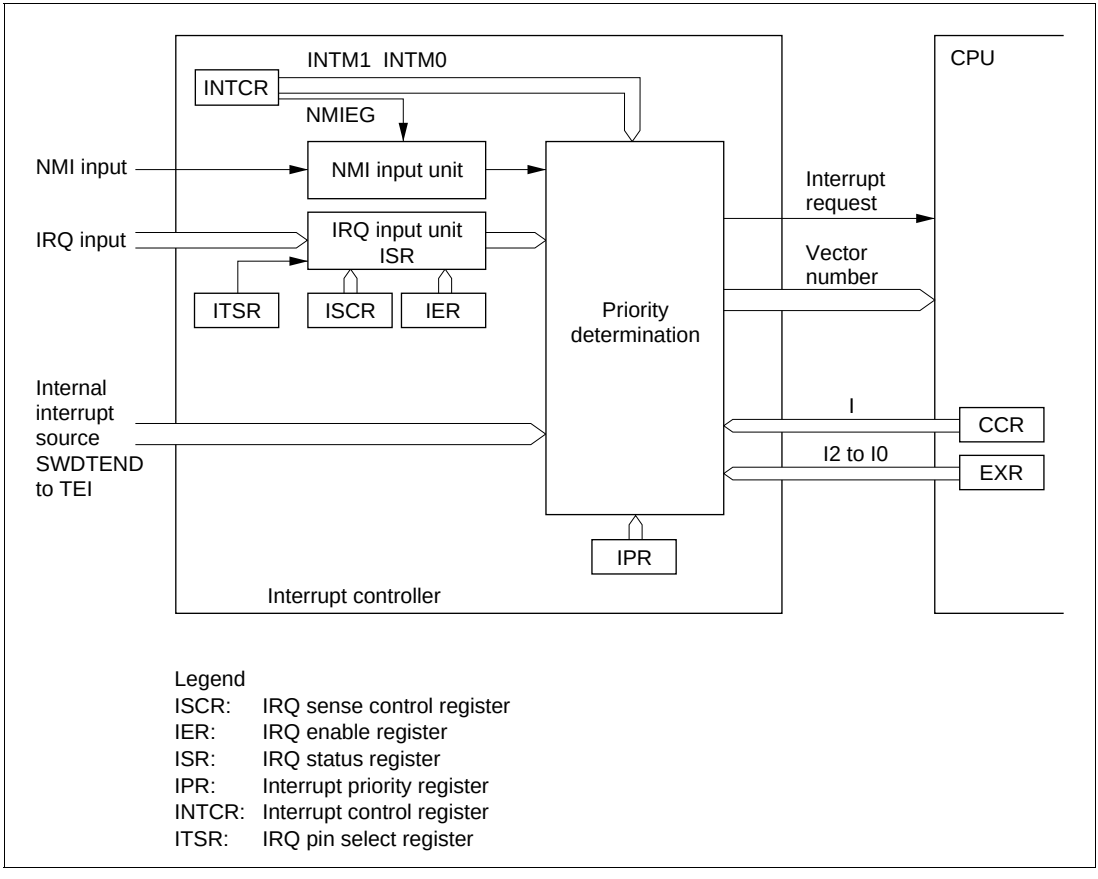


Figure 6.1 Block Diagram of Interrupt Controller

6.1.3 Pins

Table 6.1 Interrupt Controller Pins

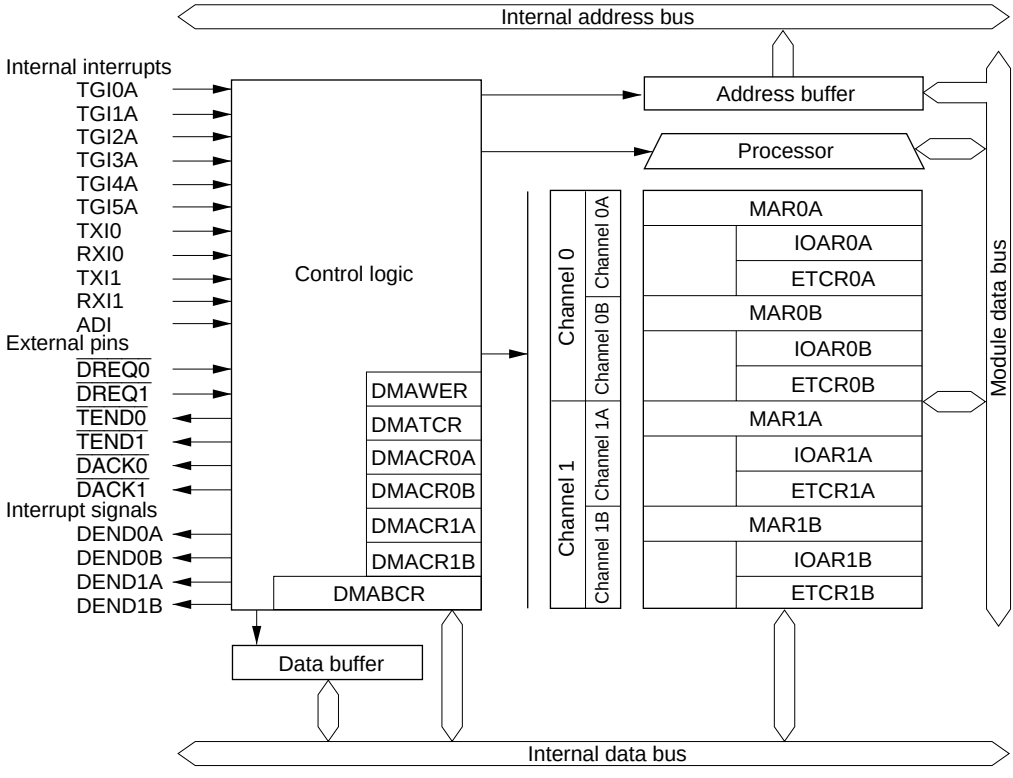
Name	Abbreviation	I/O	Function
Nonmaskable interrupt	NMI	Input	Nonmaskable external interrupt; rising or falling edge can be selected
External interrupt requests 15 to 0	$\overline{\text{IRQ15}}$ to $\overline{\text{IRQ0}}$	Input	Maskable external interrupts; rising, falling, or both edges, or level sensing, can be selected

6.2 DMA Controller

6.2.1 Features

- Selection of short address mode or full address mode
- 16-Mbyte address space can be specified directly
- Byte or word can be set as the transfer unit
- Activation sources: internal interrupt, external request, auto-request (depending on transfer mode)
- Module stop mode can be set

6.2.2 Block Diagram



Legend

DMAWER:	DMA write enable register
DMATCR:	DMA terminal control register
DMABCR:	DMA band control register (for all channels)
DMACR:	DMA control register
MAR:	Memory address register
IOAR:	I/O address register
ETCR:	Execute transfer count register

Figure 6.2 Block Diagram of DMAC

6.2.3 Pins

Table 6.2 DMAC Pins

Channel	Name	Abbreviation	I/O	Function
0	DMA request 0	$\overline{\text{DREQ0}}$	Input	DMAC channel 0 external request
	DMA transfer acknowledge 0	$\overline{\text{DACK0}}$	Output	DMAC channel 0 single address transfer acknowledge
	DMA transfer end 0	$\overline{\text{TEND0}}$	Output	DMAC channel 0 transfer end
1	DMA request 1	$\overline{\text{DREQ1}}$	Input	DMAC channel 1 external request
	DMA transfer acknowledge 1	$\overline{\text{DACK1}}$	Output	DMAC channel 1 single address transfer acknowledge
	DMA transfer end 1	$\overline{\text{TEND1}}$	Output	DMAC channel 1 transfer end

6.3 Data Transfer Controller

6.3.1 Features

- Transfer possible over any number of channels
- Variety of transfer modes, including normal, repeat, and block transfer
- Direct specification of 16-Mbyte address space possible
- Byte or word can be selected as the transfer unit
- A CPU interrupt can be requested for an interrupt that activates the DTC
- Can be activated by software
- Module stop mode can be set

6.3.2 Block Diagram

DTC register information is located in on-chip RAM*. As the DTC and on-chip RAM (1-kbyte) are connected by a 32-bit bus, a 32-bit read or write of DTC register information can be executed in one state.

Note: * When the DTC is used, the RAME bit must be set to 1 in SYSCR.

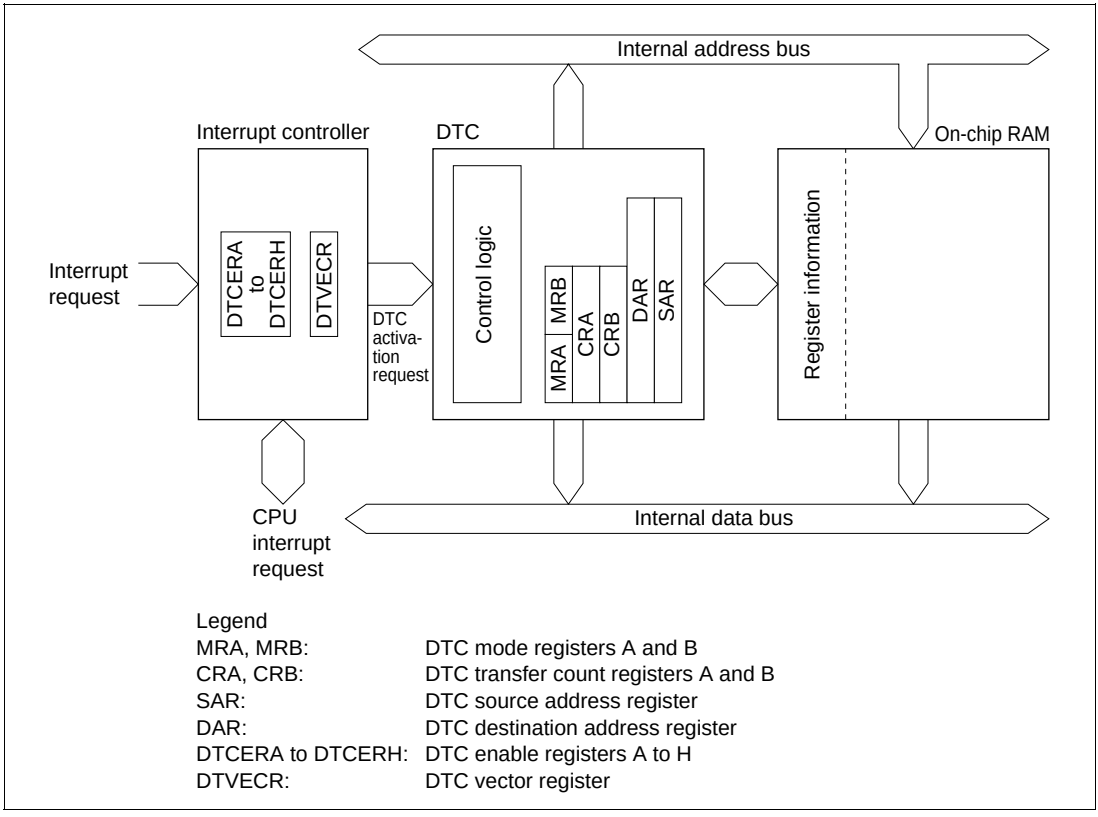


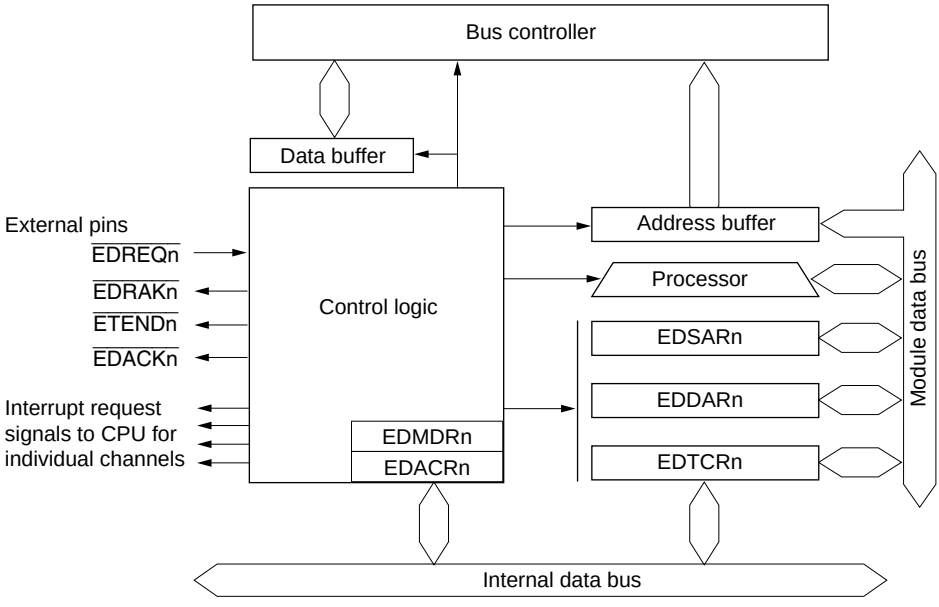
Figure 6.3 Block Diagram of DTC

6.4 EXDMA Controller (EXDMAC)

6.4.1 Features

- Four channels
- Physical address space (16-Mbyte flat external space)
- Byte or word transfer data length can be selected
- Maximum number of transfers: 16M (16,777,215)/infinite (free-running)
- Selection of dual address mode or single address mode
- Two kinds of EXDMAC transfer activation requests: external request and auto request
- Cycle steal mode or burst mode can be selected as bus mode
- Normal mode or block transfer mode can be selected as transfer mode

6.4.2 Block Diagram



Legend
EDSARn: EXDMA source address register
EDDARn: EXDMA destination address register
EDTCRn: EXDMA transfer count register
EDMDRn: EXDMA mode control register
EDACRn: EXDMA address control register
$\overline{\text{EDREQ}}$n: EXDMA transfer request
$\overline{\text{EDRAK}}$n: $\overline{\text{EDREQ}}$n acknowledge
$\overline{\text{ETEND}}$n: EXDMA transfer end
$\overline{\text{EDACK}}$n: EXDMA transfer acknowledge
n = 0 to 3

Figure 6.4 Block Diagram of EXDMAC

6.4.3 Pins

Table 6.3 EXDMAC Pins

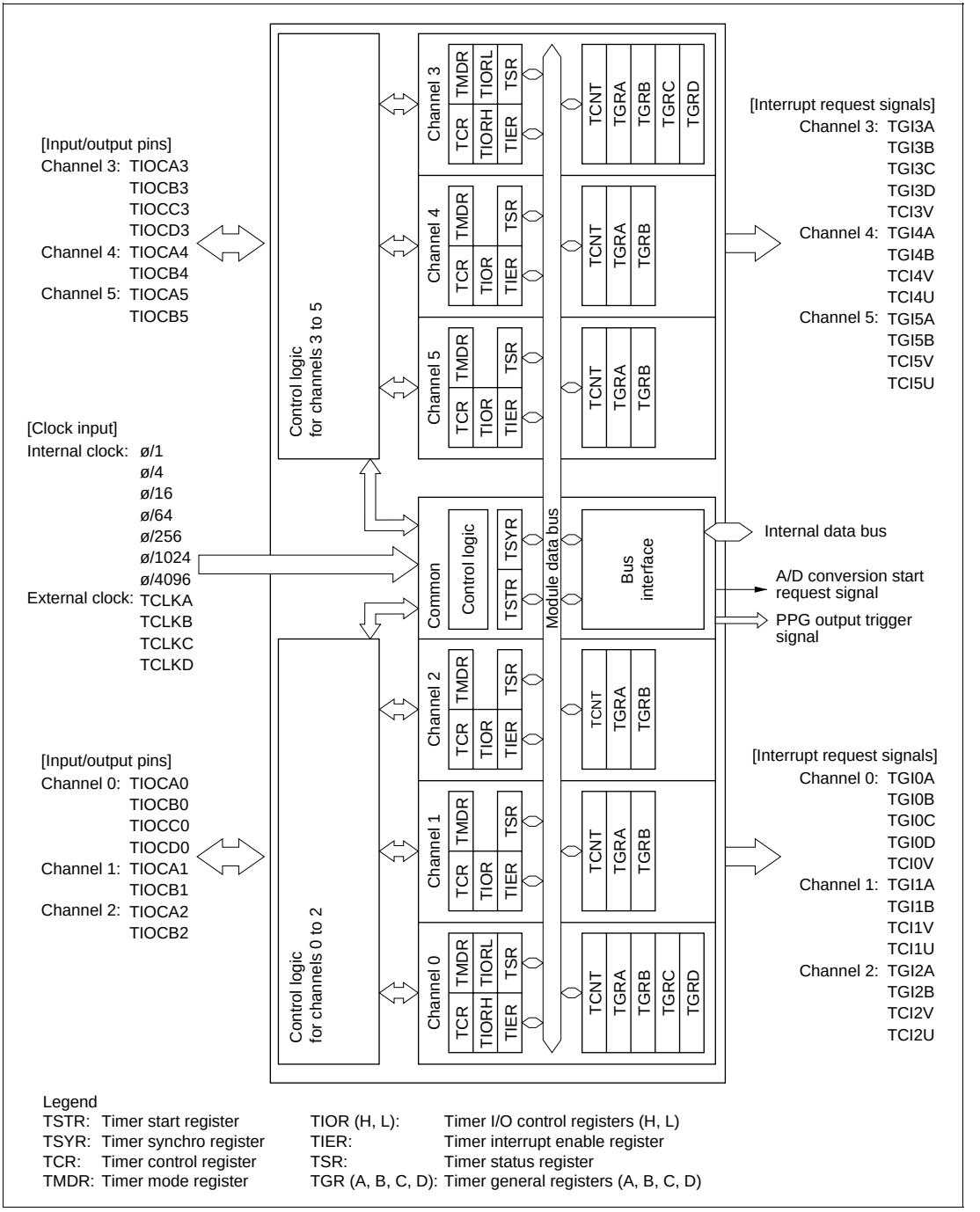
Channel	Name	Abbreviation	I/O	Function
0	EXDMA transfer request 0	$\overline{\text{EDREQ0}}$	Input	EXDMAC channel 0 external request
	EXDMA transfer acknowledge 0	$\overline{\text{EDACK0}}$	Output	EXDMAC channel 0 single address transfer acknowledge
	EXDMA transfer end 0	$\overline{\text{ETEND0}}$	Output	EXDMAC channel 0 transfer end
	$\overline{\text{EDREQ0}}$ acknowledge	$\overline{\text{EDRAK0}}$	Output	Notification to external device of channel 0 external request acceptance and start of execution
1	EXDMA transfer request 1	$\overline{\text{EDREQ1}}$	Input	EXDMAC channel 1 external request
	EXDMA transfer acknowledge 1	$\overline{\text{EDACK1}}$	Output	EXDMAC channel 1 single address transfer acknowledge
	EXDMA transfer end 1	$\overline{\text{ETEND1}}$	Output	EXDMAC channel 1 transfer end
	$\overline{\text{EDREQ1}}$ acknowledge	$\overline{\text{EDRAK1}}$	Output	Notification to external device of channel 1 external request acceptance and start of execution
2	EXDMA transfer request 2	$\overline{\text{EDREQ2}}$	Input	EXDMAC channel 2 external request
	EXDMA transfer acknowledge 2	$\overline{\text{EDACK2}}$	Output	EXDMAC channel 2 single address transfer acknowledge
	EXDMA transfer end 2	$\overline{\text{ETEND2}}$	Output	EXDMAC channel 2 transfer end
	$\overline{\text{EDREQ2}}$ acknowledge	$\overline{\text{EDRAK2}}$	Output	Notification to external device of channel 2 external request acceptance and start of execution
3	EXDMA transfer request 3	$\overline{\text{EDREQ3}}$	Input	EXDMAC channel 3 external request
	EXDMA transfer acknowledge 3	$\overline{\text{EDACK3}}$	Output	EXDMAC channel 3 single address transfer acknowledge
	EXDMA transfer end 3	$\overline{\text{ETEND3}}$	Output	EXDMAC channel 3 transfer end
	$\overline{\text{EDREQ3}}$ acknowledge	$\overline{\text{EDRAK3}}$	Output	Notification to external device of channel 3 external request acceptance and start of execution

6.5 16-bit Timer Pulse Unit

6.5.1 Features

- Six 16-bit timer channels
- Maximum 16 pulse inputs/outputs
- Selection of 8 counter input clocks for each channel
- Compare match, input capture, counter clear operation, synchronous operation, and PWM mode can be set for each channel
- Buffer operation can be set for channels 0 and 3
- Phase counting mode can be set independently for each of channels 1, 2, 4, and 5
- Cascaded operation possible by connecting two 16-bit counter channels to form a 32-bit counter
- Fast access via internal 16-bit bus
- Programmable pulse generator (PPG) output trigger can be generated
- A/D converter conversion start trigger can be generated
- Module stop mode can be set

6.5.2 Block Diagram



Legend

TSTR:	Timer start register	TIOR (H, L):	Timer I/O control registers (H, L)
TSYR:	Timer synchro register	TIER:	Timer interrupt enable register
TCR:	Timer control register	TSR:	Timer status register
TMDR:	Timer mode register	TGR (A, B, C, D):	Timer general registers (A, B, C, D)

Figure 6.5 Block Diagram of TPU

6.5.3 Pins

Table 6.4 TPU Pins

Channel	Name	Abbre-viation	I/O	Function
All	Clock input A	TCLKA	Input	External clock A input pin (Channel 1 and 5 phase counting mode A-phase input)
	Clock input B	TCLKB	Input	External clock B input pin (Channel 1 and 5 phase counting mode B-phase input)
	Clock input C	TCLKC	Input	External clock C input pin (Channel 2 and 4 phase counting mode A-phase input)
	Clock input D	TCLKD	Input	External clock D input pin (Channel 2 and 4 phase counting mode B-phase input)
0	Input capture/out compare match A0	TIOCA0	I/O	TGR0A input capture input/output compare output/PWM output pin
	Input capture/out compare match B0	TIOCB0	I/O	TGR0B input capture input/output compare output/PWM output pin
	Input capture/out compare match C0	TIOCC0	I/O	TGR0C input capture input/output compare output/PWM output pin
	Input capture/out compare match D0	TIOCD0	I/O	TGR0D input capture input/output compare output/PWM output pin
1	Input capture/out compare match A1	TIOCA1	I/O	TGR1A input capture input/output compare output/PWM output pin
	Input capture/out compare match B1	TIOCB1	I/O	TGR1B input capture input/output compare output/PWM output pin
2	Input capture/out compare match A2	TIOCA2	I/O	TGR2A input capture input/output compare output/PWM output pin
	Input capture/out compare match B2	TIOCB2	I/O	TGR2B input capture input/output compare output/PWM output pin
3	Input capture/out compare match A3	TIOCA3	I/O	TGR3A input capture input/output compare output/PWM output pin
	Input capture/out compare match B3	TIOCB3	I/O	TGR3B input capture input/output compare output/PWM output pin
	Input capture/out compare match C3	TIOCC3	I/O	TGR3C input capture input/output compare output/PWM output pin
	Input capture/out compare match D3	TIOCD3	I/O	TGR3D input capture input/output compare output/PWM output pin

Channel	Name	Abbre-viation	I/O	Function
4	Input capture/out compare match A4	TIOCA4	I/O	TGR4A input capture input/output compare output/PWM output pin
	Input capture/out compare match B4	TIOCB4	I/O	TGR4B input capture input/output compare output/PWM output pin
5	Input capture/out compare match A5	TIOCA5	I/O	TGR5A input capture input/output compare output/PWM output pin
	Input capture/out compare match B5	TIOCB5	I/O	TGR5B input capture input/output compare output/PWM output pin

6.6 Programmable Pulse Generator

6.6.1 Features

- Maximum 16-bit data output capability
- Up to four different 4-bit outputs
- Output trigger signals can be selected
- Non-overlap margin can be set
- Can operate together with the data transfer controller (DTC) and DMA controller (DMAC)
- Inverse output can be selected
- Module stop mode can be set

6.6.2 Block Diagram

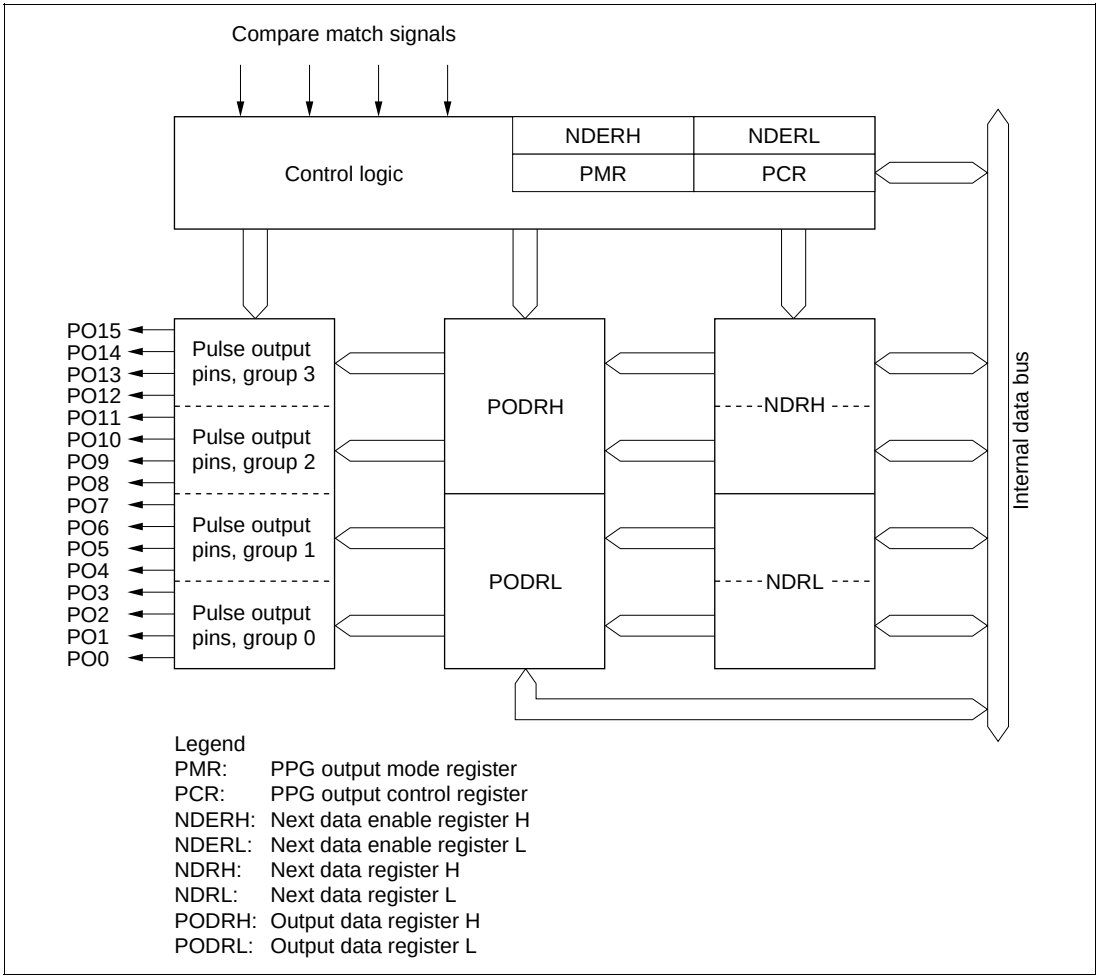


Figure 6.6 Block Diagram of PPG

6.6.3 Pins

Table 6.5 PPG Pins

Name	Abbreviation	I/O	Function
Pulse output 0	PO0	Output	Group 0 pulse output
Pulse output 1	PO1	Output	
Pulse output 2	PO2	Output	
Pulse output 3	PO3	Output	
Pulse output 4	PO4	Output	Group 1 pulse output
Pulse output 5	PO5	Output	
Pulse output 6	PO6	Output	
Pulse output 7	PO7	Output	
Pulse output 8	PO8	Output	Group 2 pulse output
Pulse output 9	PO9	Output	
Pulse output 10	PO10	Output	
Pulse output 11	PO11	Output	
Pulse output 12	PO12	Output	Group 3 pulse output
Pulse output 13	PO13	Output	
Pulse output 14	PO14	Output	
Pulse output 15	PO15	Output	

6.7 8-Bit Timer

6.7.1 Features

- Two-channel timer using 8-bit counters as base
- Selection of four counter input clocks
- Counter clearing can be specified
- Timer output by combination of two compare match signals
- Cascaded operation possible by connecting both counter channels to form a 16-bit counter
- Three interrupt sources for each channel
- A/D converter conversion start trigger can be generated
- Module stop mode can be set

6.7.2 Block Diagram

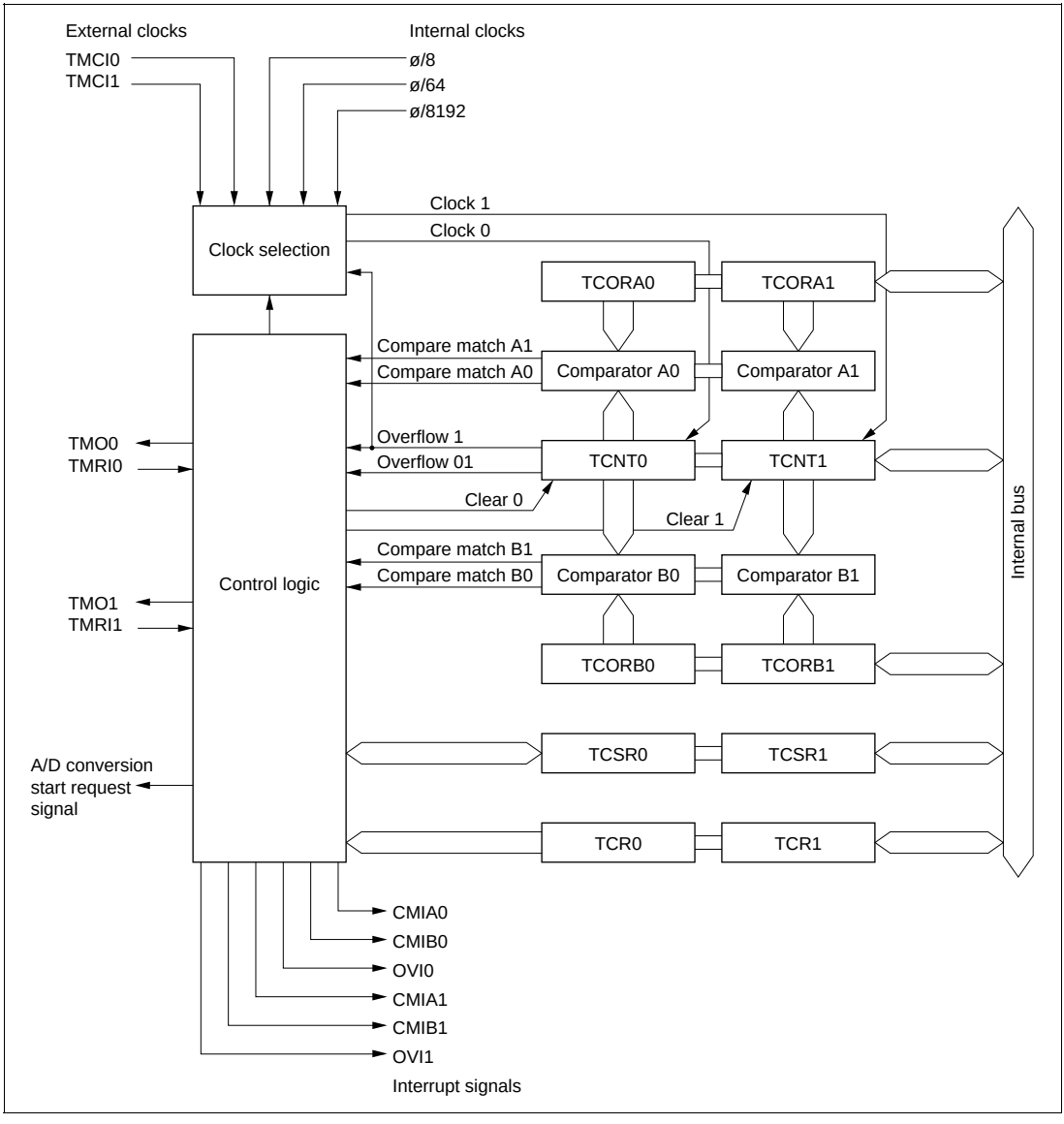


Figure 6.7 Block Diagram of 8-Bit Timer

6.7.3 Pins

Table 6.6 8-Bit Timer Pins

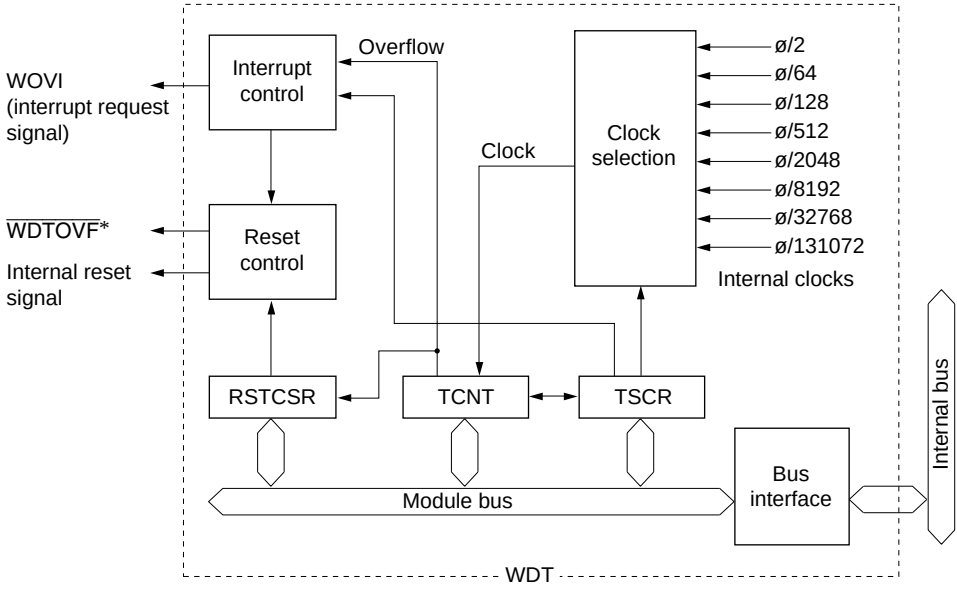
Channel	Name	Abbreviation	I/O	Function
0	Timer output pin 0	TMO0	Output	Compare match output
	Timer clock input pin 0	TMCI0	Input	Counter external clock input
	Timer reset input pin 0	TMRI0	Input	Counter external reset input
1	Timer output pin 1	TMO1	Output	Compare match output
	Timer clock input pin 1	TMCI1	Input	Counter external clock input
	Timer reset input pin 1	TMRI1	Input	Counter external reset input

6.8 Watchdog Timer

6.8.1 Features

- Switchable between watchdog timer mode and interval timer mode
- $\overline{\text{WDTOVF}}$ output in watchdog timer mode
- Interrupt generation when counter overflows in interval timer mode
- Selection of eight counter input clocks

6.8.2 Block Diagram



Legend
TCSR: Timer control/status register
TCNT: Timer counter
RSTCSR: Reset control/status register

Note: * The $\overline{\text{WDTOVF}}$ output function is not available in some models.

Figure 6.8 Block Diagram of WDT

6.8.3 Pins

Table 6.7 WDT Pin

Name	Abbreviation	I/O	Function
Watchdog timer overflow	$\overline{\text{WDTOVF}}$*	Output	Outputs counter overflow signal in watchdog timer mode

Note: * The $\overline{\text{WDTOVF}}$ output function is not available in some models.

6.9 Serial Communication Interface

6.9.1 Features

- Three independent on-chip channels in the H8S/2678 Series
- Selection of synchronous or asynchronous serial communication mode
- Full-duplex communication capability
- Selection of LSB-first or MSB-first transfer
- Built-in baud rate generator allows any bit rate to be selected
- Selection of transmit/receive clock source
- DTC and DMAC can be activated by four interrupts (ERI, RXI, TXI, and TEI)
- Module stop mode can be set

6.9.2 Block Diagram

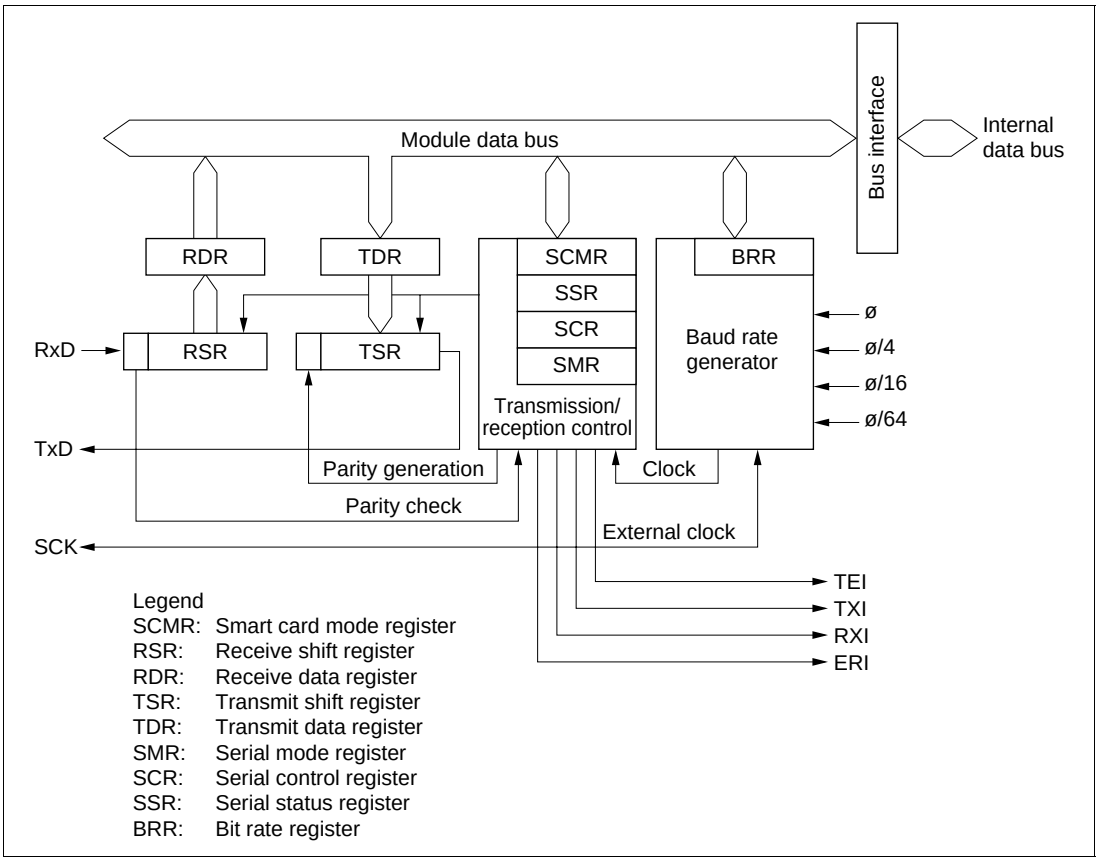


Figure 6.9 Block Diagram of SCI

6.9.3 Pins

Table 6.8 SCI Pins

Channel	Name	Abbreviation	I/O	Function
0	Serial clock pin 0	SCK0	I/O	SCI0 clock input/output
	Receive data pin 0	RxD0	Input	SCI0 receive data input
	Transmit data pin 0	TxD0	Output	SCI0 transmit data output
1	Serial clock pin 1	SCK1	I/O	SCI1 clock input/output
	Receive data pin 1	RxD1	Input	SCI1 receive data input
	Transmit data pin 1	TxD1	Output	SCI1 transmit data output
2	Serial clock pin 2	SCK2	I/O	SCI2 clock input/output
	Receive data pin 2	RxD2	Input	SCI2 receive data input
	Transmit data pin 2	TxD2	Output	SCI2 transmit data output

6.10 Smart Card Interface

6.10.1 Features

- IC card (smart card) interface conforming to ISO/IEC7816-3 supported as SCI extension function
- Switching between normal SCI and smart card interface by means of register setting
- Built-in baud rate generator allows any bit rate to be selected
- DTC and DMAC can be activated by three interrupts (TXI, RXI, and ERI)

6.10.2 Block Diagram

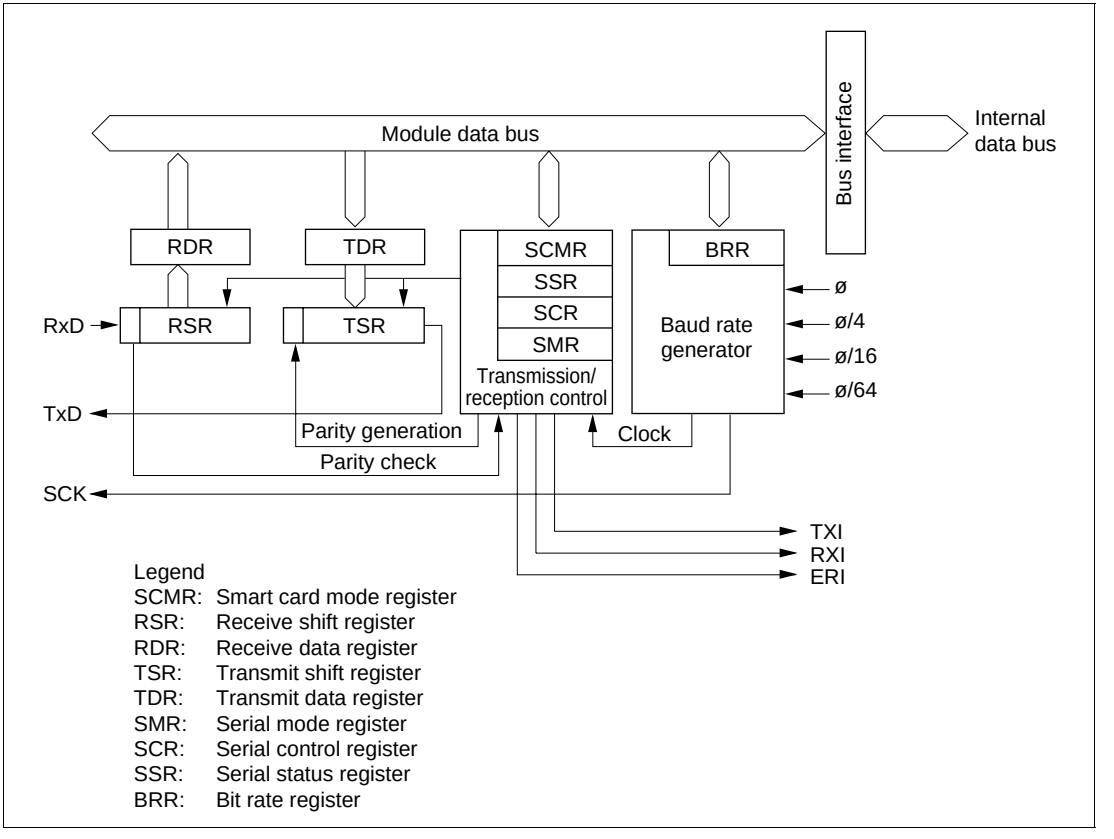


Figure 6.10 Block Diagram of Smart Card Interface

6.10.3 Pins

Table 6.9 Smart Card Interface Pins

Channel	Name	Abbreviation	I/O	Function
0	Serial clock pin 0	SCK0	I/O	SCI0 clock input/output
	Receive data pin 0	RxD0	Input	SCI0 receive data input
	Transmit data pin 0	TxD0	Output	SCI0 transmit data output
1	Serial clock pin 1	SCK1	I/O	SCI1 clock input/output
	Receive data pin 1	RxD1	Input	SCI1 receive data input
	Transmit data pin 1	TxD1	Output	SCI1 transmit data output
2	Serial clock pin 2	SCK2	I/O	SCI2 clock input/output
	Receive data pin 2	RxD2	Input	SCI2 receive data input
	Transmit data pin 2	TxD2	Output	SCI2 transmit data output

6.11 IrDA

6.11.1 Features

- SCI channel 0 TxD0 and RxD0 signals can be subjected to waveform encoding/decoding conforming to IrDA specification version 1.0 (IrTxD and IrRxD pins)
- Infrared transmission/reception conforming to the IrDA specification version 1.0 system can be implemented by connecting these pins to an infrared transceiver/receiver
- Transfer rate can be set by software

6.11.2 Block Diagram

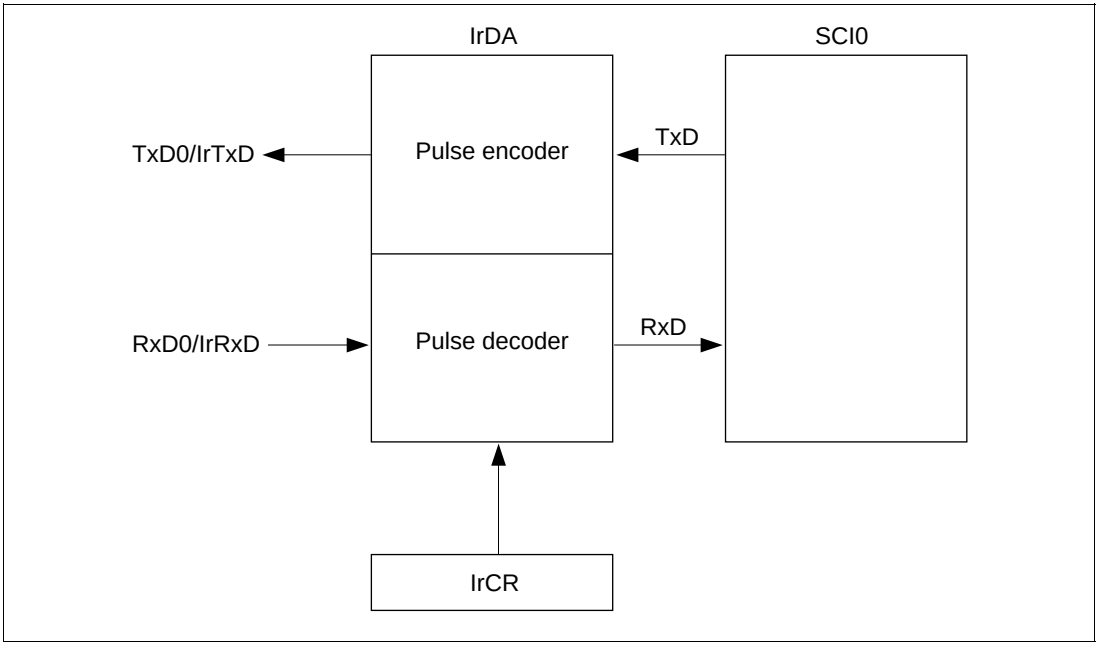


Figure 6.11 Block Diagram of IrDA

6.11.3 Pins

Table 6.10 IrDA Pins

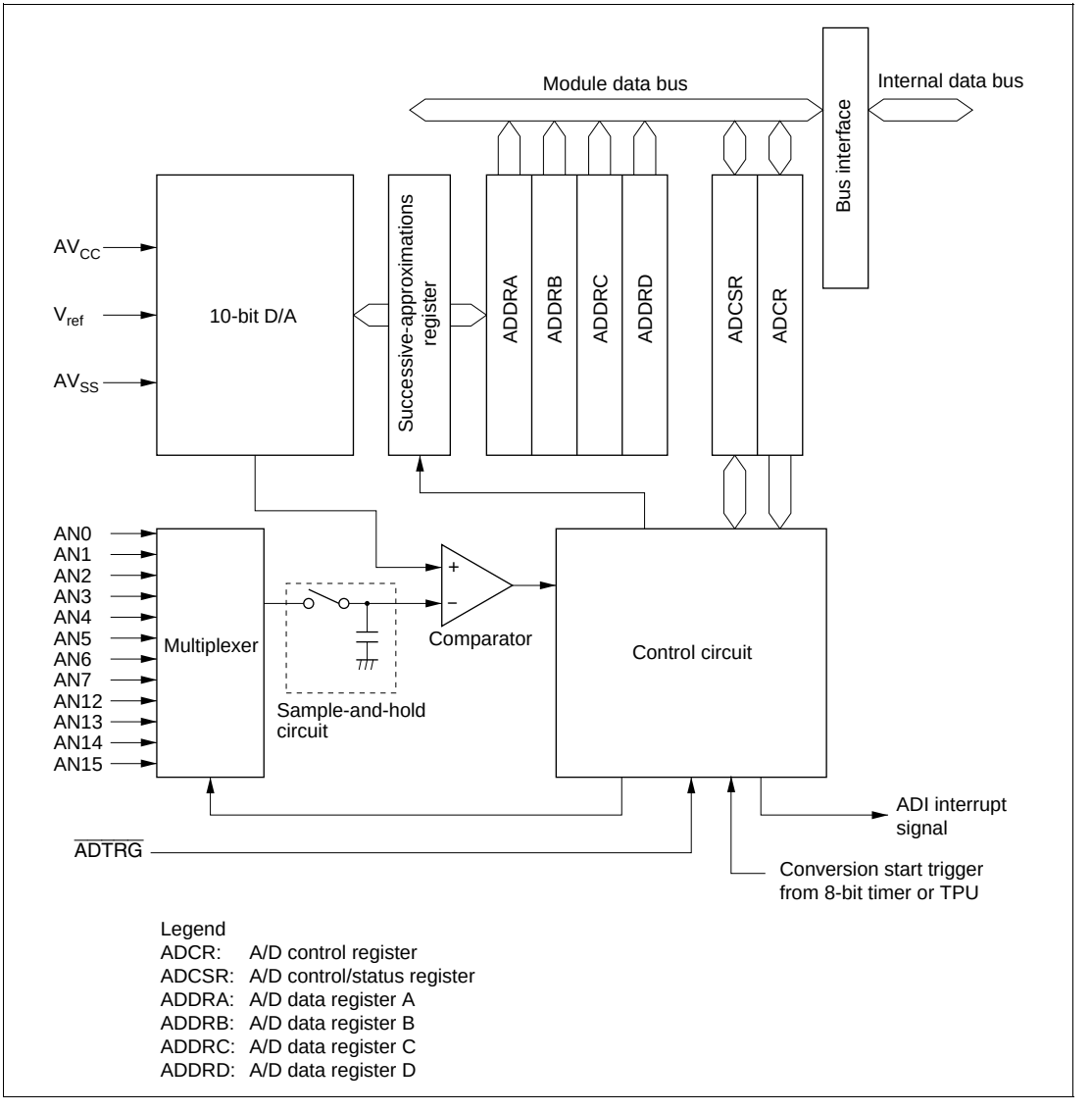
Channel	Name	Abbreviation	I/O	Function
0	Serial clock pin 0	SCK0	I/O	SCI0 clock input/output
	Receive data pin 0	RxD0/IrRxD	Input	SCI0 receive data input (normal/IrDA)
	Transmit data pin 0	TxD0/IrTxD	Output	SCI0 transmit data output (normal/IrDA)

6.12 A/D Converter

6.12.1 Features

- 10-bit resolution
- Twelve input channels
- Settable analog conversion voltage range
- Conversion time: 6.7 μs per channel (at 20 MHz operation)
- Selection of single mode or scan mode as operating mode
- Four data registers
- Sample-and-hold function
- Three kinds of conversion start (software, timer conversion start trigger, and $\overline{\text{ADTRG}}$ pin)
- A/D conversion end interrupt request generation
- Module stop mode can be set

6.12.2 Block Diagram



Legend
ADCR: A/D control register
ADCSR: A/D control/status register
ADDRA: A/D data register A
ADDRB: A/D data register B
ADDRC: A/D data register C
ADDRD: A/D data register D

Figure 6.12 Block Diagram of A/D Converter

6.12.3 Pins

Table 6.11 A/D Converter Pins

Name	Abbre-viation	I/O	Function
Analog power supply pin	AVCC	Input	Analog circuit power supply
Analog ground pin	AVSS	Input	Analog circuit ground and reference voltage
Reference voltage pin	Vref	Input	A/D conversion reference voltage
Analog input pin 0	AN0	Input	Channel set 0 (CH3 =1) group 0 analog input
Analog input pin 1	AN1	Input	
Analog input pin 2	AN2	Input	
Analog input pin 3	AN3	Input	
Analog input pin 4	AN4	Input	Channel set 1 (CH3 =1) group 1 analog input
Analog input pin 5	AN5	Input	
Analog input pin 6	AN6	Input	
Analog input pin 7	AN7	Input	
Analog input pin 12	AN12	Input	Channel set 1 (CH3 =0) group 1 analog input
Analog input pin 13	AN13	Input	
Analog input pin 14	AN14	Input	
Analog input pin 15	AN15	Input	
A/D external trigger input pin	$\overline{\text{ADTRG}}$	Input	External trigger for starting A/D conversion

6.13 D/A Converter

6.13.1 Features

- 8-bit resolution
- Output on two channels to maximum four channels
- Maximum conversion time of 10 µs (with 20 pF capacitive load)
- Output voltage of 0 V to Vref
- D/A output hold function in software standby mode
- Module stop mode can be set

6.13.2 Block Diagram

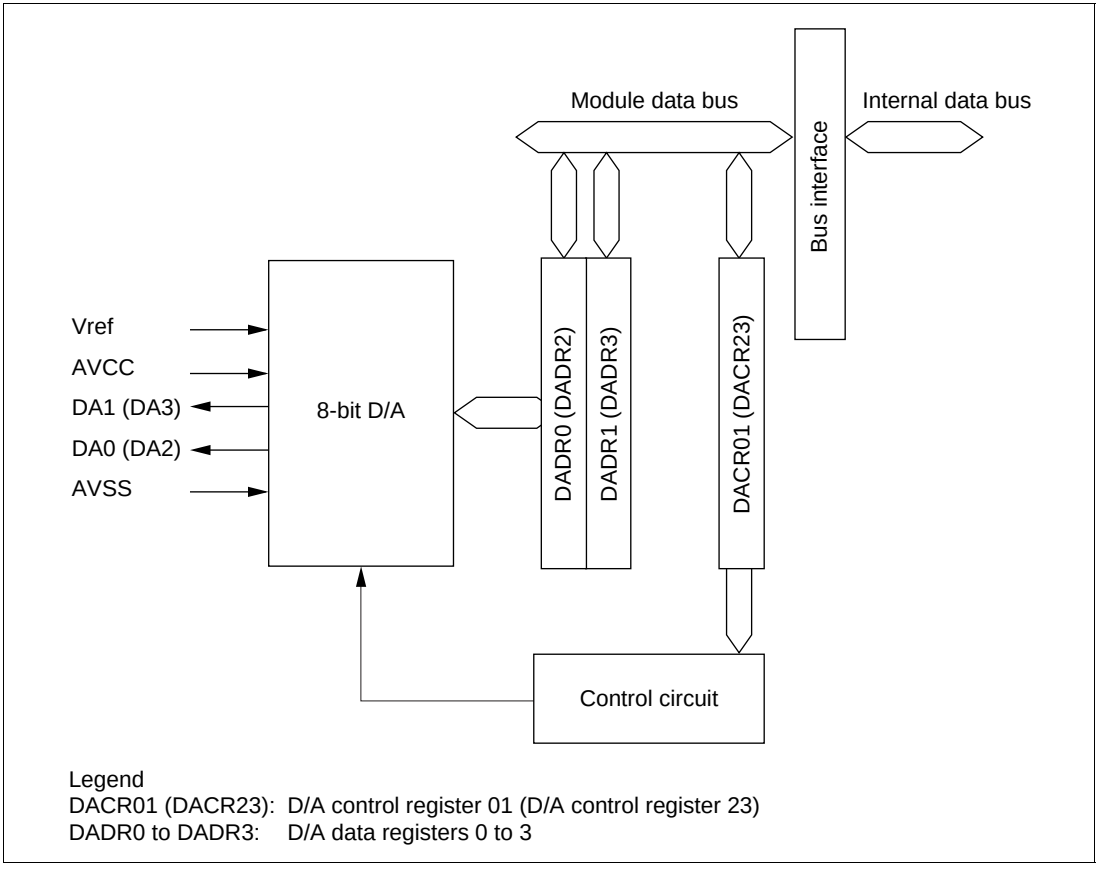


Figure 6.13 Block Diagram of D/A Converter

6.13.3 Pins

Table 6.12 D/A Converter Pins

Name	Abbreviation	I/O	Function
Analog power supply pin	AVCC	Input	Analog circuit power supply
Analog ground pin	AVSS	Input	Analog circuit ground and reference voltage
Analog output pin 0	DA0	Output	Channel 0 analog output
Analog output pin 1	DA1	Output	Channel 1 analog output
Analog output pin 2	DA2	Output	Channel 2 analog output
Analog output pin 3	DA3	Output	Channel 3 analog output
Reference voltage pin	Vref	Input	Analog circuit reference voltage

6.14 RAM

6.14.1 Features

- Sixteen kbytes or eight kbytes of on-chip high-speed static RAM
- Connected to the CPU by a 16-bit data bus, enabling one-state access to both byte data and word data
- Can be enabled or disabled by means of the RAM enable bit (RAME) in the system control register (SYSCR)

6.14.2 Block Diagram

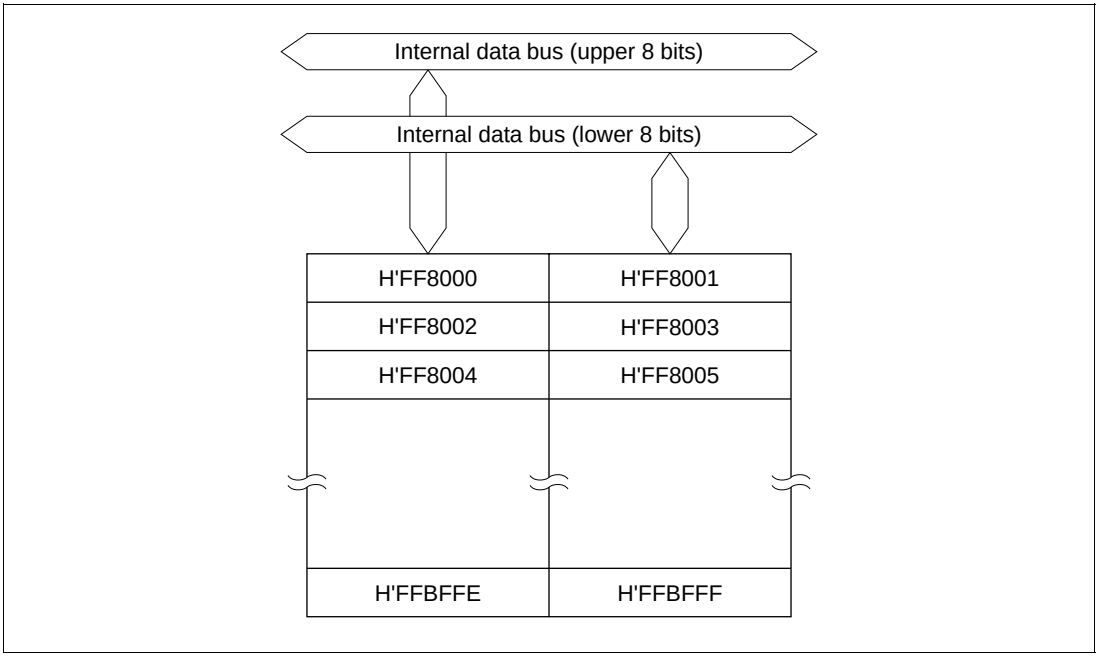


Figure 6.14 Block Diagram of RAM (16 kbytes)

6.15 ROM

6.15.1 Features

- Connected to the bus master by a 16-bit data bus, enabling one-state access to both byte data and word data
- The flash memory version (F-ZTAT) can be erased and programmed on-board as well as with a PROM programmer
- The H8S/2678 has 512 kbytes, the H8S/2676 256 kbytes, and the H8S/2675 128 kbytes, of on-chip mask ROM

6.15.2 Block Diagrams

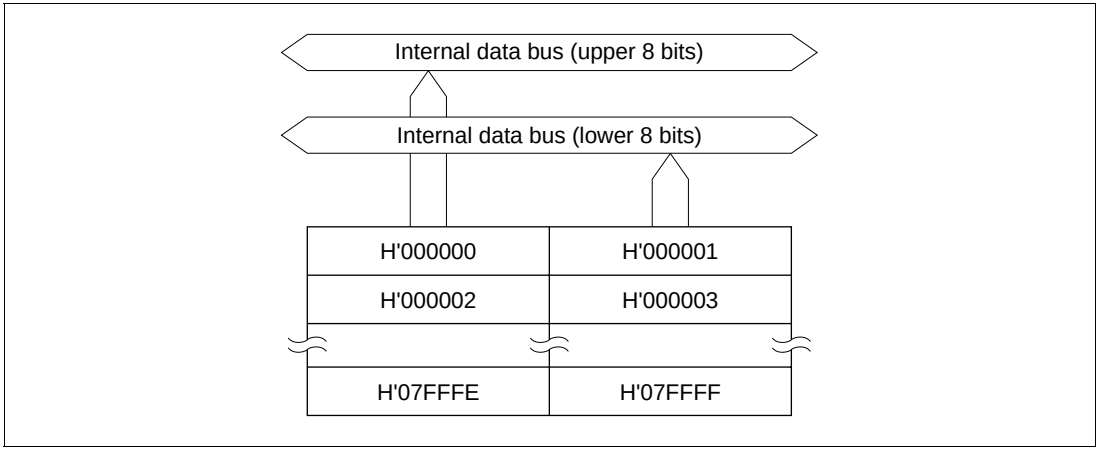
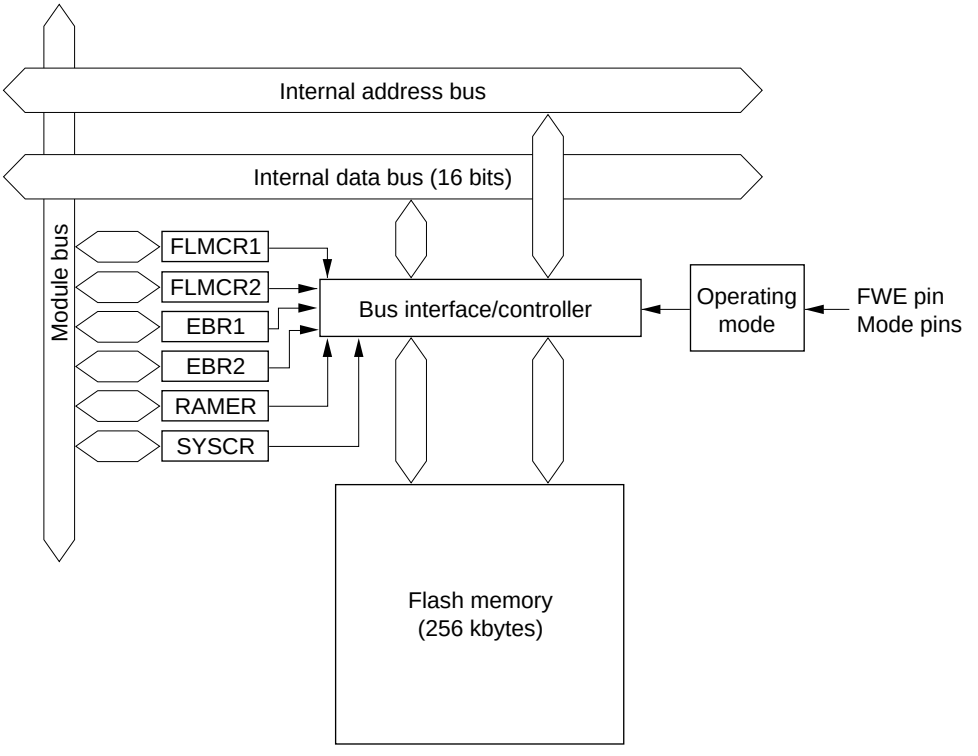


Figure 6.15 Block Diagram of Mask ROM (256 kbytes)



Legend
FLMCR1: Flash memory control register 1
FLMCR2: Flash memory control register 2
EBR1: Erase block register 1
EBR2: Erase block register 2
RAMER: RAM emulation register
SYSCR: System control register

Figure 6.16 Block Diagram of Flash Memory

6.16 Clock Pulse Generator

6.16.1 Features

- Comprises an oscillator, PLL (phase-locked loop) circuit, and frequency divider
- Generates system clock (ø) and internal clock

6.16.2 Block Diagram

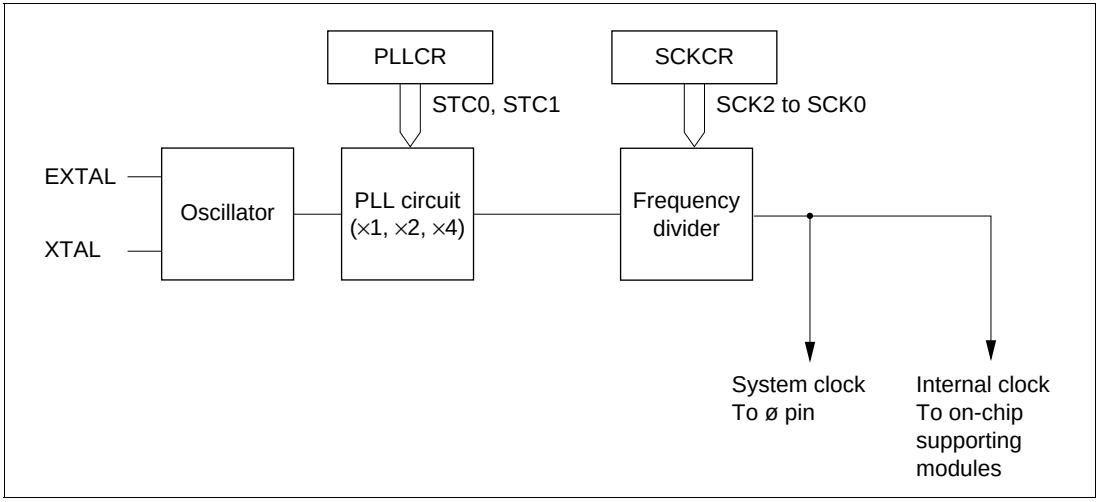


Figure 6.17 Block Diagram of Clock Pulse Generator

Section 7 Electrical Characteristics

7.1 Electrical Characteristics of Mask ROM Version (H8S/2677, H8S/2676, H8S/2675, H8S/2673) and ROMless Version (H8S/2670)

7.1.1 Absolute Maximum Ratings

Table 7.1 lists the absolute maximum ratings.

Table 7.1 Absolute Maximum Ratings — Preliminary —

Item	Symbol	Value	Unit
Power supply voltage	V_{CC} $PLLV_{CC}$	–0.3 to +4.6	V
Input voltage (except port 4, P54 to P57)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (port 4, P54 to P57)	V_{in}	–0.3 to AV_{CC} +0.3	V
Reference power supply voltage	V_{ref}	–0.3 to AV_{CC} +0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +4.6	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75	°C
		Wide-range specifications: –40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded.

Preliminary

7.1.2 DC Characteristics

Table 7.2 DC Characteristics — Preliminary —

Conditions: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V*[1], T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	Port 1, port 2, P50 to P53*[2], port 6*[2], port 8*[2], PF1*[2], PF2*[2], PH2*[2], PH3*[2]	VT^-	$V_{CC} \times 0.2$	—	—	V	
		VT^+	—	—	$V_{CC} \times 0.7$	V	
		$VT^+ - VT^-$	TBD	—	—	V	
	P54 to P57*[2]	VT^-	$AV_{CC} \times 0.2$	—	—	V	
		VT^+	—	—	$AV_{CC} \times 0.7$	V	
		$VT^+ - VT^-$	TBD	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD2 to MD0	V_{IH}	$V_{CC} \times 0.9$	—	V_{CC} + 0.3	V	
	EXTAL		$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V	
	Port 3, P50 to P53*[3], ports 6 to 8 *[3], ports A to H *[3]		$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V	
	Port 4, P54 to P57*[3]		$AV_{CC} \times 0.7$	—	AV_{CC} + 0.3	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD2 to MD0	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL, ports 3 to 8, ports A to H*[3]		–0.3	—	$V_{CC} \times 0.2$	V	
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA

Preliminary

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	$\overline{RES}$	$\|I_{in}\|$	—	—	TBD	µA	V_{in} = 0.5 to V_{CC} – TBD V
	$\overline{STBY}$, NMI, MD2 to MD0		—	—	TBD	µA	
	Port 4, P54 to P57		—	—	TBD	µA	V_{in} = 0.5 to AV_{CC} – TBD V
Three-state leakage current (off state)	Ports 1 to 3, P50 to P53, ports 6 to 8, ports A to H	$\| I_{TSI} \|$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
Input pull-up MOS current	Ports A to E	$-I_p$	10	—	300	µA	V_{CC} = 2.7 to 3.6 V V_{in} = 0 V
Input capacitance	$\overline{RES}$	C_{in}	—	—	30	pF	V_{in} = 0 V
	NMI		—	—	30	pF	f = 1 MHz
	All input pins except $\overline{RES}$ and NMI		—	—	15	pF	T_a = 25°C
Current dissipation*4	Normal operation	I_{CC}*7	—	50 (3.0 V)	95	mA	f = 20 MHz
				80 (3.3 V)	150	mA	f = 33 MHz
	Sleep mode		—	TBD (3.0 V)	TBD	mA	f = 20 MHz
				TBD (3.3 V)	TBD	mA	f = 33 MHz
	Standby mode*5		—	0.01	10	µA	$T_a \leq$ 50°C
			—	—	80	µA	50°C < T_a
	All-module-clocks-stop mode*6		—	TBD	—	µA	50°C < T_a
Analog power supply current	During A/D and D/A conversion	AI_{CC}	—	TBD (3.0 V)	TBD	mA	
	Idle		—	0.01	5.0	µA	
Reference power supply current	During A/D and D/A conversion	AI_{CC}	—	TBD (3.0 V)	TBD	mA	
	Idle		—	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Preliminary

Notes: 1. If the A/D and D/A converters are not used, do not leave the AV_{CC}, V_{ref}, and AV_{SS} pins open. Connect the AV_{CC} and V_{ref} pins to V_{CC}, and the AV_{SS} pin to V_{SS}.
2. When used as $\overline{IRQ0}$ to $\overline{IRQ15}$.
3. When used as other than $\overline{IRQ0}$ to $\overline{IRQ15}$.
4. Current dissipation values are for V_{IH}min = V_{CC} – 0.5 V and V_{IL}max = 0.5 V with all output pins unloaded and all MOS input pull-ups in the off state.
5. The values are for $V_{RAM} \leq V_{CC} < 2.7$ V, V_{IH}min = $V_{CC} \times 0.9$, and V_{IL}max = 0.3 V.
6. Reference value
7. I_{CC} depends on V_{CC} and f as follows:
   I_{CC}max = 1.0 (mA) + TBD (mA/(MHz × V)) × V_{CC} × f (normal operation)
   I_{CC}max = 1.0 (mA) + TBD (mA/(MHz × V)) × V_{CC} × f (sleep mode)

Table 7.3 Permissible Output Currents — Preliminary —

Conditions: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V*[1], T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	All output pins	I_{OL}	—	—	2.0	mA
Permissible output low current (total)	Total of all output pins	ΣI_{OL}	—	—	TBD	mA
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	$\Sigma -I_{OH}$	—	—	TBD	mA

Notes: 1. If the A/D and D/A converters are not used, do not leave the AV_{CC}, V_{ref}, and AV_{SS} pins open. Connect the AV_{CC} and V_{ref} pins to V_{CC}, and the AV_{SS} pin to V_{SS}.
2. To protect chip reliability, do not exceed the output current values in table 7.4.

Preliminary

7.1.3 AC Characteristics

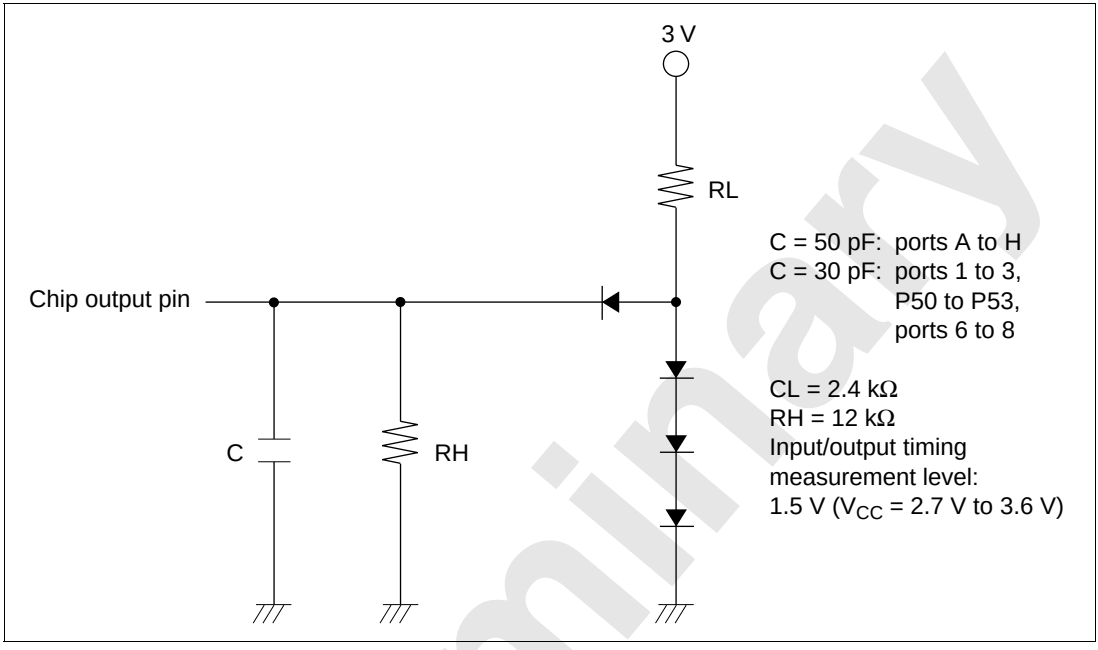


Figure 7.1 Output Load Circuit

Preliminary

Table 7.4 Clock Timing **— Preliminary —**

Condition A*: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 33 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

* In planning stage

		Condition A		Condition B			Test
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
Clock cycle time	t_{cyc}	50	500	30.3	500	ns	Figure 7.2
Clock pulse high width	t_{CH}	20	—	10	—	ns	Figure 7.2
Clock pulse low width	t_{CL}	20	—	10	—	ns	
Clock rise time	t_{Cr}	—	5	—	5	ns	
Clock fall time	t_{Cf}	—	5	—	5	ns	
Reset oscillation settling time (crystal)	t_{OSC1}	10	—	10	—	ms	Figure 7.3
Software standby oscillation settling time (crystal)	t_{OSC2}	10	—	10	—	ms	
External clock output delay settling time	t_{DEXT}	500	—	500	—	µs	Figure 7.3

Preliminary

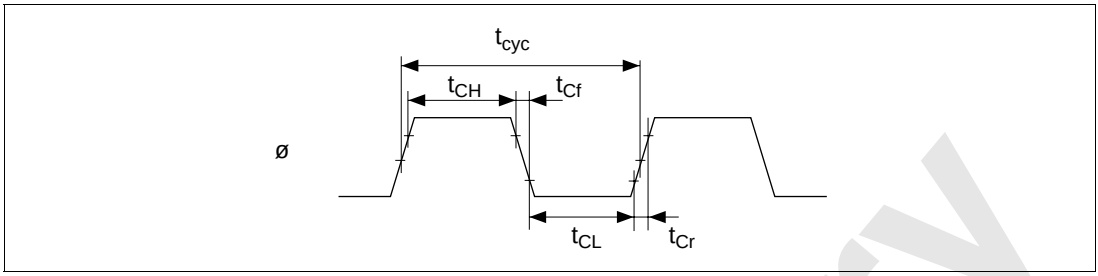


Figure 7.2 System Clock Timing

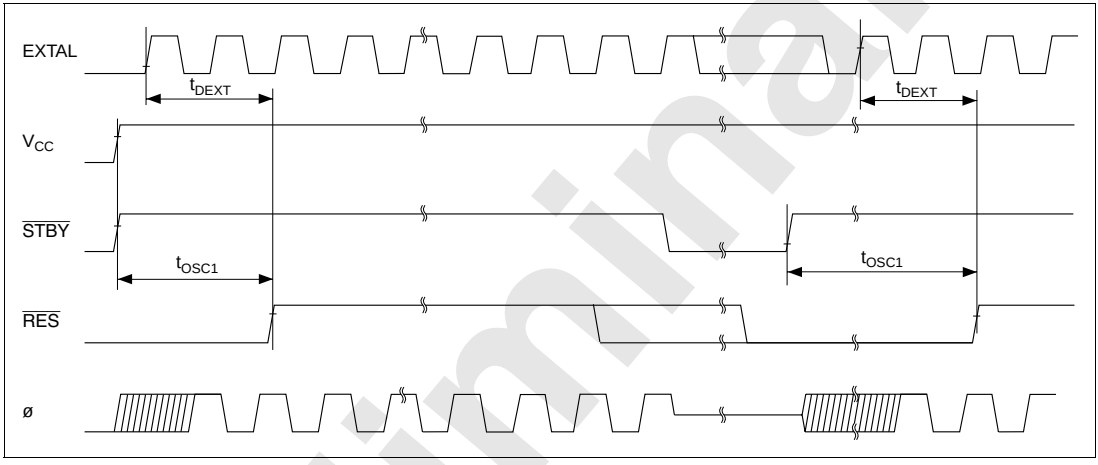


Figure 7.3 Oscillation Settling Timing

Preliminary

Table 7.5 Control Signal Timing **— Preliminary —**

Condition A*: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 33 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

* In planning stage

		Condition A		Condition B			Test
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
$\overline{RES}$ setup time	t_{RESS}	200	—	200	—	ns	Figure 7.4
$\overline{RES}$ pulse width	t_{RESW}	20	—	20	—	t_{cyc}	
NMI setup time	t_{NMIS}	150	—	150	—	ns	Figure 7.5
NMI hold time	t_{NMIH}	10	—	10	—		
NMI pulse width (in recovery from software standby mode)	t_{NMIW}	200	—	200	—		
$\overline{IRQ}$ setup time	t_{IRQS}	150	—	150	—	ns	
$\overline{IRQ}$ hold time	t_{IRQH}	10	—	10	—		
$\overline{IRQ}$ pulse width (in recovery from software standby mode)	t_{IRQW}	200	—	200	—		

Preliminary

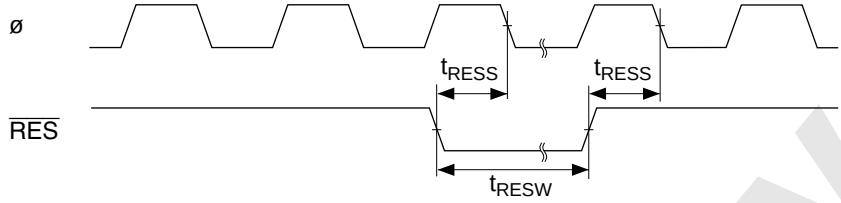
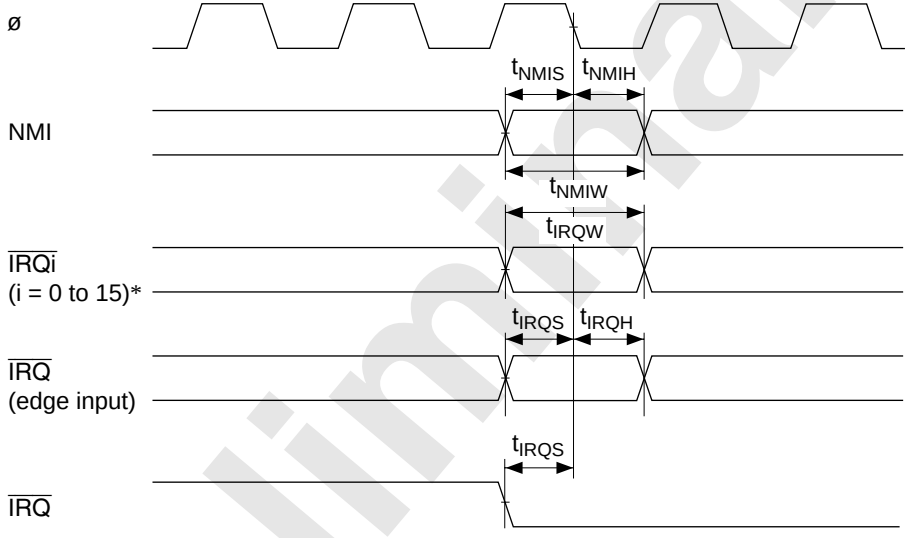


Figure 7.4 Reset Input Timing



Note: * Necessary for SSIER setting to clear software standby mode.

Figure 7.5 Interrupt Input Timing

Preliminary

Table 7.6 Bus Timing **— Preliminary —**

Condition A*: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 33 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

* In planning stage

		Condition A		Condition B			Test
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
Address delay time	t_{AD}	—	20	—	20	ns	Figure 7.6 to Figure 7.19
Address setup time 1	t_{AS1}	$0.5 \times t_{cyc} - 15$	—	$0.5 \times t_{cyc} - 13$	—	ns	
Address setup time 2	t_{AS2}	$1.0 \times t_{cyc} - 15$	—	$1.0 \times t_{cyc} - 13$	—	ns	
Address setup time 3	t_{AS3}	$1.5 \times t_{cyc} - 15$	—	$1.5 \times t_{cyc} - 13$	—	ns	
Address setup time 4	t_{AS4}	$2.0 \times t_{cyc} - 15$	—	$2.0 \times t_{cyc} - 13$	—	ns	
Address hold time 1	t_{AH1}	$0.5 \times t_{cyc} - 10$	—	$0.5 \times t_{cyc} - 8$	—	ns	
Address hold time 2	t_{AH2}	$1.0 \times t_{cyc} - 10$	—	$1.0 \times t_{cyc} - 8$	—	ns	
Address hold time 3	t_{AH3}	$1.5 \times t_{cyc} - 10$	—	$1.5 \times t_{cyc} - 8$	—	ns	
$\overline{CS}$ delay time 1	t_{CSD1}	—	20	—	15	ns	
$\overline{CS}$ delay time 2	t_{CSD2}	—	20	—	15	ns	
$\overline{CS}$ delay time 3	t_{CSD3}	—	20	—	20	ns	
$\overline{AS}$ delay time	t_{ASD}	—	20	—	15	ns	
$\overline{RD}$ delay time 1	t_{RSD1}	—	20	—	15	ns	
$\overline{RD}$ delay time 2	t_{RSD2}	—	20	—	15	ns	
Read data setup time 1	t_{RDS1}	15	—	15	—	ns	
Read data setup time 2	t_{RDS2}	15	—	15	—	ns	
Read data hold time 1	t_{RDH1}	0	—	0	—	ns	

Preliminary

Item	Symbol	Condition A		Condition B		Unit	Test Conditions
		Min	Max	Min	Max		
Read data hold time 2	t_{RDH2}	0	—	0	—	ns	Figure 7.6 to Figure 7.19
Read data access time 1	t_{AC1}	—	$1.0 \times t_{cyc} - 25$	—	$1.0 \times t_{cyc} - 20$	ns	
Read data access time 2	t_{AC2}	—	$1.5 \times t_{cyc} - 25$	—	$1.5 \times t_{cyc} - 20$	ns	
Read data access time 3	t_{AC3}	—	$2.0 \times t_{cyc} - 25$	—	$2.0 \times t_{cyc} - 20$	ns	
Read data access time 4	t_{AC4}	—	$2.5 \times t_{cyc} - 25$	—	$2.5 \times t_{cyc} - 20$	ns	
Read data access time 5	t_{AC5}	—	$1.0 \times t_{cyc} - 25$	—	$1.0 \times t_{cyc} - 20$	ns	
Read data access time 6	t_{AC6}	—	$2.0 \times t_{cyc} - 25$	—	$2.0 \times t_{cyc} - 20$	ns	
Read data access time 7	t_{AC7}	—	$4.0 \times t_{cyc} - 25$	—	$4.0 \times t_{cyc} - 20$	ns	
Read data access time 8	t_{AC8}	—	$3.0 \times t_{cyc} - 25$	—	$3.0 \times t_{cyc} - 20$	ns	
Address read data access time 1	t_{AA1}	—	$1.0 \times t_{cyc} - 25$	—	$1.0 \times t_{cyc} - 20$	ns	
Address read data access time 2	t_{AA2}	—	$1.5 \times t_{cyc} - 25$	—	$1.5 \times t_{cyc} - 20$	ns	
Address read data access time 3	t_{AA3}	—	$2.0 \times t_{cyc} - 25$	—	$2.0 \times t_{cyc} - 20$	ns	
Address read data access time 4	t_{AA4}	—	$2.5 \times t_{cyc} - 25$	—	$2.5 \times t_{cyc} - 20$	ns	
Address read data access time 5	t_{AA5}	—	$3.0 \times t_{cyc} - 25$	—	$3.0 \times t_{cyc} - 20$	ns	
$\overline{WR}$ delay time 1	t_{WRD1}	—	20	—	15	ns	
$\overline{WR}$ delay time 2	t_{WRD2}	—	20	—	15	ns	
$\overline{WR}$ pulse width 1	t_{WSW1}	$1.0 \times t_{cyc} - 20$	—	$1.0 \times t_{cyc} - 13$	—	ns	
$\overline{WR}$ pulse width 2	t_{WSW2}	$1.5 \times t_{cyc} - 20$	—	$1.5 \times t_{cyc} - 13$	—	ns	
Write data delay time	t_{WDD}	—	30	—	20	ns	
Write data setup time 1	t_{WDS1}	$0.5 \times t_{cyc} - 20$	—	$0.5 \times t_{cyc} - 13$	—	ns	

Preliminary

Item	Symbol	Condition A		Condition B		Unit	Test Conditions
		Min	Max	Min	Max		
Write data setup time 2	t_{WDS2}	$1.0 \times t_{cyc} - 20$	—	$1.0 \times t_{cyc} - 13$	—	ns	Figure 7.6 to Figure 7.19
Write data setup time 3	t_{WDS3}	$1.5 \times t_{cyc} - 20$	—	$1.5 \times t_{cyc} - 13$	—	ns	
Write data hold time 1	t_{WDH1}	$0.5 \times t_{cyc} - 10$	—	$0.5 \times t_{cyc} - 8$	—	ns	
Write data hold time 2	t_{WDH2}	$1.0 \times t_{cyc} - 10$	—	$1.0 \times t_{cyc} - 8$	—	ns	
Write data hold time 3	t_{WDH3}	$1.5 \times t_{cyc} - 10$	—	$1.5 \times t_{cyc} - 8$	—	ns	
Write command setup time 1	t_{WCS1}	$0.5 \times t_{cyc} - 10$	—	$0.5 \times t_{cyc} - 10$	—	ns	
Write command setup time 2	t_{WCS2}	$1.0 \times t_{cyc} - 10$	—	$1.0 \times t_{cyc} - 10$	—	ns	
Write command hold time 1	t_{WCH1}	$0.5 \times t_{cyc} - 10$	—	$0.5 \times t_{cyc} - 10$	—	ns	
Write command hold time 2	t_{WCH2}	$1.0 \times t_{cyc} - 10$	—	$1.0 \times t_{cyc} - 10$	—	ns	
Read command setup time 1	t_{RCS1}	$1.5 \times t_{cyc} - 10$	—	$1.5 \times t_{cyc} - 10$	—	ns	
Read command setup time 2	t_{RCS2}	$2.0 \times t_{cyc} - 10$	—	$2.0 \times t_{cyc} - 10$	—	ns	
Read command hold time	t_{RCH}	$0.5 \times t_{cyc} - 10$	—	$0.5 \times t_{cyc} - 10$	—	ns	
$\overline{CAS}$ delay time 1	t_{CASD1}	—	20	—	15	ns	
$\overline{CAS}$ delay time 2	t_{CASD2}	—	20	—	15	ns	
$\overline{CAS}$ setup time 1	t_{CSR1}	$0.5 \times t_{cyc} - 10$	—	$0.5 \times t_{cyc} - 10$	—	ns	
$\overline{CAS}$ setup time 2	t_{CSR2}	$1.5 \times t_{cyc} - 10$	—	$1.5 \times t_{cyc} - 10$	—	ns	
$\overline{CAS}$ pulse width 1	t_{CASW1}	$1.0 \times t_{cyc} - 20$	—	$1.0 \times t_{cyc} - 20$	—	ns	
$\overline{CAS}$ pulse width 2	t_{CASW2}	$1.5 \times t_{cyc} - 20$	—	$1.5 \times t_{cyc} - 20$	—	ns	
$\overline{CAS}$ precharge time 1	t_{CPW1}	$1.0 \times t_{cyc} - 20$	—	$1.0 \times t_{cyc} - 20$	—	ns	
$\overline{CAS}$ precharge time 2	t_{CPW2}	$1.5 \times t_{cyc} - 20$	—	$1.5 \times t_{cyc} - 20$	—	ns	
$\overline{OE}$ delay time 1	t_{OED1}	—	20	—	15	ns	
$\overline{OE}$ delay time 2	t_{OED2}	—	20	—	15	ns	

Preliminary

Item	Symbol	Condition A		Condition B		Unit	Test Conditions
		Min	Max	Min	Max		
Precharge time 1	t_{PCH1}	$1.0 \times t_{cyc} - 20$	—	$1.0 \times t_{cyc} - 20$	—	ns	Figure 7.6 to Figure 7.19
Precharge time 2	t_{PCH2}	$1.5 \times t_{cyc} - 20$	—	$1.5 \times t_{cyc} - 20$	—	ns	
Self-refresh precharge time 1	t_{RPS1}	$2.5 \times t_{cyc} - 20$	—	$2.5 \times t_{cyc} - 20$	—	ns	Figure 7.20 Figure 7.21
Self-refresh precharge time 2	t_{RPS2}	$3.0 \times t_{cyc} - 20$	—	$3.0 \times t_{cyc} - 20$	—	ns	
$\overline{WAIT}$ setup time	t_{WTS}	30	—	25	—	ns	Figure 7.14
$\overline{WAIT}$ hold time	t_{WTH}	5	—	5	—	ns	
$\overline{BREQ}$ setup time	t_{BREQS}	30	—	30	—	ns	Figure 7.22
$\overline{BACK}$ delay time	t_{BACD}	—	15	—	15	ns	
Bus floating time	t_{BZD}	—	50	—	40	ns	
$\overline{BREQO}$ delay time	t_{BRQOD}	—	30	—	25	ns	Figure 7.23

Preliminary

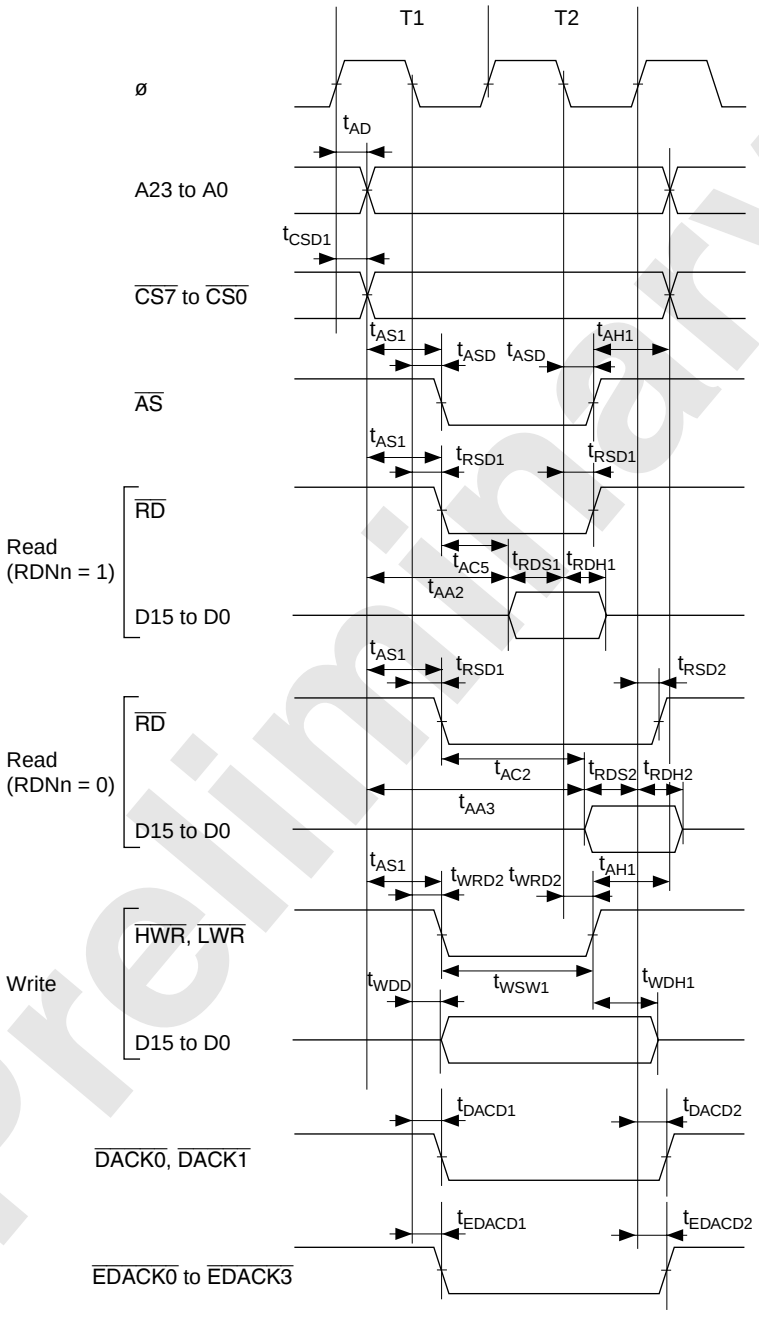


Figure 7.6 Basic Bus Timing: Two-State Access

Preliminary

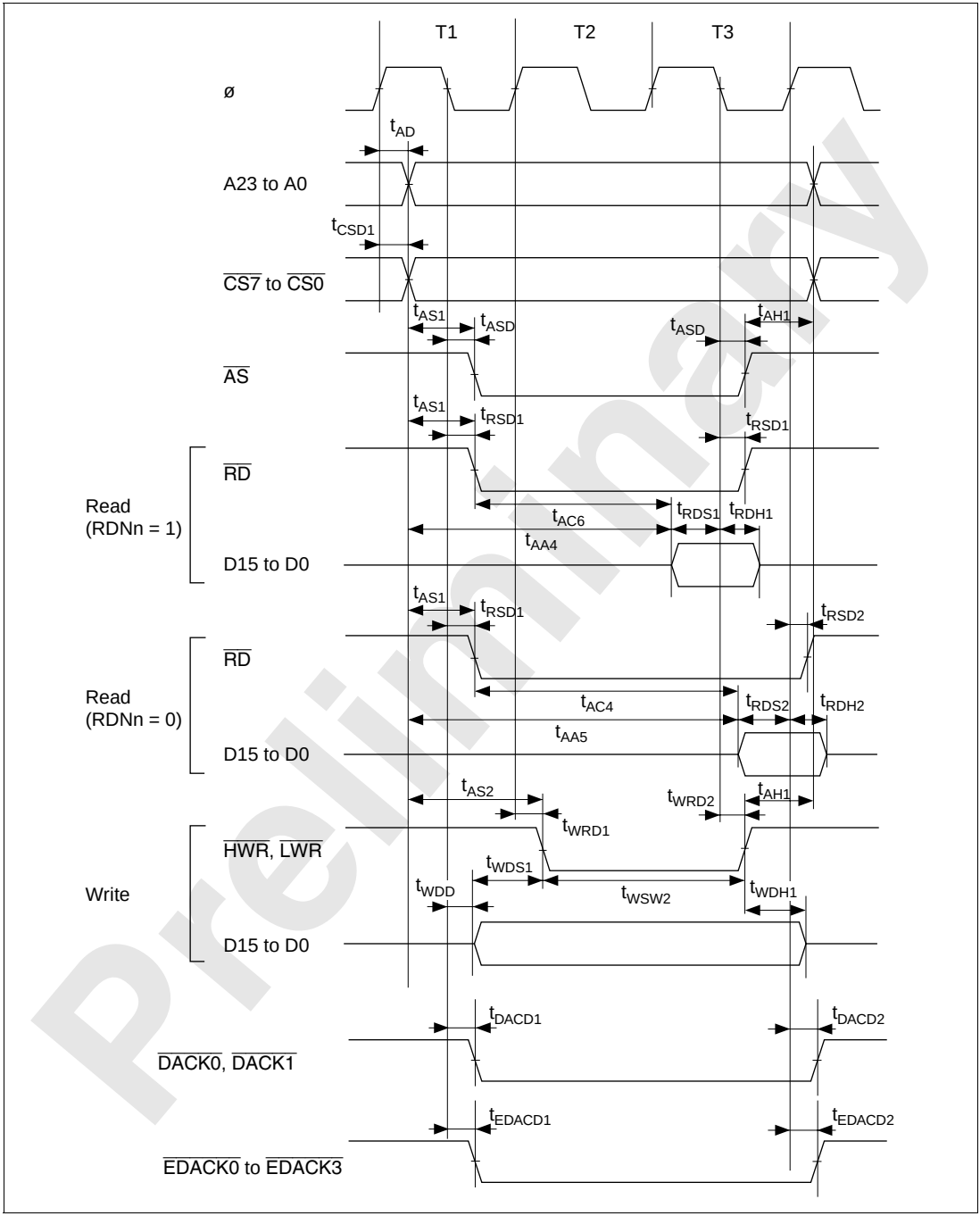


Figure 7.7 Basic Bus Timing: Three-State Access

Preliminary

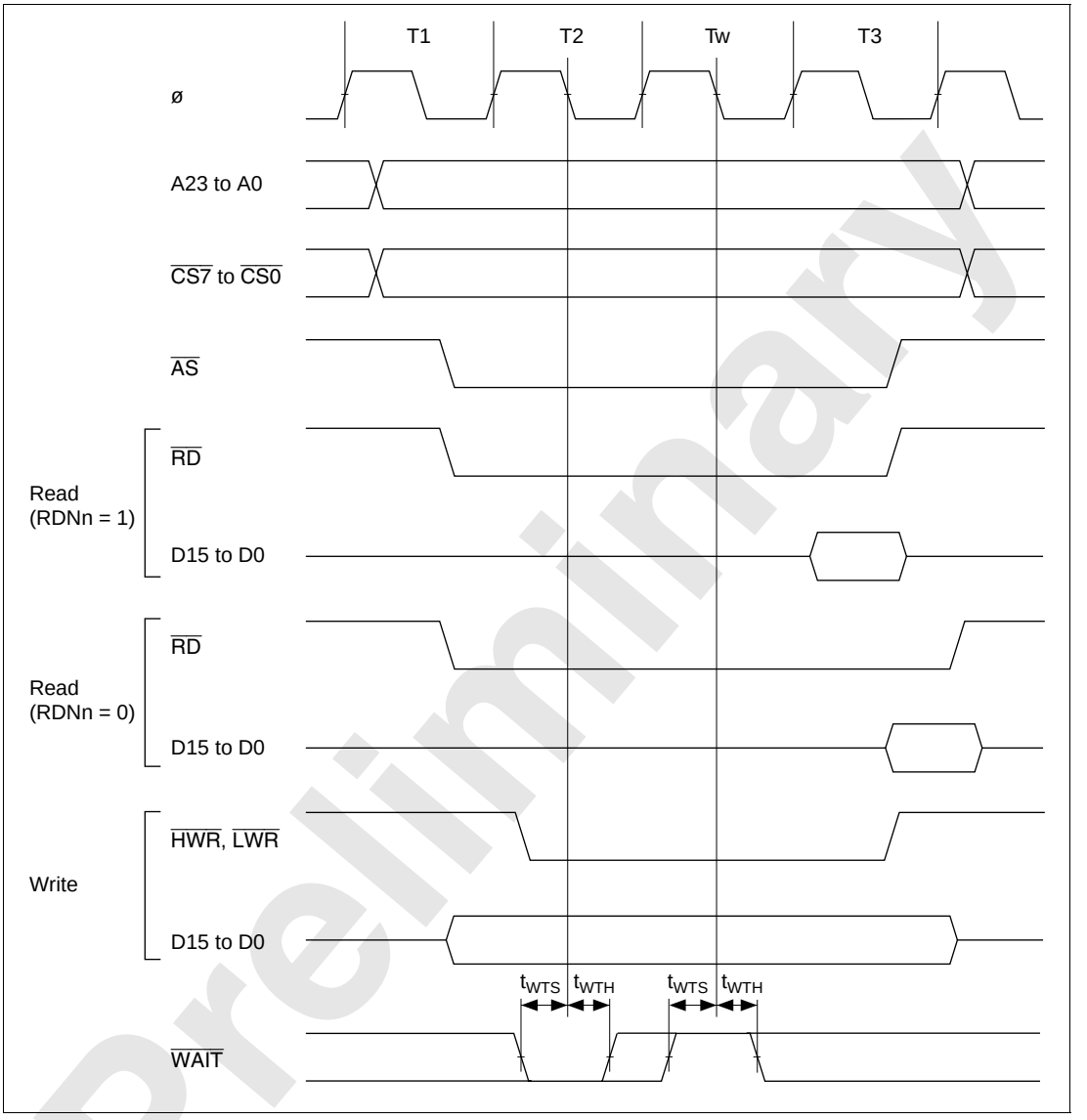


Figure 7.8 Basic Bus Timing: Three-State Access, One Wait

Preliminary

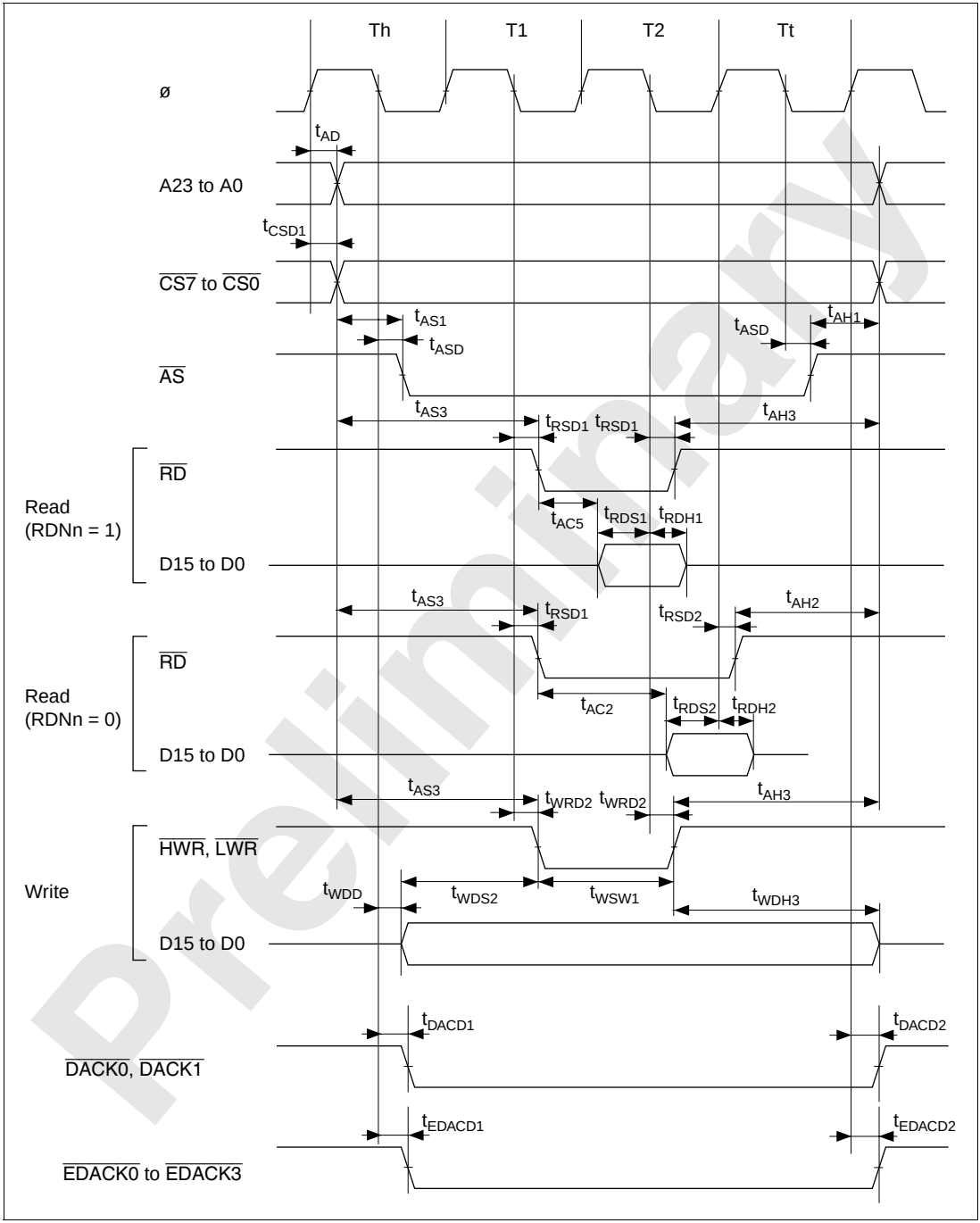


Figure 7.9 Basic Bus Timing: Two-State Access ($\overline{CS}$ Assertion Period Extended)

Preliminary

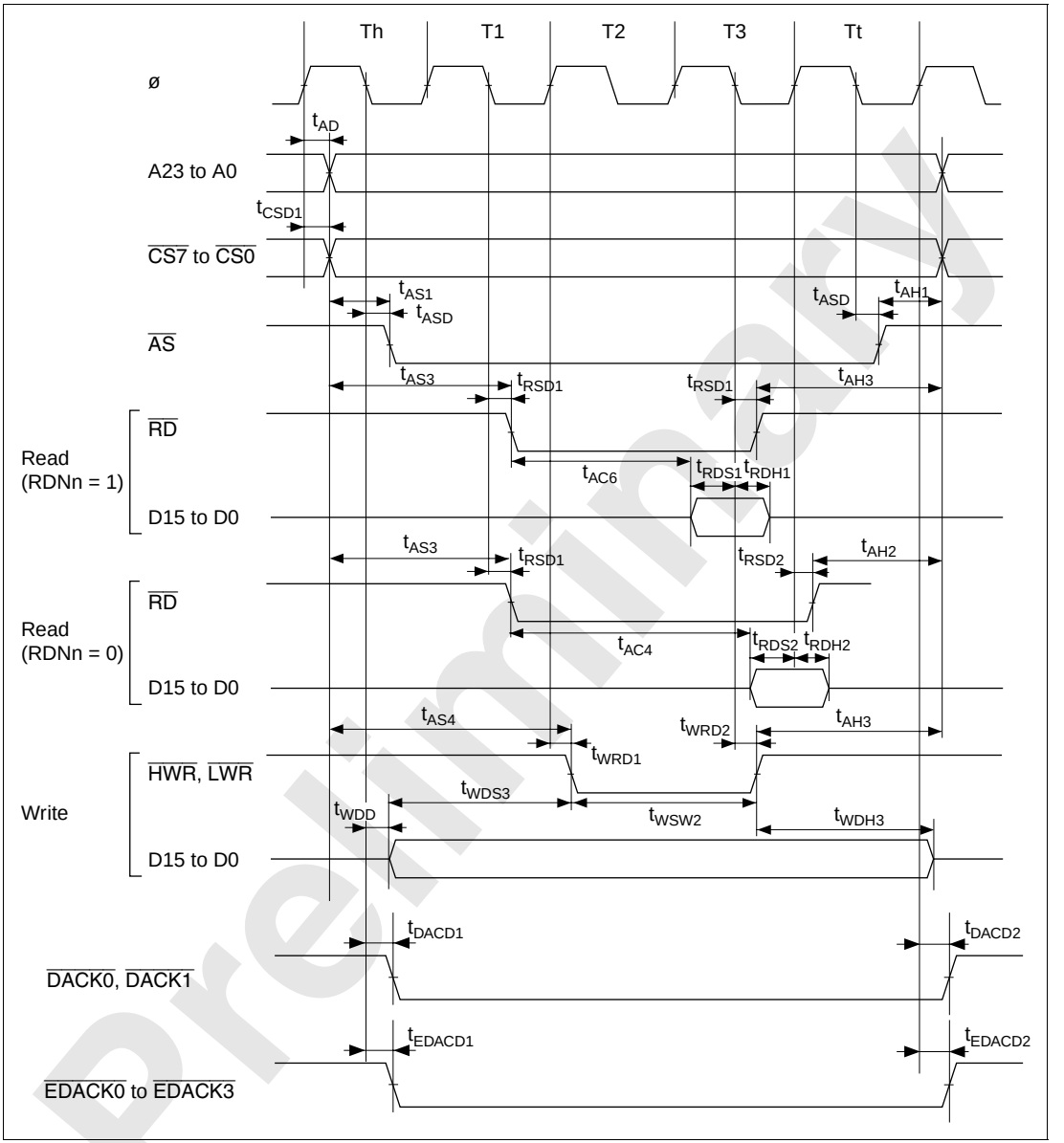


Figure 7.10 Basic Bus Timing: Three-State Access ($\overline{CS}$ Assertion Period Extended)

Preliminary

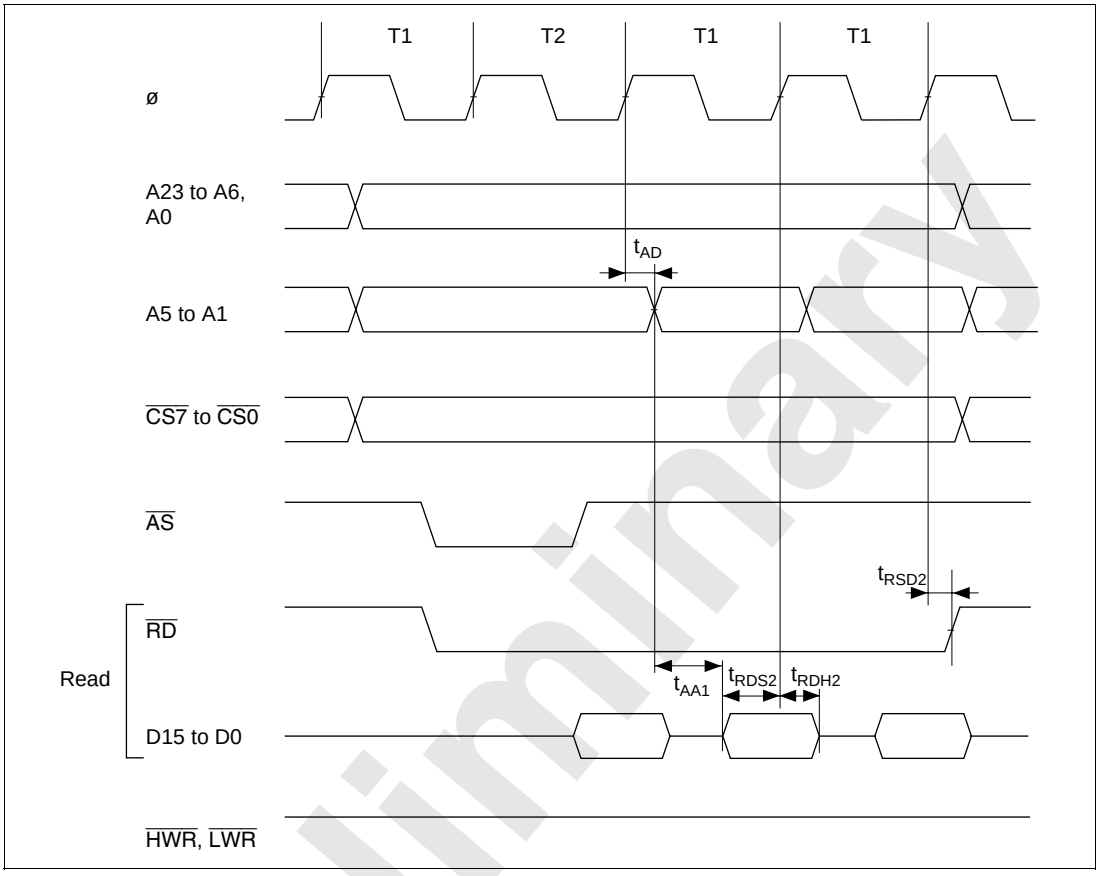


Figure 7.11 Burst ROM Access Timing: One-State Burst Access

Preliminary

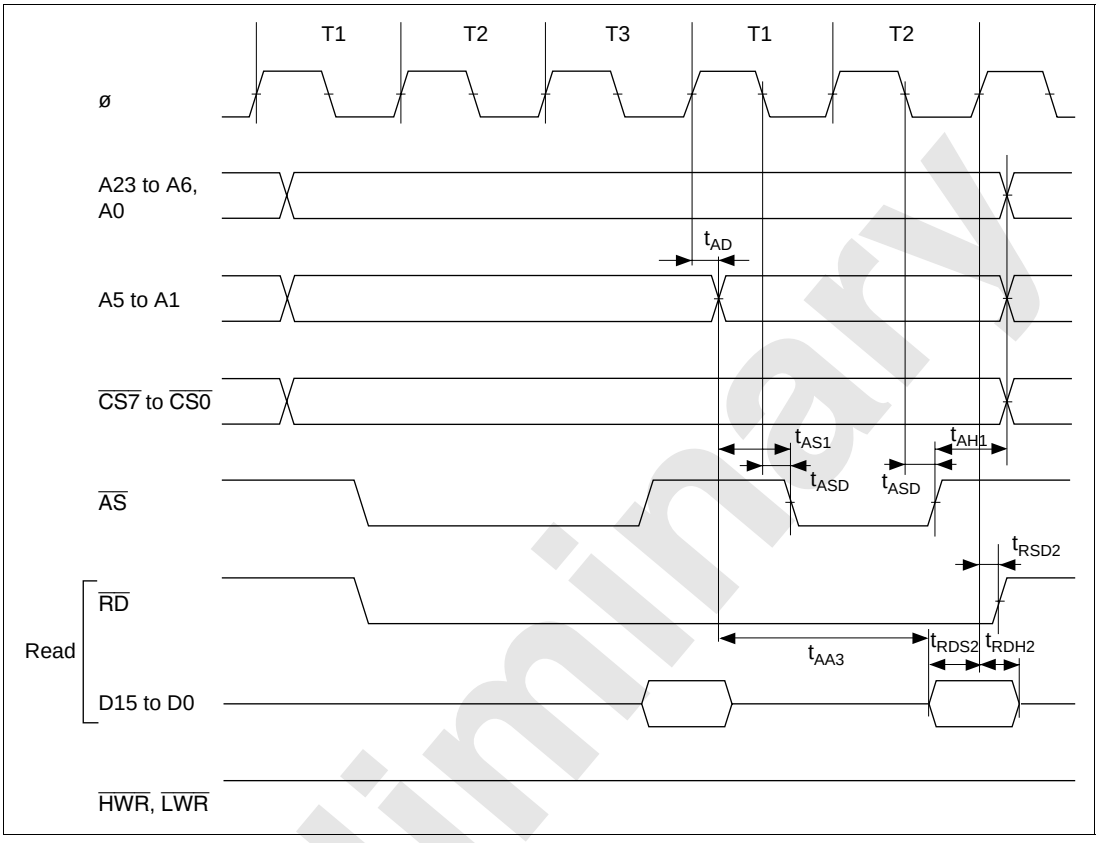
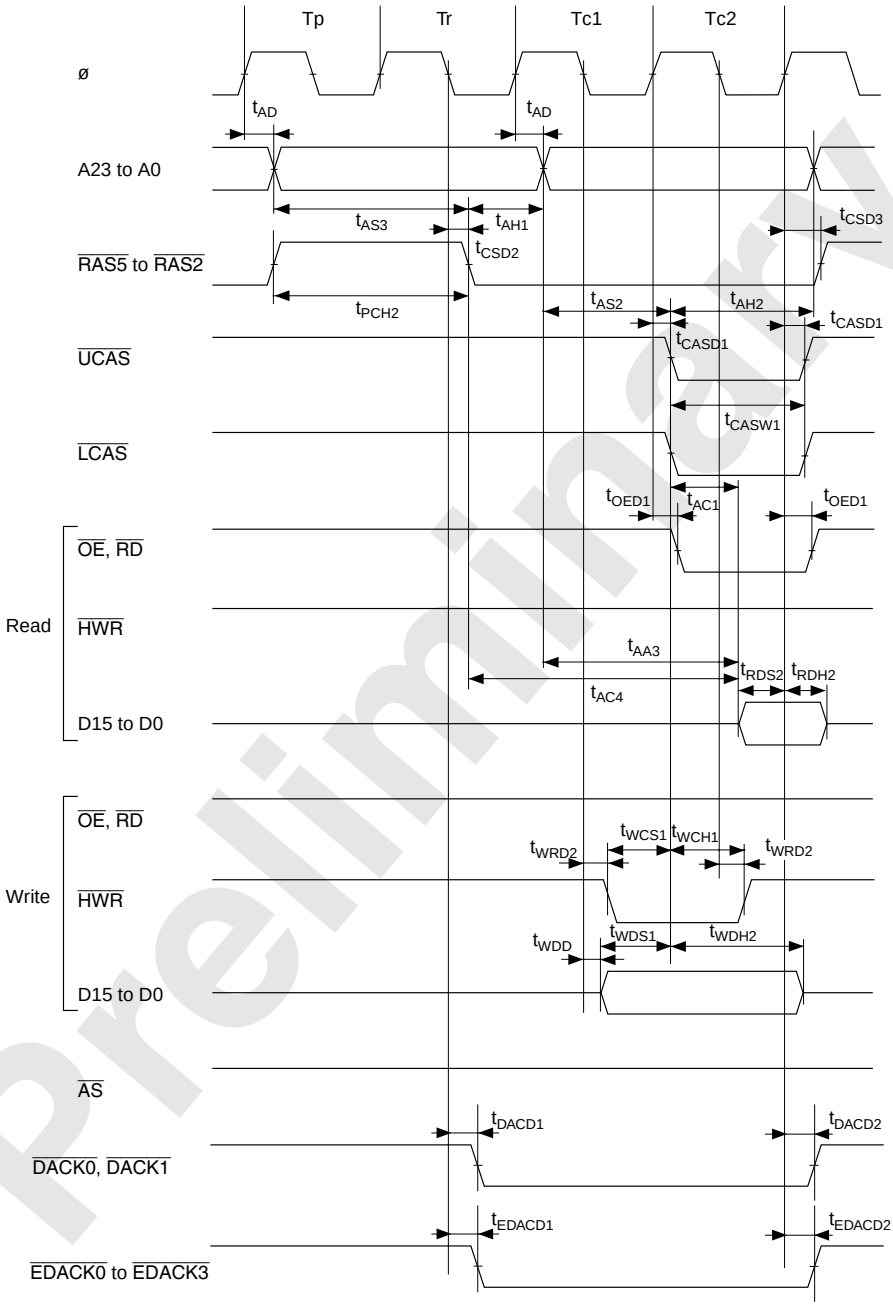


Figure 7.12 Burst ROM Access Timing: Two-State Burst Access

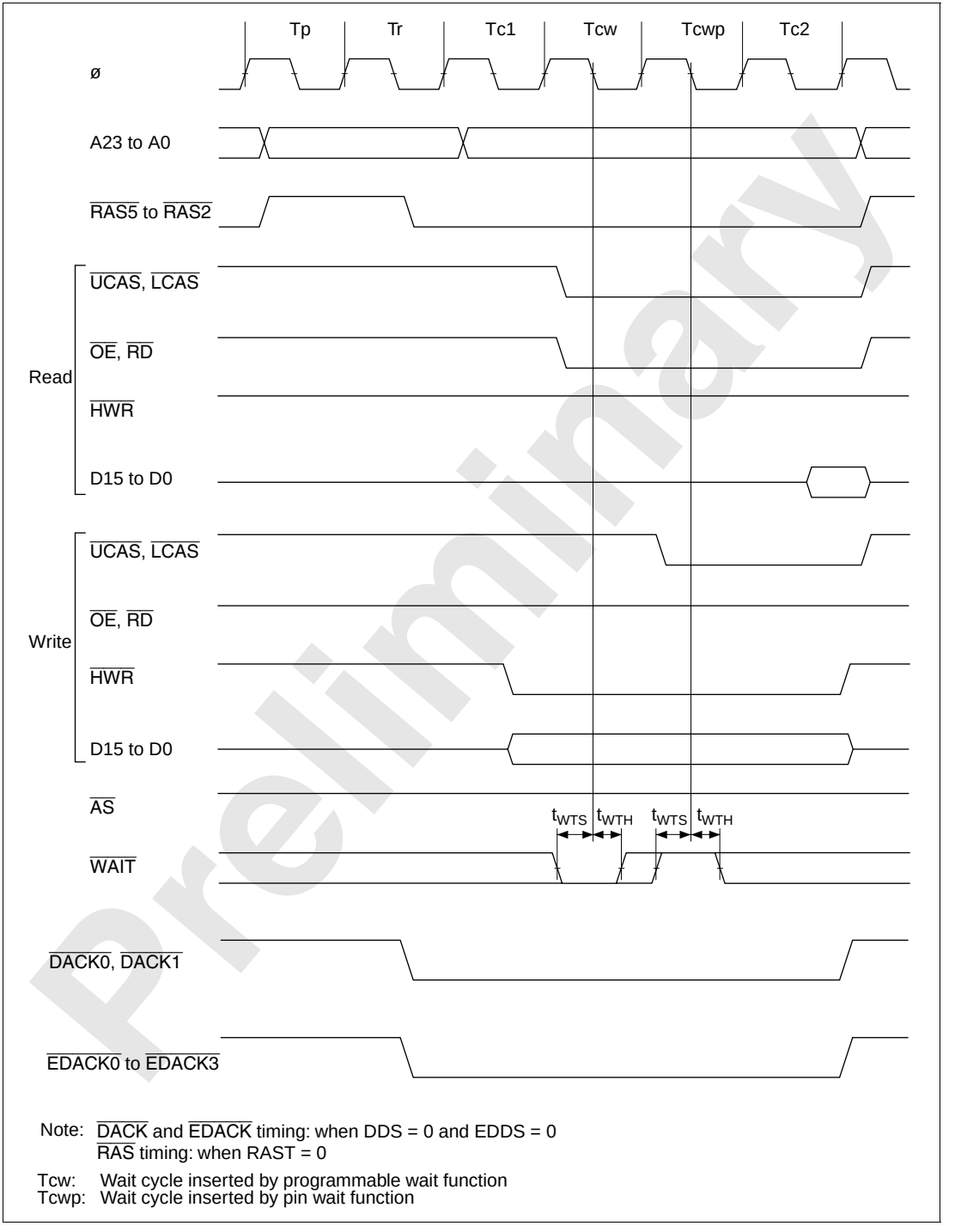
Preliminary



Note: DACK and EDACK timing: when DDS = 0 and EDDS = 0
RAS timing: when RAST = 0

Figure 7.13 DRAM Access Timing: Two-State Access

Preliminary

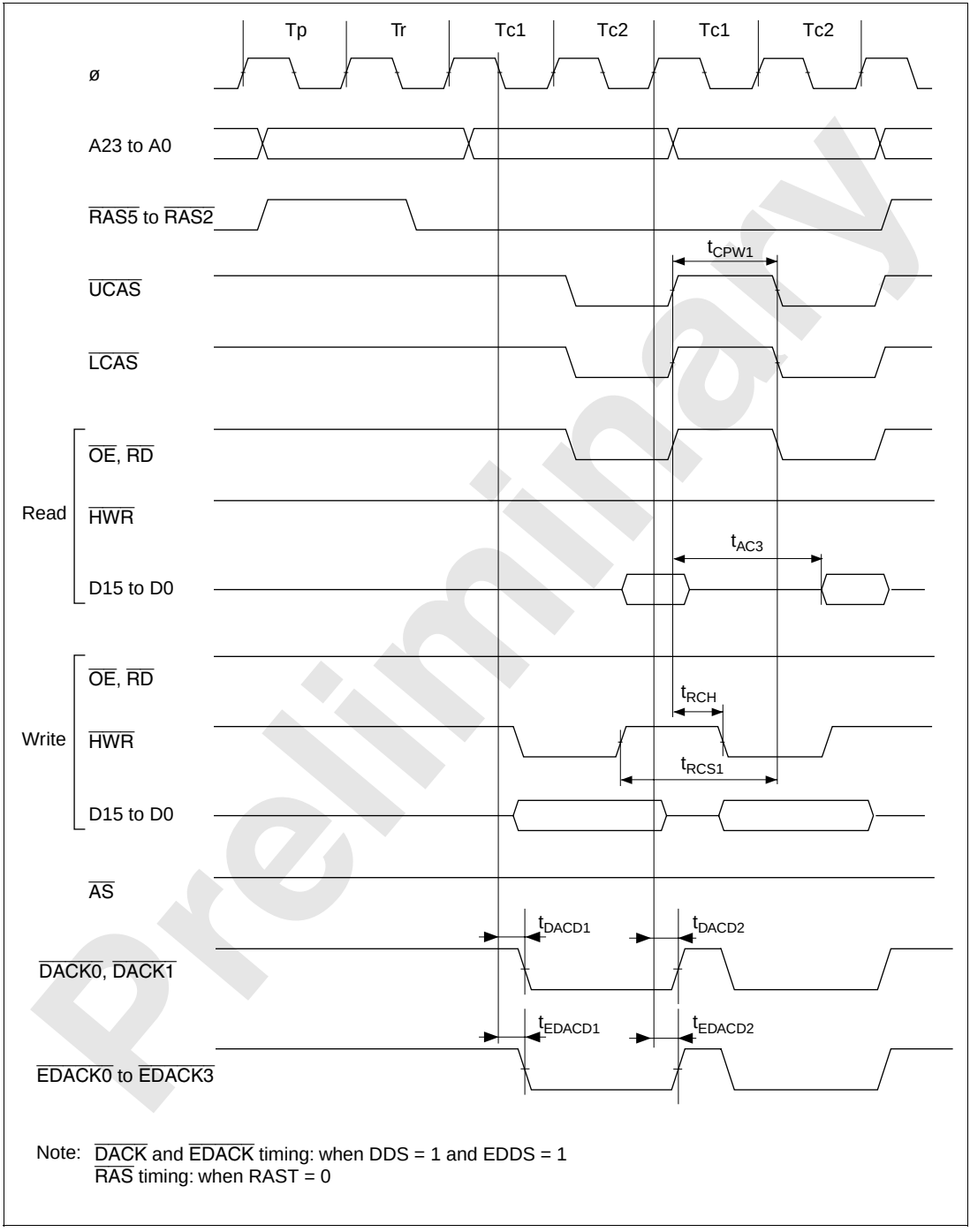


Note: DACK and EDACK timing: when DDS = 0 and EDDS = 0
RAS timing: when RAST = 0

Tcw: Wait cycle inserted by programmable wait function
Tcwp: Wait cycle inserted by pin wait function

Figure 7.14 DRAM Access Timing: Two-State Access, One Wait

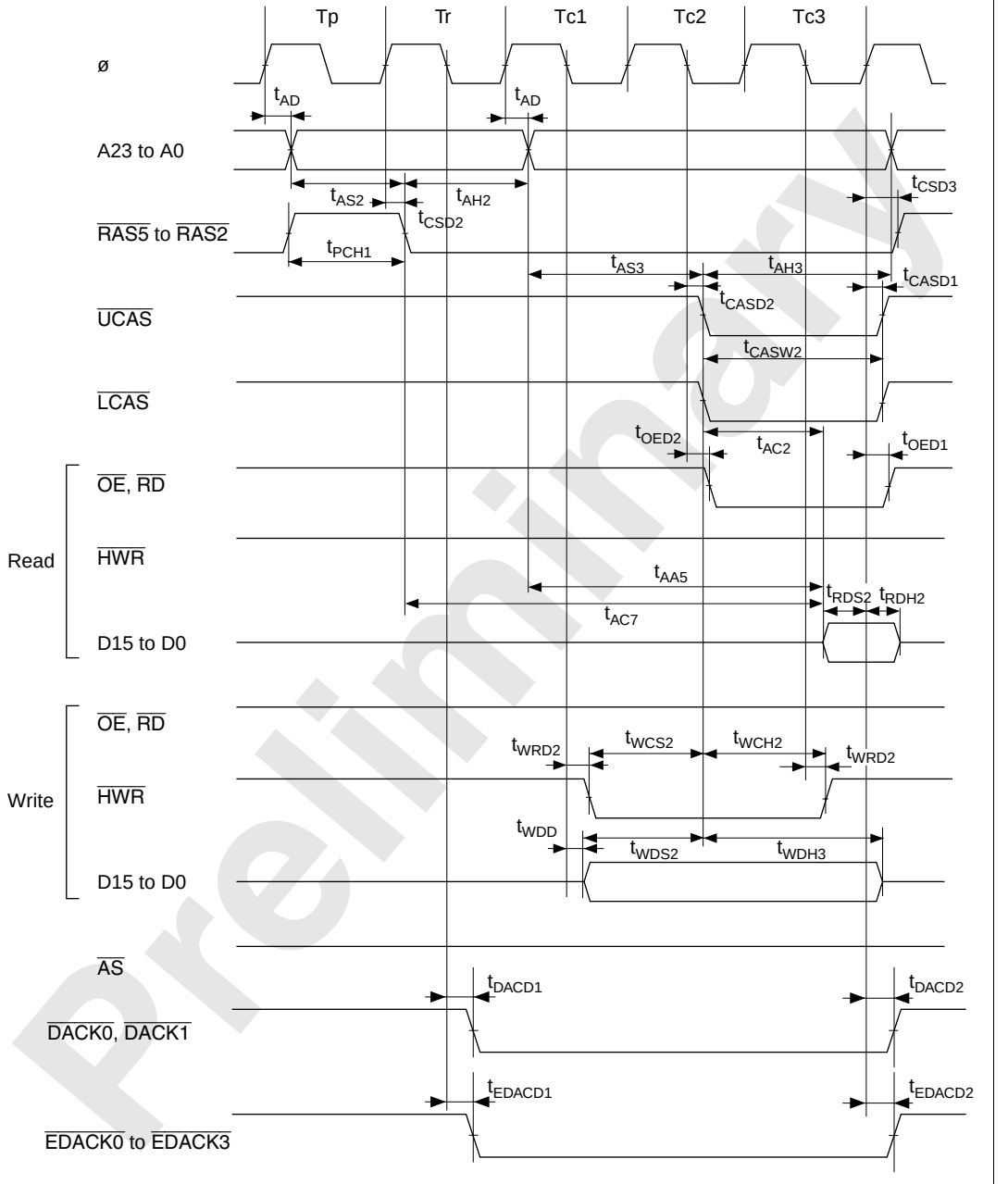
Preliminary



Note: DACK and EDACK timing: when DDS = 1 and EDDS = 1
RAS timing: when RAST = 0

Preliminary

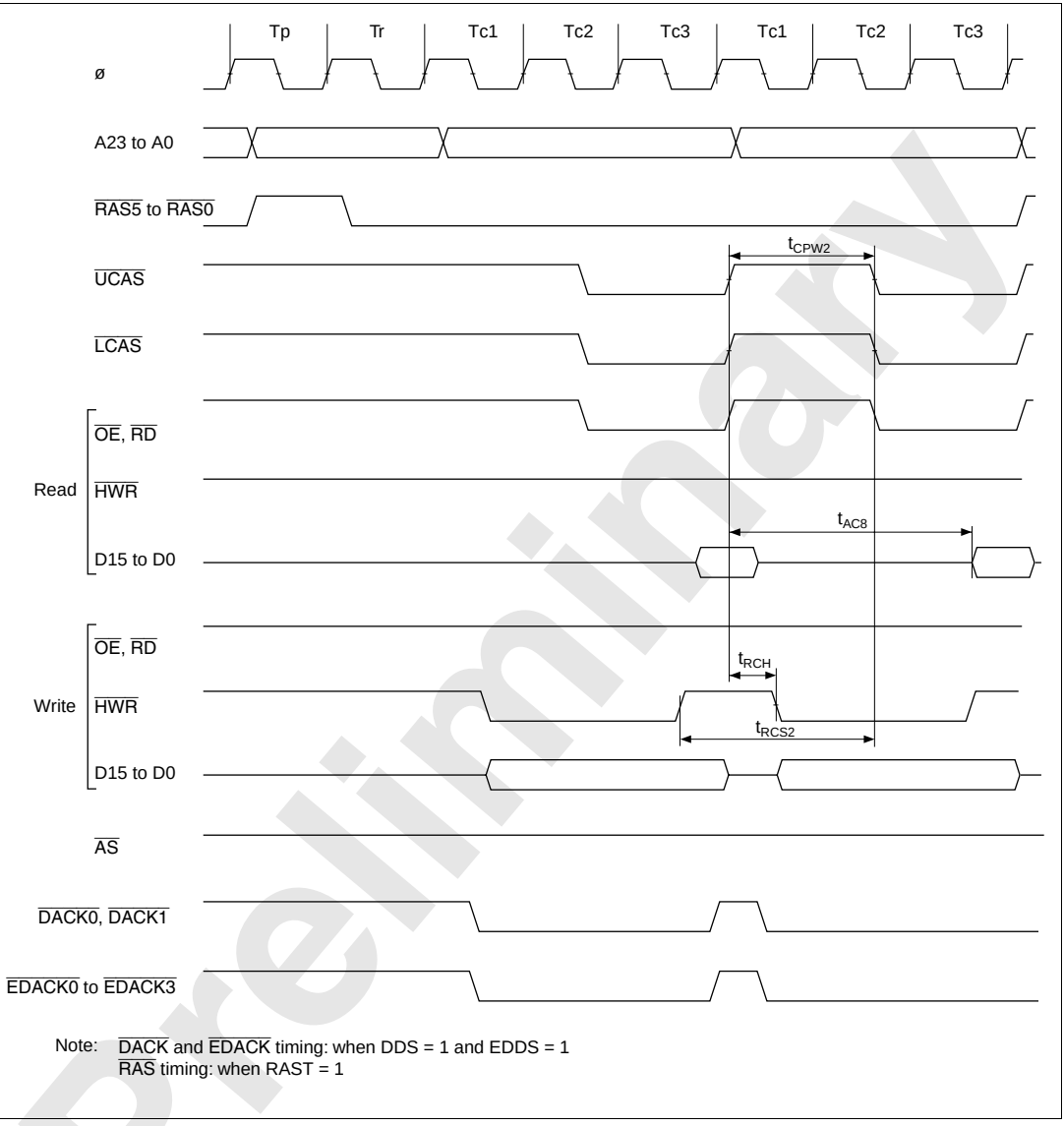
Figure 7.15 DRAM Access Timing: Two-State Burst Access



Note: $\overline{\text{DACK}}$ and $\overline{\text{EDACK}}$ timing: when DDS = 0 and EDDS = 0
$\overline{\text{RAS}}$ timing: when RAST = 1

Figure 7.16 DRAM Access Timing: Three-State Access (RAST = 1)

Preliminary



Note: DACK and EDACK timing: when DDS = 1 and EDDS = 1
RAS timing: when RAST = 1

Figure 7.17 DRAM Access Timing: Three-State Burst Access

Preliminary

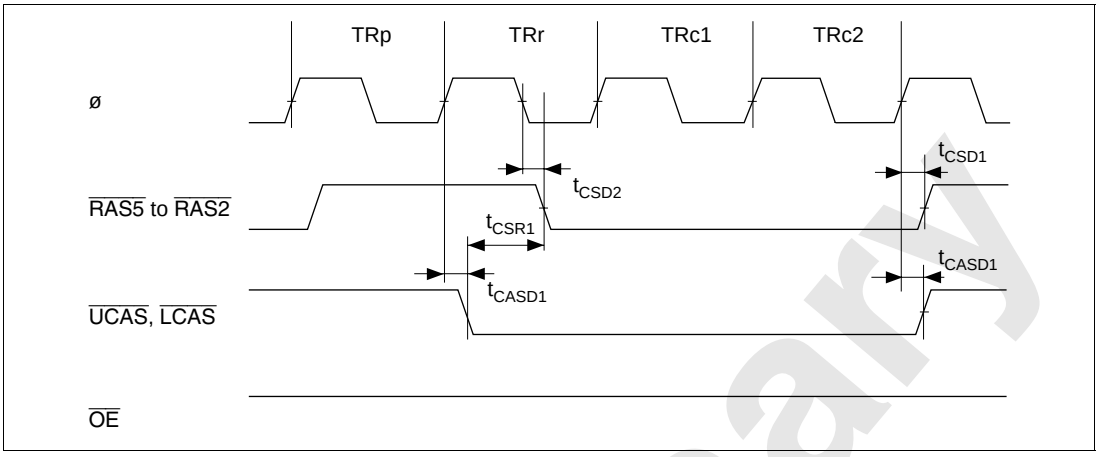


Figure 7.18 CAS-Before-RAS Refresh Timing

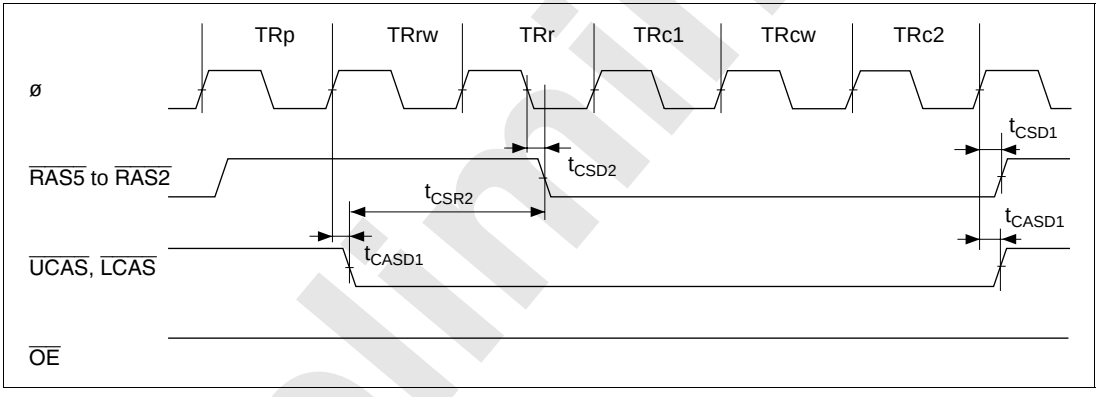


Figure 7.19 CAS-Before-RAS Refresh Timing (with Wait Cycle Insertion)

Preliminary

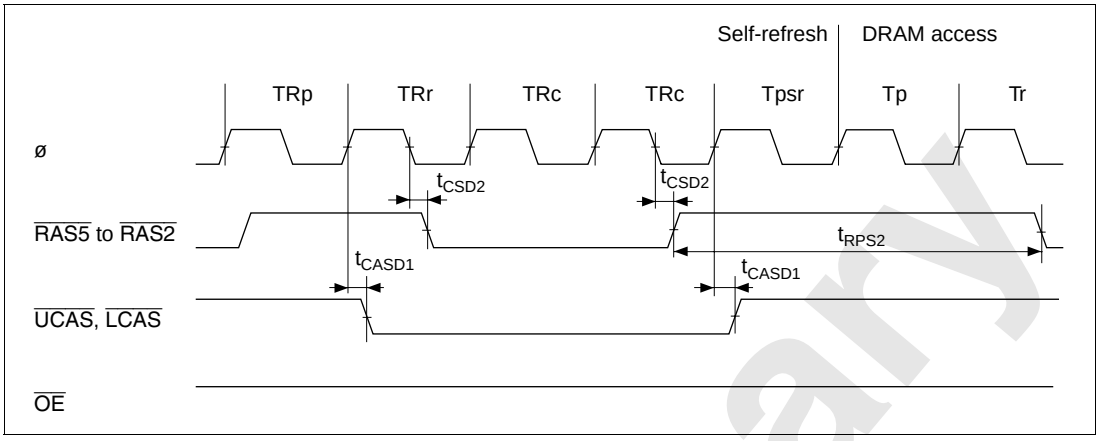


Figure 7.20 Self-Refresh Timing
(Return from Software Standby Mode: RAST = 0)

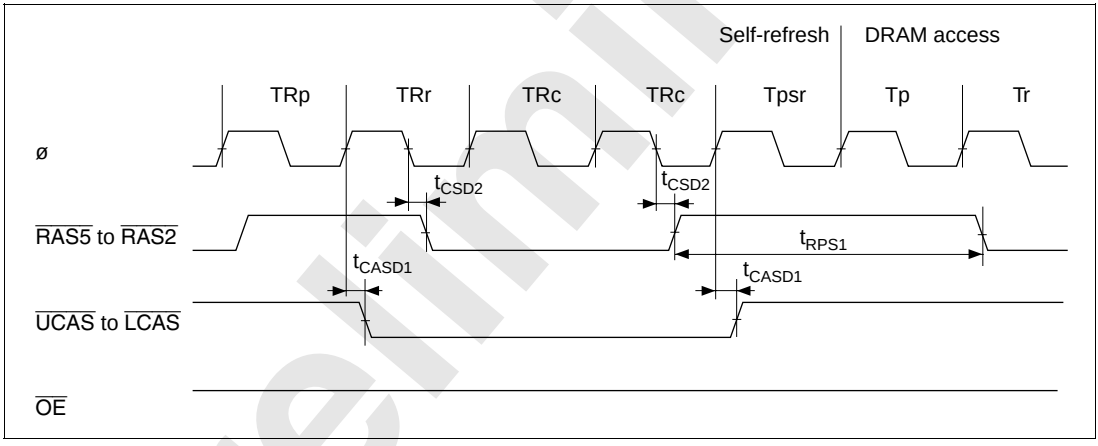


Figure 7.21 Self-Refresh Timing
(Return from Software Standby Mode: RAST = 1)

Preliminary

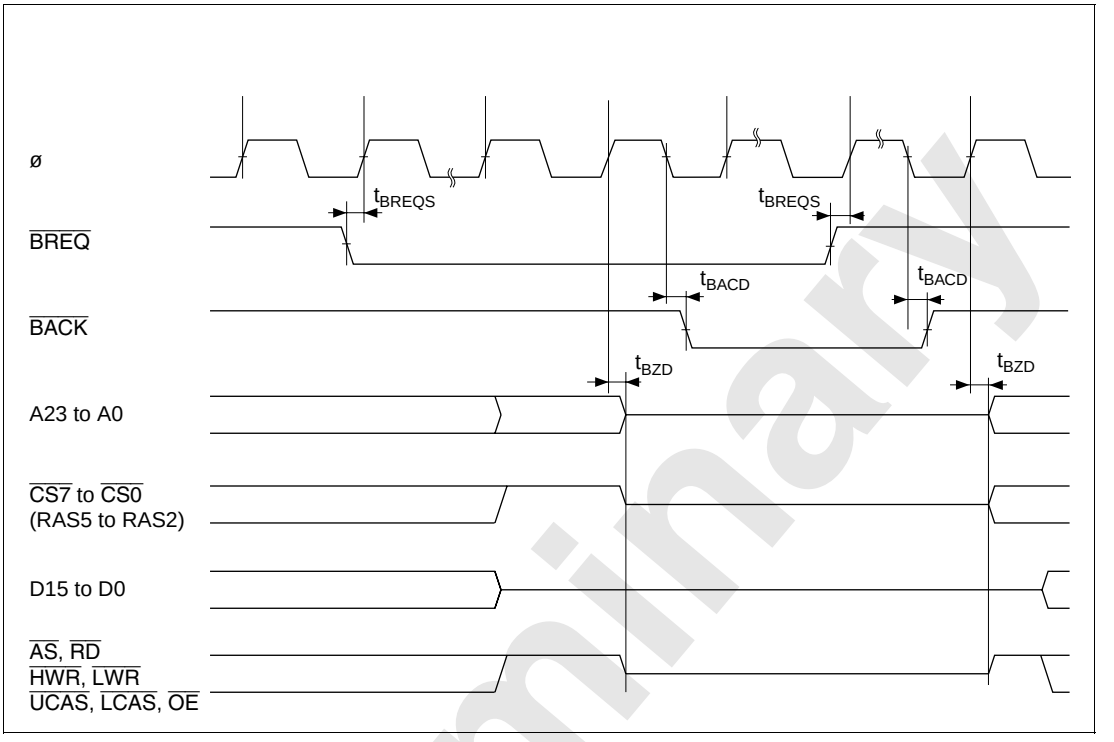


Figure 7.22 External Bus Release Timing

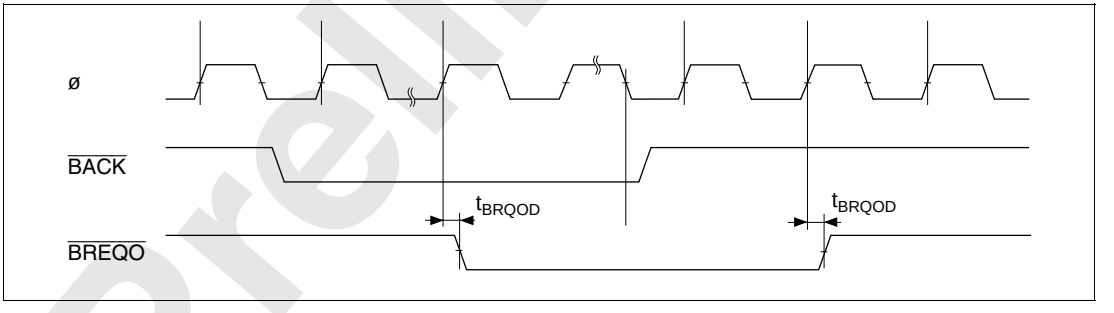


Figure 7.23 External Bus Request Output Timing

Preliminary

Table 7.7 DMAC and EXDMAC Timing — Preliminary —

Condition A*: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 33 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

* In planning stage

		Condition A		Condition B			Test
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
$\overline{\text{DREQ}}$ setup time	t_{DRQS}	30	—	25	—	ns	Figure7.27
$\overline{\text{DREQ}}$ hold time	t_{DRQH}	10	—	10	—		
$\overline{\text{TEND}}$ delay time	t_{TED}	—	20	—	18	ns	Figure7.26
$\overline{\text{DACK}}$ delay time 1	t_{DACD1}	—	20	—	18		Figure7.24
$\overline{\text{DACK}}$ delay time 2	t_{DACD2}	—	20	—	18		Figure7.25
$\overline{\text{EDREQ}}$ setup time	t_{EDRQS}	30	—	25	—	ns	Figure7.27
$\overline{\text{EDREQ}}$ hold time	t_{EDRQH}	10	—	10	—		
$\overline{\text{ETEND}}$ delay time	t_{ETED}	—	20	—	18	ns	Figure7.26
$\overline{\text{EDACK}}$ delay time 1	t_{EDACD1}	—	20	—	18		Figure7.24
$\overline{\text{EDACK}}$ delay time 2	t_{EDACD2}	—	20	—	18		Figure7.25
$\overline{\text{EDRAK}}$ delay time	t_{EDRKD}	—	20	—	18	ns	Figure7.28

Preliminary

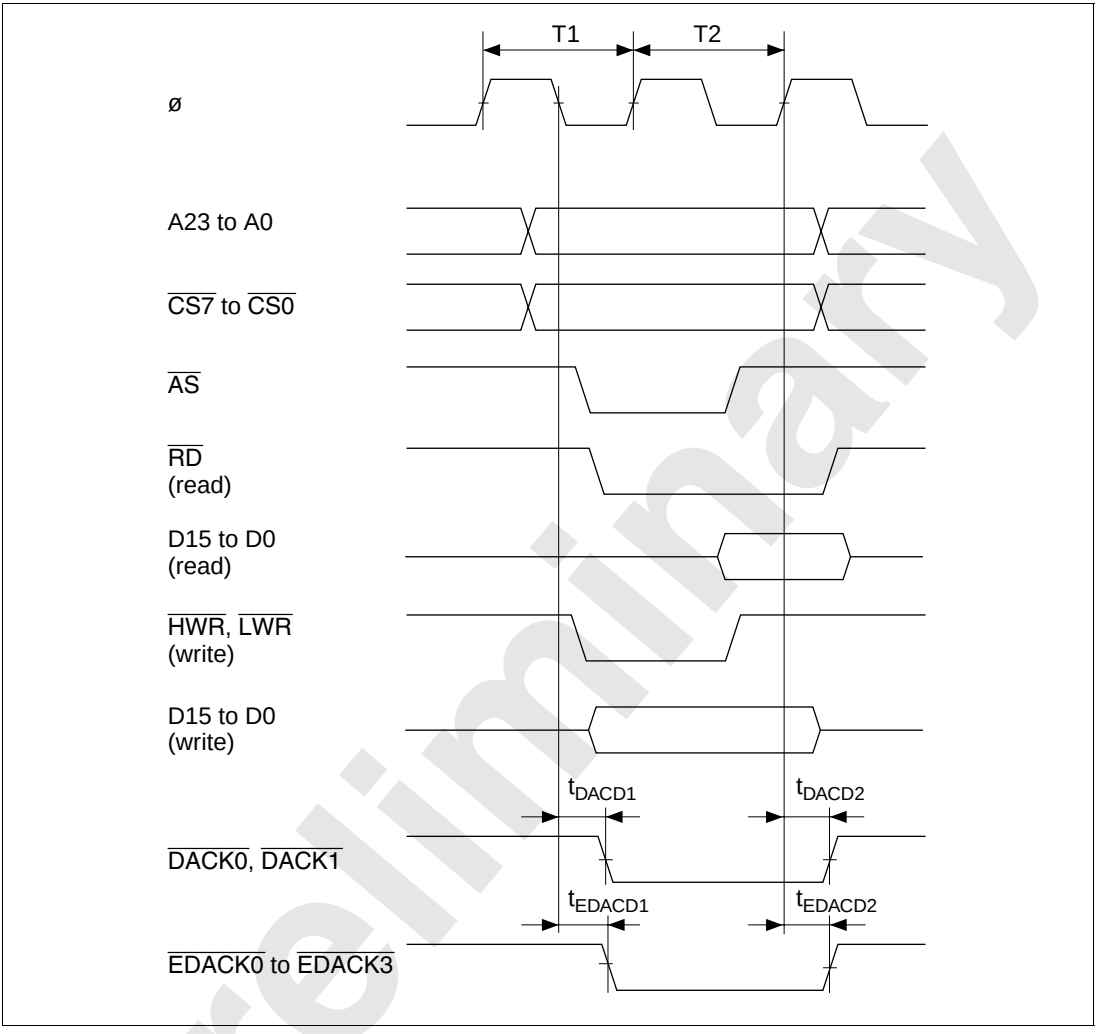


Figure 7.24 DMAC and EXDMAC Single Address Transfer Timing: Two-State Access

Preliminary

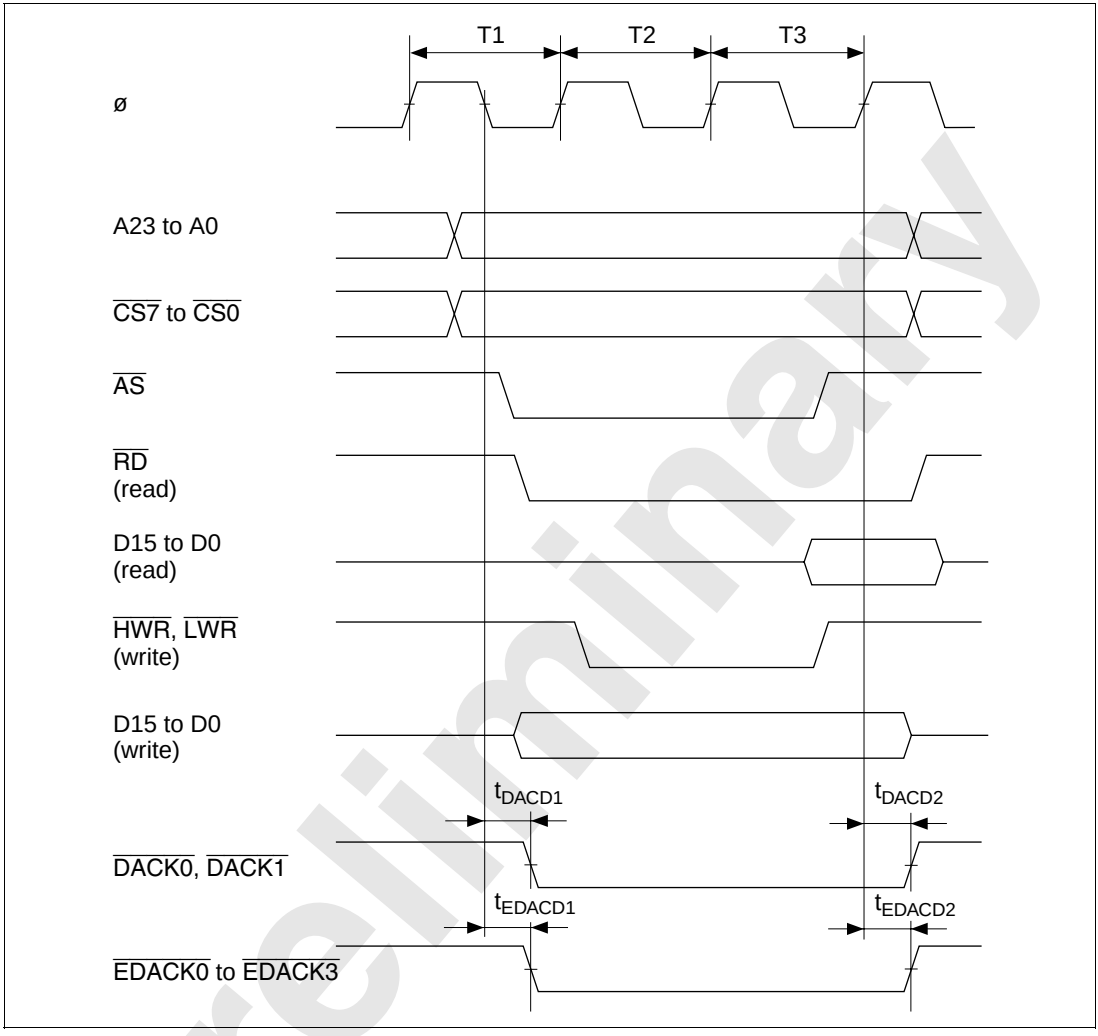


Figure 7.25 DMAC and EXDMAC Single Address Transfer Timing: Three-State Access

Preliminary

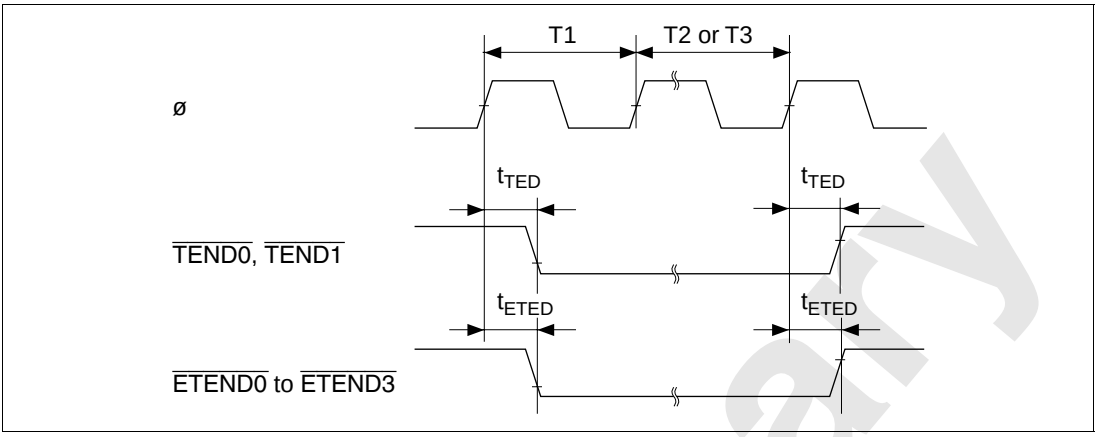


Figure 7.26 DMAC and EXDMAC $\overline{\text{TEND}}$/$\overline{\text{ETEND}}$ Output Timing

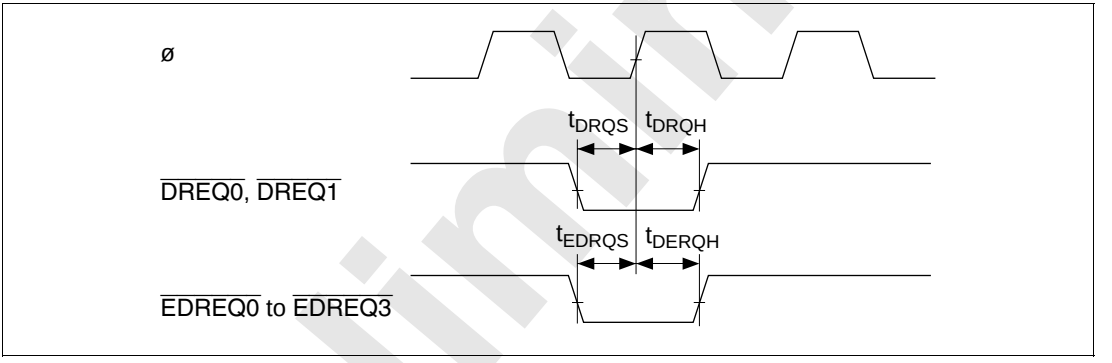


Figure 7.27 DMAC and EXDMAC $\overline{\text{DREQ}}$/$\overline{\text{EDREQ}}$ Input Timing

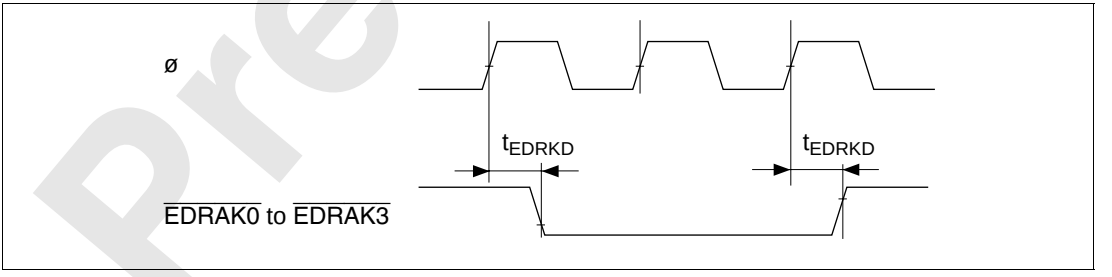


Figure 7.28 EXDMAC $\overline{\text{EDRAK}}$ Output Timing

Preliminary

Table 7.8 Timing of On-Chip Supporting Modules — Preliminary —

Condition A*: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 33 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

* In planning stage

Item			Symbol	Condition A Min	Condition A Max	Condition B Min	Condition B Max	Unit	Test Conditions
I/O ports	Output data delay time		t_{PWD}	—	50	—	40	ns	Figure7.29
	Input data setup time		t_{PRS}	30	—	25	—	ns	
	Input data hold time		t_{PRH}	30	—	25	—	ns	
PPG	Pulse output delay time		t_{POD}	—	50	—	40	ns	Figure7.30
TPU	Timer output delay time		t_{TOCD}	—	50	—	40	ns	Figure7.31
	Timer input setup time		t_{TICS}	30	—	25	—	ns	
	Timer clock input setup time		t_{TCKS}	30	—	25	—	ns	Figure7.32
	Timer clock pulse width	Single-edge specification	t_{TCKWH}	1.5	—	1.5	—	ns	
		Both-edge specification	t_{TCKWL}	2.5	—	2.5	—	t_{cyc}	

Preliminary

Item			Symbol	Condition A Min	Condition A Max	Condition B Min	Condition B Max	Unit	Test Conditions
8-bit timer	Timer output delay time		t_{TMOD}	—	50	—	40	ns	Figure7.33
	Timer reset input setup time		t_{TMRS}	30	—	25	—	ns	Figure7.35
	Timer clock input setup time		t_{TMCS}	30	—	25	—	ns	Figure7.34
	Timer clock pulse width	Single-edge specification	t_{TMCWH}	1.5	—	1.5	—	ns	
		Both-edge specification	t_{TMCWL}	2.5	—	2.5	—	ns	
WDT	Overflow output delay time		t_{WOVD}	—	50	—	40	ns	Figure7.36
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	4	—	t_{cyc}	Figure7.37
		Synchronous		6	—	6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	1.5	—	1.5	t_{cyc}	
	Input clock fall time		t_{SCKf}	—	1.5	—	1.5		
	Transmit data delay time		t_{TXD}	—	50	—	40	ns	Figure7.38
	Receive data setup time (synchronous)		t_{RXS}	50	—	40	—	ns	
	Receive data hold time (synchronous)		t_{RXH}	50	—	40	—	ns	
A/D converter	Trigger input setup time		t_{TRGS}	30	—	30	—	ns	Figure7.39

Preliminary

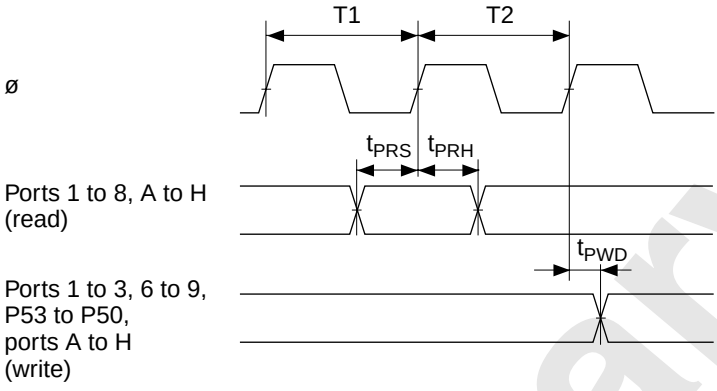


Figure 7.29 I/O Port Input/Output Timing

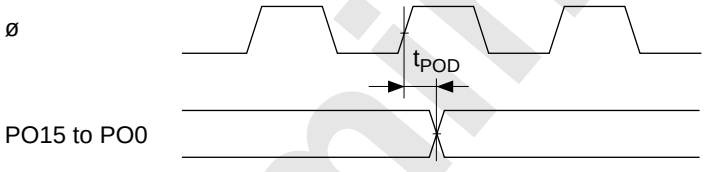
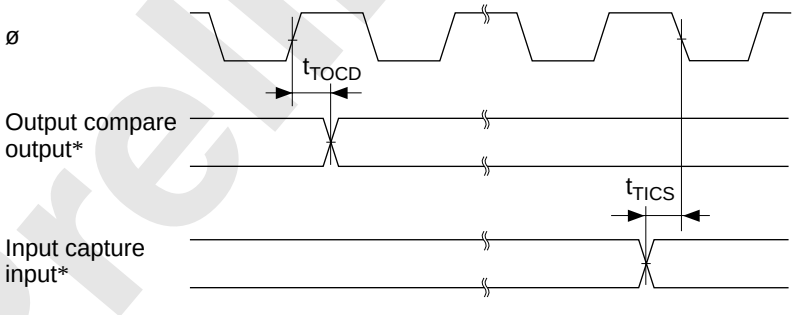


Figure 7.30 PPG Output Timing



Note: * TIOCA0 to TIOCA5, TIOCB0 to TIOCB5, TIOCC0, TIOCC3, TIOCD0, TIOCD3

Figure 7.31 TPU Input/Output Timing

Preliminary

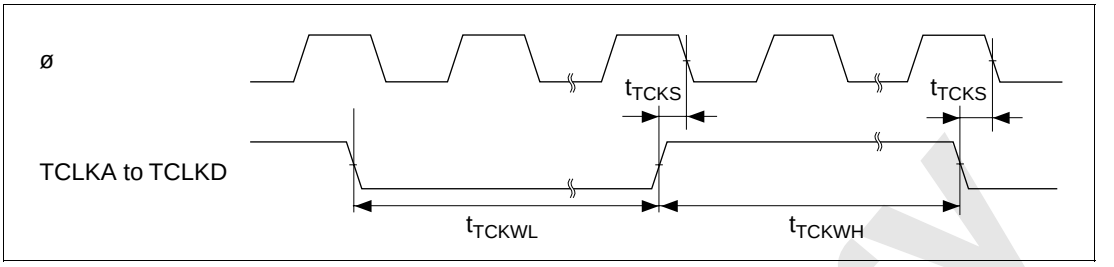


Figure 7.32 TPU Clock Input Timing

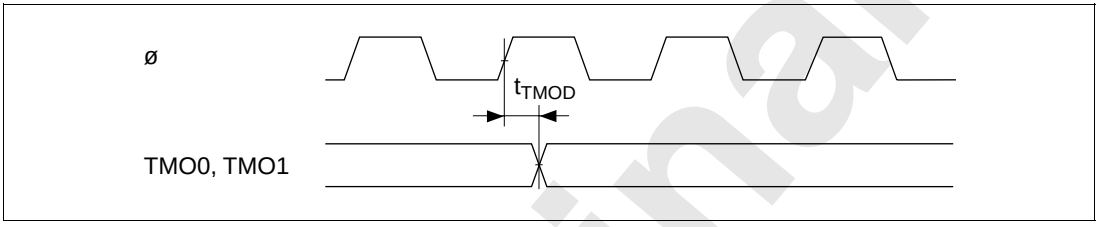


Figure 7.33 8-Bit Timer Output Timing

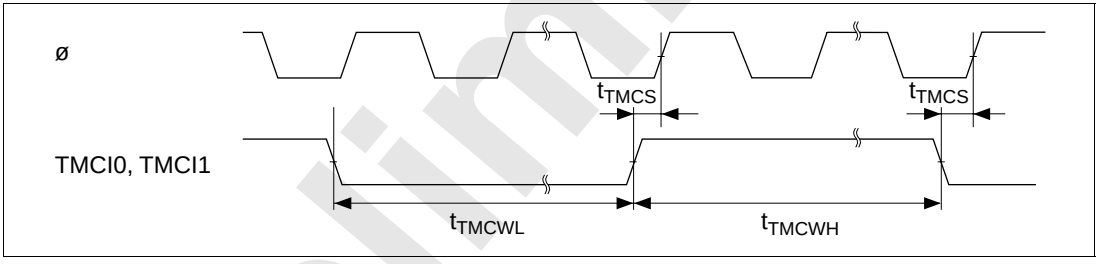


Figure 7.34 8-Bit Timer Clock Input Timing

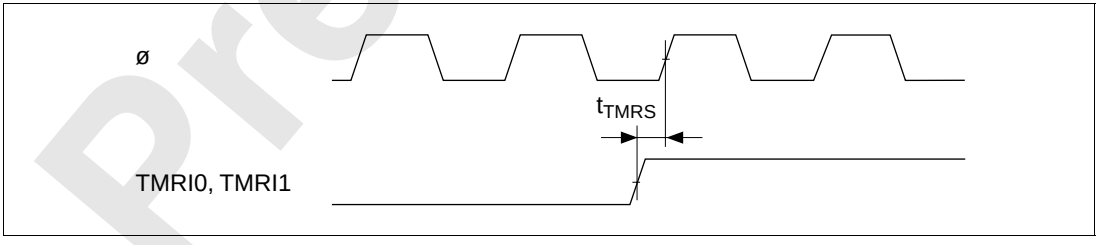


Figure 7.35 8-Bit Timer Reset Input Timing

Preliminary

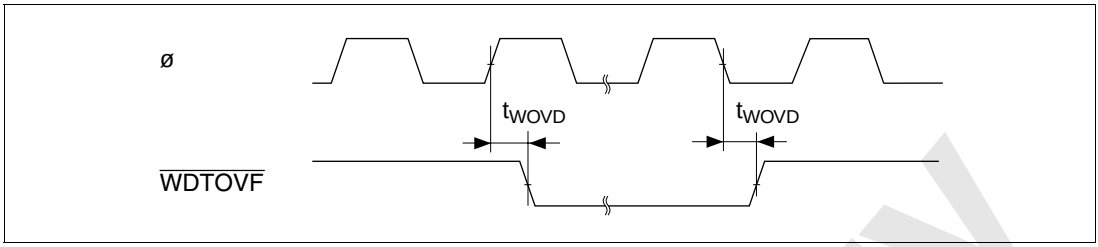


Figure 7.36 WDT Output Timing

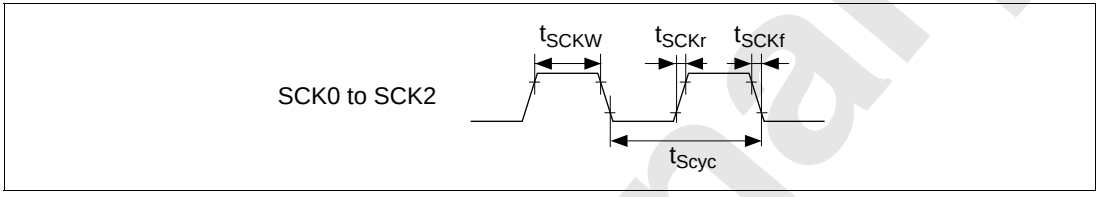


Figure 7.37 SCK Clock Input Timing

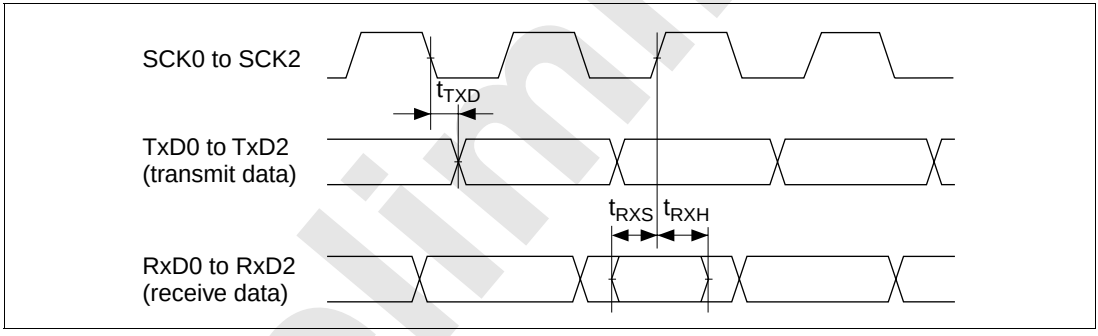


Figure 7.38 SCI Input/Output Timing: Synchronous Mode

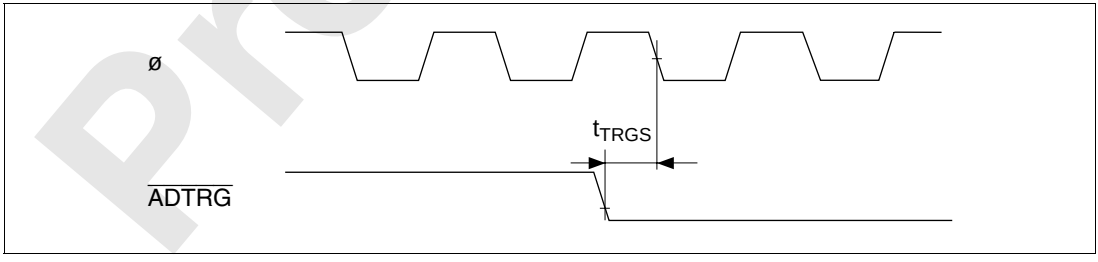


Figure 7.39 A/D Converter External Trigger Input Timing

Preliminary

7.1.4 A/D Conversion Characteristics

Table 7.9 A/D Conversion Characteristics — Preliminary —

Condition A*: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 33 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

* In planning stage

	Condition A			Condition B			
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	10	10	10	Bit
Conversion time	—	—	6.7	—	—	8.1	µs
Analog input capacitance	—	—	20	—	—	20	pF
Permissible signal source impedance	—	—	5	—	—	5	kΩ
Nonlinearity error	—	—	±7.5	—	—	±7.5	LSB
Offset error	—	—	±7.5	—	—	±7.5	LSB
Full-scale error	—	—	±7.5	—	—	±7.5	LSB
Quantization error	—	±0.5	—	—	±0.5	—	LSB
Absolute accuracy	—	—	±8.0	—	—	±8.0	LSB

Preliminary

7.1.5 D/A Conversion Characteristics

Table 7.10 D/A Conversion Characteristics — Preliminary —

Condition A*: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 33 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

* In planning stage

	Condition A			Condition B				
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Resolution	8	8	8	8	8	8	Bit	
Conversion time	—	—	10	—	—	10	µs	20 pF capacitive load
Absolute accuracy	—	±2.0	±3.0	—	±2.0	±3.0	LSB	2 MΩ resistive load
	—	—	±2.0	—	—	±2.0	LSB	4 MΩ resistive load

Preliminary

7.2 Electrical Characteristics of F-ZTAT Version (H8S/2677, H8S/2676)

7.2.1 Absolute Maximum Ratings

Table 7.11 lists the absolute maximum ratings.

Table 7.11 Absolute Maximum Ratings — Preliminary —

Item	Symbol	Value	Unit
Power supply voltage	V_{CC} $PLLV_{CC}$	–0.3 to +4.0	V
Input voltage (FWE)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (except port 4, P54 to P57)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (port 4, P54 to P57)	V_{in}	–0.3 to AV_{CC} +0.3	V
Reference power supply voltage	V_{ref}	–0.3 to AV_{CC} +0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +4.0	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75*	°C
		Wide-range specifications: –40 to +85*	°C
Storage temperature	T_{stg}	–55to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded.

Note: * The operating temperature ranges for flash memory programming/erasing are as follows:

T_a = 0°C to +TBD°C (regular specifications)

T_a = 0°C to +TBD°C (wide-range specifications)

Preliminary

7.2.2 DC Characteristics

Table 7.12 DC Characteristics — Preliminary —

Conditions: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V*[1], T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	Port 1, port 2, P50 to P53*[2], port 6*[2], port 8*[2], PF1*[2], PF2*[2], PH2*[2], PH3*[3]	VT^-	$V_{CC} \times 0.2$	—	—	V	
		VT^+	—	—	$V_{CC} \times 0.7$	V	
		$VT^+ - VT^-$	TBD	—	—	V	
	P54 to P57*[2]	VT^-	$AV_{CC} \times 0.2$	—	—	V	
		VT^+	—	—	$AV_{CC} \times 0.7$	V	
		$VT^+ - VT^-$	TBD	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD2 to MD0, FEW	V_{IH}	$V_{CC} \times 0.9$	—	V_{CC} + 0.3	V	
	EXTAL		$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V	
	Port 3, P50 to P53*[3], ports 6 to 8*[3], ports A to H*[3]		$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V	
	Port 4, P54 to P57*[3]		$AV_{CC} \times 0.7$	—	AV_{CC} + 0.3	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD2 to MD0, FEW	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL, ports 3 to 8, ports A to H*[3]		–0.3	—	$V_{CC} \times 0.2$	V	
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA

Preliminary

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	$\overline{RES}$	$\|I_{in}\|$	—	—	TBD	µA	V_{in} = 0.5 to V_{CC} – TBD V
	$\overline{STBY}$, NMI, MD2 to MD0		—	—	TBD	µA	
	Port 4, P54 to P57		—	—	TBD	µA	V_{in} = 0.5 to AV_{CC} – TBD V
Three-state leakage current (off state)	Ports 1 to 3, P50 to P53, ports 6 to 8, ports A to H	$\|I_{TSI}\|$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
Input pull-up MOS current	Ports A to E	—I_p	10	—	300	µA	V_{CC} = 2.7 to 3.6 V V_{in} = 0 V
Input capacitance	$\overline{RES}$	C_{in}	—	—	30	pF	V_{in} = 0 V
	NMI		—	—	30	pF	f = 1 MHz
	All input pins except $\overline{RES}$ and NMI		—	—	15	pF	T_a = 25°C
Current dissipation*[4]	Normal operation	I_{CC}*[7]	—	50 (3.0 V)	95	mA	f = 20 MHz
				80 (3.3 V)	150	mA	f = 33 MHz
	Sleep mode		—	TBD (3.0 V)	TBD	mA	f = 20 MHz
				TBD (3.3 V)	TBD	mA	f = 33 MHz
	Standby mode*[5]		—	0.01	10	µA	$T_a \leq$ 50°C
			—	—	80	µA	50°C < T_a
	All-module-clocks-stop mode*[6]		—	TBD	—	µA	50°C < T_a
Analog power supply current	During A/D and D/A conversion	AI_{CC}	—	TBD (3.0 V)	TBD	mA	
	Idle		—	0.01	5.0	µA	
Reference power supply current	During A/D and D/A conversion	AI_{CC}	—	TBD (3.0 V)	TBD	mA	
	Idle		—	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Preliminary

Notes: 1. If the A/D and D/A converters are not used, do not leave the AV_{CC}, V_{ref}, and AV_{SS} pins open. Connect the AV_{CC} and V_{ref} pins to V_{CC}, and the AV_{SS} pin to V_{SS}.
2. When used as $\overline{IRQ0}$ to $\overline{IRQ15}$.
3. When used as other than $\overline{IRQ0}$ to $\overline{IRQ15}$.
4. Current dissipation values are for V_{IH}min = V_{CC} – 0.5 V and V_{IL}max = 0.5 V with all output pins unloaded and all MOS input pull-ups in the off state.
5. The values are for $V_{RAM} \leq V_{CC} < 2.7$ V, V_{IH}min = $V_{CC} \times 0.9$, and V_{IL}max = 0.3 V.
6. Reference value
7. I_{CC} depends on V_{CC} and f as follows:
   I_{CC}max = 1.0 (mA) + TBD (mA/(MHz × V)) × V_{CC} × f (normal operation)
   I_{CC}max = 1.0 (mA) + TBD (mA/(MHz × V)) × V_{CC} × f (sleep mode)

Table 7.13 Permissible Output Currents — Preliminary —

Conditions: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V*[1], T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	All output pins	I_{OL}	—	—	2.0	mA
Permissible output low current (total)	Total of all output pins	ΣI_{OL}	—	—	TBD	mA
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	$\Sigma -I_{OH}$	—	—	TBD	mA

Notes: 1. If the A/D and D/A converters are not used, do not leave the AV_{CC}, V_{ref}, and AV_{SS} pins open. Connect the AV_{CC} and V_{ref} pins to V_{CC}, and the AV_{SS} pin to V_{SS}.
2. To protect chip reliability, do not exceed the output current values in table 7.16.

Preliminary

7.2.3 AC Characteristics

Clock Timing

Table 7.14 Clock Timing **— Preliminary —**

Condition A*: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 33 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Note: * In planning stage

		Condition A		Condition B			Test
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
Clock cycle time	t_{cyc}	50	500	30.3	500	ns	Figure7.2
Clock pulse high width	t_{CH}	20	—	10	—	ns	Figure7.2
Clock pulse low width	t_{CL}	20	—	10	—	ns	
Clock rise time	t_{Cr}	—	5	—	5	ns	
Clock fall time	t_{Cf}	—	5	—	5	ns	
Reset oscillation settling time (crystal)	t_{OSC1}	10	—	10	—	ms	Figure7.3
Software standby oscillation settling time (crystal)	t_{OSC2}	10	—	10	—	ms	
External clock output delay settling time	t_{DEXT}	500	—	500	—	µs	Figure7.3

Preliminary

Table 7.15 Control Signal Timing **— Preliminary —**

Condition A*: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 33 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

* In planning stage

		Condition A		Condition B			Test
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
$\overline{RES}$ setup time	t_{RESS}	200	—	200	—	ns	Figure7.4
$\overline{RES}$ pulse width	t_{RESW}	20	—	20	—	t_{cyc}	
NMI setup time	t_{NMIS}	150	—	150	—	ns	Figure7.5
NMI hold time	t_{NMIH}	10	—	10	—		
NMI pulse width (in recovery from software standby mode)	t_{NMIW}	200	—	200	—		
$\overline{IRQ}$ setup time	t_{IRQS}	150	—	150	—	ns	
$\overline{IRQ}$ hold time	t_{IRQH}	10	—	10	—		
$\overline{IRQ}$ pulse width (in recovery from software standby mode)	t_{IRQW}	200	—	200	—		

Preliminary

Table 7.16 Bus Timing **— Preliminary —**

Condition A*: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 33 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

* In planning stage

		Condition A		Condition B			Test
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
Address delay time	t_{AD}	—	20	—	20	ns	Figure7.6 to Figure7.19
Address setup time 1	t_{AS1}	$0.5 \times t_{cyc} - 15$	—	$0.5 \times t_{cyc} - 13$	—	ns	
Address setup time 2	t_{AS2}	$1.0 \times t_{cyc} - 15$	—	$1.0 \times t_{cyc} - 13$	—	ns	
Address setup time 3	t_{AS3}	$1.5 \times t_{cyc} - 15$	—	$1.5 \times t_{cyc} - 13$	—	ns	
Address setup time 4	t_{AS4}	$2.0 \times t_{cyc} - 15$	—	$2.0 \times t_{cyc} - 13$	—	ns	
Address hold time 1	t_{AH1}	$0.5 \times t_{cyc} - 10$	—	$0.5 \times t_{cyc} - 8$	—	ns	
Address hold time 2	t_{AH2}	$1.0 \times t_{cyc} - 10$	—	$1.0 \times t_{cyc} - 8$	—	ns	
Address hold time 3	t_{AH3}	$1.5 \times t_{cyc} - 10$	—	$1.5 \times t_{cyc} - 8$	—	ns	
$\overline{CS}$ delay time 1	t_{CSD1}	—	20	—	15	ns	
$\overline{CS}$ delay time 2	t_{CSD2}	—	20	—	15	ns	
$\overline{CS}$ delay time 3	t_{CSD3}	—	20	—	20	ns	
$\overline{AS}$ delay time	t_{ASD}	—	20	—	15	ns	
$\overline{RD}$ delay time 1	t_{RSD1}	—	20	—	15	ns	
$\overline{RD}$ delay time 2	t_{RSD2}	—	20	—	15	ns	
Read data setup time 1	t_{RDS1}	15	—	15	—	ns	
Read data setup time 2	t_{RDS2}	15	—	15	—	ns	

Preliminary

Item	Symbol	Condition A		Condition B		Unit	Test Conditions
		Min	Max	Min	Max		
Read data hold time 1	t_{RDH1}	0	—	0	—	ns	Figure7.6 to Figure7.19
Read data hold time 2	t_{RDH2}	0	—	0	—	ns	
Read data access time 1	t_{AC1}	—	$1.0 \times t_{cyc} - 25$	—	$1.0 \times t_{cyc} - 20$	ns	
Read data access time 2	t_{AC2}	—	$1.5 \times t_{cyc} - 25$	—	$1.5 \times t_{cyc} - 20$	ns	
Read data access time 3	t_{AC3}	—	$2.0 \times t_{cyc} - 25$	—	$2.0 \times t_{cyc} - 20$	ns	
Read data access time 4	t_{AC4}	—	$2.5 \times t_{cyc} - 25$	—	$2.5 \times t_{cyc} - 20$	ns	
Read data access time 5	t_{AC5}	—	$1.0 \times t_{cyc} - 25$	—	$1.0 \times t_{cyc} - 20$	ns	
Read data access time 6	t_{AC6}	—	$2.0 \times t_{cyc} - 25$	—	$2.0 \times t_{cyc} - 20$	ns	
Read data access time 7	t_{AC7}	—	$4.0 \times t_{cyc} - 25$	—	$4.0 \times t_{cyc} - 20$	ns	
Read data access time 8	t_{AC8}	—	$3.0 \times t_{cyc} - 25$	—	$3.0 \times t_{cyc} - 20$	ns	
Address read data access time 1	t_{AA1}	—	$1.0 \times t_{cyc} - 25$	—	$1.0 \times t_{cyc} - 20$	ns	
Address read data access time 2	t_{AA2}	—	$1.5 \times t_{cyc} - 25$	—	$1.5 \times t_{cyc} - 20$	ns	
Address read data access time 3	t_{AA3}	—	$2.0 \times t_{cyc} - 25$	—	$2.0 \times t_{cyc} - 20$	ns	
Address read data access time 4	t_{AA4}	—	$2.5 \times t_{cyc} - 25$	—	$2.5 \times t_{cyc} - 20$	ns	
Address read data access time 5	t_{AA5}	—	$3.0 \times t_{cyc} - 25$	—	$3.0 \times t_{cyc} - 20$	ns	
$\overline{WR}$ delay time 1	t_{WRD1}	—	20	—	15	ns	
$\overline{WR}$ delay time 2	t_{WRD2}	—	20	—	15	ns	
$\overline{WR}$ pulse width 1	t_{WSW1}	$1.0 \times t_{cyc} - 20$	—	$1.0 \times t_{cyc} - 13$	—	ns	
$\overline{WR}$ pulse width 2	t_{WSW2}	$1.5 \times t_{cyc} - 20$	—	$1.5 \times t_{cyc} - 13$	—	ns	

Preliminary

Item	Symbol	Condition A		Condition B		Unit	Test Conditions
		Min	Max	Min	Max		
Write data delay time	t_{WDD}	—	30	—	20	ns	Figure7.6 to Figure7.19
Write data setup time 1	t_{WDS1}	$0.5 \times t_{cyc} - 20$	—	$0.5 \times t_{cyc} - 13$	—	ns	
Write data setup time 2	t_{WDS2}	$1.0 \times t_{cyc} - 20$	—	$1.0 \times t_{cyc} - 13$	—	ns	
Write data setup time 3	t_{WDS3}	$1.5 \times t_{cyc} - 20$	—	$1.5 \times t_{cyc} - 13$	—	ns	
Write data hold time 1	t_{WDH1}	$0.5 \times t_{cyc} - 10$	—	$0.5 \times t_{cyc} - 8$	—	ns	
Write data hold time 2	t_{WDH2}	$1.0 \times t_{cyc} - 10$	—	$1.0 \times t_{cyc} - 8$	—	ns	
Write data hold time 3	t_{WDH3}	$1.5 \times t_{cyc} - 10$	—	$1.5 \times t_{cyc} - 8$	—	ns	
Write command setup time 1	t_{WCS1}	$0.5 \times t_{cyc} - 10$	—	$0.5 \times t_{cyc} - 10$	—	ns	
Write command setup time 2	t_{WCS2}	$1.0 \times t_{cyc} - 10$	—	$1.0 \times t_{cyc} - 10$	—	ns	
Write command hold time 1	t_{WCH1}	$0.5 \times t_{cyc} - 10$	—	$0.5 \times t_{cyc} - 10$	—	ns	
Write command hold time 2	t_{WCH2}	$1.0 \times t_{cyc} - 10$	—	$1.0 \times t_{cyc} - 10$	—	ns	
Read command setup time 1	t_{RCS1}	$1.5 \times t_{cyc} - 10$	—	$1.5 \times t_{cyc} - 10$	—	ns	
Read command setup time 2	t_{RCS2}	$2.0 \times t_{cyc} - 10$	—	$2.0 \times t_{cyc} - 10$	—	ns	
Read command hold time	t_{RCH}	$0.5 \times t_{cyc} - 10$	—	$0.5 \times t_{cyc} - 10$	—	ns	
$\overline{CAS}$ delay time 1	t_{CASD1}	—	20	—	15	ns	
$\overline{CAS}$ delay time 2	t_{CASD2}	—	20	—	15	ns	
$\overline{CAS}$ setup time 1	t_{CSR1}	$0.5 \times t_{cyc} - 10$	—	$0.5 \times t_{cyc} - 10$	—	ns	
$\overline{CAS}$ setup time 2	t_{CSR2}	$1.5 \times t_{cyc} - 10$	—	$1.5 \times t_{cyc} - 10$	—	ns	
$\overline{CAS}$ pulse width 1	t_{CASW1}	$1.0 \times t_{cyc} - 20$	—	$1.0 \times t_{cyc} - 20$	—	ns	
$\overline{CAS}$ pulse width 2	t_{CASW2}	$1.5 \times t_{cyc} - 20$	—	$1.5 \times t_{cyc} - 20$	—	ns	

Preliminary

Item	Symbol	Condition A		Condition B		Unit	Test Conditions
		Min	Max	Min	Max		
$\overline{CAS}$ precharge time 1	t_{CPW1}	$1.0 \times t_{cyc} - 20$	—	$1.0 \times t_{cyc} - 20$	—	ns	Figure7.6 to Figure7.19
$\overline{CAS}$ precharge time 2	t_{CPW2}	$1.5 \times t_{cyc} - 20$	—	$1.5 \times t_{cyc} - 20$	—	ns	
$\overline{OE}$ delay time 1	t_{OED1}	—	20	—	15	ns	
$\overline{OE}$ delay time 2	t_{OED2}	—	20	—	15	ns	
Precharge time 1	t_{PCH1}	$1.0 \times t_{cyc} - 20$	—	$1.0 \times t_{cyc} - 20$	—	ns	
Precharge time 2	t_{PCH2}	$1.5 \times t_{cyc} - 20$	—	$1.5 \times t_{cyc} - 20$	—	ns	
Self-refresh precharge time 1	t_{RPS1}	$2.5 \times t_{cyc} - 20$	—	$2.5 \times t_{cyc} - 20$	—	ns	Figure7.20 Figure7.21
Self-refresh precharge time 2	t_{RPS2}	$3.0 \times t_{cyc} - 20$	—	$3.0 \times t_{cyc} - 20$	—	ns	
$\overline{WAIT}$ setup time	t_{WTS}	30	—	25	—	ns	Figure7.14
$\overline{WAIT}$ hold time	t_{WTH}	5	—	5	—	ns	
$\overline{BREQ}$ setup time	t_{BREQS}	30	—	30	—	ns	Figure7.22
$\overline{BACK}$ delay time	t_{BACD}	—	15	—	15	ns	
Bus floating time	t_{BZD}	—	50	—	40	ns	
$\overline{BREQO}$ delay time	t_{BRQOD}	—	30	—	25	ns	Figure7.23

Preliminary

Table 7.17 DMAC and EXDMAC Timing — Preliminary —

Condition A*: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 33 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

* In planning stage

		Condition A		Condition B			Test
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
$\overline{\text{DREQ}}$ setup time	t_{DRQS}	30	—	25	—	ns	Figure7.27
$\overline{\text{DREQ}}$ hold time	t_{DRQH}	10	—	10	—		
$\overline{\text{TEND}}$ delay time	t_{TED}	—	20	—	18	ns	Figure7.26
$\overline{\text{DACK}}$ delay time 1	t_{DACD1}	—	20	—	18		Figure7.24
$\overline{\text{DACK}}$ delay time 2	t_{DACD2}	—	20	—	18		Figure7.25
$\overline{\text{EDREQ}}$ setup time	t_{EDRQS}	30	—	25	—	ns	Figure7.27
$\overline{\text{EDREQ}}$ hold time	t_{EDRQH}	10	—	10	—		
$\overline{\text{ETEND}}$ delay time	t_{ETED}	—	20	—	18	ns	Figure7.26
$\overline{\text{EDACK}}$ delay time 1	t_{EDACD1}	—	20	—	18		Figure7.24
$\overline{\text{EDACK}}$ delay time 2	t_{EDACD2}	—	20	—	18		Figure7.25
$\overline{\text{EDRAK}}$ delay time	t_{EDRKD}	—	20	—	18	ns	Figure7.28

Preliminary

Table 7.18 Timing of On-Chip Supporting Modules — Preliminary —

Condition A*: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 33 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

* In planning stage

Item			Symbol	Condition A Min	Condition A Max	Condition B Min	Condition B Max	Unit	Test Conditions
I/O ports	Output data delay time		t_{PWD}	—	50	—	40	ns	Figure 7.29
	Input data setup time		t_{PRS}	30	—	25	—	ns	
	Input data hold time		t_{PRH}	30	—	25	—	ns	
PPG	Pulse output delay time		t_{POD}	—	50	—	40	ns	Figure 7.30
TPU	Timer output delay time		t_{TOCD}	—	50	—	40	ns	Figure 7.31
	Timer input setup time		t_{TICS}	30	—	25	—	ns	
	Timer clock input setup time		t_{TCKS}	30	—	25	—	ns	Figure 7.32
	Timer clock pulse width	Single-edge specification	t_{TCKWH}	1.5	—	1.5	—	ns	
		Both-edge specification	t_{TCKWL}	2.5	—	2.5	—	t_{cyc}	
8-bit timer	Timer output delay time		t_{TMOD}	—	50	—	40	ns	Figure 7.33
	Timer reset input setup time		t_{TMRS}	30	—	25	—	ns	Figure 7.35
	Timer clock input setup time		t_{TMCS}	30	—	25	—	ns	Figure 7.34
	Timer clock pulse width	Single-edge specification	t_{TMCWH}	1.5	—	1.5	—	ns	
		Both-edge specification	t_{TMCWL}	2.5	—	2.5	—	ns	

Preliminary

Item		Symbol	Condition A Min	Condition A Max	Condition B Min	Condition B Max	Unit	Test Conditions
WDT	Overflow output delay time	t_{WOVD}	—	50	—	40	ns	Figure 7.36
SCI	Input clock cycle — Asynchronous	t_{Scyc}	4	—	4	—	t_{cyc}	Figure 7.37
	Input clock cycle — Synchronous		6	—	6	—		
	Input clock pulse width	t_{SCKW}	0.4	0.6	0.4	0.6	t_{Scyc}	
	Input clock rise time	t_{SCKr}	—	1.5	—	1.5	t_{cyc}	
	Input clock fall time	t_{SCKf}	—	1.5	—	1.5		
	Transmit data delay time	t_{TXD}	—	50	—	40	ns	Figure 7.38
	Receive data setup time (synchronous)	t_{RXS}	50	—	40	—	ns	
	Receive data hold time (synchronous)	t_{RXH}	50	—	40	—	ns	
A/D converter	Trigger input setup time	t_{TRGS}	30	—	30	—	ns	Figure 7.39

Preliminary

7.2.4 A/D Conversion Characteristics

Table 7.19 A/D Conversion Characteristics — Preliminary —

Condition A*: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 33 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

* In planning stage

	Condition A			Condition B			
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	10	10	10	Bit
Conversion time	—	—	6.7	—	—	8.1	µs
Analog input capacitance	—	—	20	—	—	20	pF
Permissible signal source impedance	—	—	5	—	—	5	kΩ
Nonlinearity error	—	—	±7.5	—	—	±7.5	LSB
Offset error	—	—	±7.5	—	—	±7.5	LSB
Full-scale error	—	—	±7.5	—	—	±7.5	LSB
Quantization error	—	±0.5	—	—	±0.5	—	LSB
Absolute accuracy	—	—	±8.0	—	—	±8.0	LSB

Preliminary

7.2.5 D/A Conversion Characteristics

Table 7.20 D/A Conversion Characteristics — Preliminary —

Condition A*: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 20 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 2 MHz to 33 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

* In planning stage

	Condition A			Condition B				
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Resolution	8	8	8	8	8	8	Bit	
Conversion time	—	—	10	—	—	10	µs	20 pF capacitive load
Absolute accuracy	—	±2.0	±3.0	—	±2.0	±3.0	LSB	2 MΩ resistive load
	—	—	±2.0	—	—	±2.0	LSB	4 MΩ resistive load

Preliminary

7.2.6 Flash Memory Characteristics

Table 7.21 Flash Memory Characteristics — Preliminary —

Conditions: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = 0°C to TBD°C (program/erase operating temperature range: regular specifications), T_a = 0°C to TBD°C (program/erase operating temperature range: wide-range specifications)

Item		Symbol		Min	Typ	Max	Unit	Test Conditions
Programming time*1, *2, *4		t_P		—	10	200	ms/ 128 bytes	
Erase time*1, *3, *6		t_E		—	50	1000	ms/block	
Rewrite times		N_{WEC}		—	—	100	Times	
Programming	Wait time after SWE bit setting*1	x		1	—	—	µs	
	Wait time after PSU bit setting*1	y		50	—	—	µs	
	Wait time after P bit setting*1, *4	z	z1	—	—	30	µs	1 ≤ n ≤ 6
			z2	—	—	200	µs	7 ≤ n ≤ 1000
			z3	—	—	10	µs	Additional programming wait
	Wait time after P bit clearing*1	α		5	—	—	µs	
	Wait time after PSU bit clearing*1	β		5	—	—	µs	
	Wait time after PV bit setting*1	γ		4	—	—	µs	
	Wait time after H'FF dummy write*1	ε		2	—	—	µs	
	Wait time after PV bit clearing*1	η		2	—	—	µs	
	Wait time after SWE bit clearing*1	θ		100	—	—	µs	
	Maximum number of writes*1, *4	N		—	—	1000*5	Times	

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Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Erasing	Wait time after SWE bit setting*[1]	x	1	—	—	µs	
	Wait time after ESU bit setting*[1]	y	100	—	—	µs	
	Wait time after E bit setting*[1, *6]	z	—	—	10	ms	
	Wait time after E bit clearing*[1]	α	10	—	—	µs	
	Wait time after ESU bit clearing*[1]	β	10	—	—	µs	
	Wait time after EV bit setting*[1]	γ	6	—	—	µs	
	Wait time after H'FF dummy write*[1]	ε	2	—	—	µs	
	Wait time after EV bit clearing*[1]	η	4	—	—	µs	
	Wait time after SWE bit clearing*[1]	θ	100	—	—	µs	
	Maximum number of erases*[1, *6]	N	—	—	100	Times	

Notes: 1. Follow the program/erase algorithms when making the time settings.

3. Programming time per 128 bytes. (Indicates the total time during which the P bit is set in flash memory control register 1 (FLMCR1). Does not include the program-verify time.)

3. Time to erase one block. (Indicates the time during which the E bit is set in FLMCR1. Does not include the erase-verify time.)

4. Maximum programming time

$$t_P(\max) = \sum_{i=1}^{N} \text{wait time after P bit setting (z)}$$

5. The maximum number of writes (N) should be set as shown below according to the actual set value of z so as not to exceed the maximum programming time (t_P(max)).

The wait time after P bit setting (z) should be changed as follows according to the number of writes (n).

Number of writes (n)

$1 \leq n \leq 6$ z = 30 µs

$7 \leq n \leq 1000$ z = 200 µs

(Additional programming)

Number of writes (n)

$1 \leq n \leq 6$ z = 10 µs

6. For the maximum erase time (t_E(max)), the following relationship applies between the wait time after E bit setting (z) and the maximum number of erases (N):

t_E(max) = Wait time after E bit setting (z) × maximum number of erases (N)

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7.3 Usage Note

The F-ZTAT and mask ROM versions both satisfy the electrical characteristics shown in this manual, but actual electrical characteristic values, operating margins, noise margins, and other properties may vary due to differences in manufacturing process, on-chip ROM, layout patterns, and so on.

When system evaluation testing is carried out using the F-ZTAT version, the same evaluation testing should also be conducted for the mask ROM version when changing over to that version.

Preliminary

8.1 List of Registers (Address Order)

Table 8.1 List of Registers (Address Order)

Address	Abbre-viation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Bus Width
H'BC00	MRA	SM1	SM0	DM1	DM0	MD1	MD0	DTS	Sz	DTC	16/32*[1]
to	SAR										bits
H'BFFF											
	MRB	CHNE	DISEL	CHNS	—	—	—	—	—		
	DAR										
	CRA										
	CRB										
H'FDC0	EDSAR0	—	—	—	—	—	—	—	—	EXDMAC	16 bits
H'FDC1										channel 0	
H'FDC2											
H'FDC3											
H'FDC4	EDDAR0	—	—	—	—	—	—	—	—		
H'FDC5											
H'FDC6											
H'FDC7											
H'FDC8	EDTCR0	—	—	—	—	—	—	—	—		
H'FDC9											
H'FDCA											
H'FDCB											
H'FDCC	EDMDR0	EDA	BEF	EDRAKE	ETENDE	EDREQS	AMS	MDS1	MDS0		
H'FDCD		EDIE	IRF	TCEIE	SDIR	DTSIZE	BGUP	—	—		
H'FDCE	EDACR0	SAT1	SAT0	SARIE	SARA4	SARA3	SARA2	SARA1	SARA0		
H'FDCF		DAT1	DAT0	DARIE	DARA4	DARA3	DARA2	DARA1	DARA0		
H'FDD0	EDSAR1	—	—	—	—	—	—	—	—	EXDMAC	16 bits
H'FDD1										channel 1	
H'FDD2											
H'FDD3											

Address	Abbre-viation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Bus Width
H'FDD4	EDDAR1	—	—	—	—	—	—	—	—	EXDMAC	16 bits
H'FDD5										channel 1	
H'FDD6											
H'FDD7											
H'FDD8	EDTCR1	—	—	—	—	—	—	—	—		
H'FDD9											
H'FDDA											
H'FDDB											
H'FDDC	EDMDR1	EDA	BEF	EDRAKE	ETENDE	EDREQS	AMS	MDS1	MDS0		
H'FDDD		EDIE	IRF	TCEIE	SDIR	DTSIZE	BGUP	—	—		
H'FDDE	EDACR1	SAT1	SAT0	SARIE	SARA4	SARA3	SARA2	SARA1	SARA0		
H'FDDF		DAT1	DAT0	DARIE	DARA4	DARA3	DARA2	DARA1	DARA0		
H'FDE0	EDSAR2	—	—	—	—	—	—	—	—	EXDMAC	16 bits
H'FDE1										channel 2	
H'FDE2											
H'FDE3											
H'FDE4	EDDAR2	—	—	—	—	—	—	—	—		
H'FDE5											
H'FDE6											
H'FDE7											
H'FDE8	EDTCR2	—	—	—	—	—	—	—	—		
H'FDE9											
H'FDEA											
H'FDEB											
H'FDEC	EDMDR2	EDA	BEF	EDRAKE	ETENDE	EDREQS	AMS	MDS1	MDS0		
H'FDED		EDIE	IRF	TCEIE	SDIR	DTSIZE	BGUP	—	—		
H'FDEE	EDACR2	SAT1	SAT0	SARIE	SARA4	SARA3	SARA2	SARA1	SARA0		
H'FDEF		DAT1	DAT0	DARIE	DARA4	DARA3	DARA2	DARA1	DARA0		
H'FDF0	EDSAR3	—	—	—	—	—	—	—	—	EXDMAC	16 bits
H'FDF1										channel 3	
H'FDF2											
H'FDF3											
H'FDF4	EDDAR3	—	—	—	—	—	—	—	—		
H'FDF5											
H'FDF6											
H'FDF7											

Address	Abbre-viation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Bus Width
H'FDF8	EDTCR3	—	—	—	—	—	—	—	—	EXDMAC	16 bits
H'FDF9										channel 3	
H'FDFA											
H'FDFB											
H'FDFC	EDMDR3	EDA	BEF	EDRAKE	ETENDE	EDREQS	AMS	MDS1	MDS0		
H'FDFD		EDIE	IRF	TCEIE	SDIR	DTSIZE	BGUP	—	—		
H'FDFE	EDACR3	SAT1	SAT0	SARIE	SARA4	SARA3	SARA2	SARA1	SARA0		
H'FDFF		DAT1	DAT0	DARIE	DARA4	DARA3	DARA2	DARA1	DARA0		
H'FE00	IPRA	—	IPRA14	IPRA13	IPRA12	—	IPRA10	IPRA9	IPRA8	Interrupt	16 bits
H'FE01		—	IPRA6	IPRA5	IPRA4	—	IPRA2	IPRA1	IPRA0	controller	
H'FE02	IPRB	—	IPRB14	IPRB13	IPRB12	—	IPRB10	IPRB9	IPRB8		
H'FE03		—	IPRB6	IPRB5	IPRB4	—	IPRB2	IPRB1	IPRB0		
H'FE04	IPRC	—	IPRC14	IPRC13	IPRC12	—	IPRC10	IPRC9	IPRC8		
H'FE05		—	IPRC6	IPRC5	IPRC4	—	IPRC2	IPRC1	IPRC0		
H'FE06	IPRD	—	IPRD14	IPRD13	IPRD12	—	IPRD10	IPRD9	IPRD8		
H'FE07		—	IPRD6	IPRD5	IPRD4	—	IPRD2	IPRD1	IPRD0		
H'FE08	IPRE	—	IPRE14	IPRE13	IPRE12	—	IPRE10	IPRE9	IPRE8		
H'FE09		—	IPRE6	IPRE5	IPRE4	—	IPRE2	IPRE1	IPRE0		
H'FE0A	IPRF	—	IPRF14	IPRF13	IPRF12	—	IPRF10	IPRF9	IPRF8		
H'FE0B		—	IPRF6	IPRF5	IPRF4	—	IPRF2	IPRF1	IPRF0		
H'FE0C	IPRG	—	IPRG14	IPRG13	IPRG12	—	IPRG10	IPRG9	IPRG8		
H'FE0D		—	IPRG6	IPRG5	IPRG4	—	IPRG2	IPRG1	IPRG0		
H'FE0E	IPRH	—	IPRH14	IPRH13	IPRH12	—	IPRH10	IPRH9	IPRH8		
H'FE0F		—	IPRH6	IPRH5	IPRH4	—	IPRH2	IPRH1	IPRH0		
H'FE10	IPRI	—	IPRI14	IPRI13	IPRI12	—	IPRI10	IPRI9	IPRI8		
H'FE11		—	IPRI6	IPRI5	IPRI4	—	IPRI2	IPRI1	IPRI0		
H'FE12	IPRJ	—	IPRJ14	IPRJ13	IPRJ12	—	IPRJ10	IPRJ9	IPRJ8		
H'FE13		—	IPRJ6	IPRJ5	IPRJ4	—	IPRJ2	IPRJ1	IPRJ0		
H'FE14	IPRK	—	IPRK14	IPRK13	IPRK12	—	IPRK10	IPRK9	IPRK8		
H'FE15		—	IPRK6	IPRK5	IPRK4	—	IPRK2	IPRK1	IPRK0		
H'FE16	ITSR	ITS15	ITS14	ITS13	ITS12	ITS11	ITS10	ITS9	ITS8		
H'FE17		ITS7	ITS6	ITS5	ITS4	ITS3	ITS2	ITS1	ITS0		
H'FE18	SSIER	SSI15	SSI14	SSI13	SSI12	SSI11	SSI10	SSI9	SSI8		
H'FE19		SSI7	SSI6	SSI5	SSI4	SSI3	SSI2	SSI1	SSI0		
H'FE1A	ISCRH	IRQ15SCB	IRQ15SCA	IRQ14SCB	IRQ14SCA	IRQ13SCB	IRQ13SCA	IRQ12SCB	IRQ12SCA		
H'FE1B		IRQ11SCB	IRQ11SCA	IRQ10SCB	IRQ10SCA	IRQ9SCB	IRQ9SCA	IRQ8SCB	IRQ8SCA		
H'FE1C	ISCRL	IRQ7SCB	IRQ7SCA	IRQ6SCB	IRQ6SCA	IRQ5SCB	IRQ5SCA	IRQ4SCB	IRQ4SCA		
H'FE1D		IRQ3SCB	IRQ3SCA	IRQ2SCB	IRQ2SCA	IRQ1SCB	IRQ1SCA	IRQ0SCB	IRQ0SCA		

Address	Abbre-viation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Bus Width
H'FE1E	IrCR	IrE	IrCKS2	IrCKS1	IrCKS0	—	—	—	—	IrDA	8 bits
H'FE20	P1DDR	P17DDR	P16DDR	P15DDR	P14DDR	P13DDR	P12DDR	P11DDR	P10DDR	Ports	8 bits
H'FE21	P2DDR	P27DDR	P26DDR	P25DDR	P24DDR	P23DDR	P22DDR	P21DDR	P20DDR		
H'FE22	P3DDR	—	—	P35DDR	P34DDR	P33DDR	P32DDR	P31DDR	P30DDR		
H'FE24	P5DDR	—	—	—	—	P53DDR	P52DDR	P51DDR	P50DDR		
H'FE25	P6DDR	—	—	P65DDR	P64DDR	P63DDR	P62DDR	P61DDR	P60DDR		
H'FE26	P7DDR	—	—	P75DDR	P74DDR	P73DDR	P72DDR	P71DDR	P70DDR		
H'FE27	P8DDR	—	—	P85DDR	P84DDR	P83DDR	P82DDR	P81DDR	P80DDR		
H'FE29	PADDR	PA7DDR	PA6DDR	PA5DDR	PA4DDR	PA3DDR	PA2DDR	PA1DDR	PA0DDR		
H'FE2A	PBDDR	PB7DDR	PB6DDR	PB5DDR	PB4DDR	PB3DDR	PB2DDR	PB1DDR	PB0DDR		
H'FE2B	PCDDR	PC7DDR	PC6DDR	PC5DDR	PC4DDR	PC3DDR	PC2DDR	PC1DDR	PC0DDR		
H'FE2C	PDDDR	PD7DDR	PD6DDR	PD5DDR	PD4DDR	PD3DDR	PD2DDR	PD1DDR	PD0DDR		
H'FE2D	PEDDR	PE7DDR	PE6DDR	PE5DDR	PE4DDR	PE3DDR	PE2DDR	PE1DDR	PE0DDR		
H'FE2E	PFDDR	PF7DDR	PF6DDR	PF5DDR	PF4DDR	PF3DDR	PF2DDR	PF1DDR	PF0DDR		
H'FE2F	PGDDR	—	PG6DDR	PG5DDR	PG4DDR	PG3DDR	PG2DDR	PG1DDR	PG0DDR		
H'FE32	PFCR0	CS7E	CS6E	CS5E	CS4E	CS3E	CS2E	CS1E	CS0E		
H'FE33	PFCR1	A23E	A22E	A21E	A20E	A19E	A18E	A17E	A16E		
H'FE34	PFCR2	—	—	—	—	ASOE	LWROE	OES	DMACS		
H'FE36	PAPCR	PA7PCR	PA6PCR	PA5PCR	PA4PCR	PA3PCR	PA2PCR	PA1PCR	PA0PCR		
H'FE37	PBPCR	PB7PCR	PB6PCR	PB5PCR	PB4PCR	PB3PCR	PB2PCR	PB1PCR	PB0PCR		
H'FE38	PCPCR	PC7PCR	PC6PCR	PC5PCR	PC4PCR	PC3PCR	PC2PCR	PC1PCR	PC0PCR		
H'FE39	PDPCR	PD7PCR	PD6PCR	PD5PCR	PD4PCR	PD3PCR	PD2PCR	PD1PCR	PD0PCR		
H'FE3A	PEPCR	PE7PCR	PE6PCR	PE5PCR	PE4PCR	PE3PCR	PE2PCR	PE1PCR	PE0PCR		
H'FE3B	—										
H'FE3C	P3ODR	—	—	P35ODR	P34ODR	P33ODR	P32ODR	P31ODR	P30ODR		
H'FE3D	PAODR	PA7ODR	PA6ODR	PA5ODR	PA4ODR	PA3ODR	PA2ODR	PA1ODR	PA0ODR		
H'FE80	TCR3	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU3	16 bits
H'FE81	TMDR3	—	—	BFB	BFA	MD3	MD2	MD1	MD0		
H'FE82	TIOR3H	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FE83	TIOR3L	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0		
H'FE84	TIER3	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA		
H'FE85	TSR3	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA		
H'FE86	TCNT3										
H'FE87											
H'FE88	TGR3A										
H'FE89											
H'FE8A	TGR3B										
H'FE8B											

Address	Abbre-viation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Bus Width
H'FE8C	TGR3C									TPU3	16 bits
H'FE8D											
H'FE8E	TGR3D										
H'FE8F											
H'FE90	TCR4	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU4	16 bits
H'FE91	TMDR4	—	—	—	—	MD3	MD2	MD1	MD0		
H'FE92	TIOR4	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FE94	TIER4	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA		
H'FE95	TSR4	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA		
H'FE96	TCNT4										
H'FE97											
H'FE98	TGR4A										
H'FE99											
H'FE9A	TGR4B										
H'FE9B											
H'FEA0	TCR5	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU5	16 bits
H'FEA1	TMDR5	—	—	—	—	MD3	MD2	MD1	MD0		
H'FEA2	TIOR5	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FEA4	TIER5	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA		
H'FEA5	TSR5	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA		
H'FEA6	TCNT5										
H'FEA7											
H'FEA8	TGR5A										
H'FEA9											
H'FEAA	TGR5B										
H'FEAB											
H'FEC0	ABWCR	ABW7	ABW6	ABW5	ABW4	ABW3	ABW2	ABW1	ABW0	Bus	16 bits
H'FEC1	ASTCR	AST7	AST6	AST5	AST4	AST3	AST2	AST1	AST0	controller	
H'FEC2	WTCRAH	—	W72	W71	W70	—	W62	W61	W60		
H'FEC3	WTCRAL	—	W52	W51	W50	—	W42	W41	W40		
H'FEC4	WTCRBH	—	W32	W31	W30	—	W22	W21	W20		
H'FEC5	WTCRBL	—	W12	W11	W10	—	W02	W01	W00		
H'FEC6	RDNCR	RDN7	RDN6	RDN5	RDN4	RDN3	RDN2	RDN1	RDN0		
H'FEC8	CSACRH	CSXH7	CSXH6	CSXH5	CSXH4	CSXH3	CSXH2	CSXH1	CSXH0		
H'FEC9	CSACRL	CSXT7	CSXT6	CSXT5	CSXT4	CSXT3	CSXT2	CSXT1	CSXT0		
H'FECA	BROMCRH	BSRM0	BSTS02	BSTS01	BSTS00	—	—	BSWD01	BSWD00		
H'FECB	BROMCRL	BSRM1	BSTS12	BSTS11	BSTS10	—	—	BSWD11	BSWD10		

Address	Abbre-viation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Bus Width
H'FECC	BCR	BRLE	BREQ0E	—	IDLC	ICIS1	ICIS0	WDBE	WAITE	Bus controller	16 bits
H'FECD		—	—	—	—	—	—	—	—		
H'FECE*[8]	RAMER	—	—	—	—	RAMS	RAM2	RAM1	RAM0	ROM	8 bits
H'FED0	DRAMCR	0EE	RAST	—	CAST	—	RMTS2	RMTS1	RMTS0	Bus controller	16 bits
H'FED1		BE	RCDM	DDS	EDDS	—	MXC2	MXC1	MXC0		
H'FED2	DRACCR	DRMI	—	TPC1	TPC0	—	—	RCD1	RCD0		
H'FED3	—										
H'FED4	REFCR	CMF	CMIE	RCW1	RCW0	—	RTCK2	RTCK1	RTCK0		
H'FED5		RFSHE	CBRM	RLW1	RLW0	SLFRF	TPCS2	TPCS1	TPCS0		
H'FED6	RTCNT										
H'FED7	RTCOR										
H'FEE0	MAR0AH	—	—	—	—	—	—	—	—	DMAC	16 bits
H'FEE1											
H'FEE2	MAR0AL										
H'FEE3											
H'FEE4	IOAR0A										
H'FEE5											
H'FEE6	ETCR0A										
H'FEE7											
H'FEE8	MAR0BH	—	—	—	—	—	—	—	—		
H'FEE9											
H'FEEA	MAR0BL										
H'FEEB											
H'FEEC	IOAR0B										
H'FEED											
H'FEEE	ETCR0B										
H'FEEF											
H'FEF0	MAR1AH	—	—	—	—	—	—	—	—		
H'FEF1											
H'FEF2	MAR1AL										
H'FEF3											
H'FEF4	IOAR1A										
H'FEF5											
H'FEF6	ETCR1A										
H'FEF7											
H'FEF8	MAR1BH	—	—	—	—	—	—	—	—		
H'FEF9											

Address	Abbre-viation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Bus Width
H'FEFA	MAR1BL									DMAC	16 bits
H'FEFB											
H'FEFC	IOAR1B										
H'FEFD											
H'FEFE	ETCR1B										
H'FEFF											
H'FF20	DMAWER	—	—	—	—	WE1B	WE1A	WE0B	WE0A		8 bits
H'FF21	DMATCR	—	—	TEE1	TEE0	—	—	—	—		
H'FF22	DMACR0A	DTSZ	DTID	RPE	DTDIR	DTF3	DTF2	DTF1	DTF0	Short address mode	16 bits
		DTSZ	SAID	SAIDE	BLKDIR	BLKE	—	—	—	Full address mode	
H'FF23	DMACR0B	DTSZ	DTID	RPE	DTDIR	DTF3	DTF2	DTF1	DTF0	Short address mode	
		—	DAID	DAIDE	—	DTF3	DTF2	DTF1	DTF0	Full address mode	
H'FF24	DMACR1A	DTSZ	DTID	RPE	DTDIR	DTF3	DTF2	DTF1	DTF0	Short address mode	
		DTSZ	SAID	SAIDE	BLKDIR	BLKE	—	—	—	Full address mode	
H'FF25	DMACR1B	DTSZ	DTID	RPE	DTDIR	DTF3	DTF2	DTF1	DTF0	Short address mode	
		—	DAID	DAIDE	—	DTF3	DTF2	DTF1	DTF0	Full address mode	
H'FF26	DMABCRH	FAE1	FAE0	SAE1	SAE0	DTA1B	DTA1A	DTA0B	DTA0A	Short address mode	
		FAE1	FAE0	—	—	DTA1	—	DTA0	—	Full address mode	

Address	Abbre-viation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Bus Width
H'FF27	DMABCRL	DTE1B	DTE1A	DTE0B	DTE0A	DTIE1B	DTIE1A	DTIE0B	DTIE0A	Short address mode	16 bits
		DTME1	DTE1	DTME0	DTE0	DTIE1B	DTIE1A	DTIE0B	DTIE0A	Full address mode	
H'FF28 to H'FF2F	DTCER	DTCE7	DTCE6	DTCE5	DTCE4	DTCE3	DTCE2	DTCE1	DTCE0	DTC	16 bits
H'FF30	DTVECR	SWDTE	DTVEC6	DTVEC5	DTVEC4	DTVEC3	DTVEC2	DTVEC1	DTVEC0	Interrupt controller	16 bits
H'FF31	INTCR	—	—	INTM1	INTM0	NMIEG	—	—	—		
H'FF32	IER	IRQ15E	IRQ14E	IRQ13E	IRQ12E	IRQ11E	IRQ10E	IRQ9E	IRQ8E		
H'FF33		IRQ7E	IRQ6E	IRQ5E	IRQ4E	IRQ3E	IRQ2E	IRQ1E	IRQ0E		
H'FF34	ISR	IRQ15F	IRQ14F	IRQ13F	IRQ12F	IRQ11F	IRQ10F	IRQ9F	IRQ8F		
H'FF35		IRQ7F	IRQ6F	IRQ5F	IRQ4F	IRQ3F	IRQ2F	IRQ1F	IRQ0F		
H'FF3A	SBYCR	SSBY	OPE	—	—	STS3	STS2	STS1	STS0	System controller	8 bits
H'FF3B	SCKCR	PSTOP	—	—	—	STCS	SCK2	SCK1	SCK0		
H'FF3D	SYSCR	—	—	MACS	—	FLSHE	—	EXPE	RAME		
H'FF3E	MDCR	—	—	—	—	—	MDS2	MDS1	MDS0		
H'FF40	MSTPCRH	ACSE	MSTP14	MSTP13	MSTP12	MSTP11	MSTP10	MSTP9	MSTP8		
H'FF41	MSTPCRL	MSTP7	MSTP6	MSTP5	MSTP4	MSTP3	MSTP2	MSTP1	MSTP0		
H'FF45	PLLCR	0	0	0	0	0	0	STC1	STC0		
H'FF46	PCR	G3CMS1	G3CMS0	G2CMS1	G2CMS0	G1CMS1	G1CMS0	G0CMS1	G0CMS0	PPG	8 bits
H'FF47	PMR	G3INV	G2INV	G1INV	G0INV	G3NOV	G2NOV	G1NOV	G0NOV		
H'FF48	NDERH	NDER15	NDER14	NDER13	NDER12	NDER11	NDER10	NDER9	NDER8		
H'FF49	NDERL	NDER7	NDER6	NDER5	NDER4	NDER3	NDER2	NDER1	NDER0		
H'FF4A	PODRH	POD15	POD14	POD13	POD12	POD11	POD10	POD9	POD8		
H'FF4B	PODRL	POD7	POD6	POD5	POD4	POD3	POD2	POD1	POD0		
H'FF4C*2	NDRH	NDR15	NDR14	NDR13	NDR12	NDR11	NDR10	NDR9	NDR8		
H'FF4D*2	NDRL	NDR7	NDR6	NDR5	NDR4	NDR3	NDR2	NDR1	NDR0		
H'FF4E*2	NDRH	—	—	—	—	NDR11	NDR10	NDR9	NDR8		
H'FF4F*2	NDRL	—	—	—	—	NDR3	NDR2	NDR1	NDR0		
H'FF50	PORT1	P17	P16	P15	P14	P13	P12	P11	P10	Ports	8 bits
H'FF51	PORT2	P27	P26	P25	P24	P23	P22	P21	P20		
H'FF52	PORT3	—	—	P35	P34	P33	P32	P31	P30		
H'FF53	PORT4	P47	P46	P45	P44	P43	P42	P41	P40		
H'FF54	PORT5	P57	P56	P55	P54	P53	P52	P51	P50		
H'FF55	PORT6	—	—	P65	P64	P63	P62	P61	P60		
H'FF56	PORT7	—	—	P75	P74	P73	P72	P71	P70		
H'FF57	PORT8	—	—	P85	P84	P83	P82	P81	P80		

Address	Abbre-viation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Bus Width
H'FF59	PORTA	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	Ports	8 bits
H'FF5A	PORTB	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0		
H'FF5B	PORTC	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0		
H'FF5C	PORTD	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0		
H'FF5D	PORTE	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0		
H'FF5E	PORTF	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0		
H'FF5F	PORTG	—	PG6	PG5	PG4	PG3	PG2	PG1	PG0		
H'FF60	P1DR	P17DR	P16DR	P15DR	P14DR	P13DR	P12DR	P11DR	P10DR		
H'FF61	P2DR	P27DR	P26DR	P25DR	P24DR	P23DR	P22DR	P21DR	P20DR		
H'FF62	P3DR	—	—	P35DR	P34DR	P33DR	P32DR	P31DR	P30DR		
H'FF64	P5DR	—	—	—	—	P53DR	P52DR	P51DR	P50DR		
H'FF65	P6DR	—	—	P65DR	P64DR	P63DR	P62DR	P61DR	P60DR		
H'FF66	P7DR	—	—	P75DR	P74DR	P73DR	P72DR	P71DR	P70DR		
H'FF67	P8DR	—	—	P85DR	P84DR	P83DR	P82DR	P81RD	P80DR		
H'FF69	PADR	PA7DR	PA6DR	PA5DR	PA4DR	PA3DR	PA2DR	PA1DR	PA0DR		
H'FF6A	PBDR	PB7DR	PB6DR	PB5DR	PB4DR	PB3DR	PB2DR	PB1DR	PB0DR		
H'FF6B	PCDR	PC7DR	PC6DR	PC5DR	PC4DR	PC3DR	PC2DR	PC1DR	PC0DR		
H'FF6C	PDDR	PD7DR	PD6DR	PD5DR	PD4DR	PD3DR	PD2DR	PD1DR	PD0DR		
H'FF6D	PEDR	PE7DR	PE6DR	PE5DR	PE4DR	PE3DR	PE2DR	PE1DR	PE0DR		
H'FF6E	PFDR	PF7DR	PF6DR	PF5DR	PF4DR	PF3DR	PF2DR	PF1DR	PF0DR		
H'FF6F	PGDR	—	PG6DR	PG5DR	PG4DR	PG3DR	PG2DR	PG1DR	PG0DR		
H'FF70	PORTH	—	—	—	—	PH3	PH2	PH1	PH0		
H'FF72	PHDR	—	—	—	—	PH3DR	PH2DR	PH1DR	PH0DR		
H'FF74	PHDDR	—	—	—	—	PH3DDR	PH2DDR	PH1DDR	PH0DDR		
H'FF78	SMR0	C/$\overline{A}$/ GM*[3]	CHR/ BLK*[4]	PE	O/$\overline{E}$	STOP/ BCP1*[5]	MP/ BCP 0*[6]	CKS1	CKS0	SCI0, smart card interface 0	8 bits
H'FF79	BRR0										
H'FF7A	SCR0	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0		
H'FF7B	TDR0										
H'FF7C	SSR0	TDRE	RDRF	ORER	FER/ ERS*[7]	PER	TEND	MPB	MPBT		
H'FF7D	RDR0										
H'FF7E	SCMR0	—	—	—	—	SDIR	SINV	—	SMIF		
H'FF80	SMR1	C/$\overline{A}$/ GM*[3]	CHR/ BLK*[4]	PE	O/$\overline{E}$	STOP/ BCP1*[5]	MP/ BCP0*[6]	CKS1	CKS0	SCI1, smart card interface 1	8 bits
H'FF81	BRR1										
H'FF82	SCR1	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0		
H'FF83	TDR1										

Address	Abbre-viation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Bus Width
H'FF84	SSR1	TDRE	RDRF	ORER	FER/ ERS*[7]	PER	TEND	MPB	MPBT	SCI1, smart card interface 1	8 bits
H'FF85	RDR1										
H'FF86	SCMR1	—	—	—	—	SDIR	SINV	—	SMIF		
H'FF88	SMR2	C/$\overline{A}$/ GM*[3]	CHR/ BLK*[4]	PE	O/$\overline{E}$	STOP/ BCP1*[5]	MP/ BCP0*[6]	CKS1	CKS0	SCI2, smart card interface 2	8 bits
H'FF89	BRR2										
H'FF8A	SCR2	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0		
H'FF8B	TDR2										
H'FF8C	SSR2	TDRE	RDRF	ORER	FER/ ERS*[7]	PER	TEND	MPB	MPBT		
H'FF8D	RDR2										
H'FF8E	SCMR2	—	—	—	—	SDIR	SINV	—	SMIF		
H'FF90	ADDRAH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	A/D converter	8 bits
H'FF91	ADDRAL	AD1	AD0	—	—	—	—	—	—		
H'FF92	ADDRBH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FF93	ADDRBL	AD1	AD0	—	—	—	—	—	—		
H'FF94	ADDRCH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FF95	ADDRCL	AD1	AD0	—	—	—	—	—	—		
H'FF96	ADDRDH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FF97	ADDRDL	AD1	AD0	—	—	—	—	—	—		
H'FF98	ADCSR	ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0		
H'FF99	ADCR	TRGS1	TRGS0	—	—	CKS1	CH3	—	—		
H'FFA4	DADR0									D/A	8 bits
H'FFA5	DADR1										
H'FFA6	DACR01	DAOE1	DAOE0	DAE	—	—	—	—	—		
H'FFA8	DADR2										
H'FFA9	DADR3										
H'FFAA	DACR23	DAOE1	DAOE0	DAE	—	—	—	—	—		
H'FFB0	TCR0	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0	8-bit timer channel 0, 1	16 bits
H'FFB1	TCR1	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0		
H'FFB2	TCSR0	CMFB	CMFA	OVF	ADTE	OS3	OS2	OS1	OS0		
H'FFB3	TCSR1	CMFB	CMFA	OVF	—	OS3	OS2	OS1	OS0		
H'FFB4	TCORA0										
H'FFB5	TCORA1										
H'FFB6	TCORB0										
H'FFB7	TCORB1										
H'FFB8	TCNT0										
H'FFB9	TCNT1										

Address	Abbre-viation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Bus Width
H'FFBC (read)	TCSR	OVF	WT/$\overline{IT}$	TME	—	—	CKS2	CKS1	CKS0	Watchdog timer	16 bits
H'FFBD (read)	TCNT										
H'FFBF (read)	RSTCSR	WOVF	RSTE	—	—	—	—	—	—		
H'FFC0	TSTR	—	—	CST5	CST4	CST3	CST2	CST1	CST0	TPU	16 bits
H'FFC1	TSYR	—	—	SYNC5	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0		
H'FFC8	FLMCR1*[8]	FWE	SWE	ESU	PSU	EV	PV	E	P	FLASH	8 bits
H'FFC9	FLMCR2*[8]	FLER	—	—	—	—	—	ESU	PSU		
H'FFCA	EBR1*[8]	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0		
H'FFCB	EBR2*[8]	—	—	—	—	—	EB10	EB9	EB8		
H'FFD0	TCR0	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU0	16 bits
H'FFD1	TMDR0	—	—	BFB	BFA	MD3	MD2	MD1	MD0		
H'FFD2	TIOR0H	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FFD3	TIOR0L	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0		
H'FFD4	TIER0	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA		
H'FFD5	TSR0	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA		
H'FFD6	TCNT0										
H'FFD7											
H'FFD8	TGR0A										
H'FFD9											
H'FFDA	TGR0B										
H'FFDB											
H'FFDC	TGR0C										
H'FFDD											
H'FFDE	TGR0D										
H'FFDF											
H'FFE0	TCR1	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU1	16 bits
H'FFE1	TMDR1	—	—	—	—	MD3	MD2	MD1	MD0		
H'FFE2	TIOR1	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FFE4	TIER1	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA		
H'FFE5	TSR1	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA		
H'FFE6	TCNT1										
H'FFE7											
H'FFE8	TGR1A										
H'FFE9											
H'FFEA	TGR1B										
H'FFEB											

Address	Abbre-viation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Bus Width
H'FFF0	TCR2	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU2	16 bits
H'FFF1	TMDR2	—	—	—	—	MD3	MD2	MD1	MD0		
H'FFF2	TIOR2	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FFF4	TIER2	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA		
H'FFF5	TSR2	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA		
H'FFF6	TCNT2										
H'FFF7											
H'FFF8	TGR2A										
H'FFF9											
H'FFFA	TGR2B										
H'FFFB											

Notes:
1. Located in on-chip RAM. The bus width is 32 bits when the DTC accesses this area as register information, and 16 bits otherwise.
2. If the pulse output group 2 and pulse output group 3 output triggers are the same according to the PCR setting, the NDRH address will be H'FF4C, and if different, the address of NDRH for group 2 will be H'FF4E, and that for group 3 will be H'FF4C. Similarly, if the pulse output group 0 and pulse output group 1 output triggers are the same according to the PCR setting, the NDRL address will be H'FF4D, and if different, the address of NDRL for group 0 will be H'FF4F, and that for group 1 will be H'FF4D.
3. Functions as C/$\overline{A}$ for SCI use, and as GM for smart card interface use.
4. Functions as CHR for SCI use, and as BLK for smart card interface use.
5. Functions as STOP for SCI use, and as BCP1 for smart card interface use.
6. Functions as MP for SCI use, and as BCP0 for smart card interface use.
7. Functions as FER for SCI use, and as ERS for smart card interface use.
8. Valid only in F-ZTAT version

8.2 List of Registers (By Module)

Table 8.2 List of Registers (By Module)

Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
Interrupt controller	Interrupt control register	INTCR	R/W	H'00	H'FF31
	IRQ sense control register H	ISCRH	R/W	H'0000	H'FF1A
	IRQ sense control register L	ISCRL	R/W	H'0000	H'FF1C
	IRQ enable register	IER	R/W	H'0000	H'FF32
	IRQ status register	ISR	R/(W)*[2]	H'0000	H'FF34
	IRQ pin select register	ITSR	R/W	H'0000	H'FE16
	Software standby clearing IRQ enable register	SSIER	R/W	H'0007	H'FE18
	Interrupt priority register A	IPRA	R/W	H'7777	H'FE00
	Interrupt priority register B	IPRB	R/W	H'7777	H'FE02
	Interrupt priority register C	IPRC	R/W	H'7777	H'FE04
	Interrupt priority register D	IPRD	R/W	H'7777	H'FE06
	Interrupt priority register E	IPRE	R/W	H'7777	H'FE08
	Interrupt priority register F	IPRF	R/W	H'7777	H'FE0A
	Interrupt priority register G	IPRG	R/W	H'7777	H'FE0C
	Interrupt priority register H	IPRH	R/W	H'7777	H'FE0E
	Interrupt priority register I	IPRI	R/W	H'7777	H'FE10
	Interrupt priority register J	IPRJ	R/W	H'7777	H'FE12
	Interrupt priority register K	IPRK	R/W	H'7777	H'FE14
DMAC channel 0	Memory address register 0A	MAR0A	R/W	Undefined	H'FEE0
	I/O address register 0A	IOAR0A	R/W	Undefined	H'FEE4
	Execute transfer count register 0A	ETCR0A	R/W	Undefined	H'FEE6
	Memory address register 0B	MAR0B	R/W	Undefined	H'FEE8
	I/O address register 0B	IOAR0B	R/W	Undefined	H'FEEC
	Execute transfer count register 0B	ETCR0B	R/W	Undefined	H'FEEE
DMAC channel 1	Memory address register 1A	MAR1A	R/W	Undefined	H'FEF0
	I/O address register 1A	IOAR1A	R/W	Undefined	H'FEF4
	Execute transfer count register 1A	ETCR1A	R/W	Undefined	H'FEF6
	Memory address register 1B	MAR1B	R/W	Undefined	H'FEF8
	I/O address register 1B	IOAR1B	R/W	Undefined	H'FEFC
	Execute transfer count register 1B	ETCR1B	R/W	Undefined	H'FEFE

Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
DMAC channels 0 and 1	DMA write enable register	DMAWER	R/W	H'00	H'FF20
	DMA terminal control register	DMATCR	R/W	H'00	H'FF21
	DMA control register 0A	DMACR0A	R/W	H'00	H'FF22
	DMA control register 0B	DMACR0B	R/W	H'00	H'FF23
	DMA control register 1A	DMACR1A	R/W	H'00	H'FF24
	DMA control register 1B	DMACR1B	R/W	H'00	H'FF25
	DMA band control register	DMABCR	R/W	H'0000	H'FF26
	Module stop control register	MSTPCR	R/W	H'0FFF	H'FF40
DTC	DTC mode register A	MRA	—*[3]	Undefined	—*[4]
	DTC mode register B	MRB	—*[3]	Undefined	—*[4]
	DTC source address register	SAR	—*[3]	Undefined	—*[4]
	DTC destination address register	DAR	—*[3]	Undefined	—*[4]
	DTC transfer count register A	CRA	—*[3]	Undefined	—*[4]
	DTC transfer count register B	CRB	—*[3]	Undefined	—*[4]
	DTC enable register	DTCER	R/W	H'00	H'FF28 to H'FF2F
	DTC vector register	DTVECR	R/W	H'00	H'FF30
	Module stop control register	MSTPCR	R/W	H'0FFF	H'FF40
EXDMAC channel 0	EXDMA source address register 0	EDSAR0	R/W	Undefined	H'FDC0
	EXDMA destination address register 0	EDDAR0	R/W	Undefined	H'FDC4
	EXDMA transfer count register 0	EDTCR0	R/W	Undefined	H'FDC8
	EXDMA mode control register 0	EDMDR0	R/W*[5]	H'0000	H'FDCC
	EXDMA address control register 0	EDACR0	R/W	H'0000	H'FDCE
EXDMAC channel 1	EXDMA source address register 1	EDSAR1	R/W	Undefined	H'FDD0
	EXDMA destination address register 1	EDDAR1	R/W	Undefined	H'FDD4
	EXDMA transfer count register 1	EDTCR1	R/W	Undefined	H'FDD8
	EXDMA mode control register 1	EDMDR1	R/W*[5]	H'0000	H'FDDC
	EXDMA address control register 1	EDACR1	R/W	H'0000	H'FDDE

Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
EXDMAC channel 2	EXDMA source address register 2	EDSAR2	R/W	Undefined	H'FDE0
	EXDMA destination address register 2	EDDAR2	R/W	Undefined	H'FDE4
	EXDMA transfer count register 2	EDTCR2	R/W	Undefined	H'FDE8
	EXDMA mode control register 2	EDMDR2	R/W*[5]	H'0000	H'FDEC
	EXDMA address control register 2	EDACR2	R/W	H'0000	H'FDEE
EXDMAC channel 3	EXDMA source address register 3	EDSAR3	R/W	Undefined	H'FDF0
	EXDMA destination address register 3	EDDAR3	R/W	Undefined	H'FDF4
	EXDMA transfer count register 3	EDTCR3	R/W	Undefined	H'FDF8
	EXDMA mode control register 3	EDMDR3	R/W*[5]	H'0000	H'FDFC
	EXDMA address control register 3	EDACR3	R/W	H'0000	H'FDFE
All EXDMAC channels	Module stop control register	MSTPCR	R/W	H'0FFF	H'FF40
Bus controller	Bus width control register	ABWCR	R/W	H'FF/H'00*[6]	H'FEC0
	Access state control register	ASTCR	R/W	H'FF	H'FEC1
	Wait control register A	WTCRA	R/W	H'7777	H'FEC2
	Wait control register B	WTCRB	R/W	H'7777	H'FEC4
	Read strobe timing control register	RDNCR	R/W	H'00	H'FEC6
	Chip select assertion period control register	CSACRH	R/W	H'00	H'FEC8
		CSACRL	R/W	H'00	H'FEC9
	Burst ROM interface control register	BROMCRH	R/W	H'00	H'FECA
		BROMCRL	R/W	H'00	H'FECB
	Bus control register	BCR	R/W	H'1C00	H'FECC
	DRAM control register	DRAMCR	R/W	H'0000	H'FED0
	DRAM access control register	DRACCR	R/W	H'00	H'FED2
	Refresh control register	REFCR	R/W	H'0000	H'FED4
	Refresh timer counter	RTCNT	R/W	H'00	H'FED6
	Refresh time constant register	RTCOR	R/W	H'FF	H'FED7
TPU0	Timer control register 0	TCR0	R/W	H'00	H'FFD0
	Timer mode register 0	TMDR0	R/W	H'C0	H'FFD1
	Timer I/O control register 0H	TIOR0H	R/W	H'00	H'FFD2
	Timer I/O control register 0L	TIOR0L	R/W	H'00	H'FFD3

Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
TPU0	Timer interrupt enable register 0	TIER0	R/W	H'40	H'FFD4
	Timer status register 0	TSR0	R/(W)*[2]	H'C0	H'FFD5
	Timer counter 0	TCNT0	R/W	H'0000	H'FFD6
	Timer general register 0A	TGR0A	R/W	H'FFFF	H'FFD8
	Timer general register 0B	TGR0B	R/W	H'FFFF	H'FFDA
	Timer general register 0C	TGR0C	R/W	H'FFFF	H'FFDC
	Timer general register 0D	TGR0D	R/W	H'FFFF	H'FFDE
TPU1	Timer control register 1	TCR1	R/W	H'00	H'FFE0
	Timer mode register 1	TMDR1	R/W	H'C0	H'FFE1
	Timer I/O control register 1	TIOR1	R/W	H'00	H'FFE2
	Timer interrupt enable register 1	TIER1	R/W	H'40	H'FFE4
	Timer status register 1	TSR1	R/(W)*[2]	H'C0	H'FFE5
	Timer counter 1	TCNT1	R/W	H'0000	H'FFE6
	Timer general register 1A	TGR1A	R/W	H'FFFF	H'FFE8
	Timer general register 1B	TGR1B	R/W	H'FFFF	H'FFEA
TPU2	Timer control register 2	TCR2	R/W	H'00	H'FFF0
	Timer mode register 2	TMDR2	R/W	H'C0	H'FFF1
	Timer I/O control register 2	TIOR2	R/W	H'00	H'FFF2
	Timer interrupt enable register 2	TIER2	R/W	H'40	H'FFF4
	Timer status register 2	TSR2	R/(W)*[2]	H'C0	H'FFF5
	Timer counter 2	TCNT2	R/W	H'0000	H'FFF6
	Timer general register 2A	TGR2A	R/W	H'FFFF	H'FFF8
	Timer general register 2B	TGR2B	R/W	H'FFFF	H'FFFA
TPU3	Timer control register 3	TCR3	R/W	H'00	H'FE80
	Timer mode register 3	TMDR3	R/W	H'C0	H'FE81
	Timer I/O control register 3H	TIOR3H	R/W	H'00	H'FE82
	Timer I/O control register 3L	TIOR3L	R/W	H'00	H'FE83
	Timer interrupt enable register 3	TIER3	R/W	H'40	H'FE84
	Timer status register 3	TSR3	R/(W)*[2]	H'C0	H'FE85
	Timer counter 3	TCNT3	R/W	H'0000	H'FE86
	Timer general register 3A	TGR3A	R/W	H'FFFF	H'FE88
	Timer general register 3B	TGR3B	R/W	H'FFFF	H'FE8A

Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
TPU3	Timer general register 3C	TGR3C	R/W	H'FFFF	H'FE8C
	Timer general register 3D	TGR3D	R/W	H'FFFF	H'FE8E
TPU4	Timer control register 4	TCR4	R/W	H'00	H'FE90
	Timer mode register 4	TMDR4	R/W	H'C0	H'FE91
	Timer I/O control register 4	TIOR4	R/W	H'00	H'FE92
	Timer interrupt enable register 4	TIER4	R/W	H'40	H'FE94
	Timer status register 4	TSR4	R/(W)*[2]	H'C0	H'FE95
	Timer counter 4	TCNT4	R/W	H'0000	H'FE96
	Timer general register 4A	TGR4A	R/W	H'FFFF	H'FE98
	Timer general register 4B	TGR4B	R/W	H'FFFF	H'FE9A
TPU5	Timer control register 5	TCR5	R/W	H'00	H'FEA0
	Timer mode register 5	TMDR5	R/W	H'C0	H'FEA1
	Timer I/O control register 5	TIOR5	R/W	H'00	H'FEA2
	Timer interrupt enable register 5	TIER5	R/W	H'40	H'FEA4
	Timer status register 5	TSR5	R/(W)*[2]	H'C0	H'FEA5
	Timer counter 5	TCNT5	R/W	H'0000	H'FEA6
	Timer general register 5A	TGR5A	R/W	H'FFFF	H'FEA8
	Timer general register 5B	TGR5B	R/W	H'FFFF	H'FEAA
All TPU channels	Timer start register	TSTR	R/W	H'00	H'FFC0
	Timer sync register	TSYR	R/W	H'00	H'FFC1
	Module stop control register	MSTPCR	R/W	H'0FFF	H'FF40
PPG	PPG output control register	PCR	R/W	H'FF	H'FF46
	PPG output mode register	PMR	R/W	H'F0	H'FF47
	Next data enable register H	NDERH	R/W	H'00	H'FF48
	Next data enable register L	NDERL	R/W	H'00	H'FF49
	Output data register H	PODRH	R/(W)*[7]	H'00	H'FF4A
	Output data register L	PODRL	R/(W)*[7]	H'00	H'FF4B
	Next data register H	NDRH	R/W	H'00	H'FF4C*[8] H'FF4E
	Next data register L	NDRL	R/W	H'00	H'FF4D*[8] H'FF4F
	Port 1 data direction register	P1DDR	W	H'00	H'FE20
	Port 2 data direction register	P2DDR	W	H'00	H'FE21
	Module stop control register	MSTPCR	R/W	H'0FFF	H'FF40

Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
8-bit timer 0	Timer control register 0	TCR0	R/W	H'00	H'FFB0
	Timer control/status register 0	TCSR0	R/(W)*[9]	H'00	H'FFB2
	Timer constant register A0	TCORA0	R/W	H'FF	H'FFB4
	Timer constant register B0	TCORB0	R/W	H'FF	H'FFB6
	Timer counter 0	TCNT0	R/W	H'00	H'FFB8
8-bit timer 1	Timer control register 1	TCR1	R/W	H'00	H'FFB1
	Timer control/status register 1	TCSR1	R/(W)*[9]	H'10	H'FFB3
	Timer constant register A1	TCORA1	R/W	H'FF	H'FFB5
	Timer constant register B1	TCORB1	R/W	H'FF	H'FFB7
	Timer counter 1	TCNT1	R/W	H'00	H'FFB9
Both 8-bit timer channels	Module stop control register	MSTPCR	R/W	H'0FFF	H'FF40
WDT	Timer control/status register	TCSR	R/(W)*[11]	H'18	H'FFBC*[10]
	Timer counter	TCNT	R/W	H'00	H'FFBC: Write*[10] H'FFBD: Read
	Reset control/status register	RSTCSR	R/(W)*[11]	H'1F	H'FFBE: Write*[10] H'FFBF: Read
SCI0	Serial mode register 0	SMR0	R/W	H'00	H'FF78
	Bit rate register 0	BRR0	R/W	H'FF	H'FF79
	Serial control register 0	SCR0	R/W	H'00	H'FF7A
	Transmit data register 0	TDR0	R/W	H'FF	H'FF7B
	Serial status register 0	SSR0	R/(W)*[2]	H'84	H'FF7C
	Receive data register 0	RDR0	R	H'00	H'FF7D
	Smart card mode register 0	SCMR0	R/W	H'F2	H'FF7E
	IrDA control register	IrCR	R/W	H'00	H'FE1E
SCI1	Serial mode register 1	SMR1	R/W	H'00	H'FF80
	Bit rate register 1	BRR1	R/W	H'FF	H'FF81
	Serial control register 1	SCR1	R/W	H'00	H'FF82

Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
SCI1	Transmit data register 1	TDR1	R/W	H'FF	H'FF83
	Serial status register 1	SSR1	R/(W)*[2]	H'84	H'FF84
	Receive data register 1	RDR1	R	H'00	H'FF85
	Smart card mode register 1	SCMR1	R/W	H'F2	H'FF86
SCI2	Serial mode register 2	SMR2	R/W	H'00	H'FF88
	Bit rate register 2	BRR2	R/W	H'FF	H'FF89
	Serial control register 2	SCR2	R/W	H'00	H'FF8A
	Transmit data register 2	TDR2	R/W	H'FF	H'FF8B
	Serial status register 2	SSR2	R/(W)*[2]	H'84	H'FF8C
	Receive data register 2	RDR2	R	H'00	H'FF8D
	Smart card mode register 2	SCMR2	R/W	H'F2	H'FF8E
All SCI channels	Module stop control register	MSTPCR	R/W	H'0FFF	H'FF40
ADC	A/D data register AH	ADDRAH	R	H'00	H'FF90
	A/D data register AL	ADDRAL	R	H'00	H'FF91
	A/D data register BH	ADDRBH	R	H'00	H'FF92
	A/D data register BL	ADDRBL	R	H'00	H'FF93
	A/D data register CH	ADDRCH	R	H'00	H'FF94
	A/D data register CL	ADDRCL	R	H'00	H'FF95
	A/D data register DH	ADDRDH	R	H'00	H'FF96
	A/D data register DL	ADDRDL	R	H'00	H'FF97
	A/D control/status register	ADCSR	R/(W)*[11]	H'00	H'FF98
	A/D control register	ADCR	R/W	H'3F	H'FF99
	Module stop control register	MSTPCR	R/W	H'0FFF	H'FF40
DAC0, 1	D/A data register 0	DADR0	R/W	H'00	H'FFA4
	D/A data register 1	DADR1	R/W	H'00	H'FFA5
	D/A control register 01	DACR01	R/W	H'1F	H'FFA6
DAC2, 3	D/A data register 2	DADR2	R/W	H'00	H'FFA8
	D/A data register 3	DADR3	R/W	H'00	H'FFA9
	D/A control register 23	DACR23	R/W	H'1F	H'FFAA
All DAC channels	Module stop control register	MSTPCR	R/W	H'0FFF	H'FF40

Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
On-chip RAM	System control register	SYSCR	R/W	H'81	H'FF3D
Flash memory	Flash memory control register 1	FLMCR1*[16]	R/W*[13]	H'00*[14]	H'FFC8*[12]
	Flash memory control register 2	FLMCR2*[16]	R/W*[13]	H'00*[15]	H'FFC9*[12]
	Erase block register 1	EBR1*[16]	R/W*[13]	H'00*[15]	H'FFCA*[12]
	Erase block register 2	EBR2*[16]	R/W*[13]	H'00*[15]	H'FFCB*[12]
	RAM emulation register	RAMER	R/W	H'00	H'FECE*[18]
System control	Standby control register	SBYCR	R/W	H'0F	H'FF3A
	System clock control register	SCKCR	R/W	H'00	H'FF3B
	System control register	SYSCR	R/W	Undefined	H'FF3D
	Mode control register	MDCR	R	Undefined	H'FF3E
	Module stop control register H	MSTPCRH	R/W	H'0F	H'FF40
	Module stop control register L	MSTPCRL	R/W	H'FF	H'FF41
	PLL control register	PLLCR	R/W	H'00	H'FF45
	Software standby clearing IRQ enable register	SSIER	R/W	H'0007	H'FE18
Power-down state	Standby control register	SBYCR	R/W	H'0F	H'FF3A
	System clock control register	SCKCR	R/W	H'00	H'FF3B
	Module stop control register H	MSTPCRH	R/W	H'0F	H'FF40
	Module stop control register L	MSTPCRL	R/W	H'FF	H'FF41
	Software standby clearing IRQ enable register	SSIER	R/W	H'FF	H'FE18
Port 1	Port 1 data direction register	P1DDR	W	H'00	H'FE20
	Port 1 data register	P1DR	R/W	H'00	H'FF60
	Port 1 register	PORT1	R	Undefined	H'FF50
Port 2	Port 2 data direction register	P2DDR	W	H'00	H'FE21
	Port 2 data register	P2DR	R/W	H'00	H'FF61
	Port 2 register	PORT2	R	Undefined	H'FF51
Port 3	Port 3 data direction register	P3DDR	W	H'00	H'FE22
	Port 3 data register	P3DR	R/W	H'00	H'FF62
	Port 3 register	PORT3	R	Undefined	H'FF52
	Port 3 open drain control register	P3ODR	R/W	H'00	H'FE3C
Port 4	Port 4 register	PORT4	R	Undefined	H'FF53
	Port function control register 2	PFCR2	R/W	H'0E	H'FE34

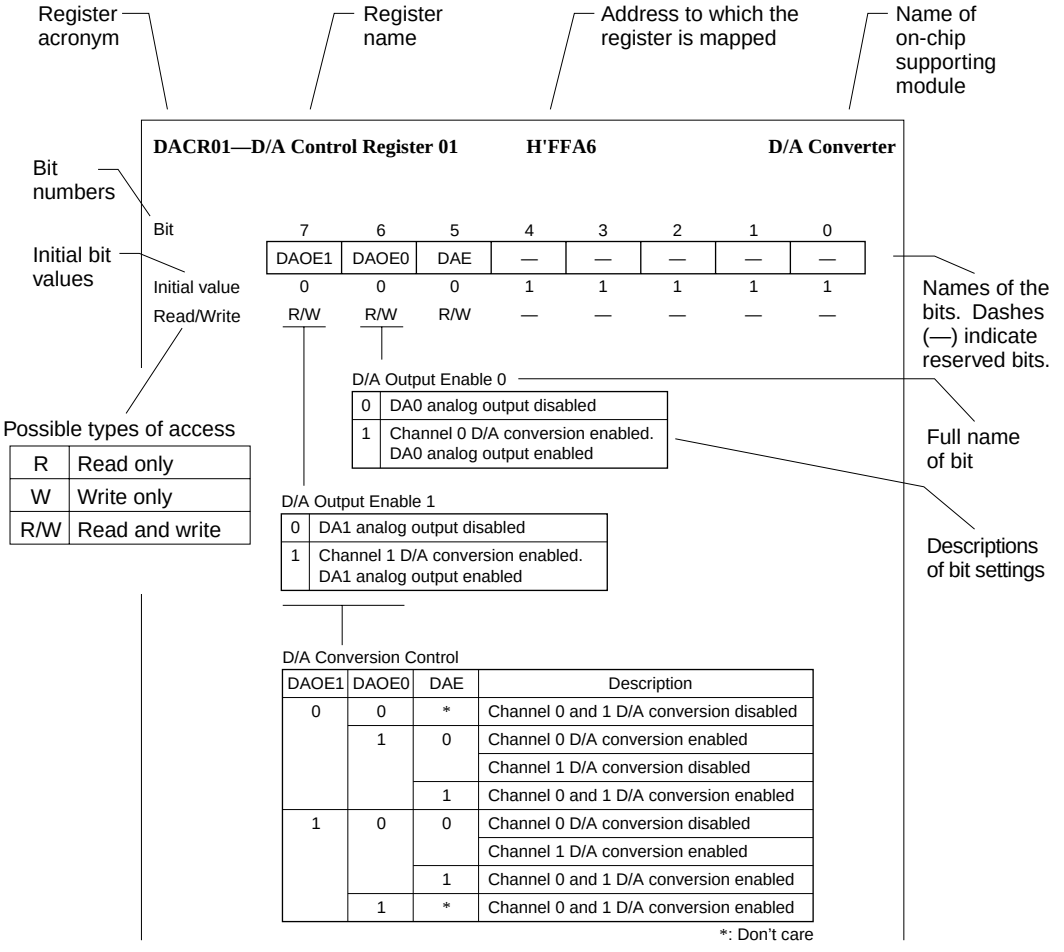
Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
Port 5	Port 5 data direction register	P5DDR	W	H'00	H'FE24
	Port 5 data register	P5DR	R/W	H'00	H'FF64
	Port 5 register	PORT5	R	Undefined	H'FF54
Port 6	Port 6 data direction register	P6DDR	W	H'00	H'FE25
	Port 6 data register	P6DR	R/W	H'00	H'FF65
	Port 6 register	PORT6	R	Undefined	H'FF55
	Port function control register 2	PFCR2	R/W	H'0E	H'FE34
Port 7	Port 7 data direction register	P7DDR	W	H'00	H'FE26
	Port 7 data register	P7DR	R/W	H'00	H'FF66
	Port 7 register	PORT7	R	Undefined	H'FF56
	Port function control register 2	PFCR2	R/W	H'00	H'FE34
Port 8	Port 8 data direction register	P8DDR	W	H'00	H'FE27
	Port 8 data register	P8DR	R/W	H'00	H'FF67
	Port 8 register	PORT8	R	Undefined	H'FF57
Port A	Port A data direction register	PADDR	W	H'00	H'FE29
	Port A data register	PADR	R/W	H'00	H'FF69
	Port A register	PORTA	R	Undefined	H'FF59
	Port A MOS pull-up control register	PAPCR	R/W	H'00	H'FE36
	Port A open drain control register	PAODR	R/W	H'00	H'FE3D
	Port function control register 1	PFCR1	R/W	H'FF	H'FE33
Port B	Port B data direction register	PBDDR	W	H'00	H'FE2A
	Port B data register	PBDR	R/W	H'00	H'FF6A
	Port B register	PORTB	R	Undefined	H'FF5A
	Port B MOS pull-up control register	PBPCR	R/W	H'00	H'FE37
Port C	Port C data direction register	PCDDR	W	H'00	H'FE2B
	Port C data register	PCDR	R/W	H'00	H'FF6B
	Port C register	PORTC	R	Undefined	H'FF5B
	Port C MOS pull-up control register	PCPCR	R/W	H'00	H'FE38
Port D	Port D data direction register	PDDDR	W	H'00	H'FE2C
	Port D data register	PDDR	R/W	H'00	H'FF6C
	Port D register	PORTD	R	Undefined	H'FF5C
	Port D MOS pull-up control register	PDPCR	R/W	H'00	H'FE39

Module	Register	Abbreviation	R/W	Initial Value	Address*[1]
Port E	Port E data direction register	PEDDR	W	H'00	H'FE2D
	Port E data register	PEDR	R/W	H'00	H'FF6D
	Port E register	PORTE	R	Undefined	H'FF5D
	Port E MOS pull-up control register	PEPCR	R/W	H'00	H'FE3A
Port F	Port F data direction register	PFDDR	W	H'80/H'00*[17]	H'FE2E
	Port F data register	PFDR	R/W	H'00	H'FF6E
	Port F register	PORTF	R	Undefined	H'FF5E
	Port function control register 2	PFCR2	R/W	H'0E	H'FE34
Port G	Port G data direction register	PGDDR	W	H'01/H'00*[17]	H'FE2F
	Port G data register	PGDR	R/W	H'00	H'FF6F
	Port G register	PORTG	R	Undefined	H'FF5F
	Port function control register 0	PFCR0	R/W	H'FF	H'FE32
Port H	Port H data direction register	PHDDR	W	H'00	H'FF74
	Port H data register	PHDR	R/W	H'00	H'FF72
	Port H register	PORTH	R	Undefined	H'FF70
	Port function control register 0	PFCR0	R/W	H'FF	H'FE32
	Port function control register 2	PFCR2	R/W	H'0E	H'FE34

Notes:
1. Lower 16 bits of the address.
2. Only 0 can be written for flag clearing.
3. Registers in the DTC cannot be read or written to directly.
4. Located as register information in on-chip RAM addresses H'BC00 to H'BFFF. Cannot be located in external memory space. Do not clear the RAME bit in SYSCR to 0 when using the DTC.
5. The value written in bit 15 of EDMDR0 to EDMDR3 may not be effective immediately.
   Bits 14 and 6 of EDMDR0 to EDMDR3 can only be written with 0 after being read as 1, to clear the flags.
6. Determined by the MCU operating mode.
7. Bits used for pulse output cannot be written to.
8. If the pulse output group 2 and pulse output group 3 output triggers are the same according to the PCR setting, the NDRH address will be H'FF4C, and if different, the address of NDRH for group 2 will be H'FF4E, and that for group 3 will be H'FF4C. Similarly, if the pulse output group 0 and pulse output group 1 output triggers are the same according to the PCR setting, the NDRL address will be H'FF4D, and if different, the address of NDRL for group 0 will be H'FF4F, and that for group 1 will be H'FF4D.
9. Only 0 can be written to bits 7 to 5, to clear the flags.
10. For information on writing, see section 11.2.4, Notes on Register Access, in the H8S/2678 Series Hardware Manual.
11. Only 0 can be written to bit 7, to clear the flag.

12. Flash memory registers are allocated to the same addresses as other registers. Register selection is performed by means of the FLSHE bit in the system control register (SYSCR).
13. In modes in which the on-chip flash memory is disabled, a read will return H'00, and writes are invalid. Writes are also disabled when the FWE bit in FLMCR1 is cleared to 0.
14. When a high level is input to the FWE pin, the initial value is H'80.
15. When a low level is input to the FWE pin, or if a high level is input but the SWE bit in FLMCR1 is not set, these registers are initialized to H'00.
16. FLMCR1, FLMCR2, EBR1, and EBR2 are 8-bit registers. Only byte access can be used on these registers, with the access requiring two states.
17. The initial value depends on the mode.
18. Valid in the F-ZTAT version only.

8.3 Register Descriptions



Bit	7	6	5	4	3	2	1	0
	SM1	SM0	DM1	DM0	MD1	MD0	DTS	Sz
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	—	—	—	—	—	—	—	—

DTC Data Transfer Size

0	Byte-size transfer
1	Word-size transfer

DTC Transfer Mode Select

0	Destination is repeat area or block area
1	Source is repeat area or block area

DTC Mode (MD1, MD0)

0	0	Normal mode
	1	Repeat mode
1	0	Block transfer mode
	1	—

Destination Address Mode

0	—	DAR is fixed
1	0	DAR is incremented after a transfer (+1 when Sz = 0, +2 when Sz = 1)
	1	DAR is decremented after a transfer (–1 when Sz = 0, –2 when Sz = 1)

Source Address Mode

0	—	SAR is fixed
1	0	SAR is incremented after a transfer (+1 when Sz = 0, +2 when Sz = 1)
	1	SAR is decremented after a transfer (–1 when Sz = 0, –2 when Sz = 1)

Bit	7	6	5	4	3	2	1	0
	CHNE	DISEL	CHNS	—	—	—	—	—
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	—	—	—	—	—	—	—	—

Reserved bits
(write 0)

DTC Chain Transfer Select

CHNE	CHNS	Description
0	—	No chain transfer (activation-standby state entered at end of DTC data transfer)
1	0	Chain transfer every time
1	1	Chain transfer only when transfer counter = 0

DTC Interrupt Select

0	After a data transfer ends, the CPU interrupt is disabled unless the transfer counter is 0
1	After a data transfer ends, the CPU interrupt is enabled

DTC Chain Transfer Enable

0	DTC data transfer finished (waiting for activation)
1	DTC chain transfer (new register information is read, and data transfer performed)

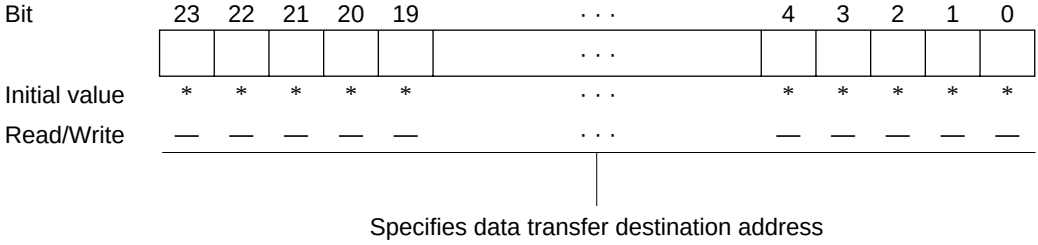
SAR—DTC Source Address Register **H'BC00 to H'BFFF** **DTC**

Bit	23	22	21	20	19	- - -	4	3	2	1	0
						- - -					
Initial value	*	*	*	*	*	- - -	*	*	*	*	*
Read/Write	—	—	—	—	—	- - -	—	—	—	—	—

Specifies data transfer source address

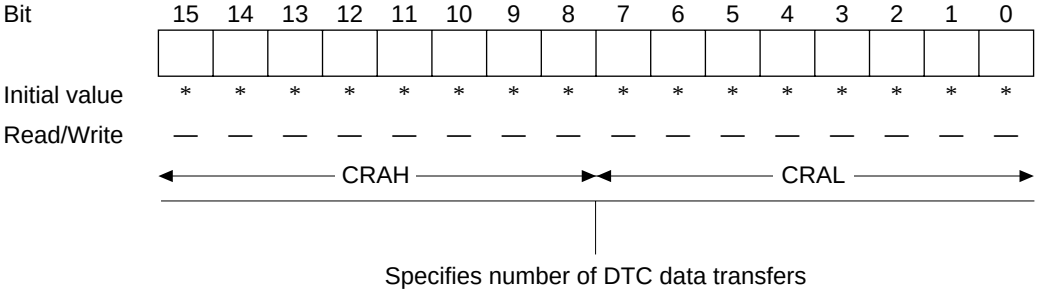
*: Undefined

DAR—DTC Destination Address Register **H'BC00 to H'BFFF** **DTC**



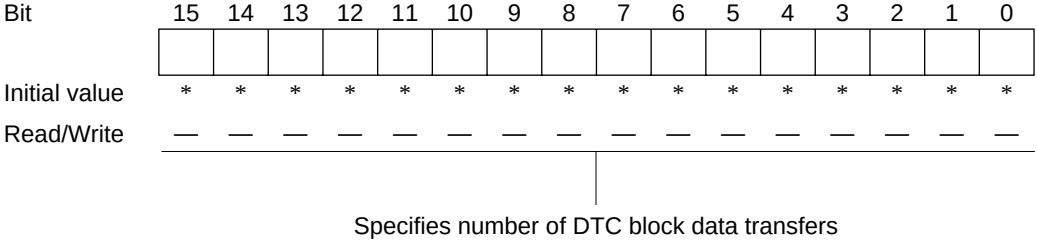
*: Undefined

CRA—DTC Transfer Count Register A **H'BC00 to H'BFFF** **DTC**



*: Undefined

CRB—DTC Transfer Count Register B **H'BC00 to H'BFFF** **DTC**



*: Undefined

EDSAR0—EXDMA Source Address Register 0 H'FDC0 EXDMAC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—								
Initial value	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	*
Read/Write	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Specifies transfer source address

*: Undefined

EDDAR0—EXDMA Destination Address Register 0 H'FDC4 EXDMAC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—								
Initial value	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	*
Read/Write	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Specifies transfer destination address

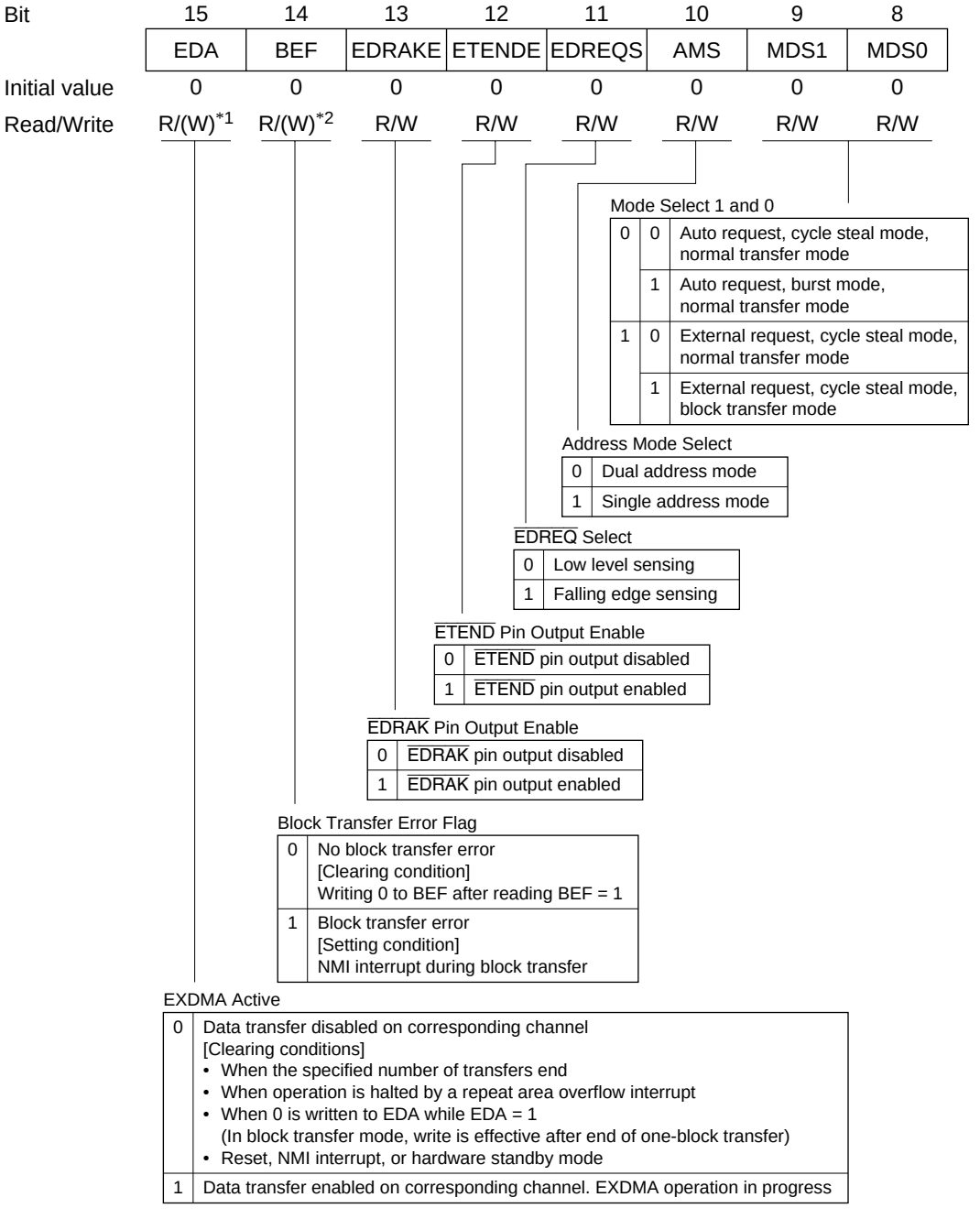
*: Undefined

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—								
Initial value	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	*
Read/Write	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Normal transfer mode: 24-bit transfer counter
Block transfer mode: Block size (bits 23 to 16)
16-bit transfer counter (bits 15 to 0)

*: Undefined



Notes: 1. The value written in bit EDA may not be effective immediately.
2. Bit BEF can only be written with 0 after being read as 1, to clear the flag.

Bit	7	6	5	4	3	2	1	0
	EDIE	IRF	TCEIE	SDIR	DTSIZE	BGUP	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)	R/(W)*	R/W	R/W	R/W	R/W	R/W	R/W

Bus Give-Up

0	Bus is not released in burst mode or block transfer mode
1	In burst mode or block transfer mode, the bus is transferred if requested by an internal bus master

Data Transmit Size

0	Byte-size (8-bit) specification
1	Word-size (16-bit) specification

Single Address Direction

0	Transfer direction: EDSAR → external device with DACK
1	Transfer direction: External device with DACK → EDDAR

Transfer Counter End Interrupt Enable

0	Transfer end interrupt requests by transfer counter are disabled
1	Transfer end interrupt requests by transfer counter are enabled

Interrupt Request Flag

0	No interrupt request source [Clearing conditions] • Writing 1 to the EDA bit in EDMDR • Writing 0 to IRF after reading IRF = 1
1	Interrupt request source occurrence [Setting conditions] • Transfer end interrupt request generated by transfer counter • Source address repeat area overflow interrupt request • Destination address repeat area overflow interrupt request

EXDMA Interrupt Enable

0	Interrupt request is not generated
1	Interrupt request is generated

Note: * Bit IRF can only be written with 0 after being read as 1, to clear the flag.

Bit	15	14	13	12	11	10	9	8
	SAT1	SAT0	SARIE	SARA4	SARA3	SARA2	SARA1	SARA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Source Address Repeat Area

0	0	0	0	0	Source address (EDSAR) is not designated as repeat area
0	0	0	0	1	Lower 1 bit of EDSAR (2-byte area) designated as repeat area
0	0	0	1	0	Lower 2 bits of EDSAR (4-byte area) designated as repeat area
0	0	0	1	1	Lower 3 bits of EDSAR (8-byte area) designated as repeat area
0	0	1	0	0	Lower 4 bits of EDSAR (16-byte area) designated as repeat area
:	:	:	:	:	: (Continues in the same way)
1	0	0	1	1	Lower 19 bits of EDSAR (512-kbyte area) designated as repeat area
1	0	1	0	0	Lower 20 bits of EDSAR (1-Mbyte area) designated as repeat area
1	0	1	0	1	Lower 21 bits of EDSAR (2-Mbyte area) designated as repeat area
1	0	1	1	0	Lower 22 bits of EDSAR (4-Mbyte area) designated as repeat area
1	0	1	1	1	Lower 23 bits of EDSAR (8-Mbyte area) designated as repeat area
1	1	*	*	*	Reserved (setting prohibited)

*: Don't care

Source Address Repeat Interrupt Enable

0	Source address repeat interrupt is not requested
1	When source address repeat area overflow occurs, the IRF bit in EDMDR is set to 1 and an interrupt is requested

Source Address Update Mode

0	*	Source address (EDSAR) is fixed
1	0	Source address is incremented (+1 in byte transfer, +2 in word transfer)
	1	Source address is decremented (–1 in byte transfer, –2 in word transfer)

*: Don't care

Bit	7	6	5	4	3	2	1	0
	DAT1	DAT0	DARIE	DARA4	DARA3	DARA2	DARA1	DARA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Destination Address Repeat Area

0	0	0	0	0	Destination address (EDDAR) is not designated as repeat area
0	0	0	0	1	Lower 1 bit of EDDAR (2-byte area) designated as repeat area
0	0	0	1	0	Lower 2 bits of EDDAR (4-byte area) designated as repeat area
0	0	0	1	1	Lower 3 bits of EDDAR (8-byte area) designated as repeat area
0	0	1	0	0	Lower 4 bits of EDDAR (16-byte area) designated as repeat area
:	:	:	:	:	: (Continues in the same way)
1	0	0	1	1	Lower 19 bits of EDDAR (512-kbyte area) designated as repeat area
1	0	1	0	0	Lower 20 bits of EDDAR (1-Mbyte area) designated as repeat area
1	0	1	0	1	Lower 21 bits of EDDAR (2-Mbyte area) designated as repeat area
1	0	1	1	0	Lower 22 bits of EDDAR (4-Mbyte area) designated as repeat area
1	0	1	1	1	Lower 23 bits of EDDAR (8-Mbyte area) designated as repeat area
1	1	*	*	*	Reserved (setting prohibited)

*: Don't care

Destination Address Repeat Interrupt Enable

0	Destination address repeat interrupt is not requested
1	When destination address repeat area overflow occurs, the IRF bit in EDMDR is set to 1 and an interrupt is requested

Destination Address Update Mode

0	*	Destination address (EDDAR) is fixed
1	0	Destination address is incremented (+1 in byte transfer, +2 in word transfer)
	1	Destination address is decremented (–1 in byte transfer, –2 in word transfer)

*: Don't care

EDSAR1—EXDMA Source Address Register 1 H'FDD0 EXDMAC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—								
Initial value	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	*
Read/Write	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Specifies transfer source address

*: Undefined

EDDAR1—EXDMA Destination Address Register 1 H'FDD4 EXDMAC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—								
Initial value	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	*
Read/Write	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Specifies transfer destination address

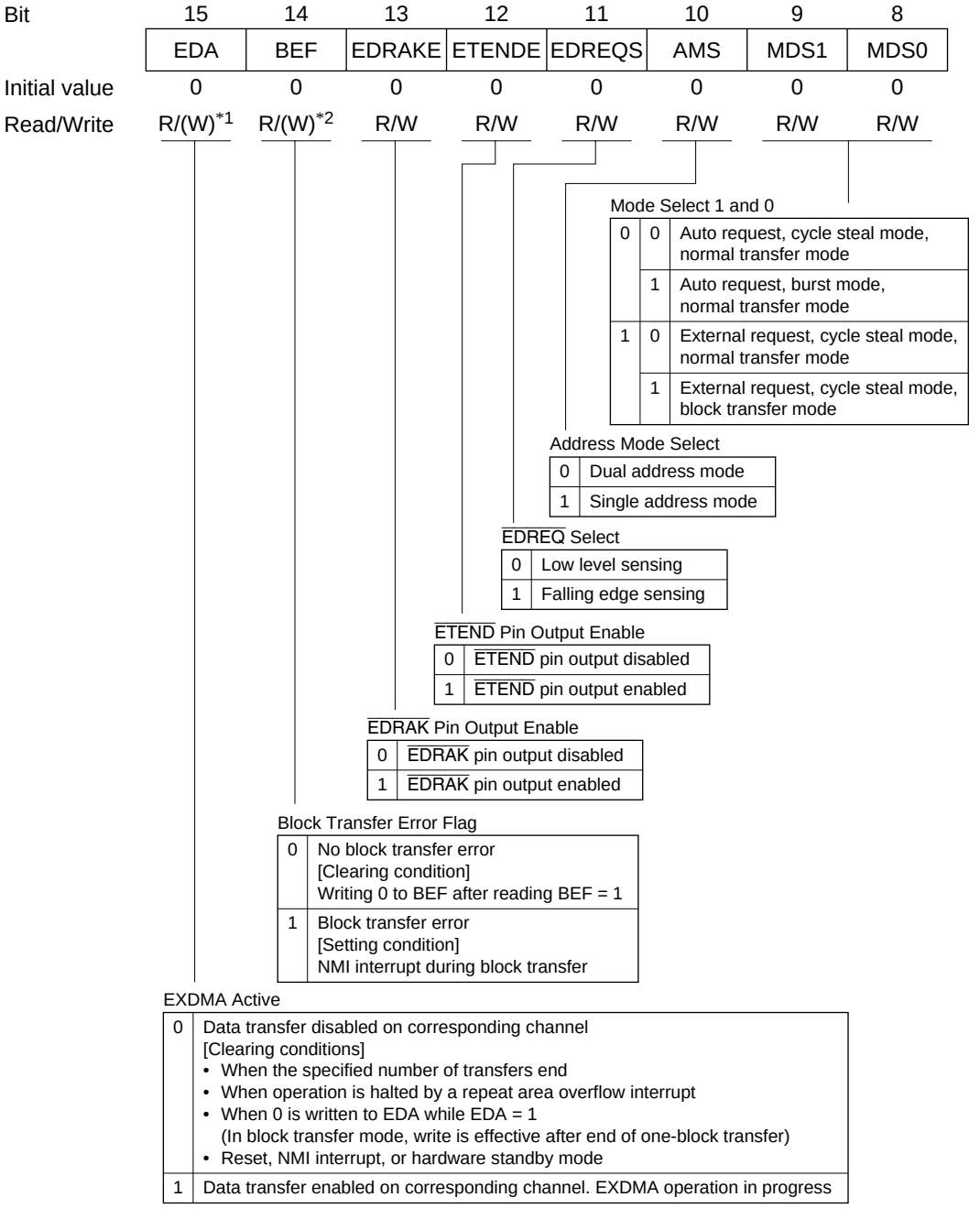
*: Undefined

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—								
Initial value	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	*
Read/Write	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Normal transfer mode: 24-bit transfer counter
Block transfer mode: Block size (bits 23 to 16)
16-bit transfer counter (bits 15 to 0)

*: Undefined



Notes: 1. The value written in bit EDA may not be effective immediately.
2. Bit BEF can only be written with 0 after being read as 1, to clear the flag.

Bit	7	6	5	4	3	2	1	0
	EDIE	IRF	TCEIE	SDIR	DTSIZE	BGUP	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)	R/(W)*	R/W	R/W	R/W	R/W	R/W	R/W

Bus Give-Up

0	Bus is not released in burst mode or block transfer mode
1	In burst mode or block transfer mode, the bus is transferred if requested by an internal bus master

Data Transmit Size

0	Byte-size (8-bit) specification
1	Word-size (16-bit) specification

Single Address Direction

0	Transfer direction: EDSAR → external device with DACK
1	Transfer direction: External device with DACK → EDDAR

Transfer Counter End Interrupt Enable

0	Transfer end interrupt requests by transfer counter are disabled
1	Transfer end interrupt requests by transfer counter are enabled

Interrupt Request Flag

0	No interrupt request source [Clearing conditions] • Writing 1 to the EDA bit in EDMDR • Writing 0 to IRF after reading IRF = 1
1	Interrupt request source occurrence [Setting conditions] • Transfer end interrupt request generated by transfer counter • Source address repeat area overflow interrupt request • Destination address repeat area overflow interrupt request

EXDMA Interrupt Enable

0	Interrupt request is not generated
1	Interrupt request is generated

Note: * Bit IRF can only be written with 0 after being read as 1, to clear the flag.

Bit	15	14	13	12	11	10	9	8
	SAT1	SAT0	SARIE	SARA4	SARA3	SARA2	SARA1	SARA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Source Address Repeat Area

0	0	0	0	0	Source address (EDSAR) is not designated as repeat area
0	0	0	0	1	Lower 1 bit of EDSAR (2-byte area) designated as repeat area
0	0	0	1	0	Lower 2 bits of EDSAR (4-byte area) designated as repeat area
0	0	0	1	1	Lower 3 bits of EDSAR (8-byte area) designated as repeat area
0	0	1	0	0	Lower 4 bits of EDSAR (16-byte area) designated as repeat area
:	:	:	:	:	: (Continues in the same way)
1	0	0	1	1	Lower 19 bits of EDSAR (512-kbyte area) designated as repeat area
1	0	1	0	0	Lower 20 bits of EDSAR (1-Mbyte area) designated as repeat area
1	0	1	0	1	Lower 21 bits of EDSAR (2-Mbyte area) designated as repeat area
1	0	1	1	0	Lower 22 bits of EDSAR (4-Mbyte area) designated as repeat area
1	0	1	1	1	Lower 23 bits of EDSAR (8-Mbyte area) designated as repeat area
1	1	*	*	*	Reserved (setting prohibited)

*: Don't care

Source Address Repeat Interrupt Enable

0	Source address repeat interrupt is not requested
1	When source address repeat area overflow occurs, the IRF bit in EDMDR is set to 1 and an interrupt is requested

Source Address Update Mode

0	*	Source address (EDSAR) is fixed
1	0	Source address is incremented (+1 in byte transfer, +2 in word transfer)
	1	Source address is decremented (–1 in byte transfer, –2 in word transfer)

*: Don't care

Bit	7	6	5	4	3	2	1	0
	DAT1	DAT0	DARIE	DARA4	DARA3	DARA2	DARA1	DARA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Destination Address Repeat Area

0	0	0	0	0	Destination address (EDDAR) is not designated as repeat area
0	0	0	0	1	Lower 1 bit of EDDAR (2-byte area) designated as repeat area
0	0	0	1	0	Lower 2 bits of EDDAR (4-byte area) designated as repeat area
0	0	0	1	1	Lower 3 bits of EDDAR (8-byte area) designated as repeat area
0	0	1	0	0	Lower 4 bits of EDDAR (16-byte area) designated as repeat area
:	:	:	:	:	: (Continues in the same way)
1	0	0	1	1	Lower 19 bits of EDDAR (512-kbyte area) designated as repeat area
1	0	1	0	0	Lower 20 bits of EDDAR (1-Mbyte area) designated as repeat area
1	0	1	0	1	Lower 21 bits of EDDAR (2-Mbyte area) designated as repeat area
1	0	1	1	0	Lower 22 bits of EDDAR (4-Mbyte area) designated as repeat area
1	0	1	1	1	Lower 23 bits of EDDAR (8-Mbyte area) designated as repeat area
1	1	*	*	*	Reserved (setting prohibited)

*: Don't care

Destination Address Repeat Interrupt Enable

0	Destination address repeat interrupt is not requested
1	When destination address repeat area overflow occurs, the IRF bit in EDMDR is set to 1 and an interrupt is requested

Destination Address Update Mode

0	*	Destination address (EDDAR) is fixed
1	0	Destination address is incremented (+1 in byte transfer, +2 in word transfer)
	1	Destination address is decremented (–1 in byte transfer, –2 in word transfer)

*: Don't care

EDSAR2—EXDMA Source Address Register 2 **H'FDE0** **EXDMAC**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—								
Initial value	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	*
Read/Write	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Specifies transfer source address

*: Undefined

EDDAR2—EXDMA Destination Address Register 2 **H'FDE4** **EXDMAC**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—								
Initial value	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	*
Read/Write	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Specifies transfer destination address

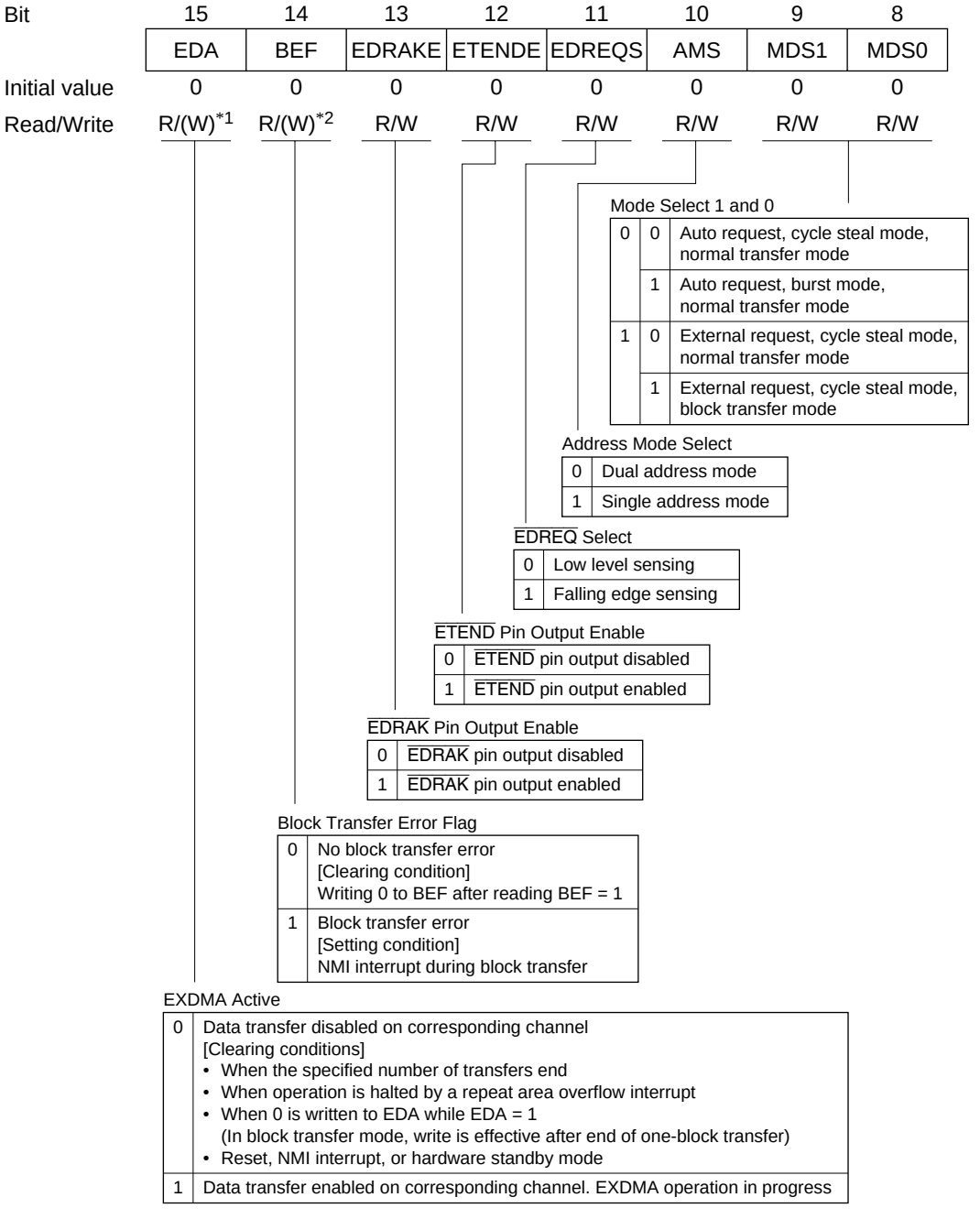
*: Undefined

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—								
Initial value	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	*
Read/Write	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Normal transfer mode: 24-bit transfer counter
Block transfer mode: Block size (bits 23 to 16)
16-bit transfer counter (bits 15 to 0)

*: Undefined



Notes: 1. The value written in bit EDA may not be effective immediately.
2. Bit BEF can only be written with 0 after being read as 1, to clear the flag.

Bit	7	6	5	4	3	2	1	0
	EDIE	IRF	TCEIE	SDIR	DTSIZE	BGUP	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)	R/(W)*	R/W	R/W	R/W	R/W	R/W	R/W

Bus Give-Up

0	Bus is not released in burst mode or block transfer mode
1	In burst mode or block transfer mode, the bus is transferred if requested by an internal bus master

Data Transmit Size

0	Byte-size (8-bit) specification
1	Word-size (16-bit) specification

Single Address Direction

0	Transfer direction: EDSAR → external device with DACK
1	Transfer direction: External device with DACK → EDDAR

Transfer Counter End Interrupt Enable

0	Transfer end interrupt requests by transfer counter are disabled
1	Transfer end interrupt requests by transfer counter are enabled

Interrupt Request Flag

0	No interrupt request source [Clearing conditions] • Writing 1 to the EDA bit in EDMDR • Writing 0 to IRF after reading IRF = 1
1	Interrupt request source occurrence [Setting conditions] • Transfer end interrupt request generated by transfer counter • Source address repeat area overflow interrupt request • Destination address repeat area overflow interrupt request

EXDMA Interrupt Enable

0	Interrupt request is not generated
1	Interrupt request is generated

Note: * Bit IRF can only be written with 0 after being read as 1, to clear the flag.

Bit	15	14	13	12	11	10	9	8
	SAT1	SAT0	SARIE	SARA4	SARA3	SARA2	SARA1	SARA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Source Address Repeat Area

0	0	0	0	0	Source address (EDSAR) is not designated as repeat area
0	0	0	0	1	Lower 1 bit of EDSAR (2-byte area) designated as repeat area
0	0	0	1	0	Lower 2 bits of EDSAR (4-byte area) designated as repeat area
0	0	0	1	1	Lower 3 bits of EDSAR (8-byte area) designated as repeat area
0	0	1	0	0	Lower 4 bits of EDSAR (16-byte area) designated as repeat area
:	:	:	:	:	: (Continues in the same way)
1	0	0	1	1	Lower 19 bits of EDSAR (512-kbyte area) designated as repeat area
1	0	1	0	0	Lower 20 bits of EDSAR (1-Mbyte area) designated as repeat area
1	0	1	0	1	Lower 21 bits of EDSAR (2-Mbyte area) designated as repeat area
1	0	1	1	0	Lower 22 bits of EDSAR (4-Mbyte area) designated as repeat area
1	0	1	1	1	Lower 23 bits of EDSAR (8-Mbyte area) designated as repeat area
1	1	*	*	*	Reserved (setting prohibited)

*: Don't care

Source Address Repeat Interrupt Enable

0	Source address repeat interrupt is not requested
1	When source address repeat area overflow occurs, the IRF bit in EDMDR is set to 1 and an interrupt is requested

Source Address Update Mode

0	*	Source address (EDSAR) is fixed
1	0	Source address is incremented (+1 in byte transfer, +2 in word transfer)
	1	Source address is decremented (–1 in byte transfer, –2 in word transfer)

*: Don't care

Bit	7	6	5	4	3	2	1	0
	DAT1	DAT0	DARIE	DARA4	DARA3	DARA2	DARA1	DARA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Destination Address Repeat Area

0	0	0	0	0	Destination address (EDDAR) is not designated as repeat area
0	0	0	0	1	Lower 1 bit of EDDAR (2-byte area) designated as repeat area
0	0	0	1	0	Lower 2 bits of EDDAR (4-byte area) designated as repeat area
0	0	0	1	1	Lower 3 bits of EDDAR (8-byte area) designated as repeat area
0	0	1	0	0	Lower 4 bits of EDDAR (16-byte area) designated as repeat area
:	:	:	:	:	: (Continues in the same way)
1	0	0	1	1	Lower 19 bits of EDDAR (512-kbyte area) designated as repeat area
1	0	1	0	0	Lower 20 bits of EDDAR (1-Mbyte area) designated as repeat area
1	0	1	0	1	Lower 21 bits of EDDAR (2-Mbyte area) designated as repeat area
1	0	1	1	0	Lower 22 bits of EDDAR (4-Mbyte area) designated as repeat area
1	0	1	1	1	Lower 23 bits of EDDAR (8-Mbyte area) designated as repeat area
1	1	*	*	*	Reserved (setting prohibited)

*: Don't care

Destination Address Repeat Interrupt Enable

0	Destination address repeat interrupt is not requested
1	When destination address repeat area overflow occurs, the IRF bit in EDMDR is set to 1 and an interrupt is requested

Destination Address Update Mode

0	*	Destination address (EDDAR) is fixed
1	0	Destination address is incremented (+1 in byte transfer, +2 in word transfer)
	1	Destination address is decremented (–1 in byte transfer, –2 in word transfer)

*: Don't care

EDSAR3—EXDMA Source Address Register 3 H'FDF0 EXDMAC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—								
Initial value	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	*
Read/Write	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Specifies transfer source address

*: Undefined

EDDAR3—EXDMA Destination Address Register 3 H'FDF4 EXDMAC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—								
Initial value	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	*
Read/Write	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Specifies transfer destination address

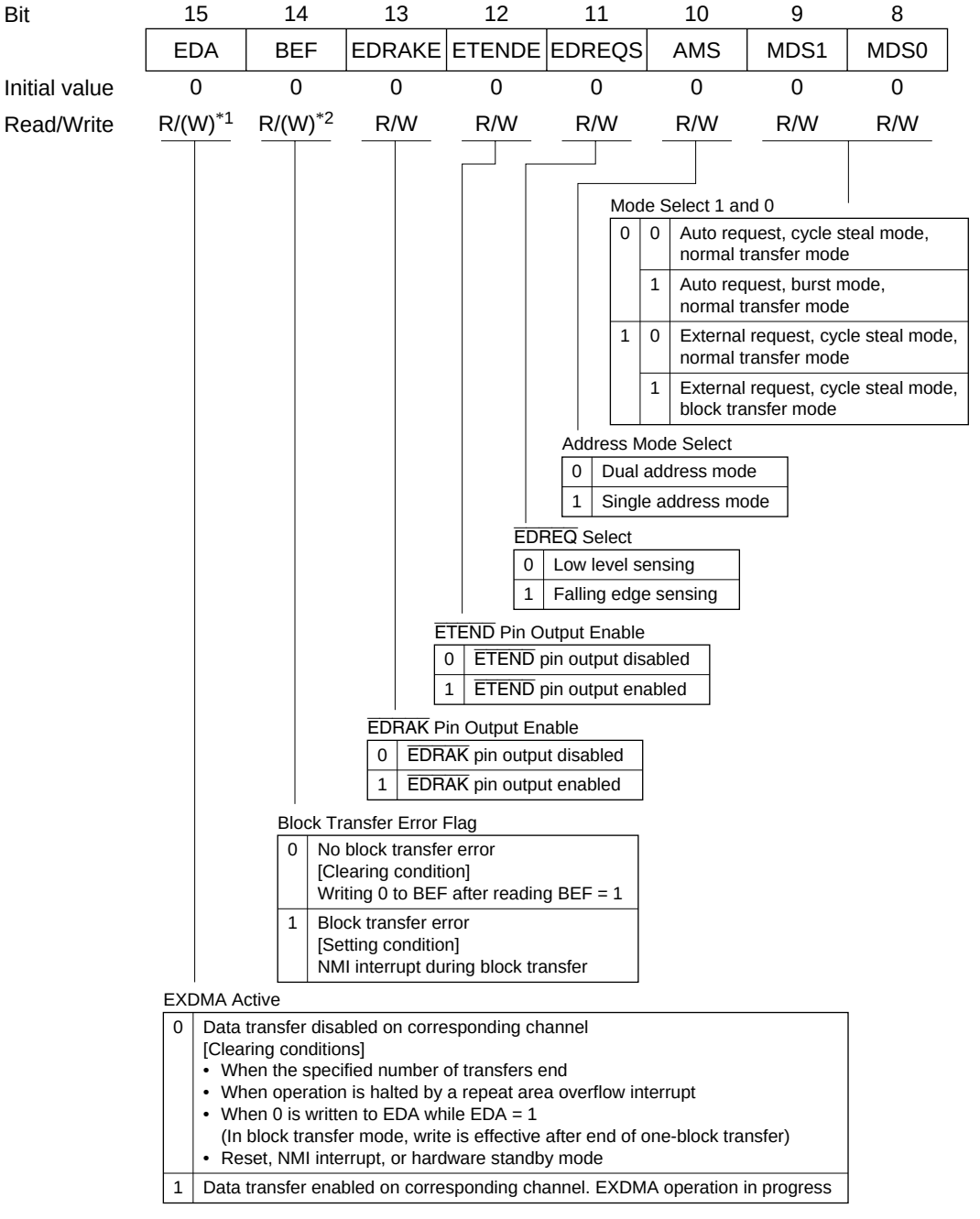
*: Undefined

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—								
Initial value	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	*
Read/Write	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Normal transfer mode: 24-bit transfer counter
Block transfer mode: Block size (bits 23 to 16)
16-bit transfer counter (bits 15 to 0)

*: Undefined



Notes: 1. The value written in bit EDA may not be effective immediately.
2. Bit BEF can only be written with 0 after being read as 1, to clear the flag.

Bit	7	6	5	4	3	2	1	0
	EDIE	IRF	TCEIE	SDIR	DTSIZE	BGUP	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)	R/(W)*	R/W	R/W	R/W	R/W	R/W	R/W

Bus Give-Up

0	Bus is not released in burst mode or block transfer mode
1	In burst mode or block transfer mode, the bus is transferred if requested by an internal bus master

Data Transmit Size

0	Byte-size (8-bit) specification
1	Word-size (16-bit) specification

Single Address Direction

0	Transfer direction: EDSAR → external device with DACK
1	Transfer direction: External device with DACK → EDDAR

Transfer Counter End Interrupt Enable

0	Transfer end interrupt requests by transfer counter are disabled
1	Transfer end interrupt requests by transfer counter are enabled

Interrupt Request Flag

0	No interrupt request source [Clearing conditions] • Writing 1 to the EDA bit in EDMDR • Writing 0 to IRF after reading IRF = 1
1	Interrupt request source occurrence [Setting conditions] • Transfer end interrupt request generated by transfer counter • Source address repeat area overflow interrupt request • Destination address repeat area overflow interrupt request

EXDMA Interrupt Enable

0	Interrupt request is not generated
1	Interrupt request is generated

Note: * Bit IRF can only be written with 0 after being read as 1, to clear the flag.

Bit	15	14	13	12	11	10	9	8
	SAT1	SAT0	SARIE	SARA4	SARA3	SARA2	SARA1	SARA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Source Address Repeat Area

0	0	0	0	0	Source address (EDSAR) is not designated as repeat area
0	0	0	0	1	Lower 1 bit of EDSAR (2-byte area) designated as repeat area
0	0	0	1	0	Lower 2 bits of EDSAR (4-byte area) designated as repeat area
0	0	0	1	1	Lower 3 bits of EDSAR (8-byte area) designated as repeat area
0	0	1	0	0	Lower 4 bits of EDSAR (16-byte area) designated as repeat area
:	:	:	:	:	: (Continues in the same way)
1	0	0	1	1	Lower 19 bits of EDSAR (512-kbyte area) designated as repeat area
1	0	1	0	0	Lower 20 bits of EDSAR (1-Mbyte area) designated as repeat area
1	0	1	0	1	Lower 21 bits of EDSAR (2-Mbyte area) designated as repeat area
1	0	1	1	0	Lower 22 bits of EDSAR (4-Mbyte area) designated as repeat area
1	0	1	1	1	Lower 23 bits of EDSAR (8-Mbyte area) designated as repeat area
1	1	*	*	*	Reserved (setting prohibited)

*: Don't care

Source Address Repeat Interrupt Enable

0	Source address repeat interrupt is not requested
1	When source address repeat area overflow occurs, the IRF bit in EDMDR is set to 1 and an interrupt is requested

Source Address Update Mode

0	*	Source address (EDSAR) is fixed
1	0	Source address is incremented (+1 in byte transfer, +2 in word transfer)
	1	Source address is decremented (–1 in byte transfer, –2 in word transfer)

*: Don't care

Bit	7	6	5	4	3	2	1	0
	DAT1	DAT0	DARIE	DARA4	DARA3	DARA2	DARA1	DARA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Destination Address Repeat Area

0	0	0	0	0	Destination address (EDDAR) is not designated as repeat area
0	0	0	0	1	Lower 1 bit of EDDAR (2-byte area) designated as repeat area
0	0	0	1	0	Lower 2 bits of EDDAR (4-byte area) designated as repeat area
0	0	0	1	1	Lower 3 bits of EDDAR (8-byte area) designated as repeat area
0	0	1	0	0	Lower 4 bits of EDDAR (16-byte area) designated as repeat area
:	:	:	:	:	: (Continues in the same way)
1	0	0	1	1	Lower 19 bits of EDDAR (512-kbyte area) designated as repeat area
1	0	1	0	0	Lower 20 bits of EDDAR (1-Mbyte area) designated as repeat area
1	0	1	0	1	Lower 21 bits of EDDAR (2-Mbyte area) designated as repeat area
1	0	1	1	0	Lower 22 bits of EDDAR (4-Mbyte area) designated as repeat area
1	0	1	1	1	Lower 23 bits of EDDAR (8-Mbyte area) designated as repeat area
1	1	*	*	*	Reserved (setting prohibited)

*: Don't care

Destination Address Repeat Interrupt Enable

0	Destination address repeat interrupt is not requested
1	When destination address repeat area overflow occurs, the IRF bit in EDMDR is set to 1 and an interrupt is requested

Destination Address Update Mode

0	*	Destination address (EDDAR) is fixed
1	0	Destination address is incremented (+1 in byte transfer, +2 in word transfer)
	1	Destination address is decremented (–1 in byte transfer, –2 in word transfer)

*: Don't care

IPRA—Interrupt Priority Register A	**H'FE00**	**Interrupt Controller**
IPRB—Interrupt Priority Register B	**H'FE02**	**Interrupt Controller**
IPRC—Interrupt Priority Register C	**H'FE04**	**Interrupt Controller**
IPRD—Interrupt Priority Register D	**H'FE06**	**Interrupt Controller**
IPRE—Interrupt Priority Register E	**H'FE08**	**Interrupt Controller**
IPRF—Interrupt Priority Register F	**H'FE0A**	**Interrupt Controller**
IPRG—Interrupt Priority Register G	**H'FE0C**	**Interrupt Controller**
IPRH—Interrupt Priority Register H	**H'FE0E**	**Interrupt Controller**
IPRI—Interrupt Priority Register I	**H'FE10**	**Interrupt Controller**
IPRJ—Interrupt Priority Register J	**H'FE12**	**Interrupt Controller**
IPRK—Interrupt Priority Register K	**H'FE14**	**Interrupt Controller**

Bit	15	14	13	12	11	10	9	8
	—	IPR14	IPR13	IPR12	—	IPR10	IPR9	IPR8
Initial value	0	1	1	1	0	1	1	1
Read/Write	—	R/W	R/W	R/W	—	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	—	IPR6	IPR5	IPR4	—	IPR2	IPR1	IPR0
Initial value	0	1	1	1	0	1	1	1
Read/Write	—	R/W	R/W	R/W	—	R/W	R/W	R/W

Interrupt priority settings

Interrupt Sources and IPR Settings

Register	Bits 14 to 12	Bits 10 to 8	Bits 6 to 4	Bits 2 to 0
IPRA	IRQ0	IRQ1	IRQ2	IRQ3
IPRB	IRQ4	IRQ5	IRQ6	IRQ7
IPRC	IRQ8	IRQ9	IRQ10	IRQ11
IPRD	IRQ12	IRQ13	IRQ14	IRQ15
IPRE	DTC	Interval timer	—*	Refresh timer
IPRF	—*	A/D converter	TPU channel 0	TPU channel 1
IPRG	TPU channel 2	TPU channel 3	TPU channel 4	TPU channel 5
IPRH	8-bit timer channel 0	8-bit timer channel 1	DMAC	EXDMAC channel 0
IPRI	EXDMAC channel 1	EXDMAC channel 2	EXDMAC channel 3	SCI channel 0
IPRJ	SCI channel 1	SCI channel 2	—*	—*
IPRK	—*	—*	—*	—*

Note: * Reserved bits. These bits are always read as H'7 and should also be written with H'7.

Bit	15	14	13	12	11	10	9	8
	ITS15	ITS14	ITS13	ITS12	ITS11	ITS10	ITS9	ITS8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	ITS7	ITS6	ITS5	ITS4	ITS3	ITS2	ITS1	ITS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IRQ Input Pin Select

ITSn	Description
0	IRQn requests are accepted at the $\overline{\text{IRQn}}$ pin
1	IRQn requests are accepted at the ($\overline{\text{IRQn}}$) pin

(n = 15 to 0)

Bit	15	14	13	12	11	10	9	8
	SSI15	SSI14	SSI13	SSI12	SSI11	SSI10	SSI9	SSI8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	SSI7	SSI6	SSI5	SSI4	SSI3	SSI2	SSI1	SSI0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Software Standby Release IRQ Setting

SSIn	Description
0	IRQn requests are not sampled in the software standby state
1	When an IRQn request occurs in the software standby state, the chip recovers from the software standby state after the elapse of the oscillation settling time

(n = 15 to 0)

ISCRH

Bit	15	14	13	12	11	10	9	8
	IRQ15SCB	IRQ15SCA	IRQ14SCB	IRQ14SCA	IRQ13SCB	IRQ13SCA	IRQ12SCB	IRQ12SCA
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	IRQ11SCB	IRQ11SCA	IRQ10SCB	IRQ10SCA	IRQ9SCB	IRQ9SCA	IRQ8SCB	IRQ8SCA
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ISCRL

Bit	15	14	13	12	11	10	9	8
	IRQ7SCB	IRQ7SCA	IRQ6SCB	IRQ6SCA	IRQ5SCB	IRQ5SCA	IRQ4SCB	IRQ4SCA
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	IRQ3SCB	IRQ3SCA	IRQ2SCB	IRQ2SCA	IRQ1SCB	IRQ1SCA	IRQ0SCB	IRQ0SCA
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IRQ15 Sense Control A and B to IRQ0 Sense Control A and B

IRQnSCB	IRQnSCA	Description
0	0	Interrupt request generated at $\overline{\text{IRQn}}$ input low level
	1	Interrupt request generated at falling edge of $\overline{\text{IRQn}}$ input
1	0	Interrupt request generated at rising edge of $\overline{\text{IRQn}}$ input
	1	Interrupt request generated at both falling and rising edges of $\overline{\text{IRQn}}$ input

(n = 15 to 0)

Bit	7	6	5	4	3	2	1	0
	IrE	IrCKS2	IrCKS1	IrCKS0	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	—	—	—	—

IrDA Clock Select 2 to 0

0	0	0	B × 3/16 (3/16 of bit rate)
		1	ø/2
	1	0	ø/4
		1	ø/8
1	0	0	ø/16
		1	ø/32
	1	0	ø/64
		1	ø/128

IrDA Enable

0	Pins TxD0/IrTxD and RxD0/IrRxD function as TxD0 and RxD0
1	Pins TxD0/IrTxD and RxD0/IrRxD function as IrTxD and IrRxD

P1DDR—Port 1 Data Direction Register **H'FE20** **Port 1**

Bit	7	6	5	4	3	2	1	0
	P17DDR	P16DDR	P15DDR	P14DDR	P13DDR	P12DDR	P11DDR	P10DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Specify input or output for individual port 1 pins

P2DDR—Port 2 Data Direction Register **H'FE21** **Port 2**

Bit	7	6	5	4	3	2	1	0
	P27DDR	P26DDR	P25DDR	P24DDR	P23DDR	P22DDR	P21DDR	P20DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Specify input or output for individual port 2 pins

P3DDR—Port 3 Data Direction Register **H'FE22** **Port 3**

Bit	7	6	5	4	3	2	1	0
	—	—	P35DDR	P34DDR	P33DDR	P32DDR	P31DDR	P30DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	W	W	W	W	W	W

Specify input or output for individual port 3 pins

P5DDR—Port 5 Data Direction Register **H'FE24** **Port 5**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	P53DDR	P52DDR	P51DDR	P50DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	W	W	W	W

Specify input or output for individual port 5 pins

P6DDR—Port 6 Data Direction Register **H'FE25** **Port 6**

Bit	7	6	5	4	3	2	1	0
	—	—	P65DDR	P64DDR	P63DDR	P62DDR	P61DDR	P60DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	W	W	W	W	W	W

Specify input or output for individual port 6 pins

P7DDR—Port 7 Data Direction Register **H'FE26** **Port 7**

Bit	7	6	5	4	3	2	1	0
	—	—	P75DDR	P74DDR	P73DDR	P72DDR	P71DDR	P70DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	W	W	W	W	W	W

Specify input or output for individual port 7 pins

P8DDR—Port 8 Data Direction Register **H'FE27** **Port 8**

Bit	7	6	5	4	3	2	1	0
	—	—	P85DDR	P84DDR	P83DDR	P82DDR	P81DDR	P80DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	W	W	W	W	W	W

Specify input or output for individual port 8 pins

PADDR—Port A Data Direction Register **H'FE29** **Port A**

Bit	7	6	5	4	3	2	1	0
	PA7DDR	PA6DDR	PA5DDR	PA4DDR	PA3DDR	PA2DDR	PA1DDR	PA0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Specify input or output for individual port A pins

PBDDR—Port B Data Direction Register **H'FE2A** **Port B**

Bit	7	6	5	4	3	2	1	0
	PB7DDR	PB6DDR	PB5DDR	PB4DDR	PB3DDR	PB2DDR	PB1DDR	PB0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Specify input or output for individual port B pins

PCDDR—Port C Data Direction Register **H'FE2B** **Port C**

Bit	7	6	5	4	3	2	1	0
	PC7DDR	PC6DDR	PC5DDR	PC4DDR	PC3DDR	PC2DDR	PC1DDR	PC0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Specify input or output for individual port C pins

PDDDR—Port D Data Direction Register **H'FE2C** **Port D**

Bit	7	6	5	4	3	2	1	0
	PD7DDR	PD6DDR	PD5DDR	PD4DDR	PD3DDR	PD2DDR	PD1DDR	PD0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Specify input or output for individual port D pins

PEDDR—Port E Data Direction Register **H'FE2D** **Port E**

Bit	7	6	5	4	3	2	1	0
	PE7DDR	PE6DDR	PE5DDR	PE4DDR	PE3DDR	PE2DDR	PE1DDR	PE0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Specify input or output for individual port E pins

PFDDR—Port F Data Direction Register **H'FE2E** **Port F**

Bit	7	6	5	4	3	2	1	0
	PF7DDR	PF6DDR	PF5DDR	PF4DDR	PF3DDR	PF2DDR	PF1DDR	PF0DDR
Modes 1, 2, 4, 5, 6								
Initial value	1	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Mode 7								
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Specify input or output for individual port F pins

PGDDR—Port G Data Direction Register **H'FE2F** **Port G**

Bit	7	6	5	4	3	2	1	0
	—	PG6DDR	PG5DDR	PG4DDR	PG3DDR	PG2DDR	PG1DDR	PG0DDR
Modes 1, 2, 5, 6								
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Modes 4, 7								
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Specify input or output for individual port G pins

Bit	7	6	5	4	3	2	1	0
	CS7E	CS6E	CS5E	CS4E	CS3E	CS2E	CS1E	CS0E
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

CS7 to CS0 Enable

0	Pin is designated as I/O port and does not function as $\overline{CSn}$ output pin
1	Pin is designated as $\overline{CSn}$ output pin

(n = 7 to 0)

Bit	7	6	5	4	3	2	1	0
	A23E	A22E	A21E	A20E	A19E	A18E	A17E	A16E
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address 23 to 16 Enable

0	DR output when PAnDDR = 1
1	Am output when PAnDDR = 1

(n = 7 to 0, m = 23 to 16)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	ASOE	LWROE	OES	DMACS
Initial value	0	0	0	0	1	1	1	1
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

DMAC Control Pin Select

0	P65 to P60 are designated as DMAC control pins
1	P75 to P70 are designated as DMAC control pins

OE Output Select

0	P35 is designated as $\overline{OE}$ output pin
1	PH3 is designated as $\overline{OE}$ output pin

LWR Output Enable

0	PF6 is designated as I/O port and does not function as $\overline{LWR}$ output pin
1	PF6 is designated as $\overline{LWR}$ output pin

AS Output Enable

0	PF6 is designated as I/O port and does not function as $\overline{AS}$ output pin
1	PF6 is designated as $\overline{AS}$ output pin

PAPCR—Port A MOS Pull-Up Control Register H'FE36 Port A

Bit	7	6	5	4	3	2	1	0
	PA7PCR	PA6PCR	PA5PCR	PA4PCR	PA3PCR	PA2PCR	PA1PCR	PA0PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit-by-bit control of MOS input pull-up function incorporated into port A

PBPCR—Port B MOS Pull-Up Control Register H'FE37 Port B

Bit	7	6	5	4	3	2	1	0
	PB7PCR	PB6PCR	PB5PCR	PB4PCR	PB3PCR	PB2PCR	PB1PCR	PB0PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit-by-bit control of MOS input pull-up function incorporated into port B

PCPCR—Port C MOS Pull-Up Control Register H'FE38 Port C

Bit	7	6	5	4	3	2	1	0
	PC7PCR	PC6PCR	PC5PCR	PC4PCR	PC3PCR	PC2PCR	PC1PCR	PC0PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit-by-bit control of MOS input pull-up function incorporated into port C

PDPCR—Port D MOS Pull-Up Control Register H'FE39 Port D

Bit	7	6	5	4	3	2	1	0
	PD7PCR	PD6PCR	PD5PCR	PD4PCR	PD3PCR	PD2PCR	PD1PCR	PD0PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit-by-bit control of MOS input pull-up function incorporated into port D

PEPCR—Port E MOS Pull-Up Control Register **H'FE3A** **Port E**

Bit	7	6	5	4	3	2	1	0
	PE7PCR	PE6PCR	PE5PCR	PE4PCR	PE3PCR	PE2PCR	PE1PCR	PE0PCR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit-by-bit control of MOS input pull-up function incorporated into port E

P3ODR—Port 3 Open Drain Control Register **H'FE3C** **Port 3**

Bit	7	6	5	4	3	2	1	0
	—	—	P35ODR	P34ODR	P33ODR	P32ODR	P31ODR	P30ODR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Control PMOS on/off status for each port 3 pin (P35 to P30)

PAODR—Port A Open Drain Control Register **H'FE3D** **Port A**

Bit	7	6	5	4	3	2	1	0
	PA7ODR	PA6ODR	PA5ODR	PA4ODR	PA3ODR	PA2ODR	PA1ODR	PA0ODR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Control PMOS on/off status for each port A pin (PA7 to PA0)

Bit	7	6	5	4	3	2	1	0
	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Timer Prescaler

0	0	0	Internal clock: count on ø/1
		1	Internal clock: count on ø/4
	1	0	Internal clock: count on ø/16
		1	Internal clock: count on ø/64
1	0	0	External clock: count on TCLKA pin input
		1	Internal clock: count on ø/1024
	1	0	Internal clock: count on ø/256
		1	Internal clock: count on ø/4096

Clock Edge

0	0	Count at rising edge
	1	Count at falling edge
1	—	Count at both edges

Counter Clear

0	0	0	TCNT clearing disabled
		1	TCNT cleared by TGRA compare match/input capture
	1	0	TCNT cleared by TGRB compare match/input capture
		1	TCNT cleared by counter clearing for another channel performing synchronous clearing/synchronous operation*1
1	0	0	TCNT clearing disabled
		1	TCNT cleared by TGRC compare match/input capture*2
	1	0	TCNT cleared by TGRD compare match/input capture*2
		1	TCNT cleared by counter clearing for another channel performing synchronous clearing/synchronous operation*1

Notes: 1. Synchronous operation is selected by setting the SYNC bit in TSYR to 1.
2. When TGRC or TGRD is used as a buffer register, TCNT is not cleared because the buffer register setting has priority, and compare match/input capture does not occur.

Bit	7	6	5	4	3	2	1	0
	—	—	BFB	BFA	MD3	MD2	MD1	MD0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Mode

0	0	0	0	Normal operation
			1	Reserved
		1	0	PWM mode 1
			1	PWM mode 2
	1	0	0	Phase counting mode 1
			1	Phase counting mode 2
		1	0	Phase counting mode 3
			1	Phase counting mode 4
1	*	*	*	—

*: Don't care

Notes: 1. MD3 is a reserved bit. In a write, it should always be written with 0.
2. Phase counting mode cannot be set for channels 0 and 3. In this case, 0 should always be written to MD2.

TGRA Buffer Operation

0	TGRA operates normally
1	TGRA and TGRC used together for buffer operation

TGRB Buffer Operation

0	TGRB operates normally
1	TGRB and TGRD used together for buffer operation

Bit	7	6	5	4	3	2	1	0
	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TGR3A I/O Control

0	0	0	0	TGR3A is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR3A is input capture register	Capture input source is TIOCA3 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is channel 4/count clock	Input capture at TCNT4 count-up/ count-down

*: Don't care

TGR3B I/O Control

0	0	0	0	TGR3B is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR3B is input capture register	Capture input source is TIOCB3 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is channel 4/count clock	Input capture at TCNT4 count-up/ count-down*1

*: Don't care

Note: 1. When bits TPSC2 to TPSC0 in TCR4 are set to B'000 and ø/1 is used as the TCNT4 count clock, this setting is invalid and input capture does not occur.

Bit	7	6	5	4	3	2	1	0
	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TRG3C I/O Control

0	0	0	0	TGR3C is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR3C is input capture register	Capture input source is TIOCC3 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is channel 4/count clock	Input capture at TCNT4 count-up/ count-down

*: Don't care

Note: When the BFA bit in TMDR3 is set to 1 and TGR3C is used as a buffer register, this setting is invalid and input capture/output compare does not occur.

TGR3D I/O Control

0	0	0	0	TGR3D is output compare register*2	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR3D is input capture register*2	Capture input source is TIOCD3 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is channel 4/count clock	Input capture at TCNT4 count-up/ count-down*1

*: Don't care

Notes: 1. When bits TPSC2 to TPSC0 in TCR4 are set to B'000 and ø/1 is used as the TCNT4 count clock, this setting is invalid and input capture does not occur.
2. When the BFB bit in TMDR3 is set to 1 and TGR3D is used as a buffer register, this setting is invalid and input capture/output compare does not occur.

Note: When TGRC or TGRD is designated for buffer operation, these settings are invalid and the register operates as a buffer register.

Bit	7	6	5	4	3	2	1	0
	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
Initial value	0	1	0	0	0	0	0	0
Read/Write	R/W	—	—	R/W	R/W	R/W	R/W	R/W

TGR Interrupt Enable A

0	Interrupt request (TGIA) by TGFA bit disabled
1	Interrupt request (TGIA) by TGFA bit enabled

TGR Interrupt Enable B

0	Interrupt request (TGIB) by TGFB bit disabled
1	Interrupt request (TGIB) by TGFB bit enabled

TGR Interrupt Enable C

0	Interrupt request (TGIC) by TGFC bit disabled
1	Interrupt request (TGIC) by TGFC bit enabled

TGR Interrupt Enable D

0	Interrupt request (TGID) by TGFD bit disabled
1	Interrupt request (TGID) by TGFD bit enabled

Overflow Interrupt Enable

0	Interrupt request (TCIV) by TCFV disabled
1	Interrupt request (TCIV) by TCFV enabled

A/D Conversion Start Request Enable

0	A/D conversion start request generation disabled
1	A/D conversion start request generation enabled

Bit	7	6	5	4	3	2	1	0
	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	—	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Input Capture/Output Compare Flag A

0	[Clearing conditions] • When DTC is activated by TGIA interrupt and DISEL bit in DTC's MRB register is 0 • When DMAC is activated by TGIA interrupt and DTA bit in DMAC's DMABCR register is 1 • When 0 is written to TGFA after reading TGFA = 1
1	[Setting conditions] • When TCNT = TGRA while TGRA is functioning as output compare register • When TCNT value is transferred to TGRA by input capture signal while TGRA is functioning as input capture register

Input Capture/Output Compare Flag B

0	[Clearing conditions] • When DTC is activated by TGIB interrupt and DISEL bit in DTC's MRB register is 0 • When 0 is written to TGFB after reading TGFB = 1
1	[Setting conditions] • When TCNT = TGRB while TGRB is functioning as output compare register • When TCNT value is transferred to TGRB by input capture signal while TGRB is functioning as input capture register

Input Capture/Output Compare Flag C

0	[Clearing conditions] • When DTC is activated by TGIC interrupt and DISEL bit in DTC's MRB register is 0 • When 0 is written to TGFC after reading TGFC = 1
1	[Setting conditions] • When TCNT = TGRC while TGRC is functioning as output compare register • When TCNT value is transferred to TGRC by input capture signal while TGRC is functioning as input capture register

Input Capture/Output Compare Flag D

0	[Clearing conditions] • When DTC is activated by TGID interrupt and DISEL bit in DTC's MRB register is 0 • When 0 is written to TGFD after reading TGFD = 1
1	[Setting conditions] • When TCNT = TGRD while TGRD is functioning as output compare register • When TCNT value is transferred to TGRD by input capture signal while TGRD is functioning as input capture register

Overflow Flag

0	[Clearing condition] When 0 is written to TCFV after reading TCFV = 1
1	[Setting condition] When the TCNT value overflows (from H'FFFF to H'0000)

Note: * Can only be written with 0, to clear the flag.

TCNT3—Timer Counter 3 **H'FE86** **TPU3**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Up-counter

TGR3A—Timer General Register 3A **H'FE88** **TPU3**
TGR3B—Timer General Register 3B **H'FE8A** **TPU3**
TGR3C—Timer General Register 3C **H'FE8C** **TPU3**
TGR3D—Timer General Register 3D **H'FE8E** **TPU3**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Timer Prescaler

0	0	0	Internal clock: count on ø/1
		1	Internal clock: count on ø/4
	1	0	Internal clock: count on ø/16
		1	Internal clock: count on ø/64
1	0	0	External clock: count on TCLKA pin input
		1	External clock: count on TCLKC pin input
	1	0	Internal clock: count on ø/1024
		1	Count on TCNT5 overflow/underflow

Note: This setting is invalid when channel 4 is in phase counting mode.

Clock Edge

0	0	Count at rising edge
	1	Count at falling edge
1	—	Count at both edges

Note: This setting is invalid when channel 4 is in phase counting mode.

Counter Clear

0	0	TCNT clearing disabled
	1	TCNT cleared by TGRA compare match/input capture
1	0	TCNT cleared by TGRB compare match/input capture
	1	TCNT cleared by counter clearing for another channel performing synchronous clearing/synchronous operation*

Note: * Synchronous operation is selected by setting the SYNC bit in TSYR to 1.

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	MD3	MD2	MD1	MD0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Mode

0	0	0	0	Normal operation
			1	Reserved
		1	0	PWM mode 1
			1	PWM mode 2
	1	0	0	Phase counting mode 1
			1	Phase counting mode 2
		1	0	Phase counting mode 3
			1	Phase counting mode 4
1	*	*	*	—

*: Don't care

Note: MD3 is a reserved bit. In a write, it should always be written with 0.

Bit	7	6	5	4	3	2	1	0
	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TGR4A I/O Control

0	0	0	0	TGR4A is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR4A is input capture register	Capture input source is TIOCA4 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is TGR3A compare match/ input capture	Input capture at generation of TGR3A compare match/input capture

*: Don't care

TGR4B I/O Control

0	0	0	0	TGR4B is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR4B is input capture register	Capture input source is TIOCB4 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is TGR3C compare match/ input capture	Input capture at generation of TGR3C compare match/input capture

*: Don't care

Bit	7	6	5	4	3	2	1	0
	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
Initial value	0	1	0	0	0	0	0	0
Read/Write	R/W	—	R/W	R/W	—	—	R/W	R/W

TGR Interrupt Enable A

0	Interrupt request (TGIA) by TGFA bit disabled
1	Interrupt request (TGIA) by TGFA bit enabled

TGR Interrupt Enable B

0	Interrupt request (TGIB) by TGFB bit disabled
1	Interrupt request (TGIB) by TGFB bit enabled

Overflow Interrupt Enable

0	Interrupt request (TCIV) by TCFV disabled
1	Interrupt request (TCIV) by TCFV enabled

Underflow Interrupt Enable

0	Interrupt request (TCIU) by TCFU disabled
1	Interrupt request (TCIU) by TCFU enabled

A/D Conversion Start Request Enable

0	A/D conversion start request generation disabled
1	A/D conversion start request generation enabled

Bit	7	6	5	4	3	2	1	0
	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
Initial value	1	1	0	0	0	0	0	0
Read/Write	R	—	R/(W)*	R/(W)*	—	—	R/(W)*	R/(W)*

Input Capture/Output Compare Flag A

0	[Clearing conditions] • When DTC is activated by TGIA interrupt and DISEL bit in DTC's MRB register is 0 • When DMAC is activated by TGIA interrupt and DTA bit in DMAC's DMABCR register is 1 • When 0 is written to TGFA after reading TGFA = 1
1	[Setting conditions] • When TCNT = TGRA while TGRA is functioning as output compare register • When TCNT value is transferred to TGRA by input capture signal while TGRA is functioning as input capture register

Input Capture/Output Compare Flag B

0	[Clearing conditions] • When DTC is activated by TGIB interrupt and DISEL bit in DTC's MRB register is 0 • When 0 is written to TGFB after reading TGFB = 1
1	[Setting conditions] • When TCNT = TGRB while TGRB is functioning as output compare register • When TCNT value is transferred to TGRB by input capture signal while TGRB is functioning as input capture register

Overflow Flag

0	[Clearing condition] When 0 is written to TCFV after reading TCFV = 1
1	[Setting condition] When the TCNT value overflows (from H'FFFF to H'0000)

Underflow Flag

0	[Clearing condition] When 0 is written to TCFU after reading TCFU = 1
1	[Setting condition] When the TCNT value underflows (from H'0000 to H'FFFF)

Count Direction Flag

0	TCNT counts down
1	TCNT counts up

Note: * Can only be written with 0, to clear the flag.

TCNT4—Timer Counter 4 **H'FE96** **TPU4**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Up/down-counter*

Note: * This timer counter can be used as an up/down-counter only in phase counting mode or when performing overflow/underflow counting on another channel. In other cases it functions as an up-counter.

TGR4A—Timer General Register 4A **H'FE98** **TPU4**
TGR4B—Timer General Register 4B **H'FE9A** **TPU4**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Time Prescaler

0	0	0	Internal clock: count on ø/1
		1	Internal clock: count on ø/4
	1	0	Internal clock: count on ø/16
		1	Internal clock: count on ø/64
1	0	0	External clock: count on TCLKA pin input
		1	External clock: count on TCLKC pin input
	1	0	Internal clock: count on ø/256
		1	External clock: count on TCLKD pin input

Note: This setting is invalid when channel 5 is in phase counting mode.

Clock Edge

0	0	Count at rising edge
	1	Count at falling edge
1	—	Count at both edges

Note: This setting is invalid when channel 5 is in phase counting mode.

Counter Clear

0	0	TCNT clearing disabled
	1	TCNT cleared by TGRA compare match/input capture
1	0	TCNT cleared by TGRB compare match/input capture
	1	TCNT cleared by counter clearing for another channel performing synchronous clearing/synchronous operation*

Note: * Synchronous operation is selected by setting the SYNC bit in TSYR to 1.

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	MD3	MD2	MD1	MD0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Mode

0	0	0	0	Normal operation
			1	Reserved
		1	0	PWM mode 1
			1	PWM mode 2
	1	0	0	Phase counting mode 1
			1	Phase counting mode 2
		1	0	Phase counting mode 3
			1	Phase counting mode 4
1	*	*	*	—

*: Don't care

Note: MD3 is a reserved bit. In a write, it should always be written with 0.

Bit	7	6	5	4	3	2	1	0
	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TGR5A I/O Control

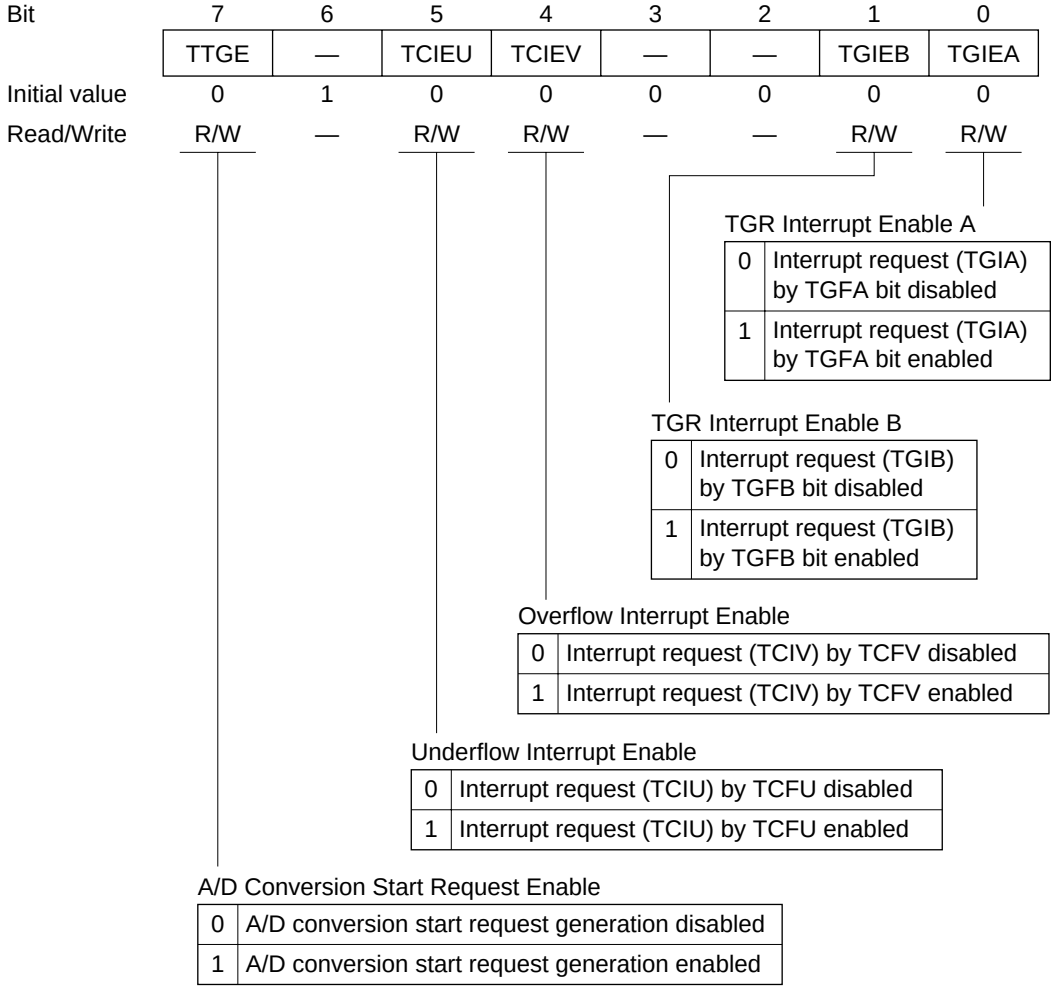
0	0	0	0	TGR5A is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	*	0	0	TGR5A is input capture register	Capture input source is TIOCA5 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges

*: Don't care

TGR5B I/O Control

0	0	0	0	TGR5B is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	*	0	0	TGR5B is input capture register	Capture input source is TIOCB5 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges

*: Don't care


Bit
7
6
5
4
3
2
1
0
TTGE
—
TCIEU
TCIEV
—
—
TGIEB
TGIEA
Initial value
0
1
0
0
0
0
0
0
Read/Write
R/W
—
R/W
R/W
—
—
R/W
R/W
TGR Interrupt Enable A
0 Interrupt request (TGIA) by TGFA bit disabled
1 Interrupt request (TGIA) by TGFA bit enabled
TGR Interrupt Enable B
0 Interrupt request (TGIB) by TGFB bit disabled
1 Interrupt request (TGIB) by TGFB bit enabled
Overflow Interrupt Enable
0 Interrupt request (TCIV) by TCFV disabled
1 Interrupt request (TCIV) by TCFV enabled
Underflow Interrupt Enable
0 Interrupt request (TCIU) by TCFU disabled
1 Interrupt request (TCIU) by TCFU enabled
A/D Conversion Start Request Enable
0 A/D conversion start request generation disabled
1 A/D conversion start request generation enabled

Bit	7	6	5	4	3	2	1	0
	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
Initial value	1	1	0	0	0	0	0	0
Read/Write	R	—	R/(W)*	R/(W)*	—	—	R/(W)*	R/(W)*

Input Capture/Output Compare Flag A

0	[Clearing conditions] • When DTC is activated by TGIA interrupt and DISEL bit in DTC's MRB register is 0 • When DMAC is activated by TGIA interrupt and DTA bit in DMAC's DMABCR register is 1 • When 0 is written to TGFA after reading TGFA = 1
1	[Setting conditions] • When TCNT = TGRA while TGRA is functioning as output compare register • When TCNT value is transferred to TGRA by input capture signal while TGRA is functioning as input capture register

Input Capture/Output Compare Flag B

0	[Clearing conditions] • When DTC is activated by TGIB interrupt and DISEL bit in DTC's MRB register is 0 • When 0 is written to TGFB after reading TGFB = 1
1	[Setting conditions] • When TCNT = TGRB while TGRB is functioning as output compare register • When TCNT value is transferred to TGRB by input capture signal while TGRB is functioning as input capture register

Overflow Flag

0	[Clearing condition] When 0 is written to TCFV after reading TCFV = 1
1	[Setting condition] When the TCNT value overflows (from H'FFFF to H'0000)

Underflow Flag

0	[Clearing condition] When 0 is written to TCFU after reading TCFU = 1
1	[Setting condition] When the TCNT value underflows (from H'0000 to H'FFFF)

Count Direction Flag

0	TCNT counts down
1	TCNT counts up

Note: * Can only be written with 0, to clear the flag.

TCNT5—Timer Counter 5 **H'FEA6** **TPU5**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Up/down-counter*

Note: * This timer counter can be used as an up/down-counter only in phase counting mode or when performing overflow/underflow counting on another channel. In other cases it functions as an up-counter.

TGR5A—Timer General Register 5A **H'FEA8** **TPU5**
TGR5B—Timer General Register 5B **H'FEAA** **TPU5**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	ABW7	ABW6	ABW5	ABW4	ABW3	ABW2	ABW1	ABW0
Modes 2, 4, 6								
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Modes 1, 5, 7								
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Area 7 to 0 Bus Width Control

0	Area n is designated as 16-bit access space
1	Area n is designated as 8-bit access space

(n = 15 to 0)

ASTCR—Access State Control Register **H'FEC1** **Bus Controller**

Bit	7	6	5	4	3	2	1	0
	AST7	AST6	AST5	AST4	AST3	AST2	AST1	AST0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Area 7 to 0 Access State Control

0	Area n is designated as 2-state access space Wait state insertion in area n external space accesses is disabled
1	Area n external space accesses are 3-state accesses Wait state insertion in area n external space accesses is enabled

(n = 7 to 0)

WTCRA

Bit	15	14	13	12	11	10	9	8
	—	W72	W71	W70	—	W62	W61	W60
Initial value	0	1	1	1	0	1	1	1
Read/Write	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	—	W52	W51	W50	—	W42	W41	W40
Initial value	0	1	1	1	0	1	1	1
Read/Write	R	R/W	R/W	R/W	R	R/W	R/W	R/W

WTCRB

Bit	15	14	13	12	11	10	9	8
	—	W32	W31	W30	—	W22	W21	W20
Initial value	0	1	1	1	0	1	1	1
Read/Write	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	—	W12	W11	W10	—	W02	W01	W00
Initial value	0	1	1	1	0	1	1	1
Read/Write	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Wait Control

Wn2	Wn1	Wn0	Description
0	0	0	Program wait not inserted in area n external access
		1	1 program wait state inserted in area n external access
	1	0	2 program wait states inserted in area n external access
		1	3 program wait states inserted in area n external access
1	0	0	4 program wait states inserted in area n external access
		1	5 program wait states inserted in area n external access
	1	0	6 program wait states inserted in area n external access
		1	7 program wait states inserted in area n external access

(n = 7 to 0)

Bit	7	6	5	4	3	2	1	0
	RDN7	RDN6	RDN5	RDN4	RDN3	RDN2	RDN1	RDN0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Read Strobe Timing Control

RDNn	Description
0	In an area n read access, the $\overline{RD}$ strobe is negated at the end of the read cycle
1	In an area n read access, the $\overline{RD}$ strobe is negated one half-state before the end of the read cycle

(n = 7 to 0)

CSACRH

Bit	15	14	13	12	11	10	9	8
	CSXH7	CSXH6	CSXH5	CSXH4	CSXH3	CSXH2	CSXH1	CSXH0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

$\overline{CS}$ and Address Signal Assertion Period Control 1

CSXHn	Description
0	In area n basic bus interface access, the $\overline{CSn}$ and address assertion period (T_h) is not extended
1	In area n basic bus interface access, the $\overline{CSn}$ and address assertion period (T_h) is extended

(n = 7 to 0)

CSACRL

Bit	7	6	5	4	3	2	1	0
	CSXT7	CSXT6	CSXT5	CSXT4	CSXT3	CSXT2	CSXT1	CSXT0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

$\overline{CS}$ and Address Signal Assertion Period Control 2

CSXTn	Description
0	In area n basic bus interface access, the $\overline{CSn}$ and address assertion period (T_t) is not extended
1	In area n basic bus interface access, the $\overline{CSn}$ and address assertion period (T_t) is extended

(n = 7 to 0)

BROMCRH

Bit	7	6	5	4	3	2	1	0
	BSRM0	BSTS02	BSTS01	BSTS00	—	—	BSWD01	BSWD00
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BROMCRL

Bit	7	6	5	4	3	2	1	0
	BSRM1	BSTS12	BSTS11	BSTS10	—	—	BSWD11	BSWD10
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Burst Word Length Select

BSWDn1	BSWDn0	Description
0	0	Maximum 4 words in area n burst access
	1	Maximum 8 words in area n burst access
1	0	Maximum 16 words in area n burst access
	1	Maximum 32 words in area n burst access

(n = 1 or 0)

Burst Cycle Select

BSTSn2	BSTSn1	BSTSn0	Description
0	0	0	Area n burst cycle comprises 1 state
		1	Area n burst cycle comprises 2 states
	1	0	Area n burst cycle comprises 3 states
		1	Area n burst cycle comprises 4 states
1	0	0	Area n burst cycle comprises 5 states
		1	Area n burst cycle comprises 6 states
	1	0	Area n burst cycle comprises 7 states
		1	Area n burst cycle comprises 8 states

(n = 1 or 0)

Burst ROM Interface Select

BSRMn	Description
0	Area n is basic bus interface space
1	Area n is burst ROM interface space

Bit	15	14	13	12	11	10	9	8
	BRLE	BREQOE	—	IDLC	ICIS1	ICIS0	WDBE	WAITE
Initial value	0	0	0	1	1	1	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

$\overline{\text{WAIT}}$ Pin Enable

0	Wait input by $\overline{\text{WAIT}}$ pin disabled $\overline{\text{WAIT}}$ pin can be used as I/O port
1	Wait input by $\overline{\text{WAIT}}$ pin enabled

Write Data Buffer Enable

0	Write data buffer function not used
1	Write data buffer function used

Idle Cycle Insert 0

0	Idle cycle not inserted when external read cycle and external write cycle are performed consecutively
1	Idle cycle inserted when external read cycle and external write cycle are performed consecutively

Idle Cycle Insert 1

0	Idle cycle not inserted in case of consecutive external read cycles in different areas
1	Idle cycle inserted in case of consecutive external read cycles in different areas

Idle Cycle State Number Select

0	Idle cycle comprises 1 state
1	Idle cycle comprises 2 states

$\overline{\text{BREQO}}$ Pin Enable

0	$\overline{\text{BREQO}}$ signal output disabled $\overline{\text{BREQO}}$ pin can be used as I/O port
1	$\overline{\text{BREQO}}$ signal output enabled

External Bus Release Enable

0	External bus release disabled $\overline{\text{BREQ}}$, $\overline{\text{BACK}}$, and $\overline{\text{BREQO}}$ pins can be used as I/O ports
1	External bus release enabled

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	RAMS	RAM2	RAM1	RAM0
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

RAM Select, Flash Memory Area Select

RAMS	RAM2	RAM1	RAM0	RAM Area		Block Name
				Modes 4, 7, 10, 11, 12, 15	Modes 5, 6, 13, 14	
0	*	*	*	H'FFA000 to H'FFAFFF		4-kbyte RAM area
1	0	0	0	H'000000 to H'000FFF	H'100000 to H'100FFF	EB0 (4 kbytes)
			1	H'001000 to H'001FFF	H'101000 to H'101FFF	EB1 (4 kbytes)
		1	0	H'002000 to H'002FFF	H'102000 to H'102FFF	EB2 (4 kbytes)
			1	H'003000 to H'003FFF	H'103000 to H'103FFF	EB3 (4 kbytes)
	1	0	0	H'004000 to H'004FFF	H'104000 to H'104FFF	EB4 (4 kbytes)
			1	H'005000 to H'005FFF	H'105000 to H'105FFF	EB5 (4 kbytes)
		1	0	H'006000 to H'006FFF	H'106000 to H'106FFF	EB6 (4 kbytes)
			1	H'007000 to H'007FFF	H'107000 to H'107FFF	EB7 (4 kbytes)

Bit	15	14	13	12	11	10	9	8
	OEE	RAST	—	CAST	—	RMTS2	RMTS1	RMTS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

DRAM Space Select

RMTS2	RMTS1	RMTS0	Description			
			Area 5	Area 4	Area 3	Area 2
0	0	0	Normal space			
		1	Normal space			DRAM space
	1	0	Normal space		DRAM space	
		1	DRAM space			
1	0	—	Reserved (setting prohibited)			
	1	0				
		1	Continuous DRAM space			

Column Address Output Cycle Number Select

0	Column address output cycle comprises 2 states
1	Column address output cycle comprises 3 states

$\overline{RAS}$ Assertion Timing Select

0	$\overline{RAS}$ is asserted from ø falling edge in T_r cycle
1	$\overline{RAS}$ is asserted from start of T_r cycle

$\overline{OE}$ Output Enable

0	$\overline{OE}$ signal output disabled $\overline{OE}$ pin can be used as I/O port
1	$\overline{OE}$ signal output enabled

Bit	7	6	5	4	3	2	1	0
	BE	RCDM	DDS	EDDS	—	MXC2	MXC1	MXC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address Multiplex Select

0	0	0	8-bit shift • When 8-bit access space is designated: Row address bits A23 to A8 used for comparison • When 16-bit access space is designated: Row address bits A23 to A9 used for comparison
		1	9-bit shift • When 8-bit access space is designated: Row address bits A23 to A9 used for comparison • When 16-bit access space is designated: Row address bits A23 to A10 used for comparison
	1	0	10-bit shift • When 8-bit access space is designated: Row address bits A23 to A10 used for comparison • When 16-bit access space is designated: Row address bits A23 to A11 used for comparison
		1	11-bit shift • When 8-bit access space is designated: Row address bits A23 to A11 used for comparison • When 16-bit access space is designated: Row address bits A23 to A12 used for comparison
1	—	—	Reserved (setting prohibited)

EXDMAC Single Address Transfer Option

0	Full access is always executed when EXDMAC single address transfer is performed in DRAM space
1	Burst access is possible when EXDMAC single address transfer is performed in DRAM space

DMAC Single Address Transfer Option

0	Full access is always executed when DMAC single address transfer is performed in DRAM space
1	Burst access is possible when DMAC single address transfer is performed in DRAM space

$\overline{\text{RAS}}$ Down Mode

0	$\overline{\text{RAS}}$ up mode selected for DRAM space access
1	$\overline{\text{RAS}}$ down mode selected for DRAM space access

Burst Access Enable

0	Full access always used for DRAM space access
1	DRAM space access performed in fast page mode

Bit	7	6	5	4	3	2	1	0
	DRMI	—	TPC1	TPC0	—	—	RCD1	RCD0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

$\overline{RAS}$-$\overline{CAS}$ Wait Control

0	0	Wait cycle not inserted between $\overline{RAS}$ assert cycle and $\overline{CAS}$ assert cycle
	1	1-state wait cycle inserted between $\overline{RAS}$ assert cycle and $\overline{CAS}$ assert cycle
1	0	2-state wait cycle inserted between $\overline{RAS}$ assert cycle and $\overline{CAS}$ assert cycle
	1	3-state wait cycle inserted between $\overline{RAS}$ assert cycle and $\overline{CAS}$ assert cycle

Precharge State Control

0	0	$\overline{RAS}$ precharge cycle comprises 1 state
	1	$\overline{RAS}$ precharge cycle comprises 2 states
1	0	$\overline{RAS}$ precharge cycle comprises 3 states
	1	$\overline{RAS}$ precharge cycle comprises 4 states

Idle Cycle Insertion

0	Idle cycle not inserted after DRAM space access
1	Idle cycle inserted after DRAM space access Idle cycle insertion conditions, setting of number of states, etc., comply with settings of bits ICIS1, ICIS0, and IDLC in BCR register

Bit	15	14	13	12	11	10	9	8
	CMF	CMIE	RCW1	RCW0	—	RTCK2	RTCK1	RTCK0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Refresh Counter Clock Select

0	0	0	Count operation halted
		1	Count on ø/2
	1	0	Count on ø/8
		1	Count on ø/32
1	0	0	Count on ø/128
		1	Count on ø/512
	1	0	Count on ø/2048
		1	Count on ø/4096

$\overline{CAS}$-$\overline{RAS}$ Wait Control

0	0	Wait state not inserted between $\overline{CAS}$ and $\overline{RAS}$ in refresh cycle
	1	1 wait state inserted between $\overline{CAS}$ and $\overline{RAS}$ in refresh cycle
1	0	2 wait states inserted between $\overline{CAS}$ and $\overline{RAS}$ in refresh cycle
	1	3 wait states inserted between $\overline{CAS}$ and $\overline{RAS}$ in refresh cycle

Compare Match Interrupt Enable

0	Interrupt request by CMF flag disabled
1	Interrupt request by CMF flag enabled

Compare Match Flag

0	[Clearing conditions] • When 0 is written to CMF after reading CMF = 1 while the RFSHE bit is cleared to 0 • When CBR refreshing is executed while the RFSHE bit is set to 1
1	[Setting condition] When RTCOR = RTCNT

Note: * Only 0 can be written, to clear the flag.

Bit	7	6	5	4	3	2	1	0
	RFSHE	CBRM	RLW1	RLW0	SLFRF	TPCS2	TPCS1	TPCS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Self-Refresh Precharge Cycle Control

0	0	0	$\overline{RAS}$ precharge cycle after self-refresh = [TPC set value] states
		1	$\overline{RAS}$ precharge cycle after self-refresh = [TPC set value + 1] states
1	1	0	$\overline{RAS}$ precharge cycle after self-refresh = [TPC set value + 2] states
		1	$\overline{RAS}$ precharge cycle after self-refresh = [TPC set value + 3] states
0	0	0	$\overline{RAS}$ precharge cycle after self-refresh = [TPC set value + 4] states
		1	$\overline{RAS}$ precharge cycle after self-refresh = [TPC set value + 5] states
1	1	0	$\overline{RAS}$ precharge cycle after self-refresh = [TPC set value + 6] states
		1	$\overline{RAS}$ precharge cycle after self-refresh = [TPC set value + 7] states

Self-Refresh Enable

0	Self-refreshing is disabled in software standby mode
1	Self-refreshing is enabled in software standby mode

Refresh Cycle Wait Control

0	0	No wait state inserted in CBR refresh
	1	1 wait state inserted in CBR refresh
1	0	2 wait states inserted in CBR refresh
	1	3 wait states inserted in CBR refresh

CBR Refresh Mode

0	External access during CAS-before-RAS refreshing is enabled
1	External access during CAS-before-RAS refreshing is disabled

Refresh Control

0	Refresh control is not performed
1	Refresh control is performed

RTCNT—Refresh Timer Counter **H'FED6** **Bus Controller**

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Count value based on internal clock

RTCOR—Refresh Time Control Register **H'FED7** **Bus Controller**

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Period for compare match operations with RTCNT

MAR0AH—Memory Address Register 0AH **H'FEE0** **DMAC**
MAR0AL—Memory Address Register 0AL **H'FEE2** **DMAC**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAR0AH	—	—	—	—	—	—	—	—								
Initial value	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	*
Read/Write	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAR0AL																
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

In short address mode: Specifies transfer destination/transfer source address
In full address mode: Specifies transfer source address

*: Undefined

IOAR0A—I/O Address Register 0A **H'FEE4** **DMAC**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IOAR0A																
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

In short address mode: Specifies transfer destination/transfer source address
In full address mode: Not used

*: Undefined

ETCR0A—Transfer Count Register 0A **H'FEE6** **DMAC**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETCR0A																
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sequential mode and idle mode Normal mode	Transfer counter	
Repeat mode	Holds number of transfers	Transfer counter
Block transfer mode	Holds block size	Block size counter

*: Undefined

MAR0BH—Memory Address Register 0BH **H'FEE8** **DMAC**
MAR0BL—Memory Address Register 0BL **H'FEEA** **DMAC**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAR0BH	—	—	—	—	—	—	—	—								
Initial value	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	*
Read/Write	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAR0BL																
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

In short address mode: Specifies transfer destination/transfer source address
In full address mode: Specifies transfer destination

*: Undefined

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IOAR0B																
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

In short address mode: Specifies transfer destination/transfer source address
In full address mode: Not used

*: Undefined

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETCR0B																
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sequential mode and idle mode: Transfer counter

Repeat mode: Holds number of transfers | Transfer counter

Block transfer mode: Block transfer counter

*: Undefined

Note: Not used in normal mode.

MAR1AH—Memory Address Register 1AH **H'FEF0** **DMAC**
MAR1AL—Memory Address Register 1AL **H'FEF2** **DMAC**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAR1AH	—	—	—	—	—	—	—	—								
Initial value	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	*
Read/Write	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAR1AL																
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

In short address mode: Specifies transfer destination/transfer source address
In full address mode: Not used

*: Undefined

IOAR1A—I/O Address Register 1A **H'FEF4** **DMAC**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IOAR1A																
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

In short address mode: Specifies transfer destination/transfer source address
In full address mode: Not used

*: Undefined

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETCR1A																
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sequential mode
Idle mode
Normal mode: Transfer counter

Repeat mode: Holds number of transfers; Transfer counter

Block transfer mode: Holds block size; Block size counter

*: Undefined

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAR1BH	—	—	—	—	—	—	—	—								
Initial value	0	0	0	0	0	0	0	0	*	*	*	*	*	*	*	*
Read/Write	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAR1BL																
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

In short address mode: Specifies transfer destination/transfer source address
In full address mode: Not used

*: Undefined

IOAR1B—I/O Address Register 1B **H'FEFC** **DMAC**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IOAR1B																
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

In short address mode: Specifies transfer destination/transfer source address
In full address mode: Not used

*: Undefined

ETCR1B—Transfer Count Register 1B **H'FEFE** **DMAC**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETCR1B																
Initial value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Sequential mode and idle mode: Transfer counter

Repeat mode: Holds number of transfers / Transfer counter

Block transfer mode: Block transfer counter

*: Undefined

Note: Not used in normal mode.

Bit	7	6	5	4	3	2	1	0
DMAWER	—	—	—	—	WE1B	WE1A	WE0B	WE0A
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Write Enable 0A

0	Writes to all bits in DMACR0A, and bits 8, 4, and 0 in DMABCR are disabled
1	Writes to all bits in DMACR0A, and bits 8, 4, and 0 in DMABCR are enabled

Write Enable 0B

0	Writes to all bits in DMACR0B, bits 9, 5, and 1 in DMABCR, and bit 4 in DMATCR are disabled
1	Writes to all bits in DMACR0B, bits 9, 5, and 1 in DMABCR, and bit 4 in DMATCR are enabled

Write Enable 1A

0	Writes to all bits in DMACR1A, and bits 10, 6, and 2 in DMABCR are disabled
1	Writes to all bits in DMACR1A, and bits 10, 6, and 2 in DMABCR are enabled

Write Enable 1B

0	Writes to all bits in DMACR1B, bits 11, 7, and 3 in DMABCR, and bit 5 in DMATCR are disabled
1	Writes to all bits in DMACR1B, bits 11, 7, and 3 in DMABCR, and bit 5 in DMATCR are enabled

Bit	7	6	5	4	3	2	1	0
DMATCR	—	—	TEE1	TEE0	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	—	—	—	—

$\overline{\text{TEND0}}$ Pin Enable

0	$\overline{\text{TEND0}}$ pin output disabled
1	$\overline{\text{TEND0}}$ pin output enabled

$\overline{\text{TEND1}}$ Pin Enable

0	$\overline{\text{TEND1}}$ pin output disabled
1	$\overline{\text{TEND1}}$ pin output enabled

Full address mode
DMACRA

Bit	15	14	13	12	11	10	9	8
DMACRA	DTSZ	SAID	SAIDE	BLKDIR	BLKE	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Block Direction/Block Enable

0	0	Transfer in normal mode
	1	Transfer in block transfer mode, destination is block area
1	0	Transfer in normal mode
	1	Transfer in block transfer mode, source is block area

Source Address Increment/Decrement

0	0	MARA is fixed
	1	MARA is incremented after a data transfer (1) When DTSZ = 0, MARA is incremented by 1 after a transfer (2) When DTSZ = 1, MARA is incremented by 2 after a transfer
1	0	MARA is fixed
	1	MARA is decremented after a data transfer (1) When DTSZ = 0, MARA is decremented by 1 after a transfer (2) When DTSZ = 1, MARA is decremented by 2 after a transfer

Data Transfer Size

0	Byte-size transfer
1	Word-size transfer

Bit	7	6	5	4	3	2	1	0
DMACRB	—	DAID	DAIDE	—	DTF3	DTF2	DTF1	DTF0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Data Transfer Factor

DTF3	DTF2	DTF1	DTF0	Block Transfer Mode	Normal Mode
0	0	0	0	—	—
			1	A/D converter conversion end interrupt	—
		1	0	$\overline{\text{DREQ}}$ pin falling edge input	$\overline{\text{DREQ}}$ pin falling edge input
			1	$\overline{\text{DREQ}}$ pin low-level input	$\overline{\text{DREQ}}$ pin low-level input
	1	0	0	SCI channel 0 transmission complete interrupt	—
			1	SCI channel 0 reception complete interrupt	—
		1	0	SCI channel 1 transmission complete interrupt	Auto-request (cycle steal)
			1	SCI channel 1 reception complete interrupt	Auto-request (burst)
1	0	0	0	TPU channel 0 compare match/ input capture A interrupt	—
			1	TPU channel 1 compare match/ input capture A interrupt	—
		1	0	TPU channel 2 compare match/ input capture A interrupt	—
			1	TPU channel 3 compare match/ input capture A interrupt	—
	1	0	0	TPU channel 4 compare match/ input capture A interrupt	—
			1	TPU channel 5 compare match/ input capture A interrupt	—
		1	0	—	—
			1	—	—

*: Don't care

Destination Address Increment/Decrement

0	0	MARB is fixed
	1	MARB is incremented after a data transfer (1) When DTSZ = 0, MARB is incremented by 1 after a transfer (2) When DTSZ = 1, MARB is incremented by 2 after a transfer
1	0	MARB is fixed
	1	MARB is decremented after a data transfer (1) When DTSZ = 0, MARB is decremented by 1 after a transfer (2) When DTSZ = 1, MARB is decremented by 2 after a transfer

Bit	7	6	5	4	3	2	1	0
DMACR	DTSZ	DTID	RPE	DTDIR	DTF3	DTF2	DTF1	DTF0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Data Transfer Size

0	Byte-size transfer
1	Word-size transfer

Data Transfer Increment/ Decrement

0	MAR is incremented after a data transfer
1	MAR is decremented after a data transfer

Repeat Enable

0	Sequential mode
1	Repeat mode or idle mode

Data Transfer Factor

				Channel A	Channel B
0	0	0	0	—	
			1	Activated by A/D converter conversion end interrupt	
		1	0	—	Activated by $\overline{\text{DREQ}}$ pin falling edge input
			1	—	Activated by $\overline{\text{DREQ}}$ pin low-level input
	1	0	0	Activated by SCI channel 0 transmission complete interrupt	
			1	Activated by SCI channel 0 reception complete interrupt	
		1	0	Activated by SCI channel 1 transmission complete interrupt	
			1	Activated by SCI channel 1 reception complete interrupt	
1	0	0	0	Activated by TPU channel 0 compare match/ input capture A interrupt	
			1	Activated by TPU channel 1 compare match/ input capture A interrupt	
		1	0	Activated by TPU channel 2 compare match/ input capture A interrupt	
			1	Activated by TPU channel 3 compare match/ input capture A interrupt	
	1	0	0	Activated by TPU channel 4 compare match/ input capture A interrupt	
			1	Activated by TPU channel 5 compare match/ input capture A interrupt	
		1	0	—	
			1	—	

Data Transfer Direction

0	Dual address mode: Transfer with MAR as source address and IOAR as destination address Single address mode: Transfer with MAR as source address and $\overline{\text{DACK}}$ pin as write strobe
1	Dual address mode: Transfer with IOAR as source address and MAR as destination address Single address mode: Transfer with $\overline{\text{DACK}}$ as read strobe and MAR as destination address

Full address mode
DMABCRH

Bit	15	14	13	12	11	10	9	8
DMABCRH	FAE1	FAE0	—	—	DTA1	—	DTA0	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Channel 0 Data Transfer Acknowledge

0	Clearing of selected internal interrupt source at time of DMA transfer is disabled
1	Clearing of selected internal interrupt source at time of DMA transfer is enabled

Channel 1 Data Transfer Acknowledge

0	Clearing of selected internal interrupt source at time of DMA transfer is disabled
1	Clearing of selected internal interrupt source at time of DMA transfer is enabled

Channel 0 Full Address Enable

0	Short address mode
1	Full address mode

Channel 1 Full Address Enable

0	Short address mode
1	Full address mode

DMABCRL

Bit	7	6	5	4	3	2	1	0
DMABCRL	DTME1	DTE1	DTME0	DTE0	DTIE1B	DTIE1A	DTIE0B	DTIE0A
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Channel 0 Data Transfer Interrupt Enable A

0	Transfer end interrupt disabled
1	Transfer end interrupt enabled

Channel 0 Data Transfer Interrupt Enable B

0	Transfer suspended interrupt disabled
1	Transfer suspended interrupt enabled

Channel 1 Data Transfer Interrupt Enable A

0	Transfer end interrupt disabled
1	Transfer end interrupt enabled

Channel 1 Data Transfer Interrupt Enable B

0	Transfer suspended interrupt disabled
1	Transfer suspended interrupt enabled

Channel 0 Data Transfer Enable

0	Data transfer disabled
1	Data transfer enabled

Channel 0 Data Transfer Master Enable

0	Data transfer disabled. In burst mode, cleared to 0 by an NMI interrupt
1	Data transfer enabled

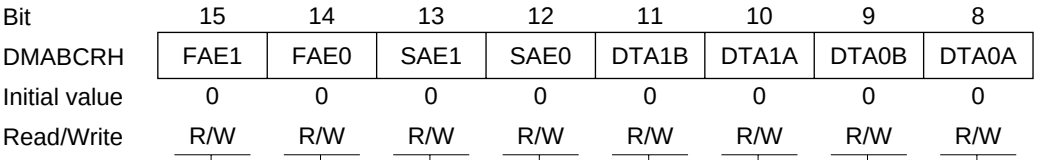
Channel 1 Data Transfer Enable

0	Data transfer disabled
1	Data transfer enabled

Channel 1 Data Transfer Master Enable

0	Data transfer disabled. In burst mode, cleared to 0 by an NMI interrupt
1	Data transfer enabled

DMABCRH



Bit	15	14	13	12	11	10	9	8
DMABCRH	FAE1	FAE0	SAE1	SAE0	DTA1B	DTA1A	DTA0B	DTA0A
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Channel 0A Data Transfer Acknowledge

0	Clearing of selected internal interrupt source at time of DMA transfer is disabled
1	Clearing of selected internal interrupt source at time of DMA transfer is enabled

Channel 0B Data Transfer Acknowledge

0	Clearing of selected internal interrupt source at time of DMA transfer is disabled
1	Clearing of selected internal interrupt source at time of DMA transfer is enabled

Channel 1A Data Transfer Acknowledge

0	Clearing of selected internal interrupt source at time of DMA transfer is disabled
1	Clearing of selected internal interrupt source at time of DMA transfer is enabled

Channel 1B Data Transfer Acknowledge

0	Clearing of selected internal interrupt source at time of DMA transfer is disabled
1	Clearing of selected internal interrupt source at time of DMA transfer is enabled

Channel 0B Single Address Enable

0	Transfer in dual address mode
1	Transfer in single address mode

Channel 1B Single Address Enable

0	Transfer in dual address mode
1	Transfer in single address mode

Channel 0 Full Address Mode

0	Short address mode
1	Full address mode

Channel 1 Full Address Mode

0	Short address mode
1	Full address mode

DMABCRL

Bit	7	6	5	4	3	2	1	0
DMABCRL	DTE1B	DTE1A	DTE0B	DTE0A	DTIE1B	DTIE1A	DTIE0B	DTIE0A
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Channel 0A Data Transfer Interrupt Enable

0	Transfer end interrupt disabled
1	Transfer end interrupt enabled

Channel 0B Data Transfer Interrupt Enable

0	Transfer end interrupt disabled
1	Transfer end interrupt enabled

Channel 1A Data Transfer Interrupt Enable

0	Transfer end interrupt disabled
1	Transfer end interrupt enabled

Channel 1B Data Transfer Interrupt Enable

0	Transfer end interrupt disabled
1	Transfer end interrupt enabled

Channel 0A Data Transfer Enable

0	Data transfer disabled
1	Data transfer enabled

Channel 0B Data Transfer Enable

0	Data transfer disabled
1	Data transfer enabled

Channel 1A Data Transfer Enable

0	Data transfer disabled
1	Data transfer enabled

Channel 1B Data Transfer Enable

0	Data transfer disabled
1	Data transfer enabled

Bit	7	6	5	4	3	2	1	0
	DTCE7	DTCE6	DTCE5	DTCE4	DTCE3	DTCE2	DTCE1	DTCE0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

DTC Activation Enable

0	DTC activation by interrupt is disabled [Clearing conditions] • When data transfer ends with the DISEL bit set to 1 • When the specified number of transfers end
1	DTC activation by this interrupt is enabled [Hold condition] When the DISEL bit is 0 and the specified number of transfers have not ended

Correspondence between Interrupt Sources and DTCER Register Bits

Register	Bits							
	7	6	5	4	3	2	1	0
DTCERA	IRQ0	IRQ1	IRQ2	IRQ3	IRQ4	IRQ5	IRQ6	IRQ7
DTCERB	IRQ8	IRQ9	IRQ10	IRQ11	IRQ12	IRQ13	IRQ14	IRQ15
DTCERC	—	ADI	TGI0A	TGI0B	TGI0C	TGI0D	TGI1A	TGI1B
DTCERD	TGI2A	TGI2B	TGI3A	TGI3B	TGI3C	TGI3D	TGI4A	TGI4B
DTCERE	TGI5A	TGI5B	—	—	CMIA0	CMIB0	CMIA1	CMIB1
DTCERF	DMTEND0A	DMTEND0B	DMTEND1A	DMTEND1B	RXI0	TXI0	RXI1	TXI1
DTCERG	RXI2	TXI2	RXI3	TXI3	RXI4	TXI4	—	—
DTCERH	—	—	—	—	—	—	—	—

Note: For DTCE bit setting, bit manipulation instructions such as BSET and BCLR must be used for reading and writing. For the initial setting only, however, when setting multiple activation sources at one time, it is possible to disable interrupts and write to the relevant register after a dummy read.

Bit	7	6	5	4	3	2	1	0
	SWDTE	DTVEC6	DTVEC5	DTVEC4	DTVEC3	DTVEC2	DTVEC1	DTVEC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*1	R/(W)*2	R/(W)*2	R/(W)*2	R/(W)*2	R/(W)*2	R/(W)*2	R/(W)*2

Sets vector number for DTC software activation

DTC Software Activation Enable

0	DTC software activation is disabled [Clearing conditions] • When the DISEL bit is 0 and the specified number of transfers have not ended • After an SWDTEND request
1	DTC software activation is enabled [Hold conditions] • When data transfer ends with the DISEL bit set to 1 • When the specified number of transfers end • During software-activated data transfer

Notes: 1. Only 1 can be written to the SWDTE bit.
2. Bits DTVEC6 to DTVEC0 can be written to when SWDTE = 0.

INTCR—Interrupt Control Register **H'FF31** **Interrupt Controller**

Bit	7	6	5	4	3	2	1	0
	—	—	INTM1	INTM0	NMIEG	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	—	—	—

NMI Edge Select

0	Interrupt request generated at falling edge of NMI input
1	Interrupt request generated at rising edge of NMI input

Interrupt Control Mode 1 and 0

INTM2	INTM1	Interrupt Control Mode	Description
0	0	0	Interrupts are controlled by I bit
	1	—	Setting prohibited
1	0	2	Interrupts are controlled by bits I2 to I0, and IPR
	1	—	Setting prohibited

IER—IRQ Enable Register **H'FF32** **Interrupt Controller**

Bit	15	14	13	12	11	10	9	8
	IRQ15E	IRQ14E	IRQ13E	IRQ12E	IRQ11E	IRQ10E	IRQ9E	IRQ8E
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	IRQ7E	IRQ6E	IRQ5E	IRQ4E	IRQ3E	IRQ2E	IRQ1E	IRQ0E
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IRQ15 to IRQ0 Enable

0	IRQn interrupts disabled
1	IRQn interrupts enabled

(n = 15 to 0)

Bit	15	14	13	12	11	10	9	8
	IRQ15F	IRQ14F	IRQ13F	IRQ12F	IRQ11F	IRQ10F	IRQ9F	IRQ8F
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Bit	7	6	5	4	3	2	1	0
	IRQ7F	IRQ6F	IRQ5F	IRQ4F	IRQ3F	IRQ2F	IRQ1F	IRQ0F
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

IRQ15 to IRQ0 Flags

0	[Clearing conditions] • When 0 is written to IRQnF after reading IRQnF = 1 • When interrupt exception handling is executed when low-level detection is set (IRQnSCB = IRQnSCA = 0) and $\overline{\text{IRQn}}$ input is high • When IRQn interrupt exception handling is executed when falling, rising, or both-edge detection is set (IRQnSCB = 1 or IRQnSCA = 1) • When the DTC is activated by an IRQn interrupt and the DISEL bit in MRB of the DTC is 0
1	[Setting conditions] • When $\overline{\text{IRQn}}$ input goes low when low-level detection is set (IRQnSCB = IRQnSCA = 0) • When a falling edge occurs in $\overline{\text{IRQn}}$ input when falling edge detection is set (IRQnSCB = 0, IRQnSCA = 1) • When a rising edge occurs in $\overline{\text{IRQn}}$ input when rising edge detection is set (IRQnSCB = 1, IRQnSCA = 0) • When a falling or rising edge occurs in $\overline{\text{IRQn}}$ input when both-edge detection is set (IRQnSCB = IRQnSCA = 1)

(n = 15 to 0)

Note: * Can only be written with 0, to clear the flag.

Bit	7	6	5	4	3	2	1	0
	SSBY	OPE	—	—	STS3	STS2	STS1	STS0
Initial value	0	1	0	0	1	1	1	1
Read/Write	R/W	R/W	—	—	R/W	R/W	R/W	R/W

Standby Timer Select 3 to 0

0	0	0	0	Reserved
			1	Reserved
		1	0	Reserved
			1	Reserved
	1	0	0	Reserved
			1	Standby time = 64 states
		1	0	Standby time = 512 states
			1	Standby time = 1,024 states
1	0	0	0	Standby time = 2,048 states
			1	Standby time = 4,096 states
		1	0	Standby time = 16,384 states
			1	Standby time = 32,768 states
	1	0	0	Standby time = 65,536 states
			1	Standby time = 131,072 states
		1	0	Standby time = 262,144 states
			1	Standby time = 524,288 states

Note: In the F-ZTAT™ version, the flash memory oscillation settling time must be secured.

Output Port Enable

0	In software standby mode, address bus and bus control signals are high-impedance
1	In software standby mode, address bus and bus control signals retain output state

Software Standby

0	Transition to sleep mode after execution of SLEEP instruction
1	Transition to software standby mode after execution of SLEEP instruction

Bit	7	6	5	4	3	2	1	0
	PSTOP	—	—	—	STCS	SCK2	SCK1	SCK0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	—	—	R/W	R/W	R/W	R/W

System Clock Select 2 to 0

0	0	0	1/1
		1	1/2
	1	0	1/4
		1	1/8
1	0	1	1/16
		1	1/32
	1	—	Setting prohibited

Frequency Multiplication Factor Switching Mode Select

0	Specified multiplication factor is valid after transition to software standby mode
1	Specified multiplication factor is valid immediately after STC bits are rewritten

ø Clock Output Control

PSTOP	Normal Operation	Sleep Mode	Software Standby Mode	Hardware Standby Mode
0	ø output	ø output	Fixed high	High impedance
1	Fixed high	Fixed high	Fixed high	High impedance

SYSCR—System Control Register **H'FF3D** **System Control**

Bit	7	6	5	4	3	2	1	0
	—	—	MACS	—	FLSHE	—	EXPE	RAME
Initial value	1	1	0	0	0	0	—*	1
Read/Write	R/W	R/W	R/W	R/W	R/W	—	R/W	R/W

RAM Enable

0	On-chip RAM disabled
1	On-chip RAM enabled

External Bus Mode Enable

0	External bus disabled
1	External bus enabled

Flash Memory Control Register Enable

0	Flash memory control registers are not selected for area H'FFFFC8 to H'FFFFCB
1	Flash memory control registers are selected for area H'FFFFC8 to H'FFFFCB

MAC Saturation

0	Non-saturating calculation for MAC instruction
1	Saturating calculation for MAC instruction

Note: * Determined by pins MD2 to MD0.

MDCR—Mode Control Register **H'FF3E** **MCU**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	MDS2	MDS1	MDS0
Initial value	0	0	0	0	0	—*	—*	—*
Read/Write	—	—	—	—	—	R	R	R

Current operating mode designated by mode pins

Note: * Determined by pins MD2 to MD0.

MSTPCRH—Module Stop Control Register H **H'FF40** **Power-Down State**
MSTPCRL—Module Stop Control Register L **H'FF41** **Power-Down State**

	MSTPCRH								MSTPCRL							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

All-module-clocks-stop mode enable

0	All-module-clocks-stop mode disabled
1	All-module-clocks-stop mode enabled

Specify Module Stop Mode

0	Module stop mode cleared
1	Module stop mode set

Correspondence between MSTP Bits and On-Chip Supporting Functions

Register	Bit	Module
MSTPCRH	ACSE	All-module-clocks-stop enable
	MSTP14	EXDMAC
	MSTP13	DMAC
	MSTP12	DTC
	MSTP11	TPU
	MSTP10	PPG
	MSTP9	D/A0, 1
	MSTP8	D/A2, 3
MSTPCRL	MSTP7	—
	MSTP6	A/D
	MSTP5	—
	MSTP4	—
	MSTP3	SCI2
	MSTP2	SCI1
	MSTP1	SCI0
	MSTP0	8-bit timer

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	STC1	STC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	R/W	—	R/W	R/W

Frequency multiplication factor

0	0	× 1
	1	× 2
1	0	× 4
	1	Setting prohibited

Bit	7	6	5	4	3	2	1	0
	G3CMS1	G3CMS0	G2CMS1	G2CMS0	G1CMS1	G1CMS0	G0CMS1	G0CMS0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Pulse Output Group 0 Output Trigger Select

0	0	TPU channel 0 compare match
	1	TPU channel 1 compare match
1	0	TPU channel 2 compare match
	1	TPU channel 3 compare match

Pulse Output Group 1 Output Trigger Select

0	0	TPU channel 0 compare match
	1	TPU channel 1 compare match
1	0	TPU channel 2 compare match
	1	TPU channel 3 compare match

Pulse Output Group 2 Output Trigger Select

0	0	TPU channel 0 compare match
	1	TPU channel 1 compare match
1	0	TPU channel 2 compare match
	1	TPU channel 3 compare match

Pulse Output Group 3 Output Trigger Select

0	0	TPU channel 0 compare match
	1	TPU channel 1 compare match
1	0	TPU channel 2 compare match
	1	TPU channel 3 compare match

Bit	7	6	5	4	3	2	1	0
	G3INV	G2INV	G1INV	G0INV	G3NOV	G2NOV	G1NOV	G0NOV
Initial value	1	1	1	1	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Group n Non-Overlap

0	Normal operation in pulse output group 0 (output values updated at compare match A in the selected TPU channel)
1	Non-overlapping operation in pulse output group n (1 output and 0 output can be performed independently at compare match A and B in the selected TPU channel)

(n = 3 to 0)

Group n Invert

0	Inverted output for pulse output group n (low-level output at pin for a 1 in PODRH)
1	Direct output for pulse output group n (high-level output at pin for a 1 in PODRH)

(n = 3 to 0)

NDERH

Bit	7	6	5	4	3	2	1	0
	NDER15	NDER14	NDER13	NDER12	NDER11	NDER10	NDER9	NDER8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Next Data Enable

0	Pulse outputs PO15 to PO8 are disabled
1	Pulse outputs PO15 to PO8 are enabled

NDERL

Bit	7	6	5	4	3	2	1	0
	NDER7	NDER6	NDER5	NDER4	NDER3	NDER2	NDER1	NDER0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Next Data Enable

0	Pulse outputs PO7 to PO0 are disabled
1	Pulse outputs PO7 to PO0 are enabled

PODRH

Bit	7	6	5	4	3	2	1	0
	POD15	POD14	POD13	POD12	POD11	POD10	POD9	POD8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Holds output data when pulse output is used

PODRL

Bit	7	6	5	4	3	2	1	0
	POD7	POD6	POD5	POD4	POD3	POD2	POD1	POD0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Holds output data when pulse output is used

Note: * A bit that has been set for pulse output in NDER is read-only.

1. When pulse output group output triggers are the same
   a. Address: H'FF4C

Bit	7	6	5	4	3	2	1	0
	NDR15	NDR14	NDR13	NDR12	NDR11	NDR10	NDR9	NDR8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Holds next data for pulse output groups 3 and 2

   b. Address: H'FF4E

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	1	1	1	1	1	1	1	1
Read/Write	—	—	—	—	—	—	—	—

2. When pulse output group output triggers are different
   a. Address: H'FF4C

Bit	7	6	5	4	3	2	1	0
	NDR15	NDR14	NDR13	NDR12	—	—	—	—
Initial value	0	0	0	0	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	—	—	—	—

Holds next data for pulse output group 3

   b. Address: H'FF4E

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	NDR11	NDR10	NDR9	NDR8
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Holds next data for pulse output group 2

1. When pulse output group output triggers are the same
   a. Address: H'FF4D

Bit	7	6	5	4	3	2	1	0
	NDR7	NDR6	NDR5	NDR4	NDR3	NDR2	NDR1	NDR0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Holds next data for pulse output groups 1 and 0

   b. Address: H'FF4F

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	1	1	1	1	1	1	1	1
Read/Write	—	—	—	—	—	—	—	—

2. When pulse output group output triggers are different
   a. Address: H'FF4D

Bit	7	6	5	4	3	2	1	0
	NDR7	NDR6	NDR5	NDR4	—	—	—	—
Initial value	0	0	0	0	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	—	—	—	—

Holds next data for pulse output group 1

   b. Address: H'FF4F

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	NDR3	NDR2	NDR1	NDR0
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Holds next data for pulse output group 0

PORT1—Port 1 Register **H'FF50** **Port 1**

Bit	7	6	5	4	3	2	1	0
	P17	P16	P15	P14	P13	P12	P11	P10
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

State of port 1 pins

Note: * Determined by the state of pins P17 to P10.

PORT2—Port 2 Register **H'FF51** **Port 2**

Bit	7	6	5	4	3	2	1	0
	P27	P26	P25	P24	P23	P22	P21	P20
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

State of port 2 pins

Note: * Determined by the state of pins P27 to P20.

PORT3—Port 3 Register **H'FF52** **Port 3**

Bit	7	6	5	4	3	2	1	0
	—	—	P35	P34	P33	P32	P31	P30
Initial value	0	0	—*	—*	—*	—*	—*	—*
Read/Write	—	—	R	R	R	R	R	R

State of port 3 pins

Note: * Determined by the state of pins P35 to P30.

PORT4—Port 4 Register **H'FF53** **Port 4**

Bit	7	6	5	4	3	2	1	0
	P47	P46	P45	P44	P43	P42	P41	P40
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

State of port 4 pins

Note: * Determined by the state of pins P47 to P40.

PORT5—Port 5 Register **H'FF54** **Port 5**

Bit	7	6	5	4	3	2	1	0
	P57	P56	P55	P54	P53	P52	P51	P50
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

State of port 5 pins

Note: * Determined by the state of pins P57 to P50.

PORT6—Port 6 Register **H'FF55** **Port 6**

Bit	7	6	5	4	3	2	1	0
	—	—	P65	P64	P63	P62	P61	P60
Initial value	0	0	—*	—*	—*	—*	—*	—*
Read/Write	—	—	R	R	R	R	R	R

State of port 6 pins

Note: * Determined by the state of pins P65 to P60.

PORT7—Port 7 Register **H'FF56** **Port 7**

Bit	7	6	5	4	3	2	1	0
	—	—	P75	P74	P73	P72	P71	P70
Initial value	0	0	—*	—*	—*	—*	—*	—*
Read/Write	—	—	R	R	R	R	R	R

State of port 7 pins

Note: * Determined by the state of pins P75 to P70.

PORT8—Port 8 Register **H'FF57** **Port 8**

Bit	7	6	5	4	3	2	1	0
	—	—	P85	P84	P83	P82	P81	P80
Initial value	0	0	—*	—*	—*	—*	—*	—*
Read/Write	—	—	R	R	R	R	R	R

State of port 8 pins

Note: * Determined by the state of pins P85 to P80.

PORTA—Port A Register **H'FF59** **Port A**

Bit	7	6	5	4	3	2	1	0
	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

State of port A pins

Note: * Determined by the state of pins PA7 to PA0.

PORTB—Port B Register **H'FF5A** **Port B**

Bit	7	6	5	4	3	2	1	0
	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

State of port B pins

Note: * Determined by the state of pins PB7 to PB0.

PORTC—Port C Register **H'FF5B** **Port C**

Bit	7	6	5	4	3	2	1	0
	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

State of port C pins

Note: * Determined by the state of pins PC7 to PC0.

PORTD—Port D Register **H'FF5C** **Port D**

Bit	7	6	5	4	3	2	1	0
	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

State of port D pins

Note: * Determined by the state of pins PD7 to PD0.

PORTE—Port E Register **H'FF5D** **Port E**

Bit	7	6	5	4	3	2	1	0
	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

State of port E pins

Note: * Determined by the state of pins PE7 to PE0.

PORTF—Port F Register **H'FF5E** **Port F**

Bit	7	6	5	4	3	2	1	0
	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
Initial value	—*	—*	—*	—*	—*	—*	—*	—*
Read/Write	R	R	R	R	R	R	R	R

State of port F pins

Note: * Determined by the state of pins PF7 to PF0.

PORTG—Port G Register **H'FF5F** **Port G**

Bit	7	6	5	4	3	2	1	0
	—	PG6	PG5	PG4	PG3	PG2	PG1	PG0
Initial value	Undefined	—*	—*	—*	—*	—*	—*	—*
Read/Write	—	R	R	R	R	R	R	R

State of port G pins

Note: * Determined by the state of pins PG6 to PG0.

P1DR—Port 1 Data Register **H'FF60** **Port 1**

Bit	7	6	5	4	3	2	1	0
	P17DR	P16DR	P15DR	P14DR	P13DR	P12DR	P11DR	P10DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port 1 pins (P17 to P10)

P2DR—Port 2 Data Register **H'FF61** **Port 2**

Bit	7	6	5	4	3	2	1	0
	P27DR	P26DR	P25DR	P24DR	P23DR	P22DR	P21DR	P20DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port 2 pins (P27 to P20)

P3DR—Port 3 Data Register **H'FF62** **Port 3**

Bit	7	6	5	4	3	2	1	0
	—	—	P35DR	P34DR	P33DR	P32DR	P31DR	P30DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Stores data for port 3 pins (P35 to P30)

P5DR—Port 5 Data Register **H'FF64** **Port 5**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	P53DR	P52DR	P51DR	P50DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Stores data for port 5 pins (P53 to P50)

P6DR—Port 6 Data Register **H'FF65** **Port 6**

Bit	7	6	5	4	3	2	1	0
	—	—	P65DR	P64DR	P63DR	P62DR	P61DR	P60DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port 6 pins (P65 to P60)

P7DR—Port 7 Data Register **H'FF66** **Port 7**

Bit	7	6	5	4	3	2	1	0
	—	—	P75DR	P74DR	P73DR	P72DR	P71DR	P70DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port 7 pins (P75 to P70)

P8DR—Port 8 Data Register **H'FF67** **Port 8**

Bit	7	6	5	4	3	2	1	0
	—	—	P85DR	P84DR	P83DR	P82DR	P81DR	P80DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port 8 pins (P85 to P80)

PADR—Port A Data Register **H'FF69** **Port A**

Bit	7	6	5	4	3	2	1	0
	PA7DR	PA6DR	PA5DR	PA4DR	PA3DR	PA2DR	PA1DR	PA0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port A pins (PA7 to PA0)

PBDR—Port B Data Register **H'FF6A** **Port B**

Bit	7	6	5	4	3	2	1	0
	PB7DR	PB6DR	PB5DR	PB4DR	PB3DR	PB2DR	PB1DR	PB0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port B pins (PB7 to PB0)

PCDR—Port C Data Register **H'FF6B** **Port C**

Bit	7	6	5	4	3	2	1	0
	PC7DR	PC6DR	PC5DR	PC4DR	PC3DR	PC2DR	PC1DR	PC0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port C pins (PC7 to PC0)

PDDR—Port D Data Register **H'FF6C** **Port D**

Bit	7	6	5	4	3	2	1	0
	PD7DR	PD6DR	PD5DR	PD4DR	PD3DR	PD2DR	PD1DR	PD0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port D pins (PD7 to PD0)

PEDR—Port E Data Register **H'FF6D** **Port E**

Bit	7	6	5	4	3	2	1	0
	PE7DR	PE6DR	PE5DR	PE4DR	PE3DR	PE2DR	PE1DR	PE0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port E pins (PE7 to PE0)

PFDR—Port F Data Register **H'FF6E** **Port F**

Bit	7	6	5	4	3	2	1	0
	PF7DR	PF6DR	PF5DR	PF4DR	PF3DR	PF2DR	PF1DR	PF0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port F pins (PF7 to PF0)

PGDR—Port G Data Register **H'FF6F** **Port G**

Bit	7	6	5	4	3	2	1	0
	—	PG6DR	PG5DR	PG4DR	PG3DR	PG2DR	PG1DR	PG0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores output data for port G pins (PG6 to PG0)

PORTH—Port H Register **H'FF70** **Port H**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	PH3	PH2	PH1	PH0
Initial value	Undefined	Undefined	Undefined	Undefined	—*	—*	—*	—*
Read/Write	—	—	—	—	R	R	R	R

State of port H pins

Note: * Determined by the state of pins PH3 to PH0.

PHDR—Port H Data Register **H'FF72** **Port H**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	PH3DR	PH2DR	PH1DR	PH0DR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Stores output data for port H pins (PH3 to PH0)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	PH3DDR	PH2DDR	PH1DDR	PH0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	W	W	W	W

Specify input or output for individual port H pins

Bit	7	6	5	4	3	2	1	0
	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

0	0	ø clock
	1	ø/4 clock
1	0	ø/16 clock
	1	ø/64 clock

Multiprocessor Mode

0	Multiprocessor function disabled
1	Multiprocessor format selected

Stop Bit Length

0	1 stop bit
1	2 stop bits

Parity Mode

0	Even parity
1	Odd parity

Parity Enable

0	Parity bit addition and checking disabled
1	Parity bit addition and checking enabled

Character Length

0	8-bit data
1	7-bit data*

Note: * When 7-bit data is selected, the MSB (bit 7) of TDR is not transmitted, and LSB-first/ MSB-first selection is not available.

Asynchronous Mode/Synchronous Mode Select

0	Asynchronous mode
1	Synchronous mode

Bit	7	6	5	4	3	2	1	0
	GM	BLK	PE	O/$\overline{E}$	BCP1	BCP0	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

0	0	ø clock
	1	ø/4 clock
1	0	ø/16 clock
	1	ø/64 clock

Basic Clock Pulse

BCP1	BCP0	Basic Clock Pulse
0	0	32 clock periods
	1	64 clock periods
1	0	372 clock periods
	1	256 clock periods

Parity Mode

0	Even parity
1	Odd parity

Parity Enable
(Set to 1 when using smart card interface)

0	Setting prohibited
1	Parity bit addition and checking enabled

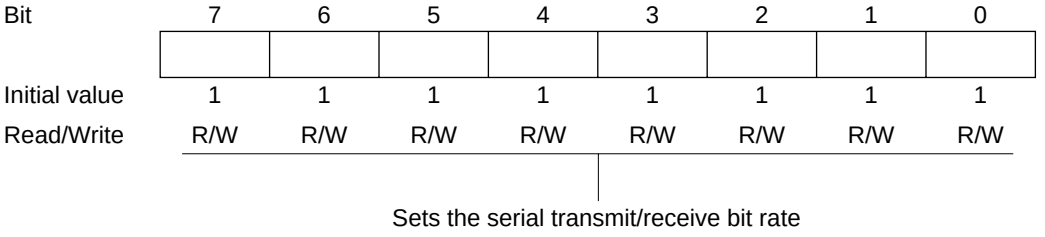
Block Transfer Mode Select

0	Normal smart card interface mode
1	Block transfer mode

GSM Mode

0	Normal smart card interface mode operation • TEND flag generation 12.5 etu after beginning of start bit (11.5 etu in block transfer mode) • Clock output on/off control only
1	GSM mode smart card interface mode operation • TEND flag generation 11.0 etu after beginning of start bit • High/low fixing control possible in addition to clock output on/off control (set by SCR)

Note: etu (Elementary Time Unit): Time for transfer of 1 bit



Note: For details see section 12.2.8, Bit Rate Register (BRR), in the H8S/2678 Series Hardware Manual.

Bit	7	6	5	4	3	2	1	0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Enable

0	0	Asynchronous mode	Internal clock/SCK pin functions as I/O port
		Synchronous mode	Internal clock/SCK pin functions as serial clock output
	1	Asynchronous mode	Internal clock/SCK pin functions as clock output*1
		Synchronous mode	Internal clock/SCK pin functions as serial clock output
1	0	Asynchronous mode	External clock/SCK pin functions as clock input*2
		Synchronous mode	External clock/SCK pin functions as serial clock input
	1	Asynchronous mode	External clock/SCK pin functions as clock input*2
		Synchronous mode	External clock/SCK pin functions as serial clock input

Notes: 1. Outputs a clock of the same frequency as the bit rate.
2. Inputs a clock with a frequency 16 times the bit rate.

Transmit-End Interrupt Enable

0	Transmit-end interrupt (TEI) request disabled
1	Transmit-end interrupt (TEI) request enabled

Multiprocessor Interrupt Enable

0	Multiprocessor interrupts disabled [Clearing conditions] • When the MPIE bit is cleared to 0 • When data with MPB = 1 is received
1	Multiprocessor interrupts enabled Receive interrupt (RXI) requests, receive-error interrupt (ERI) requests, and setting of the RDRF, FER, and ORER flags in SSR are disabled until data with the multiprocessor bit set to 1 is received

Receive Enable

0	Reception disabled
1	Reception enabled

Transmit Enable

0	Transmission disabled
1	Transmission enabled

Receive Interrupt Enable

0	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request disabled
1	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request enabled

Transmit Interrupt Enable

0	Transmit-data-empty interrupt (TXI) request disabled
1	Transmit-data-empty interrupt (TXI) request enabled

Bit	7	6	5	4	3	2	1	0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Enable
(In smart card interface mode, with bit 7 of SMR set to 1)

SCMR	SMR	SCR Setting		SCK Pin Function
SMIF	C/$\overline{A}$, GM	CKE1	CKE0	
0				See the SCI specification
1	0	0	0	Operates as port I/O pin
			1	Outputs clock as SCK output pin
	1		0	Operates as SCK output pin, with output fixed low
			1	Outputs clock as SCK output pin
		1	0	Operates as SCK output pin, with output fixed high
			1	Outputs clock as SCK output pin

Transmit-End Interrupt Enable

0	Transmit-end interrupt (TEI) request disabled
1	Transmit-end interrupt (TEI) request enabled

Multiprocessor Interrupt Enable

0	Multiprocessor interrupts disabled [Clearing conditions] • When the MPIE bit is cleared to 0 • When data with MPB = 1 is received
1	Multiprocessor interrupts enabled Receive interrupt (RXI) requests, receive-error interrupt (ERI) requests, and setting of the RDRF, FER, and ORER flags in SSR are disabled until data with the multiprocessor bit set to 1 is received

Receive Enable

0	Reception disabled
1	Reception enabled

Transmit Enable

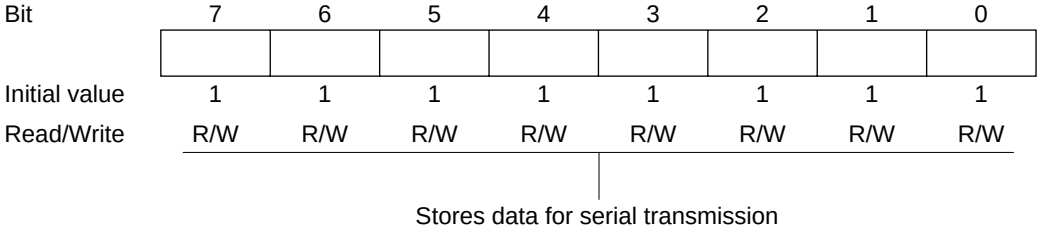
0	Transmission disabled
1	Transmission enabled

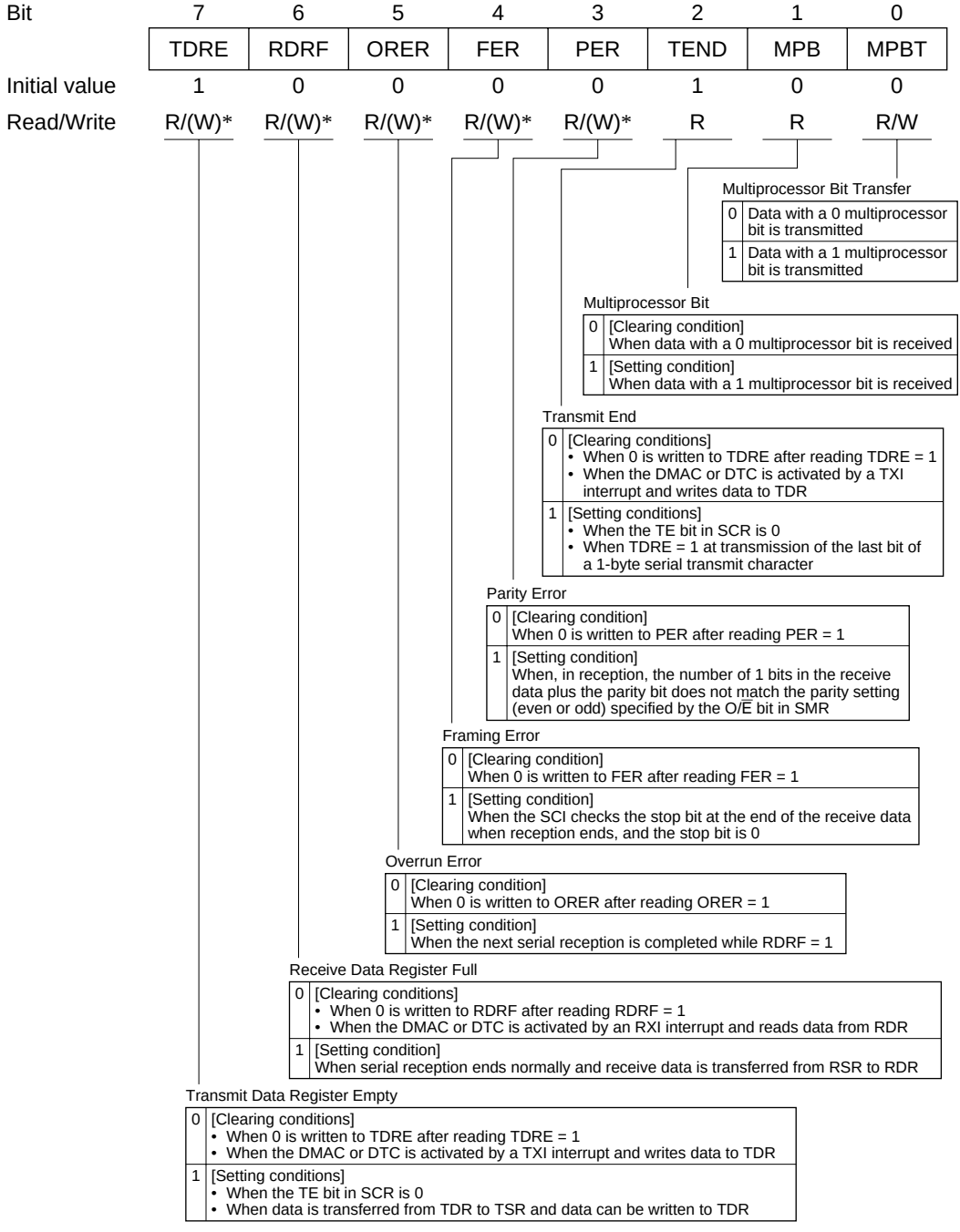
Receive Interrupt Enable

0	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request disabled
1	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request enabled

Transmit Interrupt Enable

0	Transmit-data-empty interrupt (TXI) request disabled
1	Transmit-data-empty interrupt (TXI) request enabled


Bit
7
6
5
4
3
2
1
0
Initial value
1
1
1
1
1
1
1
1
Read/Write
R/W
R/W
R/W
R/W
R/W
R/W
R/W
R/W
Stores data for serial transmission



Note: * Can only be written with 0, to clear the flag.

Bit	7	6	5	4	3	2	1	0
	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
Initial value	1	0	0	0	0	1	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Multiprocessor Bit Transfer

0	Data with a 0 multiprocessor bit is transmitted
1	Data with a 1 multiprocessor bit is transmitted

Multiprocessor Bit

0	[Clearing condition] When data with a 0 multiprocessor bit is received
1	[Setting condition] When data with a 1 multiprocessor bit is received

Transmit End

0	Transmission is in progress [Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DMAC or DTC is activated by a TXI interrupt and writes data to TDR
1	Transmission has ended [Setting conditions] • Upon reset, and in standby mode or module stop mode • When the TE bit in SCR is 0 and the ERS bit is also 0 • When TDRE = 1 ERS = 0 (normal transmission) 2.5 etu after transmission of a 1-byte serial character when GM = 0 and BLK = 0 • When TDRE = 1 ERS = 0 (normal transmission) 1.5 etu after transmission of a 1-byte serial character when GM = 0 and BLK = 1 • When TDRE = 1 ERS = 0 (normal transmission) 1.0 etu after transmission of a 1-byte serial character when GM = 1 and BLK = 0 • When TDRE = 1 ERS = 0 (normal transmission) 1.0 etu after transmission of a 1-byte serial character when GM = 1 and BLK = 1

Note: etu (Elementary Time Unit): Time for transfer of 1 bit

Parity Error

0	[Clearing condition] When 0 is written to PER after reading PER = 1
1	[Setting condition] When, in reception, the number of 1 bits in the receive data plus the parity bit does not match the parity setting (even or odd) specified by the O/$\overline{E}$ bit in SMR

Error Signal Status

0	Data received normally—no error signal [Clearing conditions] • Upon reset, and in standby mode or module stop mode • When 0 is written to ERS after reading ERS = 1
1	Error signal has been sent from receiving device, indicating parity error detection [Setting condition] When the low level of the error signal is sampled

Note: Clearing the TE bit in SCR to 0 does not affect the ERS flag, which retains its previous state.

Overrun Error

0	[Clearing condition] When 0 is written to ORER after reading ORER = 1
1	[Setting condition] When the next serial reception is completed while RDRF = 1

Receive Data Register Full

0	[Clearing conditions] • When 0 is written to RDRF after reading RDRF = 1 • When the DMAC or DTC is activated by an RXI interrupt and reads data from RDR
1	[Setting condition] When serial reception ends normally and receive data is transferred from RSR to RDR

Transmit Data Register Empty

0	[Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DMAC or DTC is activated by a TXI interrupt and writes data to TDR
1	[Setting conditions] • When the TE bit in SCR is 0 • When data is transferred from TDR to TSR and data can be written to TDR

Note: * Can only be written with 0, to clear the flag.

RDR0—Receive Data Register 0 **H'FF7D** **SCI0, Smart Card Interface 0**

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Stores received serial data

SCMR0—Smart Card Mode Register 0 **H'FF7E** **SCI0, Smart Card Interface 0**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	SDIR	SINV	—	SMIF
Initial value	1	1	1	1	0	0	1	0
Read/Write	—	—	—	—	R/W	R/W	—	R/W

Smart Card Interface Mode Select

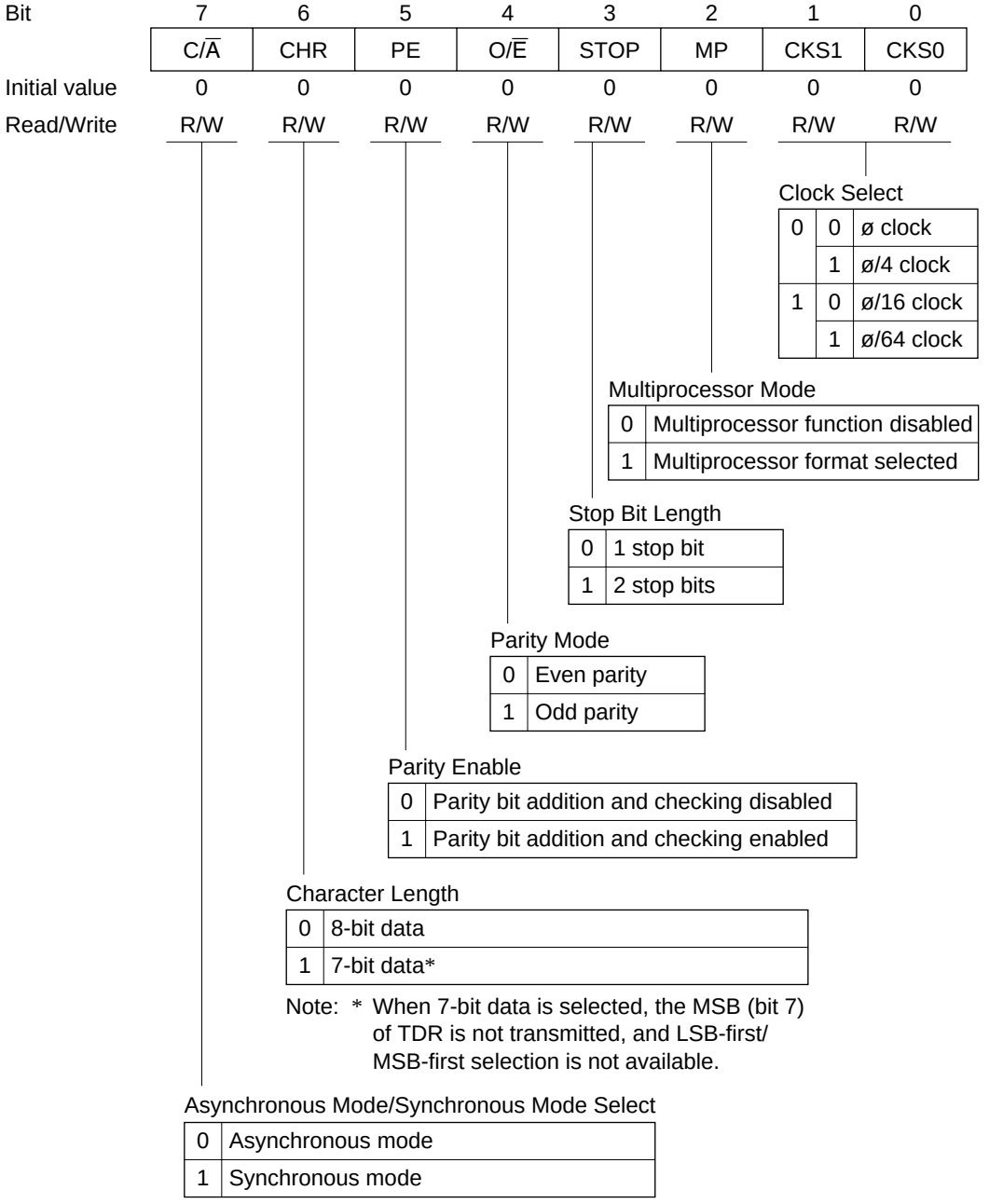
0	Smart card interface function is disabled
1	Smart card interface function is enabled

Data Invert

0	TDR contents are transmitted as they are Receive data is stored as it is in RDR
1	TDR contents are inverted before being transmitted Receive data is stored in inverted form in RDR

Data Direction

0	TDR contents are transmitted LSB-first Receive data is stored in RDR LSB-first
1	TDR contents are transmitted MSB-first Receive data is stored in RDR MSB-first


Bit
7
6
5
4
3
2
1
0
C/$\overline{A}$
CHR
PE
O/$\overline{E}$
STOP
MP
CKS1
CKS0
Initial value
0 0 0 0 0 0 0 0
Read/Write
R/W R/W R/W R/W R/W R/W R/W R/W
Clock Select
0 0 ø clock
1 ø/4 clock
1 0 ø/16 clock
1 ø/64 clock
Multiprocessor Mode
0 Multiprocessor function disabled
1 Multiprocessor format selected
Stop Bit Length
0 1 stop bit
1 2 stop bits
Parity Mode
0 Even parity
1 Odd parity
Parity Enable
0 Parity bit addition and checking disabled
1 Parity bit addition and checking enabled
Character Length
0 8-bit data
1 7-bit data*
Note: * When 7-bit data is selected, the MSB (bit 7) of TDR is not transmitted, and LSB-first/ MSB-first selection is not available.
Asynchronous Mode/Synchronous Mode Select
0 Asynchronous mode
1 Synchronous mode

Bit	7	6	5	4	3	2	1	0
	GM	BLK	PE	O/$\overline{E}$	BCP1	BCP0	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

0	0	ø clock
	1	ø/4 clock
1	0	ø/16 clock
	1	ø/64 clock

Basic Clock Pulse

BCP1	BCP0	Basic Clock Pulse
0	0	32 clock periods
	1	64 clock periods
1	0	372 clock periods
	1	256 clock periods

Parity Mode

0	Even parity
1	Odd parity

Parity Enable
(Set to 1 when using smart card interface)

0	Setting prohibited
1	Parity bit addition and checking enabled

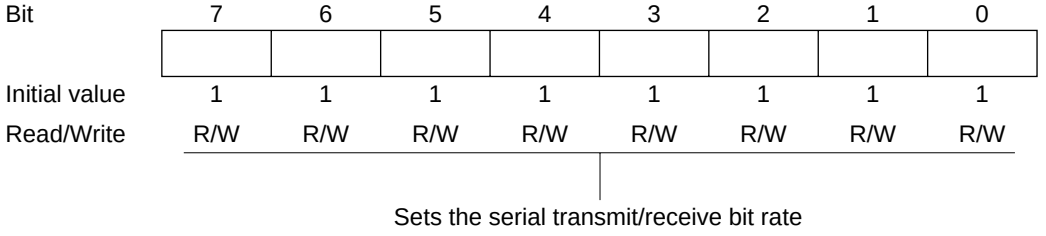
Block Transfer Mode Select

0	Normal smart card interface mode
1	Block transfer mode

GSM Mode

0	Normal smart card interface mode operation • TEND flag generation 12.5 etu after beginning of start bit (11.5 etu in block transfer mode) • Clock output on/off control only
1	GSM mode smart card interface mode operation • TEND flag generation 11.0 etu after beginning of start bit • High/low fixing control possible in addition to clock output on/off control (set by SCR)

Note: etu (Elementary Time Unit): Time for transfer of 1 bit



Note: For details see section 12.2.8, Bit Rate Register (BRR), in the H8S/2678 Series Hardware Manual.

Bit	7	6	5	4	3	2	1	0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Enable

0	0	Asynchronous mode	Internal clock/SCK pin functions as I/O port
		Synchronous mode	Internal clock/SCK pin functions as serial clock output
	1	Asynchronous mode	Internal clock/SCK pin functions as clock output*1
		Synchronous mode	Internal clock/SCK pin functions as serial clock output
1	0	Asynchronous mode	External clock/SCK pin functions as clock input*2
		Synchronous mode	External clock/SCK pin functions as serial clock input
	1	Asynchronous mode	External clock/SCK pin functions as clock input*2
		Synchronous mode	External clock/SCK pin functions as serial clock input

Notes: 1. Outputs a clock of the same frequency as the bit rate.
2. Inputs a clock with a frequency 16 times the bit rate.

Transmit-End Interrupt Enable

0	Transmit-end interrupt (TEI) request disabled
1	Transmit-end interrupt (TEI) request enabled

Multiprocessor Interrupt Enable

0	Multiprocessor interrupts disabled [Clearing conditions] • When the MPIE bit is cleared to 0 • When data with MPB = 1 is received
1	Multiprocessor interrupts enabled Receive interrupt (RXI) requests, receive-error interrupt (ERI) requests, and setting of the RDRF, FER, and ORER flags in SSR are disabled until data with the multiprocessor bit set to 1 is received

Receive Enable

0	Reception disabled
1	Reception enabled

Transmit Enable

0	Transmission disabled
1	Transmission enabled

Receive Interrupt Enable

0	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request disabled
1	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request enabled

Transmit Interrupt Enable

0	Transmit-data-empty interrupt (TXI) request disabled
1	Transmit-data-empty interrupt (TXI) request enabled

Bit	7	6	5	4	3	2	1	0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Enable
(In smart card interface mode, with bit 7 of SMR set to 1)

SCMR	SMR	SCR Setting		SCK Pin Function
SMIF	C/$\overline{A}$, GM	CKE1	CKE0	
0				See the SCI specification
1	0	0	0	Operates as port I/O pin
			1	Outputs clock as SCK output pin
	1		0	Operates as SCK output pin, with output fixed low
			1	Outputs clock as SCK output pin
		1	0	Operates as SCK output pin, with output fixed high
			1	Outputs clock as SCK output pin

Transmit-End Interrupt Enable

0	Transmit-end interrupt (TEI) request disabled
1	Transmit-end interrupt (TEI) request enabled

Multiprocessor Interrupt Enable

0	Multiprocessor interrupts disabled [Clearing conditions] • When the MPIE bit is cleared to 0 • When data with MPB = 1 is received
1	Multiprocessor interrupts enabled Receive interrupt (RXI) requests, receive-error interrupt (ERI) requests, and setting of the RDRF, FER, and ORER flags in SSR are disabled until data with the multiprocessor bit set to 1 is received

Receive Enable

0	Reception disabled
1	Reception enabled

Transmit Enable

0	Transmission disabled
1	Transmission enabled

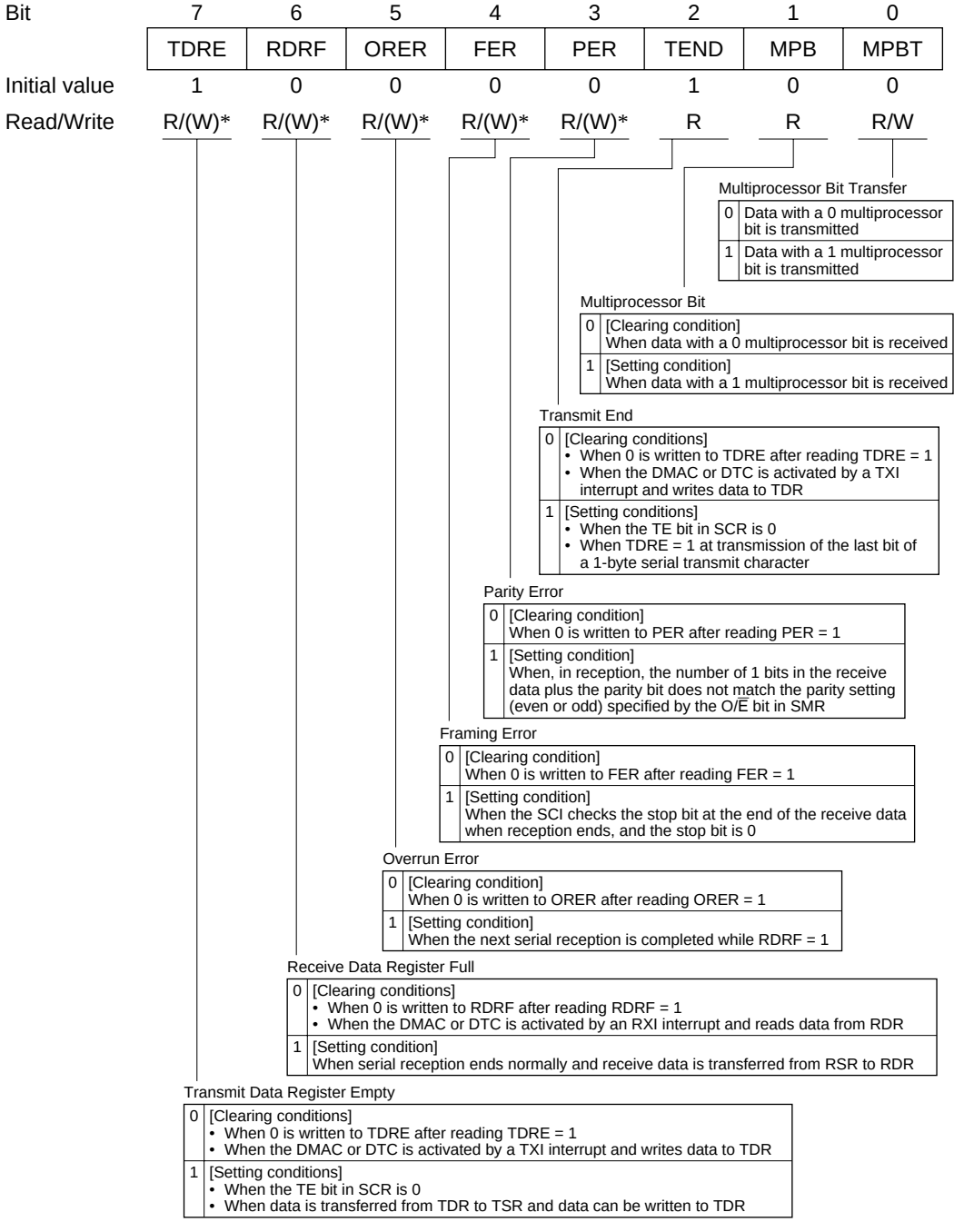
Receive Interrupt Enable

0	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request disabled
1	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request enabled

Transmit Interrupt Enable

0	Transmit-data-empty interrupt (TXI) request disabled
1	Transmit-data-empty interrupt (TXI) request enabled

Bit
7
6
5
4
3
2
1
0
Initial value
1
1
1
1
1
1
1
1
Read/Write
R/W
R/W
R/W
R/W
R/W
R/W
R/W
R/W
Stores data for serial transmission



Note: * Can only be written with 0, to clear the flag.

Bit	7	6	5	4	3	2	1	0
	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
Initial value	1	0	0	0	0	1	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Multiprocessor Bit Transfer

0	Data with a 0 multiprocessor bit is transmitted
1	Data with a 1 multiprocessor bit is transmitted

Multiprocessor Bit

0	[Clearing condition] When data with a 0 multiprocessor bit is received
1	[Setting condition] When data with a 1 multiprocessor bit is received

Transmit End

0	Transmission is in progress [Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DMAC or DTC is activated by a TXI interrupt and writes data to TDR
1	Transmission has ended [Setting conditions] • Upon reset, and in standby mode or module stop mode • When the TE bit in SCR is 0 and the ERS bit is also 0 • When TDRE = 1 ERS = 0 (normal transmission) 2.5 etu after transmission of a 1-byte serial character when GM = 0 and BLK = 0 • When TDRE = 1 ERS = 0 (normal transmission) 1.5 etu after transmission of a 1-byte serial character when GM = 0 and BLK = 1 • When TDRE = 1 ERS = 0 (normal transmission) 1.0 etu after transmission of a 1-byte serial character when GM = 1 and BLK = 0 • When TDRE = 1 ERS = 0 (normal transmission) 1.0 etu after transmission of a 1-byte serial character when GM = 1 and BLK = 1

Note: etu (Elementary Time Unit): Time for transfer of 1 bit

Parity Error

0	[Clearing condition] When 0 is written to PER after reading PER = 1
1	[Setting condition] When, in reception, the number of 1 bits in the receive data plus the parity bit does not match the parity setting (even or odd) specified by the O/$\overline{E}$ bit in SMR

Error Signal Status

0	Data received normally—no error signal [Clearing conditions] • Upon reset, and in standby mode or module stop mode • When 0 is written to ERS after reading ERS = 1
1	Error signal has been sent from receiving device, indicating parity error detection [Setting condition] When the low level of the error signal is sampled

Note: Clearing the TE bit in SCR to 0 does not affect the ERS flag, which retains its previous state.

Overrun Error

0	[Clearing condition] When 0 is written to ORER after reading ORER = 1
1	[Setting condition] When the next serial reception is completed while RDRF = 1

Receive Data Register Full

0	[Clearing conditions] • When 0 is written to RDRF after reading RDRF = 1 • When the DMAC or DTC is activated by an RXI interrupt and reads data from RDR
1	[Setting condition] When serial reception ends normally and receive data is transferred from RSR to RDR

Transmit Data Register Empty

0	[Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DMAC or DTC is activated by a TXI interrupt and writes data to TDR
1	[Setting conditions] • When the TE bit in SCR is 0 • When data is transferred from TDR to TSR and data can be written to TDR

Note: * Can only be written with 0, to clear the flag.

RDR1—Receive Data Register 1 **H'FF85** **SCI1, Smart Card Interface 1**

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Stores received serial data

SCMR1—Smart Card Mode Register 1 **H'FF86** **SCI1, Smart Card Interface 1**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	SDIR	SINV	—	SMIF
Initial value	1	1	1	1	0	0	1	0
Read/Write	—	—	—	—	R/W	R/W	—	R/W

Smart Card Interface Mode Select

0	Smart card interface function is disabled
1	Smart card interface function is enabled

Data Invert

0	TDR contents are transmitted as they are Receive data is stored as it is in RDR
1	TDR contents are inverted before being transmitted Receive data is stored in inverted form in RDR

Data Direction

0	TDR contents are transmitted LSB-first Receive data is stored in RDR LSB-first
1	TDR contents are transmitted MSB-first Receive data is stored in RDR MSB-first

Bit	7	6	5	4	3	2	1	0
	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

0	0	ø clock
	1	ø/4 clock
1	0	ø/16 clock
	1	ø/64 clock

Multiprocessor Mode

0	Multiprocessor function disabled
1	Multiprocessor format selected

Stop Bit Length

0	1 stop bit
1	2 stop bits

Parity Mode

0	Even parity
1	Odd parity

Parity Enable

0	Parity bit addition and checking disabled
1	Parity bit addition and checking enabled

Character Length

0	8-bit data
1	7-bit data*

Note: * When 7-bit data is selected, the MSB (bit 7) of TDR is not transmitted, and LSB-first/ MSB-first selection is not available.

Asynchronous Mode/Synchronous Mode Select

0	Asynchronous mode
1	Synchronous mode

Bit	7	6	5	4	3	2	1	0
	GM	BLK	PE	O/$\overline{E}$	BCP1	BCP0	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

0	0	ø clock
	1	ø/4 clock
1	0	ø/16 clock
	1	ø/64 clock

Basic Clock Pulse

BCP1	BCP0	Basic Clock Pulse
0	0	32 clock periods
	1	64 clock periods
1	0	372 clock periods
	1	256 clock periods

Parity Mode

0	Even parity
1	Odd parity

Parity Enable
(Set to 1 when using smart card interface)

0	Setting prohibited
1	Parity bit addition and checking enabled

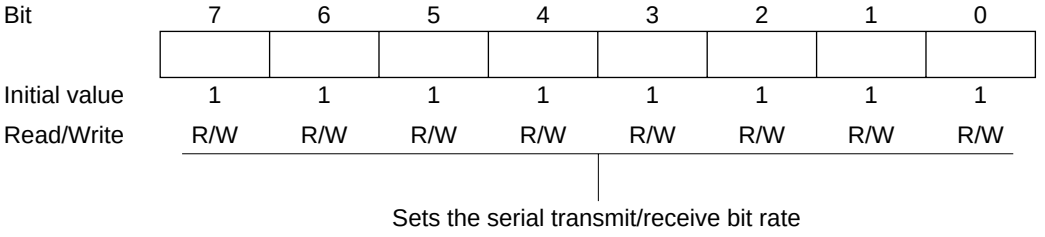
Block Transfer Mode Select

0	Normal smart card interface mode
1	Block transfer mode

GSM Mode

0	Normal smart card interface mode operation • TEND flag generation 12.5 etu after beginning of start bit (11.5 etu in block transfer mode) • Clock output on/off control only
1	GSM mode smart card interface mode operation • TEND flag generation 11.0 etu after beginning of start bit • High/low fixing control possible in addition to clock output on/off control (set by SCR)

Note: etu (Elementary Time Unit): Time for transfer of 1 bit



Note: For details see section 12.2.8, Bit Rate Register (BRR), in the H8S/2678 Series Hardware Manual.

Bit	7	6	5	4	3	2	1	0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Enable

0	0	Asynchronous mode	Internal clock/SCK pin functions as I/O port
		Synchronous mode	Internal clock/SCK pin functions as serial clock output
	1	Asynchronous mode	Internal clock/SCK pin functions as clock output*1
		Synchronous mode	Internal clock/SCK pin functions as serial clock output
1	0	Asynchronous mode	External clock/SCK pin functions as clock input*2
		Synchronous mode	External clock/SCK pin functions as serial clock input
	1	Asynchronous mode	External clock/SCK pin functions as clock input*2
		Synchronous mode	External clock/SCK pin functions as serial clock input

Notes: 1. Outputs a clock of the same frequency as the bit rate.
2. Inputs a clock with a frequency 16 times the bit rate.

Transmit-End Interrupt Enable

0	Transmit-end interrupt (TEI) request disabled
1	Transmit-end interrupt (TEI) request enabled

Multiprocessor Interrupt Enable

0	Multiprocessor interrupts disabled [Clearing conditions] • When the MPIE bit is cleared to 0 • When data with MPB = 1 is received
1	Multiprocessor interrupts enabled Receive interrupt (RXI) requests, receive-error interrupt (ERI) requests, and setting of the RDRF, FER, and ORER flags in SSR are disabled until data with the multiprocessor bit set to 1 is received

Receive Enable

0	Reception disabled
1	Reception enabled

Transmit Enable

0	Transmission disabled
1	Transmission enabled

Receive Interrupt Enable

0	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request disabled
1	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request enabled

Transmit Interrupt Enable

0	Transmit-data-empty interrupt (TXI) request disabled
1	Transmit-data-empty interrupt (TXI) request enabled

Bit	7	6	5	4	3	2	1	0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Enable
(In smart card interface mode, with bit 7 of SMR set to 1)

SCMR	SMR	SCR Setting		SCK Pin Function
SMIF	C/$\overline{A}$, GM	CKE1	CKE0	
0				See the SCI specification
1	0	0	0	Operates as port I/O pin
			1	Outputs clock as SCK output pin
	1		0	Operates as SCK output pin, with output fixed low
			1	Outputs clock as SCK output pin
		1	0	Operates as SCK output pin, with output fixed high
			1	Outputs clock as SCK output pin

Transmit-End Interrupt Enable

0	Transmit-end interrupt (TEI) request disabled
1	Transmit-end interrupt (TEI) request enabled

Multiprocessor Interrupt Enable

0	Multiprocessor interrupts disabled [Clearing conditions] • When the MPIE bit is cleared to 0 • When data with MPB = 1 is received
1	Multiprocessor interrupts enabled Receive interrupt (RXI) requests, receive-error interrupt (ERI) requests, and setting of the RDRF, FER, and ORER flags in SSR are disabled until data with the multiprocessor bit set to 1 is received

Receive Enable

0	Reception disabled
1	Reception enabled

Transmit Enable

0	Transmission disabled
1	Transmission enabled

Receive Interrupt Enable

0	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request disabled
1	Receive-data-full interrupt (RXI) request and receive-error interrupt (ERI) request enabled

Transmit Interrupt Enable

0	Transmit-data-empty interrupt (TXI) request disabled
1	Transmit-data-empty interrupt (TXI) request enabled

Bit
7
6
5
4
3
2
1
0
Initial value
1
1
1
1
1
1
1
1
Read/Write
R/W
R/W
R/W
R/W
R/W
R/W
R/W
R/W
Stores data for serial transmission

Bit	7	6	5	4	3	2	1	0
	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
Initial value	1	0	0	0	0	1	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Multiprocessor Bit Transfer

0	Data with a 0 multiprocessor bit is transmitted
1	Data with a 1 multiprocessor bit is transmitted

Multiprocessor Bit

0	[Clearing condition] When data with a 0 multiprocessor bit is received
1	[Setting condition] When data with a 1 multiprocessor bit is received

Transmit End

0	[Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DMAC or DTC is activated by a TXI interrupt and writes data to TDR
1	[Setting conditions] • When the TE bit in SCR is 0 • When TDRE = 1 at transmission of the last bit of a 1-byte serial transmit character

Parity Error

0	[Clearing condition] When 0 is written to PER after reading PER = 1
1	[Setting condition] When, in reception, the number of 1 bits in the receive data plus the parity bit does not match the parity setting (even or odd) specified by the O/$\overline{E}$ bit in SMR

Framing Error

0	[Clearing condition] When 0 is written to FER after reading FER = 1
1	[Setting condition] When the SCI checks the stop bit at the end of the receive data when reception ends, and the stop bit is 0

Overrun Error

0	[Clearing condition] When 0 is written to ORER after reading ORER = 1
1	[Setting condition] When the next serial reception is completed while RDRF = 1

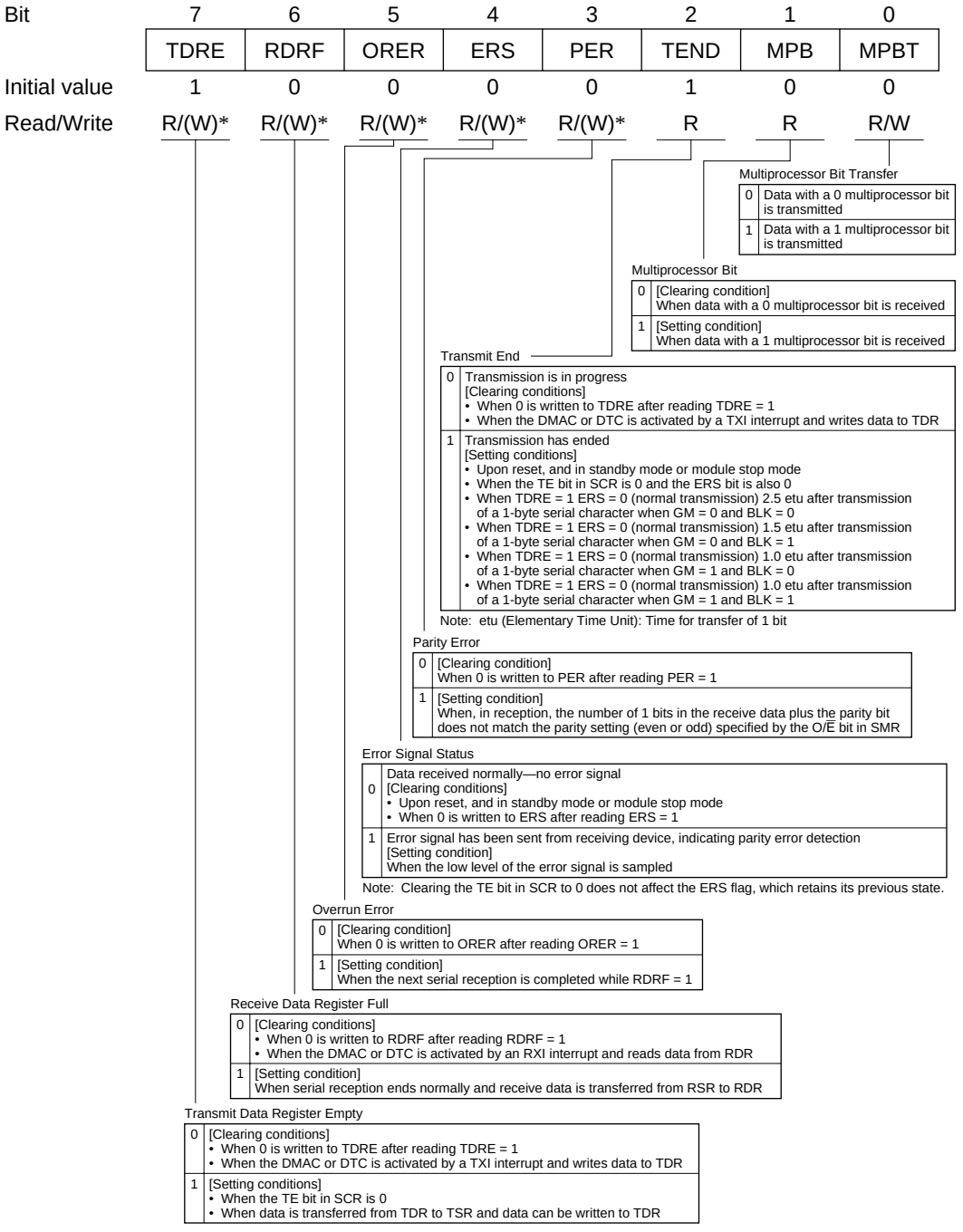
Receive Data Register Full

0	[Clearing conditions] • When 0 is written to RDRF after reading RDRF = 1 • When the DMAC or DTC is activated by an RXI interrupt and reads data from RDR
1	[Setting condition] When serial reception ends normally and receive data is transferred from RSR to RDR

Transmit Data Register Empty

0	[Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DMAC or DTC is activated by a TXI interrupt and writes data to TDR
1	[Setting conditions] • When the TE bit in SCR is 0 • When data is transferred from TDR to TSR and data can be written to TDR

Note: * Can only be written with 0, to clear the flag.



Note: * Can only be written with 0, to clear the flag.

RDR2—Receive Data Register 2 **H'FF8D** **SCI2, Smart Card Interface 2**

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Stores received serial data

SCMR2—Smart Card Mode Register 2 **H'FF8E** **SCI2, Smart Card Interface 2**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	SDIR	SINV	—	SMIF
Initial value	1	1	1	1	0	0	1	0
Read/Write	—	—	—	—	R/W	R/W	—	R/W

Smart Card Interface Mode Select

0	Smart card interface function is disabled
1	Smart card interface function is enabled

Data Invert

0	TDR contents are transmitted as they are Receive data is stored as it is in RDR
1	TDR contents are inverted before being transmitted Receive data is stored in inverted form in RDR

Data Direction

0	TDR contents are transmitted LSB-first Receive data is stored in RDR LSB-first
1	TDR contents are transmitted MSB-first Receive data is stored in RDR MSB-first

ADDRAH—A/D Data Register AH	**H'FF90**	**A/D Converter**
ADDRAL—A/D Data Register AL	**H'FF91**	**A/D Converter**
ADDRBH—A/D Data Register BH	**H'FF92**	**A/D Converter**
ADDRBL—A/D Data Register BL	**H'FF93**	**A/D Converter**
ADDRCH—A/D Data Register CH	**H'FF94**	**A/D Converter**
ADDRCL—A/D Data Register CL	**H'FF95**	**A/D Converter**
ADDRDH—A/D Data Register DH	**H'FF96**	**A/D Converter**
ADDRDL—A/D Data Register DL	**H'FF97**	**A/D Converter**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Stores the result of A/D conversion

Analog Input Channel				A/D Data Register
Channel Set 0 (CH3 = 1)		Channel Set 1 (CH3 = 0)		
Group 0	Group 1	Group 0	Group 1	
AN0	AN4	Setting prohibited	AN12	ADDRA
AN1	AN5	Setting prohibited	AN13	ADDRB
AN2	AN6	Setting prohibited	AN14	ADDRC
AN3	AN7	Setting prohibited	AN15	ADDRD

Bit	7	6	5	4	3	2	1	0
	ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W*	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Channel Select

Note: CH2, CH1, and CH0 are used in combination with bit 2 (CH3) in ADCR. See ADCR—A/D Control Register (H'FF99) for details.

Clock Select

Note: CKS is used in combination with bit 3 (CKS1) in ADCR. See ADCR—A/D Control Register (H'FF99) for details.

Scan Mode

0	Single mode
1	Scan mode

A/D Start

0	A/D conversion stopped
1	• Single mode: A/D conversion is started; cleared to 0 automatically when conversion ends • Scan mode: A/D conversion is started, and continues consecutively on the selected channels until ADST is cleared to 0 by software, a reset, or a transition to standby mode or module stop mode

A/D Interrupt Enable

0	A/D conversion end interrupt request disabled
1	A/D conversion end interrupt request enabled

A/D End Flag

0	[Clearing conditions] • When 0 is written to ADF after reading ADF = 1 • When the DTC is activated by an ADF interrupt and ADDR is read
1	[Setting conditions] • Single mode: When A/D conversion ends • Scan mode: When A/D conversion ends on all specified channels

Note: * Can only be written with 0, to clear the flag.

Bit	7	6	5	4	3	2	1	0
	TRGS1	TRGS0	—	—	CKS1	CH3	—	—
Initial value	0	0	1	1	1	1	1	1
Read/Write	R/W	R/W	—	—	R/W	R/W	—	—

Channel Select

Selects the analog input channel(s). Make the input channel setting when conversion is halted (ADST = 0).

Channel Selection				Description	
CH3	CH2*	CH1*	CH0*	Single Mode	Scan Mode
0	0	0	0	Setting prohibited	Setting prohibited
			1	Setting prohibited	Setting prohibited
		1	0	Setting prohibited	Setting prohibited
			1	Setting prohibited	Setting prohibited
	1	0	0	AN12	AN12
			1	AN13	AN12, AN13
		1	0	AN14	AN12 to AN14
			1	AN15	AN12 to AN15
1	0	0	0	AN0 (Initial value)	AN0
			1	AN1	AN0, AN1
		1	0	AN2	AN0 to AN2
			1	AN3	AN0 to AN3
	1	0	0	AN4	AN4
			1	AN5	AN4, AN5
		1	0	AN6	AN4 to AN6
			1	AN7	AN4 to AN7

Note: * CH2, CH1, and CH0 are bits in ADCSR.

Clock Select

Bit 3	ADCSR Bit 3	Description
CKS1	CKS	
0	0	Conversion time = 530 states (max.)
	1	Conversion time = 68 states (max.)
1	0	Conversion time = 266 states (max.) (Initial value)
	1	Conversion time = 134 states (max.)

Timer Trigger Select

TRGS1	TRGS0	Description
0	0	A/D conversion start by external trigger is disabled
	1	A/D conversion start by external trigger (TPU) is enabled
1	0	A/D conversion start by external trigger (8-bit timer) is enabled
	1	A/D conversion start by external trigger pin ($\overline{\text{ADTRG}}$) is enabled

DADR0—D/A Data Register 0 **H'FFA4** **D/A Converter**
DADR1—D/A Data Register 1 **H'FFA5** **D/A Converter**

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores data for D/A conversion

DACR01—D/A Control Register 01 **H'FFA6** **D/A Converter**

Bit	7	6	5	4	3	2	1	0
	DAOE1	DAOE0	DAE	—	—	—	—	—
Initial value	0	0	0	1	1	1	1	1
Read/Write	R/W	R/W	R/W	—	—	—	—	—

D/A Conversion Control

DAOE1	DAOE0	DAE	Description
0	0	*	Channel 0 and 1 D/A conversion disabled
	1	0	Channel 0 D/A conversion enabled
			Channel 1 D/A conversion disabled
		1	Channel 0 and 1 D/A conversion enabled
1	0	0	Channel 0 D/A conversion disabled
			Channel 1 D/A conversion enabled
		1	Channel 0 and 1 D/A conversion enabled
	1	*	Channel 0 and 1 D/A conversion enabled

*: Don't care

D/A Output Enable 0

0	DA0 analog output disabled
1	Channel 0 D/A conversion enabled. DA0 analog output enabled

D/A Output Enable 1

0	DA1 analog output disabled
1	Channel 1 D/A conversion enabled. DA1 analog output enabled

DADR2—D/A Data Register 2 **H'FFA8** **D/A Converter**
DADR3—D/A Data Register 3 **H'FFA9** **D/A Converter**

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores data for D/A conversion

DACR23—D/A Control Register 23 **H'FFAA** **D/A Converter**

Bit	7	6	5	4	3	2	1	0
	DAOE1	DAOE0	DAE	—	—	—	—	—
Initial value	0	0	0	1	1	1	1	1
Read/Write	R/W	R/W	R/W	—	—	—	—	—

D/A Conversion Control

DAOE1	DAOE	DAE	Description
0	0	*	Channel 2 and 3 D/A conversion disabled
	1	0	Channel 2 D/A conversion enabled
			Channel 3 D/A conversion disabled
		1	Channel 2 and 3 D/A conversion enabled
1	0	0	Channel 2 D/A conversion disabled
			Channel 3 D/A conversion enabled
		1	Channel 2 and 3 D/A conversion enabled
	1	*	Channel 2 and 3 D/A conversion enabled

*: Don't care

D/A Output Enable 0

0	DA2 analog output disabled
1	Channel 2 D/A conversion enabled. DA2 analog output enabled

D/A Output Enable 1

0	DA3 analog output disabled
1	Channel 3 D/A conversion enabled. DA3 analog output enabled

Bit	7	6	5	4	3	2	1	0
	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

0	0	0	Clock input disabled
		1	Internal clock: count at falling edge of ø/8
	1	0	Internal clock: count at falling edge of ø/64
		1	Internal clock: count at falling edge of ø/8192
1	0	0	For channel 0: Count at TCNT1 overflow signal* For channel 1: Count at TCNT0 compare match A
		1	External clock: count at rising edge
	1	0	External clock: count at falling edge
		1	External clock: count at both rising and falling edges

Note: * If the clock input of channel 0 is the TCNT1 overflow signal and that of channel 1 is the TCNT0 compare match signal, no incrementing clock is generated. Do not use this setting.

Counter Clear

0	0	Clearing is disabled
	1	Clear by compare match A
1	0	Clear by compare match B
	1	Clear by rising edge of external reset input

Timer Overflow Interrupt Enable

0	OVF interrupt request (OVI) is disabled
1	OVF interrupt request (OVI) is enabled

Compare Match Interrupt Enable A

0	CMFA interrupt request (CMIA) is disabled
1	CMFA interrupt request (CMIA) is enabled

Compare Match Interrupt Enable B

0	CMFB interrupt request (CMIB) is disabled
1	CMFB interrupt request (CMIB) is enabled

TCSR0	Bit	7	6	5	4	3	2	1	0
		CMFB	CMFA	OVF	ADTE	OS3	OS2	OS1	OS0
	Initial value	0	0	0	0	0	0	0	0
	Read/Write	R/(W)*	R/(W)*	R/(W)*	R/W	R/W	R/W	R/W	R/W

TCSR1	Bit	7	6	5	4	3	2	1	0
		CMFB	CMFA	OVF	—	OS3	OS2	OS1	OS0
	Initial value	0	0	0	1	0	0	0	0
	Read/Write	R/(W)*	R/(W)*	R/(W)*	—	R/W	R/W	R/W	R/W

Output Select

0	0	No change when compare match A occurs
	1	0 is output when compare match A occurs
1	0	1 is output when compare match A occurs
	1	Output is inverted when compare match A occurs (toggle output)

Output Select

0	0	No change when compare match B occurs
	1	0 is output when compare match B occurs
1	0	1 is output when compare match B occurs
	1	Output is inverted when compare match B occurs (toggle output)

A/D Trigger Enable (TCSR0 only)

0	A/D converter start requests by compare match A are disabled
1	A/D converter start requests by compare match A are enabled

Timer Overflow Flag

0	[Clearing condition] When 0 is written to OVF after reading OVF = 1
1	[Setting condition] When TCNT overflows (from H'FF to H'00)

Compare Match Flag A

0	[Clearing conditions] • When 0 is written to CMFA after reading CMFA = 1 • When the DTC is activated by a CMIA interrupt, and the DISEL bit in the DTC's MRB register is 0
1	[Setting condition] When TCNT = TCORA

Compare Match Flag B

0	[Clearing conditions] • When 0 is written to CMFB after reading CMFB = 1 • When the DTC is activated by a CMIB interrupt, and the DISEL bit in the DTC's MRB register is 0
1	[Setting condition] When TCNT = TCORB

Note: * Only 0 can be written to bits 7 to 5, to clear the flags.

TCORA0—Time Constant Register A0 **H'FFB4** **8-Bit Timer Channel 0**
TCORA1—Time Constant Register A1 **H'FFB5** **8-Bit Timer Channel 1**

	TCORA0								TCORA1							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TCORB0—Time Constant Register B0 **H'FFB6** **8-Bit Timer Channel 0**
TCORB1—Time Constant Register B1 **H'FFB7** **8-Bit Timer Channel 1**

	TCORB0								TCORB1							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TCNT0—Timer Counter 0 **H'FFB8** **8-Bit Timer Channel 0**
TCNT1—Timer Counter 1 **H'FFB9** **8-Bit Timer Channel 1**

	TCNT0								TCNT1							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	OVF	WT/$\overline{IT}$	TME	—	—	CKS2	CKS1	CKS0
Initial value	0	0	0	1	1	0	0	0
Read/Write	R/(W)*1	R/W	R/W	—	—	R/W	R/W	R/W

Clock Select

CKS2	CKS1	CKS0	Clock	Overflow Period* (when ø = 20 MHz)
0	0	0	ø/2 (Initial value)	25.6 µs
		1	ø/64	819.2 µs
	1	0	ø/128	1.6 ms
		1	ø/512	6.6 ms
1	0	0	ø/2048	26.2 ms
		1	ø/8192	104.9 ms
	1	0	ø/32768	419.4 ms
		1	ø/131072	1.68 s

Note: * The overflow period is the time from when TCNT starts counting up from H'00 until overflow occurs.

Timer Enable

0	TCNT is initialized to H'00 and halted
1	TCNT counts

Timer Mode Select

0	Interval timer mode: Sends the CPU an interval timer interrupt request (WOVI) when TCNT overflows
1	Watchdog timer mode: Outputs the $\overline{WDTOVF}$ signal*2 externally when TCNT overflows

Overflow Flag

0	[Clearing condition] When 0 is written to OVF after reading TCSR when OVF = 1
1	[Setting condition] When TCNT overflows (from H'FF to H'00) in interval timer mode. When internal reset requests are selected in watchdog timer mode, however, after being set OVF is cleared automatically by an internal reset.

The method for writing to TCSR is different from that for general registers to prevent accidental overwriting. For details see section 11.2.4, Notes on Register Access, in the H8S/2678 Series Hardware Manual.

Notes: 1. Can only be written with 0, to clear the flag.
2. The $\overline{WDTOVF}$ function is not available in the F-ZTAT version.

TCNT—Timer Counter **H'FFBC (W) H'FFBD (R)** **WDT**

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

RSTCSR—Reset Control/Status Register **H'FFBE (W) H'FFBF (R)** **WDT**

Bit	7	6	5	4	3	2	1	0
	WOVF	RSTE	—	—	—	—	—	—
Initial value	0	0	0	1	1	1	1	1
Read/Write	R/(W)*	R/W	R/W	—	—	—	—	—

Reserved bit
Writes to this bit are invalid.

Reset Enable

0	Internal reset is not performed when TCNT overflows*
1	Internal reset is performed when TCNT overflows

Note: * The chip is not initialized internally, but the TCNT and TCSR registers in the WDT are reset.

Watchdog Overflow Flag

0	[Clearing condition] When 0 is written to WOVF after reading TCSR when WOVF = 1
1	[Setting condition] When TCNT overflows (from H'FF to H'00) in watchdog timer mode

Notes: * Can only be written with 0, to clear the flag.

The method for writing to RSTCSR is different from that for general registers to prevent accidental overwriting. For details see section 11.2.4, Notes on Register Access, in the H8S/2678 Series Hardware Manual.

TSTR—Timer Start Register **H'FFC0** **TPU**

Bit	7	6	5	4	3	2	1	0
	—	—	CST5	CST4	CST3	CST2	CST1	CST0
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Counter start

0	TCNTn count operation is stopped
1	TCNTn performs count operation

(n = 5 to 0)

Note: If 0 is written to the CST bit during operation with the TIOC pin designated for output, the counter stops but the TIOC pin output compare output level is retained. If TIOR is written to when the CST bit is cleared to 0, the pin output level will be changed to the set initial output value.

TSYR—Timer Sync Register **H'FFC1** **TPU**

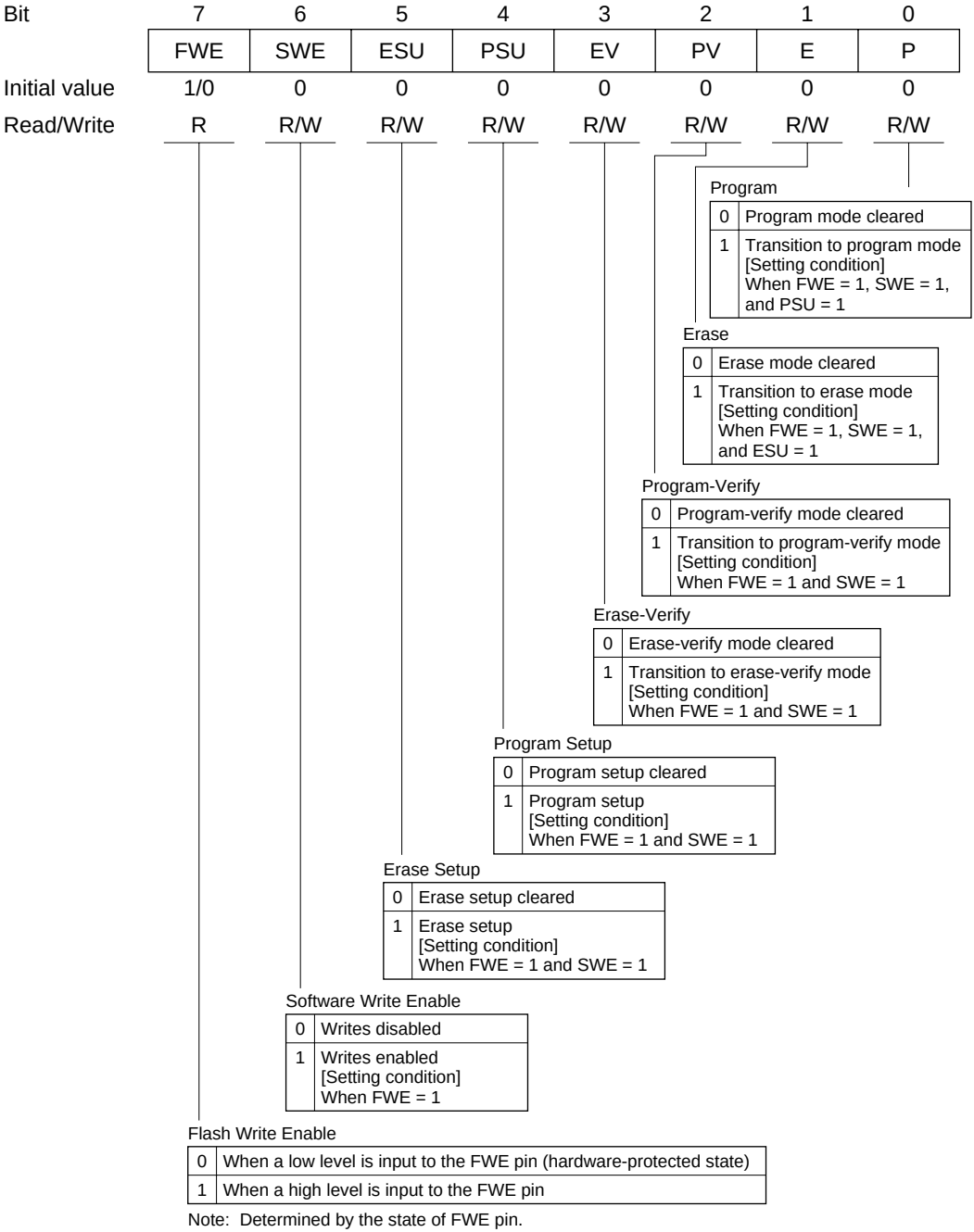
Bit	7	6	5	4	3	2	1	0
	—	—	SYNC5	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Timer Synchronization

0	TCNTn operates independently (TCNT presetting/clearing is unrelated to other channels)
1	TCNTn performs synchronous operation TCNT synchronous presetting[*1]/synchronous clearing[*2] is possible

(n = 5 to 0)

Notes: 1. To set synchronous operation, the SYNC bits for at least two channels must be set to 1.
2. To set synchronous clearing, in addition to the SYNC bit , the TCNT clearing source must also be set by means of bits CCLR2 to CCLR0 in TCR.



Note: Determined by the state of FWE pin.

FLMCR2—Flash Memory Control Register 2 **H'FFC9** **Flash Memory**
(F-ZTAT Version Only) — Preliminary —

Bit	7	6	5	4	3	2	1	0
	FLER	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Flash Memory Error

0	Flash memory is operating normally Flash memory program/erase protection (error protection) is disabled [Clearing condition] Power on reset or hardware standby mode
1	An error has occurred during flash memory programming/erasing Flash memory program/erase protection (error protection) is enabled [Setting condition] See section 18.10.3, Error Protection, in the H8S/2678 Series Hardware Manual.

EBR1—Erase Block Register 1 **H'FFCA** **Flash Memory**
EBR2—Erase Block Register 2 **H'FFCB** **Flash Memory**
(F-ZTAT Version Only) — Preliminary —

Bit	7	6	5	4	3	2	1	0
EBR1	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
EBR2	—	—	—	—	EB11	EB10	EB9	EB8
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Time Prescaler

0	0	0	Internal clock: count on ø/1
		1	Internal clock: count on ø/4
	1	0	Internal clock: count on ø/16
		1	Internal clock: count on ø/64
1	0	0	External clock: count on TCLKA pin input
		1	External clock: count on TCLKB pin input
	1	0	External clock: count on TCLKC pin input
		1	External clock: count on TCLKD pin input

Input Clock Edge Select

0	0	Count at rising edge
	1	Count at falling edge
1	—	Count at both edges

Counter Clear

0	0	0	TCNT clearing disabled
		1	TCNT cleared by TGRA compare match/input capture
	1	0	TCNT cleared by TGRB compare match/input capture
		1	TCNT cleared by counter clearing for another channel performing synchronous clearing/synchronous operation*1
1	0	0	TCNT clearing disabled
		1	TCNT cleared by TGRC compare match/input capture*2
	1	0	TCNT cleared by TGRD compare match/input capture*2
		1	TCNT cleared by counter clearing for another channel performing synchronous clearing/synchronous operation*1

Notes: 1. Synchronous operation is selected by setting the SYNC bit in TSYR to 1.
2. When TGRC or TGRD is used as a buffer register, TCNT is not cleared because the buffer register setting has priority, and compare match/input capture does not occur.

Bit	7	6	5	4	3	2	1	0
	—	—	BFB	BFA	MD3	MD2	MD1	MD0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Mode

0	0	0	0	Normal operation
			1	Reserved
		1	0	PWM mode 1
			1	PWM mode 2
	1	0	0	Phase counting mode 1
			1	Phase counting mode 2
		1	0	Phase counting mode 3
			1	Phase counting mode 4
1	*	*	*	—

*: Don't care

Notes: 1. MD3 is a reserved bit. In a write, it should always be written with 0.
2. Phase counting mode cannot be set for channels 0 and 3. In this case, 0 should always be written to MD2.

TGRA Buffer Operation

0	TGRA operates normally
1	TGRA and TGRC used together for buffer operation

TGRB Buffer Operation

0	TGRB operates normally
1	TGRB and TGRD used together for buffer operation

Bit	7	6	5	4	3	2	1	0
	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TGR0A I/O Control

0	0	0	0	TGR0A is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR0A is input capture register	Capture input source is TIOCA0 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is channel 1/count clock	Input capture at TCNT1 count-up/ count-down

*: Don't care

TGR0B I/O Control

0	0	0	0	TGR0B is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR0B is input capture register	Capture input source is TIOCB0 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is channel 1/count clock	Input capture at TCNT1 count-up/ count-down*1

*: Don't care

Note: 1. When bits TPSC2 to TPSC0 in TCR1 are set to B'000 and ø/1 is used as the TCNT1 count clock, this setting is invalid and input capture does not occur.

Bit	7	6	5	4	3	2	1	0
	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TGR0C I/O Control

0	0	0	0	TGR0C is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR0C is input capture register	Capture input source is TIOCC0 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is channel 1/count clock	Input capture at TCNT1 count-up/ count-down

*: Don't care

Note: When the BFA bit in TMDR0 is set to 1 and TGR0C is used as a buffer register, this setting is invalid and input capture/output compare does not occur.

TGR0D I/O Control

0	0	0	0	TGR0D is output compare register*2	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR0D is input capture register*2	Capture input source is TIOCD0 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is channel 1/count clock	Input capture at TCNT1 count-up/ count-down*1

*: Don't care

Notes: 1. When bits TPSC2 to TPSC0 in TCR1 are set to B'000 and ø/1 is used as the TCNT1 count clock, this setting is invalid and input capture does not occur.
2. When the BFB bit in TMDR0 is set to 1 and TGR0D is used as a buffer register, this setting is invalid and input capture does not occur.

Note: When TGRC or TGRD is designated for buffer operation, these settings are invalid and the register operates as a buffer register.

Bit	7	6	5	4	3	2	1	0
	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
Initial value	0	1	0	0	0	0	0	0
Read/Write	R/W	—	—	R/W	R/W	R/W	R/W	R/W

TGR Interrupt Enable A

0	Interrupt request (TGIA) by TGFA bit disabled
1	Interrupt request (TGIA) by TGFA bit enabled

TGR Interrupt Enable B

0	Interrupt request (TGIB) by TGFB bit disabled
1	Interrupt request (TGIB) by TGFB bit enabled

TGR Interrupt Enable C

0	Interrupt request (TGIC) by TGFC bit disabled
1	Interrupt request (TGIC) by TGFC bit enabled

TGR Interrupt Enable D

0	Interrupt request (TGID) by TGFD bit disabled
1	Interrupt request (TGID) by TGFD bit enabled

Overflow Interrupt Enable

0	Interrupt request (TCIV) by TCFV disabled
1	Interrupt request (TCIV) by TCFV enabled

A/D Conversion Start Request Enable

0	A/D conversion start request generation disabled
1	A/D conversion start request generation enabled

Bit	7	6	5	4	3	2	1	0
	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	—	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

TGRA Input Capture/Output Compare Flag

0	[Clearing conditions] • When DTC is activated by TGIA interrupt and DISEL bit in DTC's MRB register is 0 • When DMAC is activated by TGIA interrupt and DTA bit in DMAC's DMABCR register is 1 • When 0 is written to TGFA after reading TGFA = 1
1	[Setting conditions] • When TCNT = TGRA while TGRA is functioning as output compare register • When TCNT value is transferred to TGRA by input capture signal while TGRA is functioning as input capture register

TGRB Input Capture/Output Compare Flag

0	[Clearing conditions] • When DTC is activated by TGIB interrupt and DISEL bit in DTC's MRB register is 0 • When 0 is written to TGFB after reading TGFB = 1
1	[Setting conditions] • When TCNT = TGRB while TGRB is functioning as output compare register • When TCNT value is transferred to TGRB by input capture signal while TGRB is functioning as input capture register

TGRC Input Capture/Output Compare Flag

0	[Clearing conditions] • When DTC is activated by TGIC interrupt and DISEL bit in DTC's MRB register is 0 • When 0 is written to TGFC after reading TGFC = 1
1	[Setting conditions] • When TCNT = TGRC while TGRC is functioning as output compare register • When TCNT value is transferred to TGRC by input capture signal while TGRC is functioning as input capture register

TGRD Input Capture/Output Compare Flag

0	[Clearing conditions] • When DTC is activated by TGID interrupt and DISEL bit in DTC's MRB register is 0 • When 0 is written to TGFD after reading TGFD = 1
1	[Setting conditions] • When TCNT = TGRD while TGRD is functioning as output compare register • When TCNT value is transferred to TGRD by input capture signal while TGRD is functioning as input capture register

Overflow Flag

0	[Clearing condition] When 0 is written to TCFV after reading TCFV = 1
1	[Setting condition] When the TCNT value overflows (from H'FFFF to H'0000)

Note: * Can only be written with 0, to clear the flag.

TCNT0—Timer Counter 0 **H'FFD6** **TPU0**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Up-counter

TGR0A—Timer General Register 0A **H'FFD8** **TPU0**
TGR0B—Timer General Register 0B **H'FFDA** **TPU0**
TGR0C—Timer General Register 0C **H'FFDC** **TPU0**
TGR0D—Timer General Register 0D **H'FFDE** **TPU0**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Time Prescaler

0	0	0	Internal clock: count on ø/1
		1	Internal clock: count on ø/4
	1	0	Internal clock: count on ø/16
		1	Internal clock: count on ø/64
1	0	0	External clock: count on TCLKA pin input
		1	External clock: count on TCLKB pin input
	1	0	Internal clock: count on ø/256
		1	Count on TCNT2 overflow/underflow

Note: This setting is invalid when channel 1 is in phase counting mode.

Clock Edge

0	0	Count at rising edge
	1	Count at falling edge
1	—*	Count at both edges

Note: * This setting is invalid when channel 1 is in phase counting mode.

Counter Clear

0	0	TCNT clearing disabled
	1	TCNT cleared by TGRA compare match/input capture
1	0	TCNT cleared by TGRB compare match/input capture
	1	TCNT cleared by counter clearing for another channel performing synchronous clearing/synchronous operation*

Note: * Synchronous operation is selected by setting the SYNC bit in TSYR to 1.

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	MD3	MD2	MD1	MD0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Mode

0	0	0	0	Normal operation
			1	Reserved
		1	0	PWM mode 1
			1	PWM mode 2
	1	0	0	Phase counting mode 1
			1	Phase counting mode 2
		1	0	Phase counting mode 3
			1	Phase counting mode 4
1	*	*	*	—

*: Don't care

Note: MD3 is a reserved bit. In a write, it should always be written with 0.

Bit	7	6	5	4	3	2	1	0
	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TGR1A I/O Control

0	0	0	0	TGR1A is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR1A is input capture register	Capture input source is TIOCA4 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is TGR0A compare match/ input capture	Input capture at generation of channel 0/TGR0A compare match/ input capture

*: Don't care

TGR1B I/O Control

0	0	0	0	TGR1B is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR1B is input capture register	Capture input source is TIOCB1 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is TGR0C compare match/ input capture	Input capture at generation of TGR0C compare match/ input capture

*: Don't care

Bit	7	6	5	4	3	2	1	0
	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
Initial value	0	1	0	0	0	0	0	0
Read/Write	R/W	—	R/W	R/W	—	—	R/W	R/W

TGR Interrupt Enable A

0	Interrupt request (TGIA) by TGFA bit disabled
1	Interrupt request (TGIA) by TGFA bit enabled

TGR Interrupt Enable B

0	Interrupt request (TGIB) by TGFB bit disabled
1	Interrupt request (TGIB) by TGFB bit enabled

Overflow Interrupt Enable

0	Interrupt request (TCIV) by TCFV disabled
1	Interrupt request (TCIV) by TCFV enabled

Underflow Interrupt Enable

0	Interrupt request (TCIU) by TCFU disabled
1	Interrupt request (TCIU) by TCFU enabled

A/D Conversion Start Request Enable

0	A/D conversion start request generation disabled
1	A/D conversion start request generation enabled

Bit	7	6	5	4	3	2	1	0
	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
Initial value	1	1	0	0	0	0	0	0
Read/Write	R	—	R/(W)*	R/(W)*	—	—	R/(W)*	R/(W)*

TGRA Input Capture/Output Compare Flag

0	[Clearing conditions] • When DTC is activated by TGIA interrupt and DISEL bit in DTC's MRB register is 0 • When DMAC is activated by TGIA interrupt and DTA bit in DMAC's DMABCR register is 1 • When 0 is written to TGFA after reading
1	[Setting conditions] • When TCNT = TGRA while TGRA is functioning as output compare register • When TCNT value is transferred to TGRA by input capture signal while TGRA is functioning as input capture register

TGRB Input Capture/Output Compare Flag

0	[Clearing conditions] • When DTC is activated by TGIB interrupt and DISEL bit in DTC's MRB register is 0 • When 0 is written to TGFB after reading TGFB = 1
1	[Setting conditions] • When TCNT = TGRB while TGRB is functioning as output compare register • When TCNT value is transferred to TGRB by input capture signal while TGRB is functioning as input capture register

Overflow Flag

0	[Clearing condition] When 0 is written to TCFV after reading TCFV = 1
1	[Setting condition] When the TCNT value overflows (from H'FFFF to H'0000)

Underflow Flag

0	[Clearing condition] When 0 is written to TCFU after reading TCFU = 1
1	[Setting condition] When the TCNT value underflows (from H'0000 to H'FFFF)

Count Direction Flag

0	TCNT counts down
1	TCNT counts up

Note: * Can only be written with 0, to clear the flag.

TCNT1—Timer Counter 1 **H'FFE6** **TPU1**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Up/down-counter*

Note: * This timer counter can be used as an up/down-counter only in phase counting mode or when performing overflow/underflow counting on another channel. In other cases it functions as an up-counter.

TGR1A—Timer General Register 1A **H'FFE8** **TPU1**
TGR1B—Timer General Register 1B **H'FFEA** **TPU1**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Time Prescaler

0	0	0	Internal clock: count on ø/1
		1	Internal clock: count on ø/4
	1	0	Internal clock: count on ø/16
		1	Internal clock: count on ø/64
1	0	0	External clock: count on TCLKA pin input
		1	External clock: count on TCLKB pin input
	1	0	External clock: count on TCLKC pin input
		1	Internal clock: count on ø/1024

Note: This setting is invalid when channel 2 is in phase counting mode.

Clock Edge

0	0	Count at rising edge
	1	Count at falling edge
1	—*	Count at both edges

Note: * This setting is invalid when channel 2 is in phase counting mode.

Counter Clear

0	0	TCNT clearing disabled
	1	TCNT cleared by TGRA compare match/input capture
1	0	TCNT cleared by TGRB compare match/input capture
	1	TCNT cleared by counter clearing for another channel performing synchronous clearing/synchronous operation*

Note: * Synchronous operation is selected by setting the SYNC bit in TSYR to 1.

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	MD3	MD2	MD1	MD0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Mode

0	0	0	0	Normal operation
			1	Reserved
		1	0	PWM mode 1
			1	PWM mode 2
	1	0	0	Phase counting mode 1
			1	Phase counting mode 2
		1	0	Phase counting mode 3
			1	Phase counting mode 4
1	*	*	*	—

*: Don't care

Note: MD3 is a reserved bit. In a write, it should always be written with 0.

Bit	7	6	5	4	3	2	1	0
	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TGR2A I/O Control

0	0	0	0	TGR2A is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	*	0	0	TGR2A is input capture register	Capture input source is TIOCA2 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges

*: Don't care

TGR2B I/O Control

0	0	0	0	TGR2B is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	*	0	0	TGR2B is input capture register	Capture input source is TIOCB2 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges

*: Don't care

Bit	7	6	5	4	3	2	1	0
	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
Initial value	0	1	0	0	0	0	0	0
Read/Write	R/W	—	R/W	R/W	—	—	R/W	R/W

TGR Interrupt Enable A

0	Interrupt request (TGIA) by TGFA bit disabled
1	Interrupt request (TGIA) by TGFA bit enabled

TGR Interrupt Enable B

0	Interrupt request (TGIB) by TGFB bit disabled
1	Interrupt request (TGIB) by TGFB bit enabled

Overflow Interrupt Enable

0	Interrupt request (TCIV) by TCFV disabled
1	Interrupt request (TCIV) by TCFV enabled

Underflow Interrupt Enable

0	Interrupt request (TCIU) by TCFU disabled
1	Interrupt request (TCIU) by TCFU enabled

A/D Conversion Start Request Enable

0	A/D conversion start request generation disabled
1	A/D conversion start request generation enabled

Bit	7	6	5	4	3	2	1	0
	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
Initial value	1	1	0	0	0	0	0	0
Read/Write	R	—	R/(W)*	R/(W)*	—	—	R/(W)*	R/(W)*

TGRA Input Capture/Output Compare Flag

0	[Clearing conditions] • When DTC is activated by TGIA interrupt and DISEL bit in DTC's MRB register is 0 • When DMAC is activated by TGIA interrupt and DTA bit in DMAC's DMABCR register is 1 • When 0 is written to TGFA after reading
1	[Setting conditions] • When TCNT = TGRA while TGRA is functioning as output compare register • When TCNT value is transferred to TGRA by input capture signal while TGRA is functioning as input capture register

TGRB Input Capture/Output Compare Flag

0	[Clearing conditions] • When DTC is activated by TGIB interrupt and DISEL bit in DTC's MRB register is 0 • When 0 is written to TGFB after reading TGFB = 1
1	[Setting conditions] • When TCNT = TGRB while TGRB is functioning as output compare register • When TCNT value is transferred to TGRB by input capture signal while TGRB is functioning as input capture register

Overflow Flag

0	[Clearing condition] When 0 is written to TCFV after reading TCFV = 1
1	[Setting condition] When the TCNT value overflows (from H'FFFF to H'0000)

Underflow Flag

0	[Clearing condition] When 0 is written to TCFU after reading TCFU = 1
1	[Setting condition] When the TCNT value underflows (from H'0000 to H'FFFF)

Count Direction Flag

0	TCNT counts down
1	TCNT counts up

Note: * Can only be written with 0, to clear the flag.

TCNT2—Timer Counter 2 **H'FFF6** **TPU2**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Up/down-counter*

Note: * This timer counter can be used as an up/down-counter only in phase counting mode or when performing overflow/underflow counting on another channel. In other cases it functions as an up-counter.

TGR2A—Timer General Register 2A **H'FFF8** **TPU2**
TGR2B—Timer General Register 2B **H'FFFA** **TPU2**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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