May 1997

PCE 8300H

family PC Embedded in-circuit emulators

HITACHI

FEATURES

- Real-time in-circuit emulation of H8/300H Series microcontrollers up to 16mHz @ 5v from 13MHz @ 3.3.v.
- Parallel Connection to IBM ISA BUS (compatible) for fast data transfer using shared memory.
- 2Mbyte (no wait state) User memory resident on board, 1 Mbyte fixed and 1Mbyte relocatable in four 256kbyte blocks.
- Real-time trace, operational as a “rolling window” or as or as “address switchable”.
- Complex breakpoint operation.
- PCE3048F supports Flash EPROM emulation (in-circuit or stand alone).
- CIDE Windows Graphical User Interface, with:
  - easy to use menu & toolbar interface.
  - extensive window specific pop-up local menus.
  - comprehensive C debugging with watchpoints and local variable windows.
  - full access to all emulator hardware features.
- Conforms to European Electromagnetic Compatibility Directive (89/336/EEC) with metal lid (must be removed for connection to user’s target).

INTRODUCTION

The PCE8300H range of real-time, in-circuit emulators can be used for system development and debugging of H8/300H microcontroller family applications. The PCE300H emulators form part of the range of PC-based support tools for the H-Series microcontrollers, and are designed with the aim of providing a high level of performance for minimum cost.

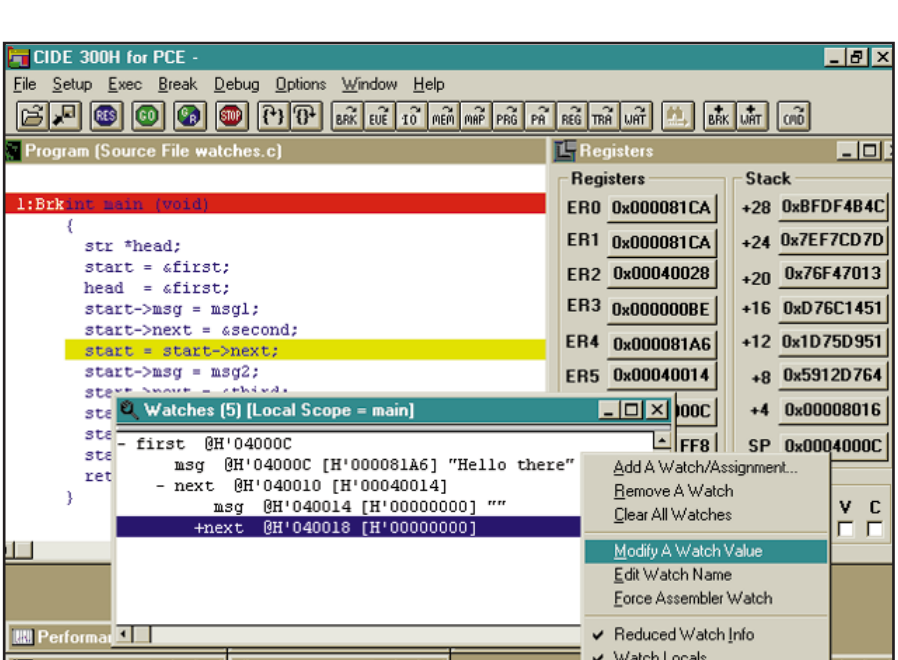
CIDE - C Integrated Debugging Environment

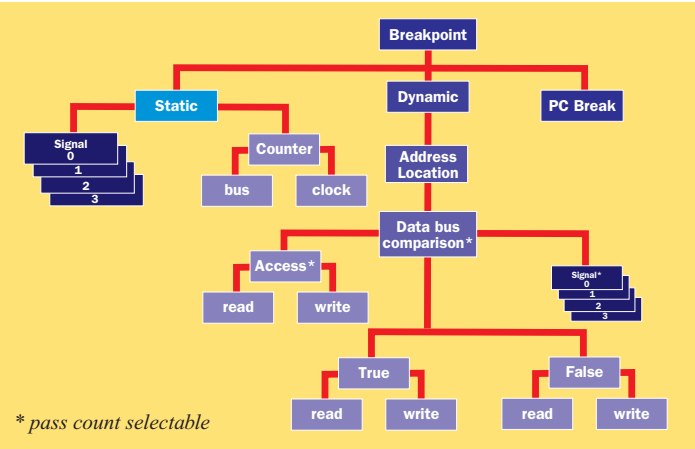
CIDE is the graphical user interface for the PCE8300H. It has an easy to learn standard Windows look and feel - with multiple windows, menus and a toolbar - yet provides full control of all emulator hardware features. Quick access to window-specific commands is provided by local pop-up menus containing commands relevant to that window’s function.

C, assembler and mixed code can be displayed in the program window and additional windows show watchpoints and local variables.

Installation is simplified with a setup program for the software and a configuration utility for the hardware.

An enhanced version of CIDE is available separately to support Hitachi OS, with windows to display task status and resources (mailboxes/semaphores/event flags/memory pools).





SPECIFICATIONS

Clock

User selectable 16,10, 8 or 5MHz, or target clock up to 16MHz, or external source clock up to 16MHz.

Memory Size

2Mbyte of emulation RAM (internal), target system (User), write protected or defined as not existing (guarded). Memory mapping is resolved to 32 word blocks.

Breakpoints

A complex breakpoint system allows a variety of conditions to be set up which, if encountered will cause emulation to halt. Three types of breakpoint are supported.

Dynamic Breakpoints

Dynamic Breakpoints are activated by a condition on an access (read or write) to a certain address and can be qualified by either

i) Nothing
ii) 8 bit compare (true/false)
iii) 16 bit compare (true/false)
iv) One of 4 external probe signals (2 high level, 2 low level)

A pass count can be specified to a dynamic breakpoint. There are two 16 bit counters and and two 16 bit comparators available to all the breakpoint logic. These enable complex pass counted breakpoint operations, e.g. to be set within nested loops.

Dynamic Breakpoint coverage is limited to 1Mbyte area fixed from H'000000 in word boundaries, and four relocatable 256Kbyte areas configurable within the possible 16Mbyte address range.

Program Counter Breakpoints

Program counter breakpoints are used on OP-code reads and halt the program if the op-code would have been executed. Program counter breakpoints cover the whole 16Mbyte address range for word access. These can also be set within ROM areas even on a target system.

Static Breakpoints

Only one static breakpoint can be set. Program execution is halted after a specified number of bus or clock cycles, or on the unconditional occurrence of an external Probe Signal.

Dynamic and Static Breakpoints can be given a priority level:
Always - causes a halt as soon as condition is met. (Default).
Level 1 - will not cause a program halt but is used to qualify a level breakpoint.
Level 2 - causes a program halt if a level 1 has already been detected.
Any level 1 breakpoint can qualify a level 2 breakpoint if more than one level 1 breakpoint is set.
Program execution can also be halted if an access to a guarded area is detected or a write cycle to a write protected location occurs. These breakpoints can be ignored if required.

Real-Time Trace

The PCE8300H trace facility allows examination of the processor activity prior to program execution being terminated. Up to 32K bus cycles can be stored, either as a "rolling buffer" where the last 32K cycles are stored, or "address selectable" which can be used for tracing subroutines and procedures. The traced signals include the address and the data buses along with processor status/control signals and the user probe signals. The trace buffer is displayed as raw unprocessed data and as disassembled instructions incorporating any defined signals.

Symbolic

Full symbolic debugging is possible with all relevant commands accepting symbol entries including the line assembler and disassembler option.

PCE3048F F-ZTAT Flash Support

The PCE3048F has support for the FLASH emulation either in-circuit, or stand-alone.

The new features include:

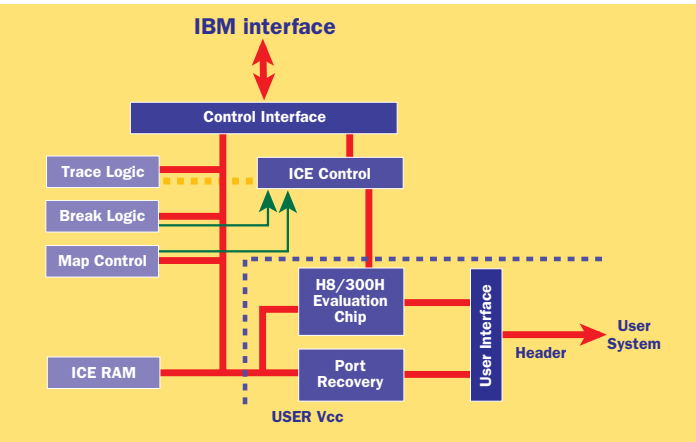
- Run-time emulation of FLASH (i.e. acts as H8/3048F would in the circuit)
- Direct control entry into BOOT mode without needing external circuitry.
- Direct control and entry into USER mode without needing external circuitry
- RS-232 port supplied which may be electronically connected to the BOOT SCI port to allow testing of download programs without needing external circuitry.

Host Interface

A small PC Interface Card plugs into a standard PC compatible ISA card slot and provides an 8-bit parallel interface to the IBM Bus. This is connected to the main PCE board via a ribbon cable. The PC/PCE Interface consists of a DPRAM that sits in the PC memory map and will operate as a swing buffer facilitating fast program transfer. The PCE address range is address selectable so as not to conflict with other cards the User may already be using. Power is supplied from the PC so no auxiliary power supply is necessary.

Other Features

- Full circuit protection when connected to User hardware.
- Regulator circuit for 3.3v target operation.
- Durable target cable.
- Run time clock giving emulation time (accuracy 0.25µS to 8.4 days).
- Oscilloscope trigger facility.
- Batch file execution.
- Session logging.
- Limited performance analysis.



	Product Code	Processors Supported
Emulator	PCE3003	H8/3001,2,3,4,5, H8/3030,1,2, H8/3040,1,2
	PCE3048	H8/3040,1,2, H8/3044,7,8 H8/3020,1,2
	PCE3048F*	H8/3030,1,2, H8/3040,1,2 H8/3044,5,7,8, H8/3048F

*Available Q3/97

	Product Code	Device	Footprint
Target Connection	PHB300HQ100A	H8/3042	QFP100A
	PHB300HQ100B	H8/3002 H8/3048	QFP100B
	PHB300HQ112	H8/3003	QFP112
	PHB300HQ80A1	H8/3001	QFP80A
	PHB300HQ80A2	H8/3032	QFP80A
	PHB300HQ80A3	H8/3003	QFP80A3
	PHB300HT80C1	H8/3001	TQFP80C
	PHB300HT80C2	H8/3032	TQFP80C
	PHB300HT80C3	H8/3003	TQFP80C3

POWER 5v @ 3A Volts from PC power supply (with no target hardware).
3.3v derived from regulator or external PSU.

SIZE PC Interface Card: 150mm x 100mm Approximately.
PCE8300H: 315mm x 257mm x 70mm

WEIGHT 2.8kg Approximately.

SALES OFFICE

U.K.

Hitachi Europe Ltd
Electronic Components Group
(Northern Europe)
Whitebrook Park, Lower Cookham Road,
Maidenhead, Berkshire SL6 8YA
Tel: (Local) (01628) 585000
(INT) +44 1628 585000
Fax: (Local) (01628) 585160
(INT) +44 1628 585160

GERMANY

Hitachi Europe GmbH
Electronics Components Group
Continental Europe
Dornacher Str. 3; D-85622 Feldkirchen
Postfach 2 01: D-85619 Feldkirchen
Tel: (Local) (089 9) 9 180-0
(INT) 49-89 99 1800
Fax: (Local) (089 9) 29 30 00
(INT) 49-89 929 3000

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