Introduction

The H8/300H series microcontrollers are high-performance Hitachi-original 16-bit microcontrollers that build in the optimum peripheral equipment for industrial machinery around high-speed H8/300 CPUs that have architecture upwardly compatible with H8/300 CPUs.

The microcontroller puts a CPU, RAM, direct memory access controller (DMAC), bus controller, timers, and a serial communication interface (SCI) on a single chip, making it suitable for a wide range of applications from small to large systems.

This microcontroller technical Q&A covers the H8/3001, H8/3002, H8/3003, H8/3042 series, H8/3032 series, and H8/3048 series.

Table 0-1 H8/300H Series

Item			H8/3003	H8/3002	H8/3001	H8/3042	H8/3041	H8/3040
CPU			H8/300H	H8/300H	H8/300H	H8/300H	H8/300H	H8/300H
Memory	ROM	Mask (byte)	_	_	_	64 k	48 k	32 k
		ZTAT™*	_	_	_	Yes	_	_
	RAM (b	yte)	512	512	512	2 k	2 k	2 k
Address sp	ace (byte	e)	16 M	16 M	16 M	16 M	16 M	16 M
External da	ata bus w	idth (bit)	8/16	8/16	8/16	8/16	8/16	8/16
Timers	ITU (inte	•	5 ch	5 ch	5 ch	5 ch	5 ch	5 ch
	Watchd	og timer	1 ch	1 ch	_	1 ch	1 ch	1 ch
DMA	Memory ↔ I/O		8 ch	4 ch	_	4 ch	4 ch	4 ch
controller	Memory	∕ ↔ memory	4 ch	2 ch	_	2 ch	2 ch	2 ch
Programmable timing pattern controller (TPC)		16 bits	16 bits	12 bits	16 bits	16 bits	16 bits	
SCI (Asynchronous/clock-synchronous)		2 ch	2 ch	1 ch	2 ch	2 ch	2 ch	
A/D	Resolut	ion	10 bits	10 bits	10 bits	10 bits	10 bits	10 bits
converter	Input ch	annel	8 ch	8 ch	4 ch	8 ch	8 ch	8 ch
	Externa	l trigger input	Yes	Yes	Yes	Yes	Yes	Yes
D/A	Resolut	ion	_	_	_	8 bits	8 bits	8 bits
converter	Input ch	annel	_	_	_	2 ch	2 ch	2 ch
Refresh co	ntroller		On-chip	On-chip	_	On-chip	On-chip	On-chip
Interrupts	Externa	l interrupts	9	7	4	7	7	7
	Internal	Interrupts	34	30	20	30	30	30
I/O port			58	46	32	78	78	78
Package			QFP-112	QFP-100 TQFP-100	QFP-80 TQFP-80	QFP-100 TQFP-100	QFP-100 TQFP-100	QFP-100 TQFP-100
Miscellane	ous		_	_	_	_	_	_

Note: ZTAT (Zero turn around time) is a trademark of Hitachi Ltd.

Table I-1 H8/300H Series (cont)

Item			H8/3048	H8/3047	H8/3044	H8/3032	H8/3031	H8/3030
CPU			H8/300H	H8/300H	H8/300H	H8/300H	H8/300H	H8/300H
Memory	ROM	Mask (byte)	128 k	96 k	32 k	64 k	32 k	16 k
		ZTAT [™] *	Yes	_	_	Yes	_	_
	RAM (b	yte)	4 k	4 k	2 k	2 k	1 k	512
Address sp	pace (byte	e)	16 M	16 M	16 M	1 M	1 M	1 M
External da	ata bus w	idth (bit)	8/16	8/16	8/16	8	8	8
Timers	ITU (inte	•	5 ch	5 ch	5 ch	5 ch	5 ch	5 ch
	Watchd	og timer	1 ch	1 ch	1 ch	1 ch	1 ch	1 ch
DMA	Memory ↔ I/O		4 ch	4 ch	4 ch	_	_	_
controller	Memory ↔ memory		2 ch	2 ch	2 ch	_	_	_
Programmable timing pattern controller (TPC)		16 bits	16 bits	16 bits	16 bits	16 bits	16 bits	
SCI (Asynchronous/clock-synchronous)		2 ch	2 ch	2 ch	1 ch	1 ch	1 ch	
A/D	Resolution		10 bits	10 bits	10 bits	10 bits	10 bits	10 bits
converter	Input ch	annel	8 ch	8 ch	8 ch	8 ch	8 ch	8 ch
	Externa	l trigger input	Yes	Yes	Yes	Yes	Yes	Yes
D/A	Resolut	ion	8 bits	8 bits	8 bits	_	_	_
converter	Input ch	annel	2 ch	2 ch	2 ch	_	_	_
Refresh co	ntroller		On-chip	On-chip	On-chip	_	_	_
Interrupts	Externa	l interrupts	7	7	7	6	6	6
	Internal	Interrupts	30	30	30	21	21	21
I/O port			78	78	78	63	63	63
Package		QFP-100 TQFP-100	QFP-100 TQFP-100	QFP-100 TQFP-100	QFP-80 TQFP-80	QFP-80 TQFP-80	QFP-80 TQFP-80	
Miscellaneous			rt card interfac low-power pe		_	_	_	

For Users of the Microcontroller Technical Q & A

This *Microcontroller Technical Q & A* was compiled from answers to technical questions we received from Hitachi microcontroller users. We hope that it will be a useful addition to the *H8/300H series user manuals*. Before starting design of products that use microcontrollers, read through the manual to deepen your understanding of microcontroller products and re-familiarize yourself with those areas of difficulty at the design stage.

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	er-Down Mode	Q - 10 0 0 0 1 0 1 0 1 0 1	
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Section 1 CPU

Product	H8/300H	Q&A No.		QA	300H-001A
Topic	The Difference Between the CCR's V	Flag and C F	lag		
Question					Classification—H8/300H
G: 41		1	.•		Software
	CCR's V flag and C flag both flag a 1 v	when an ope	ration	0	Registers
overnows	, what is the difference?				Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Re	lated Manuals
				Ma	nual Title
	s V flag is accessed to see if an overflo				
-	eration. In figure 1.1, which is a byte-si	_	-		
	when the result is smaller than the negative maximum (H'7F).	ative minim	um (H 80) or		
iaigei iliai	i die positive maximum (H /F).				
	H'80 H'00	H'7F		Otl	ner Technical
	V flag				cumentation
	Overflow <	→Overf	low	Do	cument Name
	Figure 1.1 V Flag Operati	on			
	t, the CCR's C flag is accessed to see it				
	n an unsigned operation. In figure 1.2,				
	the flag is set to 1 when the result is si	naller than t	he minimum	Re	lated Microcomputer
(H'00) or	larger than the maximum (H'FF).				chnical Q&A
	H'00	H'FF		Tit	ie
	C flag				
	Overflow◀	→Overf	low		
	Figure 1.2 C Flag Operati	on			
References					
1/616161166	2				

Product	H8/300H	Q&A No.	QA	300H-002A			
Topic	The Relationship Between Data Size and V Flag Changes						
Question			Classification—H8/300H				
Do the ch	anges in the CCR's V flag vary		Software				
Do the ch	unges in the CCR's V mag vary	with data size.	0	Registers			
				Bus controller			
				Interrupts			
				Resets			
				Power-down mode			
				Instructions			
				Miscellaneous			
				DMA controller			
				ITU			
				Watchdog timer			
				SCI			
			A/D converter				
			I/O ports				
Answer				elated Manuals			
signed ari However,	's V flag changes when an over- thmetic operation. This operation the timing of the changes in the	on is the same for all data size flag varies as follows:	of a	anual Title			
•	: When the value is smaller than	-		Other Technical			
• Word	d: When the value is smaller that	in H'8000 or larger than H"/F		ocumentation			
_	gword: When the value is smalle H'7FFFFFFF.	er than H'80000000 or larger	Do	ocument Name			
			Те	elated Microcomputer chnical Q&A			
			Tit	tle			
Reference	s						

Product	H8/300H	Q&A No.		QA3	300H-003A
Topic	Use of General Registers				
Question				С	Classification—H8/300H
C 1:66-		16 13 10	3 1.14		Software
	ent general registers be used as 8-bit, the same time?	16-bit, and 3.	2-D1t	0	Registers
registers a	t the same time:				Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Re	lated Manuals
Ves Regis	sters can be set freely for use as shown	in figure 1 3	3	Ma	nual Title
ics. Regis	sters can be set freely for use as shown	i ili liguic 1	, .		
	E0 R0H	R0L			
	ER1				
	ENI				ner Technical
	E2 R2H	R2L			cumentation
		1		-	cument Name
	ER3			1	e section 2.4.2, General gisters, in the following
	E4 I	E 4			nuals:
				1	H8/3002 Hardware Manual
	E5 I	E5		1	18/3003 Hardware Manual 18/3042 Series Hardware
	E6 R6H	R6L			Ianual
	LO KON	ROL			lated Microcomputer
	ER7 (SP)				chnical Q&A
Not	e: FR7 is used as the SP without any spe	cial notice bei	na aiven	Titl	le
Note: ER7 is used as the SP without any special notice being given.					
	Figure 1.3 Use of General Re	egisters			
References	<u>s</u>				

Product	H8/300H		Q&A No.		QA	300H-004	
Торіс	Bus State While the 0	CPU Is Operating					
Question					Classification—H8/300H		
1 11 11		CDIII. 1				Software	
1. What	t is the bus state during	CPU internal pr	ocessing?			Registers	
2. What	t is the bus state after \overline{L}	REQ is receive	d?		0	Bus controller	
	That is the bas state after Divide is received.				Interrupts		
3. What	is the bus state after \overline{E}	BREQ is received	d?			Resets	
						Power-down mode	
						Instructions	
						Miscellaneous	
						DMA controller	
						ITU	
						Watchdog timer	
						SCI	
						A/D converter	
						I/O ports	
Answer						lated Manuals	
See table	1.1.				Ma	nual Title	
Table 1.1	Bus State While the C	CPU Is Operating	5				
CPU Opera	ation	Address Bus	Data l	Bus			
During inte	rnal CPU processing	Hold	High i	mpedance	Otl	her Technical	
After DREC	ī is received	DMA address	DMA	data		cumentation	
After BREC	is received	High impedance	e High i	mpedance	Do	cument Name	
					Rel ma • H • H • H • M Re	e figure 6.18, External Bus lease State, in the following nuals: 18/3002 Hardware Manual 18/3003 Hardware Manual 18/3042 Series Hardware Manual lated Microcomputer chnical Q&A	
References	3				1		

Product	H8/300H	Q&A No.	QA300H-005A			
Topic	Bus Modes					
of the AB	2.1 of the H8/3003 Hardware Manual s WCR is cleared to 0, the bus mode becall areas can be accessed in 16-bit mod	omes 16 bits		Classification—H8/300H Software Registers Bus controller Interrupts Resets Power-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports		
Answer				Related Manuals		
ABWCR bit is clear might bett	a a given bit ADWn (bus width control (bus width control register) is cleared to red can be accessed in 16-bit mode. The ter read, "When even one area is set as a OH CPU goes into 16-bit bus mode and	o 0, only that e manual de a 16-bit acce	at area whose scription essed space,	Manual Title		
	e data bus. This means that I/O ports th			Other Technical		
lower data access spa	a bus (D7–D0) cannot be used as genera	al ports, eve	n in an 8-bit	Document Name See table 6.4, Address Space and Data Bus Used, in the following manuals: • H8/3002 Hardware Manual • H8/3003 Hardware Manual • H8/3042 Series Hardware Manual Related Microcomputer		
				Technical Q&A		
References	s l			Title		

Product	H8/300H	Q&A No.		QA3	00H-006A	
Торіс	Setting the Bus Controller in Area 7					
Question				С	lassification	on—H8/300H
a.	7 . 1: DAM 1: 4 11/6		1 ' 1		Software	
	17 mixes on-chip RAM and internal I/O he bus widths and access states set by the states are the	-			Registers	
aleas ale i	the bus widths and access states set by t	ine ous conti	ioner vanu:	0	Bus contr	oller
					Interrupts	
					Resets	
					Power-do	wn mode
					Instruction	าร
					Miscellan	eous
					DMA cont	troller
					ITU	
					Watchdog	g timer
					SCI	
					A/D conve	erter
					I/O ports	
Answer					ated Manu	ıals
In area 7,	the bus width and number of access sta	tes set by th	e bus	Mai	nual Title	
	are valid in areas other than the on-ch	-				
registers.	(The addresses of the area differ accord	ding to the p	product. See			
	al for details.) On-chip RAM has a fixed					
	d number of access states of 2. The inte	_		041	on Toolsuis	
	widths of 8-bits or 16-bits, and have a f	ixed number	r of access		er Technic cumentation	
states of 3	•			Doc	cument Na	me
				See	figure 6.2,	Access Area
				1 -		Operating Mode,
				1	ne following	g manuais: dware Manual
						dware Manual
						ies Hardware
				M	lanual	
					ated Micro	ocomputer A
				Title	е	
D-4-	_					
References	2					

When the RAME (RAM enable) bit of the SYSCR (system control register) is cleared to 0, the on-chip RAM is not valid and the settings of area 7 are followed. The CS signal outputs low in all of area 7.

Product	H8/300H	Q&A No.		QA3	00H-007A
Topic	External Installation of RAM to 8-Bit Bo	us Areas			
Question				С	lassification—H8/300H
XXII D.					Software
	M is externally installed in 8-bit bus sp	ace, which	signal		Registers
snould be	used to access it, \overline{HWR} or \overline{LWR} ?		Ī	0	Bus controller
			Ī		Interrupts
			Ī		Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer					ated Manuals
Use the H	WR signal.			Ma	nual Title
			-	011	T b i i
					ner Technical cumentation
				Do	cument Name
				See	table 6.4, Address Space
				and	Data Bus Used, in the
					owing manuals: 18/3002 Hardware Manual
					18/3002 Haraware Manual
					18/3042 Series Hardware
				M	Ianual
				Rel Tec	ated Microcomputer
			ļ	Titl	е
References	6				

Prod	luct	H8/300H	Q&A No.	QA300H-008A-1				
Topi	С	Changing the Number of Wait States In	nserted Per	Area				
Que	stion				C	Classification—H8/300H		
1.	Cont	the wait mode be set for individual areas?				Software		
1.	Can t	me wait mode de set for murviduar area	is:			Registers		
2.	If not	t, how should the wait mode be set to change the number of			0	Bus controller		
		s states inserted for individual areas?				Interrupts		
						Resets		
						Power-down mode		
						Instructions		
						Miscellaneous		
						DMA controller		
						ITU		
						Watchdog timer		
						SCI		
						A/D converter		
						I/O ports		
Ansv	wer				Re	lated Manuals		
1.	XX/X/I	E (wait made calcot) hits 1 and 0 of the	WCD (weit	aantral	Ма	nual Title		
1.		S (wait mode select) bits 1 and 0 of the ter), which set the wait mode, are common terms of the set the wait mode, are common terms of the set	•					
	_	n, the wait mode cannot be set for indiv						
	10050	ii, the wait mode cannot be set for mer	viddai arcas.	•				
2.	The f	following areas, can, however, be mixed	d:					
		Wait disabled areas			Other Technical			
		Areas to which wait states are only inse	erted by the	WAIT pin		cumentation		
		(pin wait mode 0)	10.01	···	Document Name			
		Areas in which WC (wait count) bits 1				e section 6.3.5 (5), WSC eting Example, in the		
		valid (programmable wait mode, pin w wait mode)	ait mode 1,	or pin auto-		lowing manuals:		
		wait mode)			l	H8/3002 Hardware Manual		
The		number of access states for individual a	reas can be	changed by	l .	H8/3003 Hardware Manual		
	using	these in combination. An example is s	hown below	and in		H8/3042 Series Hardware Manual		
	tables	s 1.2 and 1.3.						
					Tec	lated Microcomputer chnical Q&A		
					Tit	le		

References

The bus width and the enabled/disabled state of WSC (wait state controller) operation can be set for individual areas.

Product	H8/300H	Q&A No.	QA300H-008A-2
Topic	Changing the Number of Wait States I	nserted Per	Area
Answer			

Example: To set the following access states for the following areas:

Areas 0–1: 2 states
Area 2: 3 states
Areas 3–4: 4 states
Area 5: 5 states
Areas 6–7: 6 states

Table 1.2 Changing the Number of Wait States Inserted Per Area

Area	Memory Map	Wait States from WC Bit	Enable/Disable of Wait Insertion from WAIT Pin	Waits from WAIT pin	Access States
Area 0	2-state access space	Invalid	Disable	_	2
Area 1	Wait-disabled area				
Area 2	3-state access space pin wait mode 0	Invalid	Enable	0	3
Area 3		Valid/1 state	Enable	0	4
Area 4	3-state access space pin wait mode 1				
Area 5			Enable	1	5
Area 6	3-state access space	Invalid	Enable	3	6
Area 7	pin wait mode 0				

Table 1.3 Register Settings

Register	Address	Setting
		7 0
ASTCR (Access state control register)	H'FC	1 1 1 1 1 1 0 0
WOED (M. S. e.	1.110.0	7 0
WCER (Wait state control enable register)	H'38	0 0 1 1 1 0 0 0
		7
WOR		1 0
WCR	H'F9	

Topic Receiving BREQ in Power-Down Mode Question 1. Can BREQ be received in sleep mode? 2. Can BREQ be received in hardware/software standby mode? Registers Dusc controller Interrupts Resets Power-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports Answer 1. Yes 2. Since both the hardware standby mode and software standby mode bring on-chip peripheral modules to a halt (including the clock), BREQ cannot be received. Other Technical Document Name Related Microcomputer Technical Q&A Title Related Microcomputer Technical Q&A Title Related Microcomputer Technical Q&A Title Related Microcomputer Technical Q&A Title	Prod	uct	H8/300H	Q&A No.		QAS	300H-009A
Software Registers Registers Bus controller Interrupts Resets Power-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports I/O ports I/O ports	Topic	;	Receiving BREQ in Power-Down Mod	9			
1. Yes 2. Since both the hardware standby mode and software standby mode bring on-chip peripheral modules to a halt (including the clock), BREQ cannot be received. Other Technical Document Name Related Microcomputer Technical Q&A	1.	Can		re standby n	node?		Registers Bus controller Interrupts Resets Power-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter
Technical Q&A	1.	Yes Since bring	on-chip peripheral modules to a halt (i			Oti Do	her Technical cumentation
References	Refe	rences	3			Te	chnical Q&A

Product	H8/300H	Q&A No.		QA3	00H-010A	
Горіс	Maximum Wait Time After BREQ Inpu	ıt				
Question				C	assification—H8/300	
XX 71 1	The state of the s	1 DAOK	0		Software	
wny doe	s it take so long between BREQ input a	and BACK of	utput?		Registers	
				0	Bus controller	
					Interrupts	
					Resets	
					Power-down mode	
					Instructions	
					Miscellaneous	
					DMA controller	
					ITU	
					Watchdog timer	
					SCI	
					A/D converter	
					I/O ports	
					"O porto	
nswer				Rela	ated Manuals	
					nual Title	
Because	the BREQ request is held in the follow	ing cases:				
	en DMAC (DMA controller) data is bei e or block transfer mode.	ng transferre	d in burst			
2. Whe	en waits are inserted during accesses of	external add	resses.	I	er Technical	
Example:	When an instruction with a word-size	operand is e	xecuted	Documentation Document Name		
	with an 8-bit bus in pin wait mode 1: inserted wait states + wait states inser	•			ament Name	
				Tec	ated Microcomputer hnical Q&A	
				Title		
eference	s					

Product	H8/300H	Q&A No.		Ω Δ30	0H-011A	
Troduct	110/30011	QQA NO.		Q/30	OHOTIA	
Topic	Interrupt Sampling					
Question				Cla	ssification-	—H8/300H
When are	external interrupts (NMI, IRQn) sampl	ed?			Software	
, vinem are					Registers	
					Bus controlle	er
					Interrupts	
			-		Resets	
			-		Power-down	mode
			-		Instructions	
			-		Miscellaneo	
			-		ITU	iei
			-		Watchdog tii	mer
			-		SCI	IICI
			-		A/D converte	<u> </u>
					I/O ports	<u>. </u>
					г	
Answer				Rela	ted Manuals	S
Sampling	occurs at every fall of the system clock	ς φ.			ual Title	
					r Technical umentation	
				Doci	ıment Name	9
				Timin • H8 • H8 See fi	ng, in the follo /3002 <i>Hardw</i> /3003 <i>Hardw</i> gure 20.17, In	vare Manual nterrupt Input owing manual:
				Rela Tech	ted Microco nical Q&A	mputer
				Title		
References	S					

Prod	uct	H8/300H	Q&A No.		QA300H-012A		
Topic	•	Holding External Interrupts					
Ques	tion				С	Classification—H8/300H	
						Software	
1.		he IRQn interrupt requests held if they	•			Registers	
	_	E (IRQ enable) bit of the IER (IRQ enable extraord intermed (IRQ)) is also re-	•	r), wnich		Bus controller	
	controls external interrupts (IRQn), is cleared to 0?			0	Interrupts		
2.	Are I	RQn interrupt requests held if they are	produced w	hen		Resets	
	interr	upts are masked with the I and UI bits	of the CCR	(condition		Power-down mode	
	code	register)?				Instructions	
						Miscellaneous	
						DMA controller	
						ITU	
						Watchdog timer	
						SCI	
						A/D converter	
						I/O ports	
Ansv	ver				Re	lated Manuals	
1.	regist (IRQ the IF set to softw		Qn flag) of ffected by the 1 while the F bit can be	the ISR he state of IRQnF is cleared with	Otł Do	nual Title ner Technical cumentation cument Name	
2.	and U	As in the above case, IRQnF is not affe II bits. When the IRQnE and IRQnF bi upt mask is cleared, the interrupt is account to the interrupt is	ts are set to		See Blo foll • H • H • H • Re	e figure 5.2, IRQ Interrupt ock Diagram, in the lowing manuals: 18/3002 Hardware Manual 18/3003 Hardware Manual 18/3042 Series Hardware 1/4014 Microcomputer chnical Q&A	
Refe	rences	5			<u> </u>		

Product	H8/300H	Q&A No.		QA3	300H-013A
Topic	Receiving NMIs During NMI Processin	ng			
Question				С	lassification—H8/300H
70.1 377.5					Software
	I has the highest priority and is always	_			Registers
	eccepted if it is generated while the NMI	i interrupt pr	rocessing		Bus controller
routine is	running!			0	Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer					lated Manuals nual Title
running, t	hat interrupt request is accepted supering	nposed over	the first.		ner Technical
					cumentation
				Re	lated Microcomputer chnical Q&A
References	6				

_					
Product	H8/300H	Q&A No.		QA3	800H-014A
Topic	Edge Rise and Fall Times for Interrupt	t Pins			
Question				С	classification—H8/300H
XX 71	1	. 1 .	.1		Software
	edge trigger is used for an external inte lowed rise and fall times of the edge?	rrupt, what a	are the		Registers
longest an	lowed lise and fail times of the edge?				Bus controller
				0	Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Re	lated Manuals
effects:	o more than 2 states. More than this wi rupts will not be accepted because the eted.		-	Ма	nual Title
2. More	e than one edge will be detected interna	ally for each	change in		ner Technical cumentation
the e	xternal pin signal, so multiple interrupt	s will be rec	uested.		cument Name
				Re Tec	lated Microcomputer chnical Q&A
				Titl	le
Reference	S				

Prod	uct	H8/300H	Q&A No.		QA3	800H-015A		
Topic	C	Disable Timing for Interrupts						
Ques	stion				Classification—H8/300H			
1	A :.	ntanimunta disablad tha instant that the m		. d. 1 . ' .		Software		
1.		nterrupts disabled the instant that the poup of the po	eripnerai mo	odule s		Registers		
	men	upt enable bit is cleared to 0?				Bus controller		
2.	Wher	n the interrupt enable bit of the IER (IR	Q enable re	gister) is	0	Interrupts		
	cleare	ed to 0, are interrupt instantly disabled?	?			Resets		
						Power-down mode		
						Instructions		
						Miscellaneous		
						DMA controller		
						ITU		
						Watchdog timer		
						SCI		
						A/D converter		
						I/O ports		
Ansv	wer					lated Manuals		
1.	Interr	upts are disabled after the instruction the	hat cleared t	the interrupt	Ма	nual Title		
		e bit to 0 finishes executing. When an		•				
		rated while the zeroing instruction is ex		•				
	reque	st is accepted after the instruction com	pletes its ex	ecution.		ner Technical cumentation		
2	т.		1 . 1 1.	1		cument Name		
2.		rupts are disabled after the instruction the		_		e section 5.5.1, Interrupt		
		e bit to 0 finishes executing. When an it ated while the zeroing instruction is ex	•	•	l .	neration and Disable		
	-	st is not accepted after the instruction of	-	-	Coı	ntention, in the following		
	_	the request signal is cleared simultaneous	-			nuals:	,	
		lowever, since the IRQn flag is held, th	•			18/3002 Hardware Manua 18/3003 Hardware Manua		
		e bit is set to 1, that interrupt is accepted				18/3042 Series Hardware	·	
					N.	I anual		
						lated Microcomputer		
					Titl			
						o see section 1.3.2,		
					Ho	lding External Interrupts		
					(QA	A300H-012A), in this man	ual	
Refe	rences				•			

Product	H8/300H	Q&A No.	QA3	00H-016A	
Topic	Exception Processing After a Reset				
Question		Classification—H8/30			
				Software	
Are interri	upts ever generated immediately follow	ing resets?		Registers	
				Bus controller	
			0	Interrupts	
				Resets	
				Power-down mode	
				Instructions	
				Miscellaneous	
				DMA controller	
				ITU	
				Watchdog timer	
				SCI	
				A/D converter	
				I/O ports	
Answer			Rel	ated Manuals	
	diately after a reset, all interrupts, included However, when the first instruction of a accepted.		Ма	nual Title	
				ner Technical cumentation	
			Do	cument Name	
			Aft man • H • H	e section 4.2.3, Interrupts er a Reset, in the following nuals: 18/3002 Hardware Manual 18/3003 Hardware Manual 18/3042 Series Hardware Manual	
			Rel Tec	ated Microcomputer	
			Titl	е	
References	3				

Topic Question How should the two interrupt priority levels be used to make effective use of the interrupt controller? How should the two interrupt priority levels be used to make effective use of the interrupt controller? Registers Bus controller Interrupts Resets Power-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports By rewriting the values set in IPRA and IPRB (interrupt priority registers A and B) for every interrupt processing routine, the interrupt priority can be changed at any time. IPRA and IPRB are I-word registers, so they are easy to manipulate. A sample program is shown in figure 1.4. See the procedures after the figure for a more concrete example on use. PUSH RO Saves content of RO MOV.W @IPRA, RO Saves content of RO MOV.W RO, @IPRA ANDC #HBF, CCR Clears the UI bit POP RO Reverts to the saved IPRA value MOV.W RO, @IPRA ANDC #HBF, CCR Related Microcomputer Technical Q&A Title Related Microcomputer Technical Q&A Title Related Microcomputer Technical Q&A Title Related Microcomputer Technical Q&A Title	Product	H8/300H	Q&A No.		QA300H-017A-1
How should the two interrupt priority levels be used to make effective use of the interrupt controller? Registers Bus controller Resets Resets Power-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports	Topic	Using the Interrupt Controller			
By rewriting the values set in IPRA and IPRB (interrupt priority registers A and B) for every interrupt processing routine, the interrupt priority can be changed at any time. IPRA and IPRB are 1-word registers, so they are easy to manipulate. A sample program is shown in figure 1.4. See the procedures after the figure for a more concrete example on use. PUSH	How shou		sed to make	effective	Software Registers Bus controller Interrupts Resets Power-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter
MOV.W @IPRA, R0	By rewriting A and B) be changed easy to map procedure	for every interrupt processing routine, to dat any time. IPRA and IPRB are 1-we anipulate. A sample program is shown as after the figure for a more concrete expenses.	the interrupt ord registers in figure 1.4 kample on u	priority can , so they are . See the	Manual Title Other Technical Documentation
Figure 1.4 Sample Program	M P M M A	IOV.W @IPRA, R0 Saves IPRA USH R0 IOV.W #NEW, R0 IOV.W R0, @IPRA NDC #H'BF, CCR E COP R0 R0 IOV.W R0, @IPRA	A value w IPRA value UI bit the saved IPR	RA value	Related Microcomputer Technical Q&A
	R	TE Figure 1.4 Sample Progra		value	

Product	H8/300H	Q&A No.	QA300H-017A-2
Topic	Using the Interrupt Controller		
Answer			

- 1. Procedure for setting interrupt priority:
 - a. Set the UE (user bit enable) bit of the SYSCR (system control register) to 0, the I bit (interrupt mask) of the CCR (condition code register) to 1, and the CCR's UI (user bit/interrupt mask) bit to 0. In this state, only NMIs and priority 1 interrupt sources are accepted.
 - b. Set the interrupt priorities for each interrupt source on the user end.
 - c. Perform the following processing during the interrupt processing routines. Following the interrupt priorities set by the user, interrupts of priorities lower than the interrupt in question are masked by writing a 0 to the appropriate bits in IPRA and IPRB.
- 2. Figure 1.5 shows the processing procedures when the interrupt priorities set by the user are as shown in table 1.4.

Table 1.4 Interrupt Priorities

Interrupt Source	User-Set Priorities		Initial IPRA, IPRB Settings
Timer 1	5	Highest	1
Timer 2	4	A	1
SCI 1	3		1
Timer 3	2		1
Timer 4	1	\rightarrow	1
SCI 2	0	Lowest	1

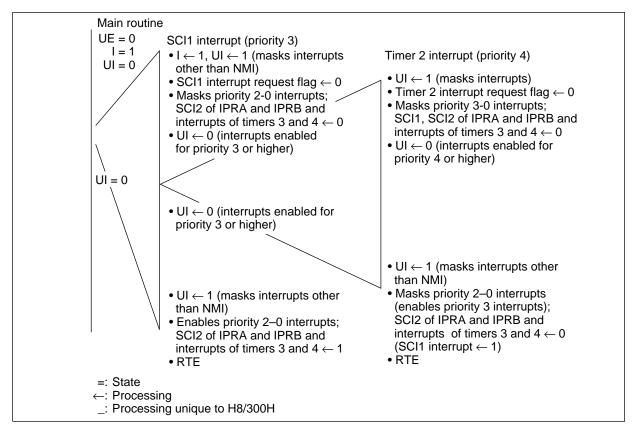


Figure 1.5 Processing Procedures

Product	H8/300H	Q&A No.		QA3	300H-018A
Topic	Receiving an External IRQ1 After Retu	urning From	Hardware Stand	lby M	lode
Question				С	Classification—H8/300H
T .1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 				Software
	dware standby mode, I set the IRQ1 pin				Registers
	standby mode. Will interrupts be accep pin remains low?	ted after ret	urning while		Bus controller
ine in Q i	pin remains low?			0	Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer					lated Manuals
Interrupts	will not be accepted immediately after	returning. A	A reset clears	Ма	nual Title
•	standby mode. This initializes the IER	•			
	becomes disabled (the IRQ1E (IRQ1 e		•		
	fter, if the IRQ1E bit of the IER is set t				
of the CCl	R enable interrupts, interrupts will be a	ccepted.			
				_	ner Technical cumentation
					cument Name
					e section 4.2.3, Interrupts
					ter a Reset, in the following
					nuals:
					18/3002 Hardware Manual 18/3003 Hardware Manual
					18/3042 Series Hardware
					<i>Ianual</i>
					lated Microcomputer
				Tit	le
References	3				

Product	H8/300H	Q&A No.		QA3	00H-019A
Topic	Interrupt Priority Within Groups				
the s 2. Whe routi	n external interrupts occur simultaneou ame priority (for example, IRQ4–IRQ7 n an IRQ4 interrupt occurs during an IR ne, what happens? (Does IRQ4 wait or priority?)) which has RQ7 interrup	priority? of processing	0	Registers Bus controller Interrupts Resets Power-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports
2. The mask the C processin the	iority is set within the IRQ4–IRQ7 interests > IRQ6 > IRQ7. IRQ7 is accepted first. After it is accepted. When the I (interrupt mask) and Ulace (condition code register) are enable essing routine, IRQ4–IRQ7 can be accepted in the IRQ4 is the IRQ7 processing routine.	ted, IRQ4—II (interrupt red during the opted. When	RQ7 are all nask) bits of e IRQ7 not enabled	Oth Doc See t Addi Rank • H • H • H M Rel	ated Manuals nual Title per Technical cumentation cument Name table 5.3, Interrupt Factors, Vector resses, and Interrupt Priority king (1), in the following manuals 8/3002 Hardware Manual 8/3003 Hardware Manual 8/3042 Series Hardware Ianual ated Microcomputer thnical Q&A e

Product	H8/300H	Q&A No.		QA3	00H-020A
Topic	Interrupts When the Bus Is Released				
Question					lassification—H8/300H
Question					Software
Are interr	upts that occur when the bus is released	l held?			Registers
					Bus controller
				0	Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Rel	ated Manuals
They are.	After the bus release ends, they are acc	ented after t	he execution	Ma	nual Title
	truction. This is the same regardless of	_			
by edge o			•		
					ner Technical cumentation
					cument Name
				Rel	ated Microcomputer
				Tec	chnical Q&A
				Titl	е
Defenses					
Reference	5				
1					

Product	H8/300H	Q&A No.		QA3	00H-021A
Topic	NMI Sampling Timing and Receiving A	After Reset			
Question				CI	assification—H8/300H
quoonon					Software
After rese	t, when does sampling of the NMI sign	al begin?			Registers
					Bus controller
					Interrupts
				0	Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Rela	ated Manuals
Commilian	of the NIMI signal begins simultaneous	1	Coll of the	Mar	nual Title
	of the NMI signal begins simultaneous ock in which the reset clear was sample	-			
	however, until after the execution of th				
_	s cleared (see figure 1.6)	c mst mstru	iction arter		
the reset is	s cleared (see figure 1.0)				
					er Technical
φ —					cumentation
Ψ		ŢIJŢ		рос	ument Name
		et clear			
	t _{RESS} t _{RESS} sam	pling			
RES —		- 	 		
				Dale	ntod Missossmanutos
		i i	i	Tec	ated Microcomputer hnical Q&A
	t _{RESW}			Title	9
	 	1 1			
	NMI not sampled	NMI samp	led		
Fig	gure 1.6 NMI Sampling Timing and Rec	eiving After	Reset		
_ e	K9	- g v -			
References	3				

Product	H8/300H	Q&A No.		QA3	300H-022A
Topic	Initializing SP After Reset				
Question				C	Classification—H8/300H
	·				Software
	the SP (stack pointer) have to be initia	lized immed	liately after		Registers
a reset?					Bus controller
					Interrupts
				0	Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer					lated Manuals
	rupt is accepted before the SP is initiality PC (program counter) is saved by the in			Ma	nual Title
processing address, to	g becomes undefined. The PC could be the I/O registers and so on, which ma ectly on return. This can cause run-awa	written to a kes it impos	blank sible to read		
processing address, to them corre	g becomes undefined. The PC could be to the I/O registers and so on, which ma	written to a kes it impos	blank sible to read		ner Technical
processing address, to them corre	g becomes undefined. The PC could be the I/O registers and so on, which materally on return. This can cause run-aware	written to a kes it impos	blank sible to read	Do	cumentation
processing address, to them corre	g becomes undefined. The PC could be the I/O registers and so on, which materally on return. This can cause run-aware	written to a kes it impos	blank sible to read	Do Do See Aft ma • H • H	
processing address, to them corre	g becomes undefined. The PC could be the I/O registers and so on, which materally on return. This can cause run-aware	written to a kes it impos	blank sible to read	Do See Aft ma • H • H • M Re	cument Name e section 4.2.3, Interrupts er a Reset, in the following nuals: I8/3002 Hardware Manual I8/3003 Hardware Manual I8/3042 Series Hardware Manual Iated Microcomputer chnical Q&A
processing address, to them corre	g becomes undefined. The PC could be the I/O registers and so on, which materally on return. This can cause run-aware	written to a kes it impos	blank sible to read	Do See Aft ma • H • H M	cument Name e section 4.2.3, Interrupts er a Reset, in the following nuals: I8/3002 Hardware Manual I8/3003 Hardware Manual I8/3042 Series Hardware Manual Iated Microcomputer chnical Q&A
processing address, to them corre	g becomes undefined. The PC could be to the I/O registers and so on, which make the true of the I/O registers and so on, which make the I/O registers are the I/O registers and so on, which make the I/O registers are the I/O registers and so on, which make the I/O registers are the I/O registers and so on, which make the I/O registers are the I/O registers and so on, which make the I/O registers are the I/O registers and the I/O registers are the I/O registers and the I/O registers are	written to a kes it impos	blank sible to read	Do See Aft ma • H • H • M Re	cument Name e section 4.2.3, Interrupts er a Reset, in the following nuals: I8/3002 Hardware Manual I8/3003 Hardware Manual I8/3042 Series Hardware Manual Iated Microcomputer chnical Q&A

Product	H8/300H	Q&A No.		QA	300H-023A
Topic	Pin State During Power-On Reset				
Question					Classification—H8/300H
*****			. 0		Software
What pin	states do I need to pay attention to duri	ing power-oi	resets?		Registers
					Bus controller
					Interrupts
				0	Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Re	lated Manuals
During a r	power-on reset, set the device to an ope	erating mode	that uses	Ma	nual Title
the mode	pins (MD0–MD2) and keep the \overline{STBY} that the ϕ output data is undefined unt	pin high. A	lso		
					her Technical ocumentation
				Do	cument Name
				Op the • <i>H</i> • <i>H</i>	e section 3.1.1, Types of serating Mode Selection, in a following manuals: H8/3002 Hardware Manual H8/3042 Series Hardware Manual
				Re Te	lated Microcomputer chnical Q&A
				Tit	le
Reference	s				

Product	H8/300H	Q&A No.	QA3	00H-024A
Topic	RESO Pin Output From RES Pin Input	t		
Question			С	lassification—H8/300H
				Software
What is th	te \overline{RESO} pin state for reset state (\overline{RES}	= low)?		Registers
				Bus controller
				Interrupts
			0	Resets
				Power-down mode
				Instructions
				Miscellaneous
				DMA controller
				ITU
				Watchdog timer
				SCI
				A/D converter
				I/O ports
				"о роло
Answer			Rel	ated Manuals
	\overline{O} pin is high impedance for reset state			nual Title
not go to i	reset output ($\overline{RESO} = low$).		Do	ner Technical cumentation cument Name
			Rel Tec	ated Microcomputer
			Titl	е
References	5			

Product	H8/300H	Q&A No.	(QA300H-025A
Горіс	Connecting RES and RESO Pins			
Question				Classification—H8/300H
	,			Software
	ny problem with taking RESO pin low	output and i	nputting it	Registers
directly to	the RES pin?			Bus controller
				Interrupts
				o Resets
				Power-down mode
				Instructions
				Miscellaneous
				DMA controller
				ITU
				Watchdog timer
				SCI
				A/D converter
				I/O ports
				<u> </u>
nswer				Related Manuals
***	, which is a second of	DEOC	<u>. </u>	Manual Title
	n a WDT (watchdog timer) overflow c irectly to the RES pin, a reset caused by			
	at that moment and everything internal			
	nitialized. This forcibly disables the \overline{R}		- 1	
	•		·	
	hat the RES input spec to rew (RES r	oin pulse wid	th) ∟	
minimum	hat the \overline{RES} input spec t_{RESW} (\overline{RES} p of 10 t_{evg} cannot be satisfied and the o			Other Technical
	hat the RES input spec t _{RESW} (RES p of 10 t _{cyc} cannot be satisfied and the c that point cannot be guaranteed. A bu	peration of t	he H8/300H	Documentation
CPU after	of $10 t_{\rm cyc}$ cannot be satisfied and the σ	operation of t ffer thus nee	he H8/300H ds to be	_
CPU after inserted to	of 10 t _{cyc} cannot be satisfied and the contact that point cannot be guaranteed. A bu	operation of t ffer thus nee	he H8/300H ds to be	Documentation
CPU after inserted to	of $10 t_{\rm cyc}$ cannot be satisfied and the of that point cannot be guaranteed. A but the ensure that the $\overline{\rm RESO}$ output does not	operation of t ffer thus nee	he H8/300H ds to be	Documentation
CPU after inserted to	of $10 t_{\rm cyc}$ cannot be satisfied and the of that point cannot be guaranteed. A but the ensure that the $\overline{\rm RESO}$ output does not	operation of t ffer thus nee	he H8/300H ds to be	Documentation
CPU after	of 10 t _{cyc} cannot be satisfied and the contract that point cannot be guaranteed. A but the ensure that the RESO output does not (See figure 1.7.)	operation of t ffer thus nee ot find its wa	he H8/300H ds to be	Document Name
CPU after inserted to	of $10 t_{\rm cyc}$ cannot be satisfied and the of that point cannot be guaranteed. A but the ensure that the $\overline{\rm RESO}$ output does not	operation of t ffer thus nee	he H8/300H ds to be	Document Name Related Microcomputer
CPU after inserted to RES pin.	of 10 t _{cyc} cannot be satisfied and the contract that point cannot be guaranteed. A but the ensure that the RESO output does not (See figure 1.7.)	operation of t ffer thus nee ot find its wa	he H8/300H ds to be	Document Name Related Microcomputer Technical Q&A
CPU after inserted to RES pin.	of 10 t _{cyc} cannot be satisfied and the contract that point cannot be guaranteed. A but the ensure that the RESO output does not (See figure 1.7.)	operation of the first state of the state of	he H8/300H ds to be y to the	Document Name Related Microcomputer
CPU after inserted to RES pin.	of 10 t _{cyc} cannot be satisfied and the contract that point cannot be guaranteed. A but the ensure that the RESO output does not (See figure 1.7.)	operation of the first state of the state of	he H8/300H ds to be y to the	Document Name Related Microcomputer Technical Q&A
CPU after inserted to RES pin.	of 10 t _{cyc} cannot be satisfied and the of that point cannot be guaranteed. A but the ensure that the RESO output does not (See figure 1.7.)	operation of the first state of	he H8/300H ds to be y to the	Document Name Related Microcomputer Technical Q&A
CPU after inserted to RES pin.	of 10 t _{cyc} cannot be satisfied and the contract that point cannot be guaranteed. A but the ensure that the RESO output does not (See figure 1.7.)	operation of the first state of	he H8/300H ds to be y to the	Document Name Related Microcomputer Technical Q&A
CPU after inserted to RES pin.	of 10 t _{cyc} cannot be satisfied and the of that point cannot be guaranteed. A but the nesure that the RESO output does not (See figure 1.7.) RES RES RESO H8/300H Figure 1.7 Connecting RES and R	operation of the first state of	he H8/300H ds to be y to the	Documentation Document Name Related Microcomputer Technical Q&A

Product	H8/300H	Q&A No.		QA3	300H-026A
Topic	Cautions for Reset Input				
Question				С	Classification—H8/300H
					Software
Are there	any cautions for reset input?				Registers
					Bus controller
					Interrupts
				0	Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
					·
Answer				Re	lated Manuals
******	DEO : : 1 1	1		Ма	nual Title
	RES pin is made low, a reset begins, b				
•	ed, it must be low for at least 20 ms wheast 10 system clock cycles when oper	•			
	reset exception processing begins. If the	•	•		
	operation thereafter cannot be guarantee		ons are not		
satisfied, (speration thereafter earnor be guarantee	ca.			ner Technical
					cumentation
					cument Name
					e section 4.2.2, Reset
					quence, in the following nuals:
					18/3002 Hardware Manual
					H8/3003 Hardware Manual
					18/3042 Series Hardware Ianual
				Tec	lated Microcomputer chnical Q&A
				Titl	
References	8				

			T			
Product	H8/300H	Q&A No.		QA	300H-027A	
Topic	Executing Instructions When Switching to Hardware Standby Mode					
Question				Classification—H8/300H		
****		OTDV : 1			Software	
What happens to executing instructions when the STBY pin goes low and the hardware standby mode is entered?				Registers		
				Bus controller		
				Interrupts		
					Resets	
				0	Power-down mode	
					Instructions	
					Miscellaneous	
					DMA controller	
					ITU	
					Watchdog timer	
					SCI	
			•		A/D converter	
					I/O ports	
Answer				RA	lated Manuals	
The executing instruction halts without waiting to finish and its operation cannot be guaranteed. To preserve the contents of RAM, clear the RAME (RAM enable) bit of the SYSCR (system control register) to 0.				Manual Title		
				1110	indui mio	
				Other Technical		
			Documentation			
			Document Name			
				See section 17.5.1, Transition		
				to Hardware Standby Mode, in the following manuals:		
				• H8/3002 Hardware Manual		
			• H8/3003 Hardware Manual			
				See section 19.5.1, Transition to Hardware Standby Mode, in		
			the following manual:			
			• H8/3042 Series Hardware			
			Manual			
			Related Microcomputer Technical Q&A			
			Title			
References	<u> </u>					

Product	H8/300H	Q&A No.		QA	300H-028A
Topic	Mode Pins During Hardware Standby	Mode			
Question					Classification—H8/300H
What ham	none when the mode nine (MD2, MD0)	ana ahanaa	ما ئە		Software
	pens when the mode pins (MD2–MD0) standby mode?	are change	ı ın		Registers
naidwaie	standby mode:				Bus controller
					Interrupts
					Resets
				0	Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Re	lated Manuals
the mode	is abnormal hardware standby mode of pins while in hardware standby mode. O PROM mode, for example, the power	When the m	ode is		her Technical
				Do	cumentation
				Re	lated Microcomputer chnical Q&A
References	5				

Product	H8/300H	Q&A No.		QAC	300H-029A
Topic	Returning From Hardware Standby Mo	ode			
Question				(Classification—H8/300H
T 1 .1	· · · · · · · · · · · · · · · · · · ·	1 <u>CTDV</u> :	. 1 1		Software
	at the RES pin has to be kept low and t	_	-		Registers
	return from hardware standby mode, by is changed to high does the \overline{RES} pin h				Bus controller
OIDIPII	is changed to high does the File pin i	iave to be in	, vv :		Interrupts
					Resets
				0	Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
				<u> </u>	Watchdog timer
					SCI
				<u> </u>	A/D converter
				-	I/O ports
				-	
				-	
Answer				Po	lated Manuals
Allowei					inual Title
To return	from hardware standby mode, the \overline{RES}	pin has to b	be low for	IVIC	illuai Titie
100 ns bet	fore the \overline{STBY} pin is changed to high. (See figure 1	.8.)		
	1				
S ⁻	ТВҮ			1	her Technical
				Do	cument Name
		1/	_	See	Appendix E, Hardware Standby
Ē	RES				de Transition (Return Timing), ir
		/			following manuals: H8/3002 Hardware Manual
	100 ns t _O .	sc _			H8/3002 Hardware Manual
					H8/3042 Series Hardware
				A	1anual
	Figure 1.8 Standby Release T	iming		Re Te	lated Microcomputer chnical Q&A
				Tit	le
D-/	_				
References	5				

Topic Interrupt Sampling and Receiving in Sleep Mode Question 1. When are external interrupts sampled during sleep mode? 2. How many states after an interrupt is sampled is sleep mode cleared? How many states after an interrupt is sampled is sleep mode cleared? Registers Bus controller interrupts interrupts interrupts is sampled interrupts. Resets Power-down mode instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports Related Manuals Manual Title Other Technical Document Name Other Technical Document Name Related Microcomputer request signal It SP-2 2: SP-4 3. 4: Interrupt vector address 5. 6: Saved PC and saved CCR 7. 8: Interrupt processing route start address (contents of vector address) Note: Example is an H8/30003 (16-bit bus mode, 2-state access, stack is	Produ	ıct	H8/300H	Q&A No.		QA3	300H-030A
1. When are external interrupts sampled during sleep mode? 2. How many states after an interrupt is sampled is sleep mode cleared? How many states after an interrupt is sampled is sleep mode cleared? Interrupts Resets	Topic		Interrupt Sampling and Receiving in S	leep Mode			
Registers Registers Bus controller Interrupt	Quest	tion				С	Classification—H8/300H
Answer 1. Sampling is the same as during program execution. Sampling occurs at every fall of the system clock. 2. Sleep mode is cleared 6 states after the interrupt is sampled. (See figure 1.9.) Address bus Data bus (D15-D0) Interrupt request signal 1: SP-2 2: SP-4 3. 4: Interrupt processing routine start address (contents of vector address) Note: Example is an Ha3/0303 (16-bit bus mode, 2-state access, stack is							Software
2. How many states after an interrupt is sampled is sleep mode cleared? Interrupts Resets	1.	Whei	n are external interrupts sampled during	g sleep mode	e?		Registers
cleared? Interrupts Resets Power-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports Related Manuals Manual Title Address bus Data bus (D15-D0) Interrupt request signal 1: SP-2 2: SP-4 3. 4: Interrupt vector address 6: Saved PC and saved CCR 7. 8: Interrupt processing routine start address (contents of vector address) Note: Example is an Ha30030 (16-bit bus mode, 2-state access, stack is	2.	How	many states after an interrupt is sample	ed is sleep m	node		Bus controller
Answer 1. Sampling is the same as during program execution. Sampling occurs at every fall of the system clock. 2. Sleep mode 6 states after the interrupt is sampled. (See figure 1.9.) Sleep mode 6 states after the interrupt is sampled. (See figure 1.9.) Other Technical Document Name Address bus 1 2 3 4 4			•	1			Interrupts
Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports Related Manuals Manual Title Title Address bus Data bus (D15-D0) Interrupt request signal 1. SP-2 2. SP-4 3. 4: Interrupt vector address 5. 6: Saved PC and saved CCR 7. 8: Interrupt processing routine start address (contents of vector address) Note: Example is an H8/3003 (16-bit bus mode, 2-state access, stack is							Resets
Answer 1. Sampling is the same as during program execution. Sampling occurs at every fall of the system clock. 2. Sleep mode 6 states after the interrupt is sampled. (See figure 1.9.) Sleep mode 6 states after the interrupt is sampled. (See figure 1.9.) Other Technical Documentation Document Name Related Microcomputer Technical Q&A Title 1: SP-2 2: SP-4 3, 4: Interrupt vector address 5, 6: Saved PC and saved CCR 7, 8: Interrupt processing routine start address (contents of vector address) Note: Example is an H8/3003 (16-bit bus mode, 2-state access, stack is						0	Power-down mode
DMA controller ITU Watchdog timer SCI A/D converter I/O ports 1. Sampling is the same as during program execution. Sampling occurs at every fall of the system clock. 2. Sleep mode is cleared 6 states after the interrupt is sampled. (See figure 1.9.) Other Technical Documentation Document Name Other Technical Documentation Document Name Related Microcomputer Technical Q&A Title 1: SP-2 2: SP-4 3, 4: Interrupt vector address 5, 6: Saved PC and saved CCR 7, 8: Interrupt processing routine start address (contents of vector address) Note: Example is an H8/3003 (16-bit bus mode, 2-state access, stack is							Instructions
Answer 1. Sampling is the same as during program execution. Sampling occurs at every fall of the system clock. 2. Sleep mode is cleared 6 states after the interrupt is sampled. (See figure 1.9.) Sleep mode 6 states Address bus 1 2 3 4 Documentation Document Name Other Technical Documentation Document Name Related Microcomputer Technical Q&A Title 1: SP-2 2: SP-4 3, 4: Interrupt vector address 5, 6: Saved PC and saved CCR 7, 8: Interrupt processing routine start address (contents of vector address) Note: Example is an H8/3003 (16-bit bus mode, 2-state access, stack is							Miscellaneous
Answer 1. Sampling is the same as during program execution. Sampling occurs at every fall of the system clock. 2. Sleep mode is cleared 6 states after the interrupt is sampled. (See figure 1.9.) Sleep mode 6 states Address bus 1 2 3 4 Document Name Other Technical Document Name Other Technical Document Name Title 1: SP-2 2: SP-4 3, 4: Interrupt vector address 5, 6: Saved PC and saved CCR 7, 8: Interrupt processing routine start address (contents of vector address) Note: Example is an H8/3003 (16-bit bus mode, 2-state access, stack is							DMA controller
Answer 1. Sampling is the same as during program execution. Sampling occurs at every fall of the system clock. 2. Sleep mode is cleared 6 states after the interrupt is sampled. (See figure 1.9.) Sleep mode 6 states Address bus 1 2 3 4 Data bus (D15-D0) Interrupt request signal 1: SP-2 2: SP-4 3, 4: Interrupt vector address 5, 6: Saved PC and saved CCR 7, 8: Interrupt processing routine start address (contents of vector address) Note: Example is an H8/3003 (16-bit bus mode, 2-state access, stack is							ITU
Answer 1. Sampling is the same as during program execution. Sampling occurs at every fall of the system clock. 2. Sleep mode is cleared 6 states after the interrupt is sampled. (See figure 1.9.) Sleep mode 6 states Address bus Data bus (D15-D0) Interrupt request signal 1: SP-2 2: SP-4 3, 4: Interrupt vector address 5, 6: Saved PC and saved CCR 7, 8: Interrupt processing routine start address (contents of vector address) Note: Example is an H8/3003 (16-bit bus mode, 2-state access, stack is							Watchdog timer
Answer 1. Sampling is the same as during program execution. Sampling occurs at every fall of the system clock. 2. Sleep mode is cleared 6 states after the interrupt is sampled. (See figure 1.9.) Sleep mode 6 states Address bus 1 2 3 4 4 Data bus (D15–D0) Interrupt request signal 1: SP-2 2: SP-4 3, 4: Interrupt vector address 5, 6: Saved PC and saved CCR 7, 8: Interrupt processing routine start address (contents of vector address) Note: Example is an H8/3003 (16-bit bus mode, 2-state access, stack is							SCI
Answer 1. Sampling is the same as during program execution. Sampling occurs at every fall of the system clock. 2. Sleep mode is cleared 6 states after the interrupt is sampled. (See figure 1.9.) Sleep mode 6 states Address bus 5 6 7 8							A/D converter
1. Sampling is the same as during program execution. Sampling occurs at every fall of the system clock. 2. Sleep mode is cleared 6 states after the interrupt is sampled. (See figure 1.9.) Sleep mode 6 states Other Technical Documentation Document Name Address bus 1 2 3 4 Data bus (D15-D0) Interrupt request signal 1: SP-2 2: SP-4 3, 4: Interrupt vector address 5, 6: Saved PC and saved CCR 7, 8: Interrupt processing routine start address (contents of vector address) Note: Example is an H8/3003 (16-bit bus mode, 2-state access, stack is							I/O ports
1. Sampling is the same as during program execution. Sampling occurs at every fall of the system clock. 2. Sleep mode is cleared 6 states after the interrupt is sampled. (See figure 1.9.) Sleep mode 6 states Other Technical Documentation Document Name Address bus 1 2 3 4 Data bus (D15-D0) Interrupt request signal 1: SP-2 2: SP-4 3, 4: Interrupt vector address 5, 6: Saved PC and saved CCR 7, 8: Interrupt processing routine start address (contents of vector address) Note: Example is an H8/3003 (16-bit bus mode, 2-state access, stack is							
1. Sampling is the same as during program execution. Sampling occurs at every fall of the system clock. 2. Sleep mode is cleared 6 states after the interrupt is sampled. (See figure 1.9.) Sleep mode 6 states Other Technical Documentation Document Name Address bus 1 2 3 4 Data bus (D15-D0) Interrupt request signal 1: SP-2 2: SP-4 3, 4: Interrupt vector address 5, 6: Saved PC and saved CCR 7, 8: Interrupt processing routine start address (contents of vector address) Note: Example is an H8/3003 (16-bit bus mode, 2-state access, stack is							
1. Sampling is the same as during program execution. Sampling occurs at every fall of the system clock. 2. Sleep mode is cleared 6 states after the interrupt is sampled. (See figure 1.9.) Sleep mode 6 states Other Technical Documentation Document Name Address bus 1 2 3 4 Data bus (D15-D0) Interrupt request signal 1: SP-2 2: SP-4 3, 4: Interrupt vector address 5, 6: Saved PC and saved CCR 7, 8: Interrupt processing routine start address (contents of vector address) Note: Example is an H8/3003 (16-bit bus mode, 2-state access, stack is							
1. Sampling is the same as during program execution. Sampling occurs at every fall of the system clock. 2. Sleep mode is cleared 6 states after the interrupt is sampled. (See figure 1.9.) Sleep mode 6 states Other Technical Documentation Document Name Address bus Data bus (D15-D0) Interrupt request signal 1: SP-2 2: SP-4 3, 4: Interrupt vector address 5, 6: Saved PC and saved CCR 7, 8: Interrupt processing routine start address (contents of vector address) Note: Example is an H8/3003 (16-bit bus mode, 2-state access, stack is	Answ	er				Re	lated Manuals
Address bus Data bus (D15-D0) Interrupt request signal 1: SP-2 2: SP-4 3, 4: Interrupt vector address 5, 6: Saved PC and saved CCR 7, 8: Interrupt processing routine start address (contents of vector address) Note: Example is an H8/3003 (16-bit bus mode, 2-state access, stack is	2.	at eve	ery fall of the system clock. o mode is cleared 6 states after the inter			Ma	nual Title
Address bus Data bus (D15-D0) Interrupt request signal 1: SP-2 2: SP-4 3, 4: Interrupt vector address 5, 6: Saved PC and saved CCR 7, 8: Interrupt processing routine start address (contents of vector address) Note: Example is an H8/3003 (16-bit bus mode, 2-state access, stack is		8				Otl	ner Technical
Address bus Data bus (D15–D0) Interrupt request signal 1: SP-2 2: SP-4 3, 4: Interrupt vector address 5, 6: Saved PC and saved CCR 7, 8: Interrupt processing routine start address (contents of vector address) Note: Example is an H8/3003 (16-bit bus mode, 2-state access, stack is							
Address bus Data bus (D15–D0) Interrupt request signal 1: SP-2 2: SP-4 3, 4: Interrupt vector address 5, 6: Saved PC and saved CCR 7, 8: Interrupt processing routine start address (contents of vector address) Note: Example is an H8/3003 (16-bit bus mode, 2-state access, stack is		SI	eep mode 6 states			Do	cument Name
1: SP-2 2: SP-4 3, 4: Interrupt vector address 5, 6: Saved PC and saved CCR 7, 8: Interrupt processing routine start address (contents of vector address) Note: Example is an H8/3003 (16-bit bus mode, 2-state access, stack is	,	Da	ss bus 1 2 ta bus 5 6		4 X	Re Ted	lated Microcomputer chnical Q&A
1: SP-2 2: SP-4 3, 4: Interrupt vector address 5, 6: Saved PC and saved CCR 7, 8: Interrupt processing routine start address (contents of vector address) Note: Example is an H8/3003 (16-bit bus mode, 2-state access, stack is	_					Tit	le
2: SP-4 3, 4: Interrupt vector address 5, 6: Saved PC and saved CCR 7, 8: Interrupt processing routine start address (contents of vector address) Note: Example is an H8/3003 (16-bit bus mode, 2-state access, stack is	re	equest	signal —	1 1			
external memory) Figure 1.9 Timing of Clearing Sleep Mode by Interrupt	2; 3; 5; 7;	: SP-4 , 4: Int , 6: Sa , 8: Int lote: E	errupt vector address aved PC and saved CCR errupt processing routine start address (col Example is an H8/3003 (16-bit bus mode, 2- external memory)	-state access	, stack is		

Product	H8/300H	Q&A No.		QA3	00H-031A
Topic	Execution Time in Software Standby M	1ode			
Question				CI	assification—H8/300H
					Software
· · · · · · · · · · · · · · · · · · ·	y states are needed to transition to the s	oftware star	ndby mode		Registers
using a SI	LEEP instruction?				Bus controller
					Interrupts
					Resets
					Power-down mode
				0	Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer					ated Manuals
The time 1	required to transition to the software sta	andby mode	is the time	Mar	nual Title
	quired for the SLEEP instruction to exe	-			
	n is stated in on-chip memory, it takes 2				
	struction is in external 8-bit 3-state-acc				
	e figure below shows the timing for exe	•			
	n. (See figure 1.10.)				er Technical
	,				umentation
	SLEEP			Doc	sument Name
	instruction				
	execution time				
	 ← →	Sleep mode			
	ф П П П П				
			•	Rela	ated Microcomputer
	Internal \(\sqrt{1} \)				hnical Q&A
	address bus 1 2			Title	
	Internal data				
	bus (16 bits) 3 4 4				
	1 1 1				
1: PC					
2: PC+					
	EEP instruction				
4: Nex	tt instruction (not executed)				
	Figure 1.10 Sleep Instruction	Timing			

Product	t H8/300H	Q&A No.	(QA30	00H-032A-1
Topic	Operation When an Interrupt is Request	ed During Ex	ecution or While	Fetc	hing a SLEEP Instruction
Questio	on l			С	Classification—H8/300H
TT 1		4			Software
	oes the H8/300H CPU operate when an in	_	-		Registers
a SLEI	EP instruction fetch or while a SLEEP inst	ruction is ex	recuting?		Bus controller
					Interrupts
					Resets
				0	Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Re	lated Manuals
-	ion varies, depending on the time the interbelow:	rupt request	occurs, as	Ma	nual Title
	uring SLEEP instruction fetch: The interru				
	arts after the previous instruction finishes	_			
	ecomes the address of the SLEEP instructive interrupt service routine, the SLEEP inst		•	_	ner Technical cumentation
uı	e interrupt service routine, the SEEEF mist	iruction exe	cutes.	Do	cument Name
B. D	uring SLEEP instruction execution (case 1): Interrupt	exception		
•	ocessing starts without going through the	•			
	C becomes the address of the instruction as				
	struction. After returning from the interrup	•	utine, the		
ın	struction after the SLEEP instruction exec	eutes.		Re	lated Microcomputer
C. D	uring SLEEP instruction execution (case 2	2): The sleer	mode is	-	chnical Q&A
	anceled 6 states later and the interrupt serv			Titl	le
fig	gure 1.11.)				
D. 1					
Referen	ices				

Product	H8/300H	Q&A No.	QA300H-032A-2
Topic	Operation When an Interrupt is Request	ted During Ex	ecution or While Fetching a SLEEP Instruction
Answer			

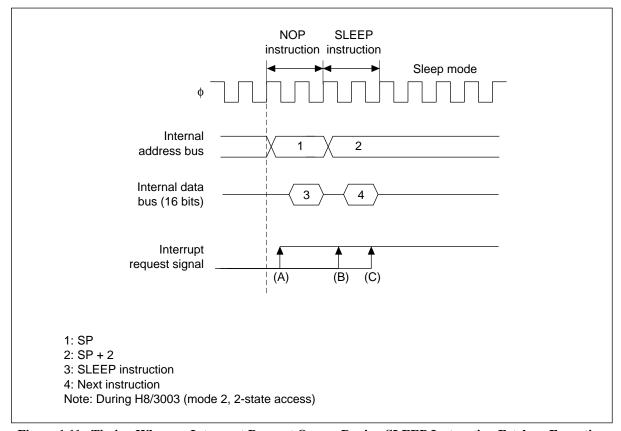


Figure 1.11 Timing When an Interrupt Request Occurs During SLEEP Instruction Fetch or Execution

Prod	luct	H8/300H	Q&A No.		QA3	300H-033A		
Topi	C	Support for the DAA (DAS) Instruction	with the INC	C (DEC) Instruct	tion			
Ques	stion				С	lassification—H8/300H		
1	The I	NAA instruction oon be used with on si	instancia a con la constancia de la constancia (ADD)		Software			
1.		DAA instruction can be used with an ac ow about executing it after an INC inst				Registers		
	out II	ow about executing it after all five first	ruction cacc	cutes:		Bus controller		
2.	The I	DAS instruction can be used with a sub	tract instruc	tion (SUB),		Interrupts		
	but h	ow about executing it after an DEC ins	truction exe	cutes?		Resets		
						Power-down mode		
					0	Instructions		
						Miscellaneous		
						DMA controller		
						ITU		
						Watchdog timer		
						SCI		
						A/D converter		
						I/O ports		
Ansv	ver					lated Manuals		
1.	Exec	ution of a DAA instruction after execut	ion of an IN	1C	Ма	nual Title		
	instru	action is not supported, since the C and	H flags do	not reflect				
	the re	esults of the operation after INC instruc	tion executi	on. To				
	incre	ment decimal data, execute a DAA inst	ruction after	r adding 1				
	with	the ADD instruction (ADD.B #1, Rd).						
2.	Evec	ution of a DAS instruction after execut	ion of an DI	FC	1	ner Technical cumentation		
2.		action is not supported, since the C and			Do	cument Name		
		esults of the operation after DEC instruc	_					
		ement decimal data, execute a DAS inst						
	with	the ADD instruction (ADD .B #-1, Rd)) and inverti	ing the C				
	and F	H flags (XORC #A0, CCR).						
					Re	lated Microcomputer		
					Tec	chnical Q&A		
					Titl	e		
- ·								
Refe	rences	<u> </u>						

Actual operation is determined by the flag state.

Prod	luct	H8/300H	Q&A No.		QAS	300H-034A
Topi	С	BRA and BRN Instructions				
Que	stion				C	Classification—H8/300H
1	XX 71	The state of the s				Software
1.		t is the difference between BRA (BT) and JMP? Also, what it mean for the condition to be "True"?		iso, wnat		Registers
	uoes	it mean for the condition to be True ?				Bus controller
2.	What	does it mean for the BRN (BF) condit	ion to be "F	alse"?		Interrupts
						Resets
						Power-down mode
					0	Instructions
						Miscellaneous
						DMA controller
						ITU
						Watchdog timer
						SCI
						A/D converter
						I/O ports
Ansv	ver				Re	lated Manuals
1.	The I	BRA instruction can be used just like th	ne IMP instr	ruction but	Ma	nual Title
1.		s in the following points:	ic sivii misti	action, but		
		It can only branch in the range $+127$ by	tes to -128	bytes for d:8		
		and +32767 bytes to -32768 bytes for o		·		
	•	If the relative values of objects do not of	change, the	program can		
	•	be relocated.				her Technical cumentation
		Execution states and instruction size ar	e different.			cument Name
	•	Assembler format is different.				Cument Name
	A co	ndition of True means that since this in	struction alv	vavs		
		thes, the branch condition is always Tru		,		
		·				
2.		ndition of False means that since this in the ches, the branch condition is always Fal		ever	Re	lated Microcomputer
		,			Tit	
					110	
Refe	rences					

Product	H8/300H		Q&A No.		QA3	800H-035A	
Topic	BRN Instruction						
Question					С	lassificatio	n—H8/300H
XX71 4 1-1	1 - C : ((DDN (DE)	0				Software	
w nat kind	d of instruction is BRN (BF)	!				Registers	
						Bus contro	oller
						Interrupts	
						Resets	
						Power-dov	vn mode
					0	Instruction	S
						Miscellane	ous
						DMA conti	roller
						ITU	
						Watchdog	timer
						SCI	
						A/D conve	rter
						I/O ports	
Answer					Re	lated Manua	als
instruction	convenient instruction that rank during debugging. It oper n, but its size and execution	ates the sar	ne as the NO)P	Ма	nual Title	
Table 1.5	The BRN Instruction				Oth	ner Technic	 al
Inatrustia	notruction Circ (Butco)	Inctruction	n Evecution	Time (States)		cumentatio	
Instruction	n Instruction Size (Bytes)	Instruction		Time (States)	Do	cument Nai	ne
BRN d:8	3 2	4*					
d:1	6 4	6*					
NOP	2	2*					
	r a 16-bit bus/2-state access sp p ROM.	ace or an in	struction fetch	from the on-	Re Tec	lated Microchnical Q&	computer \
.	p				Titl	le	
Reference	s						
IVEIGI CIICE	<u>-</u>						

Like BRN, BRA (BT) is convenient to use during debugging.

Product	H8/300H	Q&A No.		QA	300H-036A
Торіс	The SUBX Instruction				
Question				C	Classification—H8/300H
W/less de co	the CUDY instruction (subtraction with	1			Software
-	the SUBX instruction (subtraction wit the result of execution is 0?	n carry) pre	serve the Z		Registers
mag when	the result of execution is 0;				Bus controller
					Interrupts
					Resets
					Power-down mode
				0	Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Re	lated Manuals
multiple s reflects th	X instruction is used to divide a subtractions. After the SUBX instructions eresult of all of these operations (See a results of each individual SUBX instructions).	n is executed figure 1.12.)	d, the Z flag		nual Title
	┌─ SUB R	mL, RnL			ner Technical cumentation
	Reflected in Z flag ◀	RmH, RnH		Do	cument Name
	Figure 1.12 Z Flag				
When the	SUBX instruction results in a 0, the Z	flag thus ho	lds the result		
	vious operation.	nag mas no	ids the result	Re Te	lated Microcomputer chnical Q&A
				Tit	le
References	s			1	
References	5				

Product	H8/300H	Q&A No.		QA	300H-037A
Topic	Odd Address Values During STC Instr	uction Execu	tion		
Question				C	Classification—H8/300H
****		,• •	. 1 1		Software
	e odd address value when an STC instr		ecuted and		Registers
line CCR s	stored in an (register indirect) even add	ress?			Bus controller
					Interrupts
					Resets
					Power-down mode
				0	Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
					1/O ports
A				_	
Answer					lated Manuals
Undefined	1.			IVIa	nual Title
					her Technical cumentation
					cument Name
					Cament Hame
				Po	lated Microcomputer
				Tec	lated Microcomputer chnical Q&A
				Tit	le
					<u></u>
References	5				

Proc	luct	H8/300H	Q&A No.		QA:	300H-038A
Topi	С	Interrupts and DMA Transfer Reques	sts While the E	EPMOV Instru	ıction	Is Executing
Que	stion				(Classification—H8/300H
1	VV /1		ution of on EE	DMOV		Software
1.		n an interrupt occurs during the execunction, what happens to that interrupt		PMOV		Registers
	msut	action, what happens to that interrupt	request:			Bus controller
2.	What	t happens when a DMA transfer reque	est occurs dur	ing the		Interrupts
	exect	ution of an EEPMOV instruction?				Resets
						Power-down mode
					0	Instructions
						Miscellaneous
						DMA controller
						ITU
						Watchdog timer
						SCI
						A/D converter
						I/O ports
					+_	
Ans	wer					lated Manuals
1.	instru finish occur	n an interrupt occurs during the executation, the interrupt is held and acceptes executing. It is handled the same are during ordinary instruction execution during EEPMOV.W execution are a	ted when the is as when an int on. However,	nstruction terrupt NMIs that	IVIA	nual Title
		yte in transfer is completed. For inter	_		Ot	her Technical
		ation is the same as for EEPMOV.B.	1	,	_	cumentation
•	-			• •		cument Name
2.		DMA transfer is executed between the of the EEPMOV instruction.	e read cycle a	nd write	2), ma • <i>H</i>	e section 2.2.28 (items 1 and EEPMOV, in the following anual: H8/300H Series Programming Manual
					Re Te	lated Microcomputer chnical Q&A
					Tit	le
Refe	rences	<u>S</u>				

H8/300H	Q&A No.		QA30	00H-039A
The Difference Between EEPMOV.B a	and EEPMOV.W			
			CI	assification—H8/300
a difference between FEDMOVR and	EEDMOVW?			Software
e difference between EEFMOV.B and	EEFWIO V. W!			Registers
				Bus controller
				Interrupts
				Resets
				Power-down mode
			0	Instructions
				Miscellaneous
				DMA controller
				ITU
				Watchdog timer
				SCI
				A/D converter
				I/O ports
			Rela	nted Manuals
er data size of both the EEPMOV.B and as is byte, but there are some difference of register that counts the transfer byte. MOV.B: Byte (maximum number of transfer)	es, as described s:		Man	ual Title
is is byte, but there are some difference	es, as described s: unsfer bytes is 2	55).	Otho	er Technical umentation
of register that counts the transfer bytes MOV.B: Byte (maximum number of tra MOV.W: Word (maximum number of tra MOV.W: Word (maximum number of transfer)	es, as described s: ansfer bytes is 2 ransfer bytes is	55). 65535).	Othe Doc	er Technical
of register that counts the transfer bytes MOV.B: Byte (maximum number of transfer) WOV.W: Word (maximum number of transfer)	es, as described s: unsfer bytes is 2 ransfer bytes is cutes (all held).	55). 65535).	Otho Doc See EEP	er Technical umentation
of register that counts the transfer bytes MOV.B: Byte (maximum number of transfer) MOV.W: Word (maximum number of transfer) de/disable of interrupt acceptance: MOV.B: Accepted after instruction exemptors.	es, as described s: unsfer bytes is 2 ransfer bytes is cutes (all held).	55). 65535).	Otho Doc See EEP • H8 Pr	er Technical umentation ument Name section 2.2.28 (1), (2) MOV 8/300H Series
		The Difference Between EEPMOV.B and EEPMOV.W? e difference between EEPMOV.B and EEPMOV.W?		e difference between EEPMOV.B and EEPMOV.W?

Product	H8/300H	Q&A No.		QA3	300H-040A		
Topic	Cautions on Stack Operation						
Question				Classification—H8/300H			
A (1	' 				Software		
Are there	any particular cautions about stack ope	ration to be	aware or?		Registers		
					Bus controller		
					Interrupts		
					Resets		
					Power-down mode		
					Instructions		
				0	Miscellaneous		
					DMA controller		
					ITU		
					Watchdog timer		
					SCI		
					A/D converter		
					I/O ports		
_							
Answer				-	lated Manuals		
On the H8	3/300H, the stack area is always accessed	ed by word o	or longword.	Ма	nual Title		
When the	stack pointer is set to an odd number, r	nalfunctions	s can result.				
	USH or POP instructions to stack. The		of SP (stack				
pointer) is	undefined. It is initialized by the user.						
				Otl	her Technical		
					cumentation		
				Do	cument Name		
				See	section 2.4.4 Inicial CPU		
				1	sistor, section 2.5.2 Memory Data		
					mats, in the following manuals: 48/3002 Hardware Manual		
					H8/3003 Hardware Manual		
					H8/3042 Series Hardware		
				<i>N</i>	1anual		
				Re Tec	lated Microcomputer chnical Q&A		
				Titl	le		
References	3						

	T						
Product	H8/300H	Q&A No.		QA3	00H-041A		
Topic	On-Chip Peripheral LSI Access When the Bus Is Released						
Question				С	lassification—H8/300H		
					Software		
	nal devices (bus master) access internal				Registers		
device?	when the H8/300H CPU has released the	ne bus to an	external		Bus controller		
device?					Interrupts		
					Resets		
					Power-down mode		
					Instructions		
				0	Miscellaneous		
					DMA controller		
					ITU		
					Watchdog timer		
					SCI		
					A/D converter		
					I/O ports		
					у с роло		
Answer				Rel	ated Manuals		
	nal registers cannot be accessed from ex				nual Title		
				Doo	ner Technical cumentation cument Name atted Microcomputer hnical Q&A		
Poforono							
References	5						

Prod	luct	H8/300H	Q&A No.	QA300H-042A				
Торі	С	Areas That Can Be Used as ROM by t	he Vector Ta	ble	9			
Que	stion				Classification—H8/30			
1	<u> </u>	1	1.1			Software		
1. Can the empty areas reserve) be used as R			e vector table (reserved by system or			Registers		
	reser	ve) be used as ROM?				Bus controller		
2.	. Can the empty areas of the I/O registers be used as ROM?			Л?		Interrupts		
						Resets		
						Power-down mode		
						Instructions		
					0	Miscellaneous		
						DMA controller		
						ITU		
						Watchdog timer		
						SCI		
						A/D converter		
						I/O ports		
Ans	wer				Rel	ated Manuals		
1.		vector numbers reserved by the system			Ма	nual Title		
		ot be used. Reserve addresses, however ed interrupt vector addresses on the vec						
	used.	_	cioi table ca	ii aiso be				
	uscu.							
2.	The e	empty areas of the I/O registers cannot	be used.			ner Technical cumentation		
					Do	cument Name		
					Rel	ated Microcomputer		
					Titl	е		
Refe	rences							

Items reserved by the system are used by development tools. Addresses reserved by the system and reserve addresses are listed in the manual. Branch address areas of "memory indirect" addressing can use addresses other than those reserved by the system or those of used by the vector table.

Product	H8/300H	Q&A No.		QA3	800H-043A
Topic	Pin State During the Oscillation Settlin	g Time			
Question				C	Classification—H8/300H
***			G:		Software
	the pin states during oscillation settling	time after th	ne software		Registers
standby m	node is cleared?				Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
				0	DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Re	lated Manuals
The came	as in the software standby mode.			Ма	nual Title
				Otl	her Technical
					cumentation
					lated Microcomputer chnical Q&A
References	8			•	

Section 2 On-Chip Peripherals

'ania	Common		Q&A No.	QAS	300H-101-1
opic	Receiving D	DMAC Startup Requests			
Question				(Classification—H8/300I
When a D	MA controlle	r startup request occurs:			Software
vviicii a D.	Wir Controlle	r startup request occurs.			Registers
1. When	n is the reques	st forced to wait?			Bus controller
					Interrupts
	1 1				Resets
	•	10V execution			Power-down mode
	-	modify-write instruction	execution		Instructions
•]	During DMA	C cycle steal transfers.			Miscellaneous
				0	DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
nswer				Re	lated Manuals
				Ma	nual Title
1 Thak	a ambitan mui	omitre and an iou arreamed by	us mastan > mafmasl		inuai iilie
	_	ority order is: external b		n —	inuai mie
contr	oller > DMA	C > CPU. This means the	at DMA requests a	n are not	inuai Title
contro accep	coller > DMA oted when an o	C > CPU. This means the external bus master or re	at DMA requests a fresh controller w	nare not	inual fille
contro accep priori	coller > DMAC oted when an c ity higher than	C > CPU. This means the external bus master or rent the DMAC has the bus	at DMA requests a fresh controller w Since the DMAC	nre not ith a	inuai Tiue
contro accep priori chann	coller > DMAO oted when an o ity higher than nels have the j	C > CPU. This means the external bus master or re	at DMA requests a fresh controller was. Since the DMAC shown in table 2.1	are not ith a C , the Ot	her Technical ocumentation
contro accep priori chant reque	oted when an output of the color of the colo	C > CPU. This means the external bus master or render the DMAC has the bus priorities (for H8/3003)	at DMA requests a fresh controller was. Since the DMAC shown in table 2.1	are not ith a C , the Ot Dc	her Technical
contro accep priori chann	oted when an output of the policy of the pol	C > CPU. This means the external bus master or renthe DMAC has the bus priorities (for H8/3003) at a higher priority channel.	at DMA requests a fresh controller was. Since the DMAC shown in table 2.1	are not ith a C , the Ot Dc	her Technical ocumentation
contro accep priori chann reque Table 2.1 Short Addi	oted when an object when an object whigher than nels have the pest waits when DMAC Charess Mode	C > CPU. This means the external bus master or rent the DMAC has the bus priorities (for H8/3003) at a higher priority channel Priority	at DMA requests a efresh controller w. . Since the DMAC shown in table 2.1 el is transferring.	are not ith a C , the Ot Dc	her Technical ocumentation
contro accep priori chann reque Table 2.1 Short Addi Channel 0 I	roller > DMA0 oted when an o ity higher than nels have the p est waits when DMAC Cha ress Mode A B	C > CPU. This means the external bus master or restricted in the DMAC has the bus priorities (for H8/3003) in a higher priority channel annel Priority Full Address Mode Channel 0	at DMA requests a fresh controller w. . Since the DMAC shown in table 2.1 el is transferring.	are not ith a C , the Ot Dc	her Technical ocumentation
contro accep priori chann reque Table 2.1 Short Addi Channel 0 I Channel 1 I	roller > DMA0 oted when an o ity higher than nels have the p est waits when DMAC Cha ress Mode A B A	C > CPU. This means the external bus master or rein the DMAC has the bus priorities (for H8/3003) in a higher priority channel Priority Full Address Mode	at DMA requests a fresh controller w. . Since the DMAC shown in table 2.1 el is transferring.	on the state of th	her Technical ocumentation ocument Name
contro accep priori chann reque Table 2.1 Short Addi Channel 0 I Channel 1 I Channel 1 I	roller > DMAC oted when an o ity higher than nels have the p est waits when DMAC Cha ress Mode A B A B	C > CPU. This means the external bus master or rest the DMAC has the bus priorities (for H8/3003) in a higher priority channel Priority Full Address Mode Channel 0 Channel 1	at DMA requests a fresh controller w. . Since the DMAC shown in table 2.1 el is transferring.	nare not ith a C , the Ot Do	her Technical ocumentation
contro accep priori channe reque Table 2.1 Short Addr Channel 0 / Channel 1 / Channel 1 / Channel 1 / Channel 1 / Channel 1 /	roller > DMAC oted when an o ity higher than nels have the p est waits when DMAC Cha ress Mode A B A B A	C > CPU. This means the external bus master or restricted in the DMAC has the bus priorities (for H8/3003) in a higher priority channel annel Priority Full Address Mode Channel 0	at DMA requests a fresh controller w. . Since the DMAC shown in table 2.1 el is transferring.	nare not ith a C , the Ot Do	her Technical ocumentation ocument Name
contro accep priori chann reque Table 2.1 Short Addi Channel 0 I	roller > DMAO oted when an o ity higher than nels have the p est waits when DMAC Cha ress Mode A B A B A B A	C > CPU. This means the external bus master or rest the DMAC has the bus priorities (for H8/3003) in a higher priority channel Priority Full Address Mode Channel 0 Channel 1	at DMA requests a fresh controller w. . Since the DMAC shown in table 2.1 el is transferring.	nare not ith a C , the Ot Do Do	her Technical ocumentation ocument Name

Product	Common	Q&A No.	QA300H-101-2
Topic	Receiving DMAC Startup Requests		
Answer			

2. During EEPMOV execution, requests are accepted between the read cycle and the write cycle. During read-modify-write instruction execution, requests are accepted between the read cycle, instruction fetch, and the write cycle. During cycle steal transfers, requests are accepted if the channel of the transfer request is higher in priority than the current channel.

References

- 1. BSET, BCLR, BNOT, BST and BIST are read-modify-write instructions.
- 2. When the wait is longer than those described above, wait states may have been inserted by a CPU bus cycle that has a DREQ request. (See figure 2.1.)

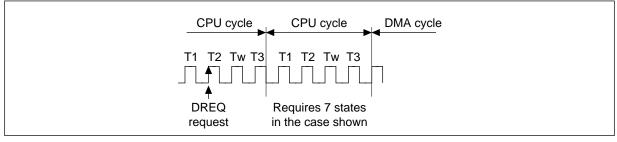


Figure 2.1 Wait State Insertion

Product	Common	Q&A No.		QA	300H-102
Topic	Addresses During DMA Transfers				
Question				С	Classification—H8/300H
Doesn't the CPU cause problems in DMAC operation if it reads the					Software
	MAR (memory address register) during DMA transfers?				Registers
MAK (IIIC	mory address register) during DWA tra	11181618 !			Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
				0	DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Re	lated Manuals
However, between re as describ	the MAR does not have any affect on Di when longword data is read, a DMA cy eading of the top 16-bits of data and the ed in the manual. As a result, the value value. The timing at which the MAR is	ycle can ente e bottom 16- read may di	er in bits of data, ffer from	Ма	nual Title
figure 2.2.	_	1			ner Technical cumentation
				Do	cument Name
	Td T1 T2 T1	T2			
	Transfer source Transfer	destination		Re	lated Microcomputer chnical Q&A
	1 2 3	1'		Titl	
	1	,		110	
2. Count 3. MAR u Note: MA	updated at transfer source. er updated. updated at transfer destination AR also updated at transfer source at 1' (du the block transfer mode).		nsfers and		
	Figure 2.2 MAR Update Tin	nıng			

References

There should be no mistake in the value read so long as the bottom 16-bit (MARH, MARL) value is read with the MOV.W instruction.

Product	Common	Q&A No.		QA	300H-103
Topic	TEND Signal Output Timing 1				
Question			Classification—H8/300H		
				Software	
Is the TEN	ND signal output at every byte/word tra	insfer?			Registers
					Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
				0	DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
					·
Answer				Re	lated Manuals
TI TENE	5 : 1: 1	. ,	1 ,	Ма	nual Title
	Signal is output when the startup sour				
	DREQ pin). In operating modes other TEND signal is driven low during the				
	transfers, it is low during the write cycl		•		
	unsfer. It is not output at every byte/wor	-			
1 olock tro	inister. It is not each at at every eyes, wer	a. (See 11gas	2.3.)		ner Technical
		1			cumentation
	Final DMA cycle	CPU cycl	le	ро	cument Name
	Td T1 T2 T1 T2				
	φ				
	Address bus	·			
	- Address bus	<u> </u>		Do.	lated Microcomputer
	RD	i I		Tec	chnical Q&A
	HWR, LWR			Tit	le
					<u></u>
	TEND				
	Figure 2.3 TEND Outpu	t			
References	3				

Product	Common		Q&A No.		QA	.300H-104
Торіс	TEND Sigr	nal Output Timing 2				
Question					(Classification—H8/300H
4 . 1	·	FEND 1 1 10				Software
At what ti	ming is the I	FEND signal output?				Registers
						Bus controller
						Interrupts
						Resets
						Power-down mode
						Instructions
						Miscellaneous
					0	DMA controller
						ITU
						Watchdog timer
						SCI
						A/D converter
						I/O ports
						, o posto
Answer					Re	lated Manuals
7 11 10 11 01	J					nual Title
		utput in the write cycle wh				
count regi	ster) become	es H'00. Figure 2.4 illustrat	tes the timin	g.		
		Final DMA cycle	CPU cy	cle		
			—		Ot	her Technical
		Td T1 T2 T1 T2				cumentation
	ф		_		Do	cument Name
	Address bus					
			_/ _			
	RD					
			<u> </u>			
	HWR, LWR				Re	lated Microcomputer
			<u></u>		Te	chnical Q&A
	TEND				Tit	le
	ETCR	H'01 H'00				
	Fi	gure 2.4 TEND Output Tin	ming			
References	s					
1.0.0.0.0.00						

Product	Common	Q&A No.		QA	300H-105	
Topic	The Relationship Between the DMAC's	s DTE and D	OTIE Bits			
Question				С	Classification—H8/300H	
W/le e e 4le e	DTIE (data tuan afan intannant anahla) h	الدادة 1 مناط	DTE (data		Software	
	DTIE (data transfer interrupt enable) benable) bit is then cleared to 0, the manu				Registers	
	ed of the CPU.	ai says illai	an interrupt		Bus controller	
is requesti	ed of the Cr o.				Interrupts	
1. Will	DMA transfer end interrupts occur con	s shown in		Resets		
figure 2.5? 2. If so, what can be done to keep interrupts from occurring?					Power-down mode	
					Instructions	
					Miscellaneous	
	DTE = 0, DTIE	= _ 1		0	DMA controller	
	DMA interrupt processing	'			ITU	
	DIMA Interrupt processing				Watchdog timer	
	Holds the valu	es			SCI	
	DTE = 0, DTIE				A/D converter	
					I/O ports	
	RTE					
-	Figure 2.5 Continuous Interrupts from	DTE and D	ГІЕ			
Answer				Re	lated Manuals	
				Ма	nual Title	
1. Yes,	interrupts will occur continuously.					
2. If D7	TE = 0 and $DTIE = 1$ (enabling interrup	ts) interrun	ts will			
	ys be produced. To prevent this, set DT	_				
	action can be used), or clear the DTIE b	•				
	iction can be used).			Other Technical		
	,			Documentation		
				Do	cument Name	
				Re	lated Microcomputer	
					chnical Q&A	
				Tit	le	
References	5					

Product	Common	Q&A No.		QA	300H-106			
Topic	DMAC Startup							
Question				С	Classification—H8/300H			
VVI. a. 41. a	DMAC is started an with an ITH sam				Software			
When the DMAC is started up with an ITU compare match interrupt, what happens if the I (interrupt mask) and UI (user bit/interrupt mask) of					Registers			
the CCR (condition code register) are masked?					Bus controller			
					Interrupts			
					Resets			
					Power-down mode			
					Instructions			
					Miscellaneous			
				0	DMA controller			
					ITU			
					Watchdog timer			
					SCI			
					A/D converter			
					I/O ports			
Answer				Re	lated Manuals			
Interrupte	selected as DMAC startup sources ar	a not affected	by the	Ма	nual Title			
_	errupt mask bits (I and UI bits). (See		by the					
	errupt mask ons (1 and 01 ons). (See	115410 2.0.)						
		SYSCR						
Per	ipheral module	UE C	CR		ner Technical			
Flag t			ו וו	F	cumentation			
compa match			- T	ро	cument Name			
the lil		•						
	Interrupt Prior determ		CPU					
	enable determined bit atio							
	circu	uit		D =	lata d Miana a ananytan			
				Tec	lated Microcomputer chnical Q&A			
			DMAC	Titl	le			
		DT	Ē					
	Figure 2.6 DMAC Start	up						
		r						

References

When an interrupt is disabled with an interrupt enable bit in a module, interrupts will not occur for either the DMAC startup request or the CPU.

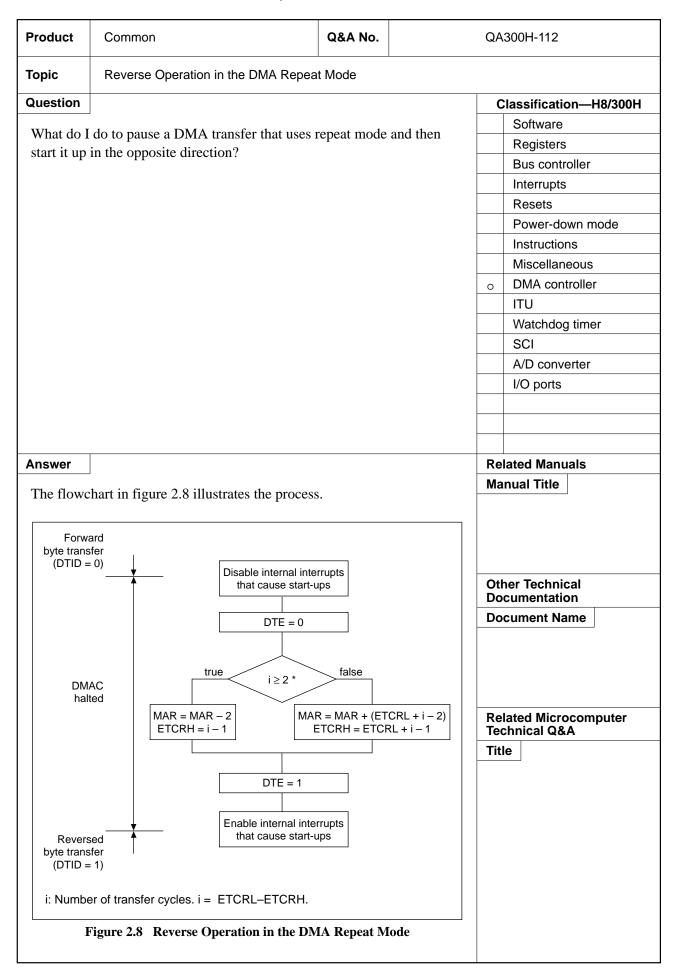
Product	Common	Q&A No.		QA	300H-107
Торіс	The DMAC and Timer Interrupts				
Question				(Classification—H8/300H
When the	DMAC startup source has compare-ma	atched the IT	TII ic an		Software
	produced to the CPU of the ITU?	attrict the 11	O, is all		Registers
merrupt	roduced to the CI of the II of.				Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
				0	DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Re	lated Manuals
DTE (data control reg When the goes to the	requests selected as startup sources star a transfer enable) bit of the DMAC's D' gister) is set to 1, and no interrupt is gen DTE bit is 0, no startup request is gene e CPU. An interrupt that is used as a sta- ously generate an interrupt to the CPU.	TCR (data to nerated to the erated and and artup source	ransfer ne CPU. n interrupt	Do	her Technical cumentation cument Name
				Re Te	lated Microcomputer chnical Q&A le
References	<u> </u>				
Keleielles	<u>*</u>				

Prod	luct	Common	Q&A No.		QA:	300H-108	
Topic	С	Operation After a DMAC End Interrupt	Is Generate	d 1			
Ques	stion				С	lassificatio	n—H8/300H
XX71 ₂	41	tuanafan aasuut uu sisten haaansa 11'0000	۱ - ماله ماله م	DMAC in in		Software	
		transfer count register becomes H'0000 end interrupt is generated:	while the I	DMAC IS III		Registers	
use	anu ai	rend interrupt is generated.				Bus contro	oller
1.	When	n is the next transfer request accepted?				Interrupts	
2		6	3.64			Resets	
2.		ransfer requests generated before the D	MA transfe	r starts		Power-do	wn mode
	ignor	ed?				Instruction	ns
						Miscellane	eous
					0	DMA cont	roller
						ITU	
						Watchdog	timer
						SCI	
						A/D conve	erter
						I/O ports	
Ansv	ver				Rel	ated Manu	als
1.	enabl reach	next transfer request is accepted when the bit is set to 1 by software. When the les H'0000 and a transfer end interrupt is DTCR (data transfer control register)	transfer cou s generated,	int register the DTE bit	Ма	nual Title	
	trans	fer is disabled. To do another transfer, se	et the transf	er count			
	regis	ter during the end interrupt routine and	then set the	DTE bit to 1.		ner Technic cumentatio	
2.	Who	the startup request is an internal inter-	nunt o CDII	interrupt is		cument Na	
2.	reque	a the startup request is an internal internested when the DTE bit is 0. For more i	nformation,	see the	See	section 8.6	Cautions on
		ware manual. When the startup request nored if it is an edge.	is an extern	al request, it	• H • H	18/3002 Har 18/3003 Har	owing manuals: dware Manual dware Manual es Hardware
					Rel Tec	ated Micro	computer A
					Titl	е	
Refe	rences	3					

Product	Common	Q&A No.		QA300H-109
Topic	Operation After a DMAC End Interrupt	Is Generate	d 2	
Question				Classification—H8/300H
When the	transfer count register becomes H'0000) while the I	DMAC is in	Software
use and th	e transfer ends, when is the transfer end	d interrupt g	enerated?	Registers
				Bus controller
				Interrupts Resets
				Power-down mode
				Instructions
				Miscellaneous
				o DMA controller
				ITU
				Watchdog timer
				SCI
				A/D converter
				I/O ports
Answer				Related Manuals
released.	transfer ends, an interrupt request is gen When the CPU captures the bus, the tra I after the executing instruction ends. (S	nsfer end in	terrupt is	
		pr	xception	Other Technical Documentation
	CPU cycle transfer cycle	CPU DM	tarted by AC transfer d interrupt	Document Name
	ф <u> </u>			
interrup	fer end t signal			Related Microcomputer Technical Q&A
	Figure 2.7 Timing at DMAC End	Interrupt		Title
References	8			

Product	Common	Q&A No.		QA	.300H-110
Topic	DMA Transfers Started up by Serial Ti	ansfers			
Question				C	Classification—H8/300H
C	than 256 tuanafana ha dana hatusaan m		(Oo la		Software
	than 256 transfers be done between med DMAC are used together to send and red	-	Os wnen		Registers
SCI allu L	DVIAC are used together to send and re-	ceive:			Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
				0	DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Re	lated Manuals
maximum more data	DMAC is started up by the SCI, I/O manumber of transfers allowed will then than this, data must be stored in memoriset with a transfer end interrupt.	be 65,536. T	To transfer	Do	her Technical cumentation cument Name
				Re	lated Microcomputer chnical Q&A
References	5				

Product	Common	Q&A No.		QA	A300H-111
Topic	Time Until DMAC Startup by the DREC	Q Pin			
Question				(Classification—H8/300H
Why is 4	states the minimum time to startup the	DMAC from	a the DDEO		Software
pin?	states the minimum time to startup the	DMAC IIOII			Registers
piii:					Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
				0	DMA controller
					ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Re	lated Manuals
	e bus arbiter internal processing time is ninimum of 4 states (the sum of these fi			Do	her Technical ocumentation
				Re	elated Microcomputer chnical Q&A
References	S				



Product	Common	Q&A No.		QA	300H-113
Topic	Use of Dual-Function Pins				
Question				С	classification—H8/300H
					Software
	DMAC is used under the following con		n the		Registers
TEND/CS	\overline{S} dual-function pin be used as a \overline{CS} ou	tput?			Bus controller
Condition	s: Full-address transfer mode, external	request (lov	v level innut		Interrupts
	$\overline{\mathbb{Q}}$ pin) for the startup source.	request (10 v	v ievei input		Resets
	ig pin, for the startup source.				Power-down mode
					Instructions
					Miscellaneous
					DMA controller
				0	ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
A					lata d Managala
Answer					lated Manuals
startup sou	be used as a $\overline{\text{CS}}$ output. When external carce, the $\overline{\text{TEND}}/\overline{\text{CS}}$ dual-function pin of the tput pin. For more information, see the manual.	concerned b	ecomes a	IVIA	nual Title
				1	ner Technical cumentation
				Do	cument Name
				foll	e section 9, I/O Ports, in the owing manual: 18/3003 Hardware Manual
				Rel	lated Microcomputer chnical Q&A
				Titl	le
References	<u> </u>				

Product	Common	Q&A No.		QA300H-114
Topic	I/O Ports and the DREQ Pin			
trans DRE	should the DTE (data transfer enable) fer control register) be set to use pins the Q pins and I/O ports as I/O ports? should dual-function pins be set for us	nat are used	both as	Classification—H8/300H Software Registers Bus controller Interrupts Resets Power-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports
2. To us direc	can be used as I/O ports without regarse dual-function pins as DREQ pins, clation register) of affected ports to 0. Whoutput is detected as DREQ input.	ear the DDF	R (data	Related Manuals Manual Title Other Technical Documentation Document Name Related Microcomputer Technical Q&A Title

Dun de et	0	00 A N-		0.0.00011.445
Product	Common	Q&A No.		QA300H-115
Topic	PWM Mode and Interrupts			
Question				Classification—H8/300H
When the	ITU is used in the PWM mode and inte	erriinte are e	nabled is it	Software
	to clear the IMFB (input capture/comp			Registers
	er status register) to 0 within the interru			Bus controller
	B automatically cleared when an IMIB		-	Interrupts
	<i>,</i>	1		Resets
				Power-down mode
				Instructions
				Miscellaneous
				DMA controller
				o ITU
				Watchdog timer
				SCI
				A/D converter
				I/O ports
Answer				Related Manuals
The IMFE	If It is flag must be cleared to 0 within the in	terrupt proc	essing	Manual Title
	he timing when the flag is cleared by the		-	
figure 2.9.		1 0		
	, T1 , T2 ,	T3 _I		
	4 11 12 1 2	-		Other Technical Documentation
		7 <u> </u>	\neg	Document Name
	φ			
Addre	ss TSR address			
				Related Microcomputer
IN	ΛF			Technical Q&A
	•	ag cleared		Title
	Figure 2.9 IMFB Flag			
				<u> </u>

References

To clear the IMFB flag, use the BCLR instruction.

Product	Common	Q&A No.		QA	300H-116
Topic	Clearing the Counters				
Question	-				lassification—H8/300H
Question			-		Software
How do I	clear the ITU counter using software?		-		Registers
			-		Bus controller
					Interrupts
			-		Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
			-	0	ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Rel	ated Manuals
	TCNT (timer counter) by writing H'000 ot cleared by rewriting the TSTR (times			Oth Doo	nual Title ner Technical cumentation
					ated Microcomputer
				Titl	е
References	8				

Product	Common	Q&A No.		QA300H-117
Topic	Pulse Output From the ITU			
Question				Classification—H8/300H
How do I	gat a specific number of pulses output	(cov. 10) and	than stan	Software
the pulse	get a specific number of pulses output	(say, 10) and	t then stop	Registers
the pulse (output:			Bus controller
				Interrupts
				Resets
				Power-down mode
				Instructions
				Miscellaneous
				DMA controller
				o ITU
				Watchdog timer
				SCI
				A/D converter
				I/O ports
Answer				Related Manuals
PWN comp	In 1 DMAC channel can be used: Pulses of M mode. In this case, the DMAC is start pare match. Set DMA transfers for 10 and anterrupt to stop the ITU. This DMA transfers for 10 and 10 an	ted up by an nd generate	ITU a transfer	Manual Title
) times; set the data transfer so that it do		- 1	
•	ation (transfer data, transfer source add	ress, transfer	destination	Other Technical Documentation
addre	ess).			Document Name
TCL (x). V	n other timers can be used: Output puls K pin (clock input pin) and events cour When the timer (x) compare register reapare match interrupt is generated and the	nted by anoth tiches a count	ner timer t of 10, a	
	00H, TIOCA0/TCLKC and TIOCB0/T ion pins. For this reason, no extra wirir			Related Microcomputer Technical Q&A
	oard to output pulses from channel 0 ar	•	-	Title
	KD as input pins.			
	n using software: Generate compare materials are using software.	_	ts each time	
References	8		'	

Topic ITU Cascade Connections Classification—H8/30 Software Registers Bus controller Interrupts Resets Power-down mode Instructions DMA controller Interrupts Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports Answer The PA2 and PA3 pins of port A are dual function pins for outputs TIOCA0 and TIOCB0 of the ITU's channel 0 and clock inputs TCLKC and TCLKD. This enables direct ITU cascade connections without external wiring. The count timing for the ITU in the host is shown in figure 2.10. Software Registers Bus controller Interrupts Related Manuals Miscellaneous DMA controller I'U Watchdog timer SCI A/D converter I/O ports	Product	Common	Q&A No.	QA300H-118	
Can cascade connections be used with the ITU? Software Registers Bus controller Interrupts Resets Power-down mode Instructions Miscellaneous DMA controller OTU Watchdog timer SCI A/D converter I/O ports	Горіс	ITU Cascade Connections			
Registers Bus controller Interrupts Resets Power-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports The PA2 and PA3 pins of port A are dual function pins for outputs TIOCA0 and TIOCB0 of the ITU's channel 0 and clock inputs TCLKC and TCLKD. This enables direct ITU cascade connections without external wiring. The count timing for the ITU in the host is shown in figure 2.10. Other Technical Document Name Related Manuals Manual Title Other Technical Document Name Related Microcomputer Technical Q&A Title Registers Bus controller Interrupts Resets Power-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports Cher Technical Document Name Related Microcomputer Technical Q&A Title	Question			Classification—	18/3001
Registers Bus controller Interrupts Resets Power-down mode Instructions Miscellaneous DMA controller o ITU Watchdog timer SCI A/D converter I/O ports Related Manuals Manual Title Related Manuals Manual Title Related Manuals Manual Title O ITU Watchdog timer SCI A/D converter I/O ports Related Manuals Manual Title O ITU Watchdog timer SCI A/D converter I/O ports O ITU Watchdog timer SCI A/D converter I/O ports O ITU Watchdog timer SCI A/D converter I/O ports O ITU Watchdog timer SCI A/D converter I/O ports O ITU Watchdog timer SCI A/D converter I/O ports O ITU Watchdog timer SCI A/D converter I/O ports Title Related Microcomputer Technical Document Name Related Microcomputer Technical Q&A Title Title	Con cosos	do connections be used with the ITI	19	Software	
Interrupts Resets Power-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports The PA2 and PA3 pins of port A are dual function pins for outputs TIOCA0 and TIOCB0 of the ITU's channel 0 and clock inputs TCLKC and TCLKD. This enables direct ITU cascade connections without external wiring. The count timing for the ITU in the host is shown in figure 2.10. (system clock) TIOCA0/TCLKC TIOCB0/TCLKD Sampling Figure 2.10 ITU Count Timing When there is no wiring from TIOCA0/TCLKC or TIOCB0/TCLKD to off the chip and the load is light, TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next \$\phi\$.	Call Casca	de connections de used with the 11 C) :	Registers	
Resets Power-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports The PA2 and PA3 pins of port A are dual function pins for outputs TIOCA0 and TIOCB0 of the ITU's channel 0 and clock inputs TCLKC and TCLKD. This enables direct ITU cascade connections without external wiring. The count timing for the ITU in the host is shown in figure 2.10. Other Technical Documentation Octument Name Related Manuals Manual Title Other Technical Document Name Related Microcomputer Technical Q&A Title				Bus controller	
Power-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports The PA2 and PA3 pins of port A are dual function pins for outputs TIOCA0 and TIOCB0 of the ITU's channel 0 and clock inputs TCLKC and TCLKD. This enables direct ITU cascade connections without external wiring. The count timing for the ITU in the host is shown in figure 2.10. Other Technical Documentation Document Name Related Microcomputer Technical Q&A Title Related Microcomputer Technical Q&A Title				Interrupts	
Instructions Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports The PA2 and PA3 pins of port A are dual function pins for outputs TIOCA0 and TIOCB0 of the ITU's channel 0 and clock inputs TCLKC and TCLKD. This enables direct ITU cascade connections without external wiring. The count timing for the ITU in the host is shown in figure 2.10. Other Technical Document Name Related Manuals Manual Title Other Technical Document Name Related Microcomputer Technical Q&A Title Title Related Microcomputer Technical Q&A Title				Resets	
Miscellaneous DMA controller ITU Watchdog timer SCI A/D converter I/O ports The PA2 and PA3 pins of port A are dual function pins for outputs TIOCA0 and TIOCB0 of the ITU's channel 0 and clock inputs TCLKC and TCLKD. This enables direct ITU cascade connections without external wiring. The count timing for the ITU in the host is shown in figure 2.10. Other Technical Documentation Other Technical Document Name Figure 2.10 ITU Count Timing When there is no wiring from TIOCA0/TCLKC or TIOCB0/TCLKD to off the chip and the load is light, TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next \$\phi\$.				Power-down m	ode
DMA controller ITU Watchdog timer SCI A/D converter I/O ports The PA2 and PA3 pins of port A are dual function pins for outputs The PA2 and TIOCB0 of the ITU's channel 0 and clock inputs TCLKC and TCLKD. This enables direct ITU cascade connections without external wring. The count timing for the ITU in the host is shown in figure 2.10. Other Technical Documentation Occument Name Related Microcomputer Toccao/TCLKC TIOCBO/TCLKD to off the chip and the load is light, TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next \$\phi\$.				Instructions	
o ITU Watchdog timer SCI A/D converter I/O ports The PA2 and PA3 pins of port A are dual function pins for outputs The PA2 and TIOCB0 of the ITU's channel 0 and clock inputs TCLKC and TCLKD. This enables direct ITU cascade connections without external wring. The count timing for the ITU in the host is shown in figure 2.10. Other Technical Documentation Document Name Figure 2.10 ITU Count Timing When there is no wiring from TIOCA0/TCLKC or TIOCB0/TCLKD to off the chip and the load is light, TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next \$\phi\$.				Miscellaneous	
Watchdog timer SCI A/D converter I/O ports Related Manuals Manual Title Related Manuals Manual Title Other Technical Document Name Figure 2.10 ITU Count Timing When there is no wiring from TIOCA0/TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next \$\phi\$.				DMA controller	
SCI A/D converter I/O ports Related Manuals Manual Title Related Manuals Manual Title Other Technical Documentation Document Name Figure 2.10 ITU Count Timing When there is no wiring from TIOCA0/TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next \$\phi\$.				o ITU	
A/D converter I/O ports				Watchdog time	r
Inswer The PA2 and PA3 pins of port A are dual function pins for outputs TIOCA0 and TIOCB0 of the ITU's channel 0 and clock inputs TCLKC and TCLKD. This enables direct ITU cascade connections without external wiring. The count timing for the ITU in the host is shown in figure 2.10. Other Technical Documentation Document Name Figure 2.10 ITU Count Timing When there is no wiring from TIOCA0/TCLKC or TIOCB0/TCLKD to off the chip and the load is light, TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next \$\phi\$.				SCI	
Related Manuals The PA2 and PA3 pins of port A are dual function pins for outputs TIOCA0 and TIOCB0 of the ITU's channel 0 and clock inputs TCLKC and TCLKD. This enables direct ITU cascade connections without external wiring. The count timing for the ITU in the host is shown in figure 2.10. Other Technical Documentation Other Technical Document Name Figure 2.10 ITU Count Timing Figure 2.10 ITU Count Timing When there is no wiring from TIOCA0/TCLKC or TIOCB0/TCLKD to off the chip and the load is light, TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next \$\phi\$.				A/D converter	
The PA2 and PA3 pins of port A are dual function pins for outputs TIOCA0 and TIOCB0 of the ITU's channel 0 and clock inputs TCLKC and TCLKD. This enables direct ITU cascade connections without external wiring. The count timing for the ITU in the host is shown in figure 2.10. Other Technical Documentation Other Technical Document Name Figure 2.10 ITU Count Timing When there is no wiring from TIOCA0/TCLKC or TIOCB0/TCLKD to off the chip and the load is light, TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next \$\phi\$.				I/O ports	
The PA2 and PA3 pins of port A are dual function pins for outputs TIOCA0 and TIOCB0 of the ITU's channel 0 and clock inputs TCLKC and TCLKD. This enables direct ITU cascade connections without external wiring. The count timing for the ITU in the host is shown in figure 2.10. Other Technical Document Name Other Technical Document Name Figure 2.10 ITU Count Timing When there is no wiring from TIOCA0/TCLKC or TIOCB0/TCLKD to off the chip and the load is light, TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next \$\phi\$.				·	
The PA2 and PA3 pins of port A are dual function pins for outputs TIOCA0 and TIOCB0 of the ITU's channel 0 and clock inputs TCLKC and TCLKD. This enables direct ITU cascade connections without external wiring. The count timing for the ITU in the host is shown in figure 2.10. Other Technical Document Name Other Technical Document Name Figure 2.10 ITU Count Timing When there is no wiring from TIOCA0/TCLKC or TIOCB0/TCLKD to off the chip and the load is light, TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next \$\phi\$.					
The PA2 and PA3 pins of port A are dual function pins for outputs TIOCA0 and TIOCB0 of the ITU's channel 0 and clock inputs TCLKC and TCLKD. This enables direct ITU cascade connections without external wiring. The count timing for the ITU in the host is shown in figure 2.10. Other Technical Document Name Other Technical Document Name Figure 2.10 ITU Count Timing When there is no wiring from TIOCA0/TCLKC or TIOCB0/TCLKD to off the chip and the load is light, TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next \$\phi\$.					
The PA2 and PA3 pins of port A are dual function pins for outputs TIOCA0 and TIOCB0 of the ITU's channel 0 and clock inputs TCLKC and TCLKD. This enables direct ITU cascade connections without external wiring. The count timing for the ITU in the host is shown in figure 2.10. Other Technical Document Name Figure 2.10 ITU Count Timing When there is no wiring from TIOCA0/TCLKC or TIOCB0/TCLKD to off the chip and the load is light, TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next \$\phi\$.	nswer			Related Manuals	
The PA2 and PA3 pins of port A are dual function pins for outputs TIOCA0 and TIOCB0 of the ITU's channel 0 and clock inputs TCLKC and TCLKD. This enables direct ITU cascade connections without external wiring. The count timing for the ITU in the host is shown in figure 2.10. Other Technical Document Name Figure 2.10 ITU Count Timing When there is no wiring from TIOCA0/TCLKC or TIOCB0/TCLKD to off the chip and the load is light, TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next \$\phi\$.				Manual Title	
and TCLKD. This enables direct ITU cascade connections without external wiring. The count timing for the ITU in the host is shown in figure 2.10. Other Technical Documentation Document Name Figure 2.10 ITU Count Timing When there is no wiring from TIOCA0/TCLKC or TIOCB0/TCLKD to off the chip and the load is light, TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next \$\phi\$.				W.C.	
external wiring. The count timing for the ITU in the host is shown in figure 2.10. Other Technical Documentation Document Name Related Microcomputer Technical Q&A Title When there is no wiring from TIOCA0/TCLKC or TIOCB0/TCLKD to off the chip and the load is light, TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next \$\phi\$.			-	KC	
figure 2.10. Other Technical Documentation Document Name Figure 2.10 ITU Count Timing When there is no wiring from TIOCA0/TCLKC or TIOCB0/TCLKD to off the chip and the load is light, TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next \$\phi\$.		CD - Enis enables direct LLU cascade			
Other Technical Documentation Compare Manage Document Name	41				
Sampling Figure 2.10 ITU Count Timing When there is no wiring from TIOCA0/TCLKC or TIOCB0/TCLKD to off the chip and the load is light, TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next φ.		viring. The count timing for the ITU		1	
Sampling Figure 2.10 ITU Count Timing When there is no wiring from TIOCA0/TCLKC or TIOCB0/TCLKD to off the chip and the load is light, TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next φ.		viring. The count timing for the ITU			
TIOCAO/TCLKC TIOCBO/TCLKD Sampling Figure 2.10 ITU Count Timing When there is no wiring from TIOCAO/TCLKC or TIOCBO/TCLKD to off the chip and the load is light, TCLKC and TCLKD sample the compare match output of TIOCAO and TIOCBO at the rise of the next \$\phi\$.		viring. The count timing for the ITU		Other Technical	
Sampling Figure 2.10 ITU Count Timing When there is no wiring from TIOCA0/TCLKC or TIOCB0/TCLKD to off the chip and the load is light, TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next \$\phi\$.	figure 2.1	viring. The count timing for the ITU 0.		Other Technical Documentation	
Sampling Figure 2.10 ITU Count Timing When there is no wiring from TIOCA0/TCLKC or TIOCB0/TCLKD to off the chip and the load is light, TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next \$\phi\$.	figure 2.1	viring. The count timing for the ITU 0.		Other Technical Documentation	
Sampling Figure 2.10 ITU Count Timing When there is no wiring from TIOCA0/TCLKC or TIOCB0/TCLKD to off the chip and the load is light, TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next φ.	figure 2.1	riring. The count timing for the ITU 0.		Other Technical Documentation	
Figure 2.10 ITU Count Timing When there is no wiring from TIOCA0/TCLKC or TIOCB0/TCLKD to off the chip and the load is light, TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next \$\phi\$.	figure 2.1 (syste	m clock)		Other Technical Documentation	
When there is no wiring from TIOCA0/TCLKC or TIOCB0/TCLKD to off the chip and the load is light, TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next \$\phi\$.	figure 2.1 (syste	on clock) O/TCLKC O/TCLKD	in the host is shown in	Other Technical Documentation	
When there is no wiring from TIOCA0/TCLKC or TIOCB0/TCLKD to off the chip and the load is light, TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next \$\phi\$.	figure 2.1 (syste	on clock) O/TCLKC O/TCLKD	in the host is shown in	Other Technical Documentation Document Name Related Microcom	puter
off the chip and the load is light, TCLKC and TCLKD sample the compare match output of TIOCA0 and TIOCB0 at the rise of the next φ.	figure 2.1 (syste	on clock) O/TCLKC O/TCLKD	in the host is shown in	Other Technical Documentation Document Name Related Microcom Technical Q&A	puter
compare match output of TIOCA0 and TIOCB0 at the rise of the next φ.	(syste	riring. The count timing for the ITU 0. m clock) O/TCLKC O/TCLKD Figure 2.10 ITU Count 7	Sampling Fiming	Other Technical Documentation Document Name Related Microcom Technical Q&A Title	puter
	(syste	re is no wiring from TIOCAO/TCLK	Sampling Timing CC or TIOCBO/TCLKE	Other Technical Documentation Document Name Related Microcom Technical Q&A Title	puter
References	(syste TIOCAC TIOCBC	re is no wiring from TIOCAO/TCLKC ip and the load is light, TCLKC and	Sampling Timing TCLKD sample the	Other Technical Documentation Document Name Related Microcom Technical Q&A Title	puter
References	(syste TIOCAC TIOCBC	re is no wiring from TIOCAO/TCLKC ip and the load is light, TCLKC and	Sampling Timing TCLKD sample the	Other Technical Documentation Document Name Related Microcom Technical Q&A Title	puter
	(syste TIOCA) TIOCBO	re is no wiring from TIOCA0/TCLKC ip and the load is light, TCLKC and match output of TIOCA0 and TIOCI	Sampling Timing TCLKD sample the	Other Technical Documentation Document Name Related Microcom Technical Q&A Title	puter

Product	Common	Q&A No.		QA	300H-119
Торіс	Setting the ITU's PWM Output				
Question				С	lassification—H8/300H
When the	ITILis used in DWM mode, how should	d the TIOD	(timer I/O		Software
	ITU is used in PWM mode, how shoul gister) be set?	a the HOR	(timer I/O		Registers
connor re	gister) be set:				Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
				0	ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
Answer				Rel	ated Manuals
each of th	ne PWM bit of the TMDRs (timer mode e channels of the ITU, GRA/GRB are user or output setting, regardless of the cont	ised as outp	ut compare	Dod	ner Technical cumentation cument Name lated Microcomputer chnical Q&A
References	5				

Product	Common	Q&A No.	QA300H-120-1
оріс	ITU Output and Port Output		
Question			Classification—H8/300H
XX71 41	ITIL : CDD	. (11	Software
	ITU is set to toggle output on a GRB lual-function register B) compare ma		- Dogictore
	figure 2.11, what kind of value is out		
	it to ITU output?	put when chang	Interrupts
ort outpe	it to 110 output.		Resets
			Power-down mode
(TCN	T value)		Instructions
GRE	A		Miscellaneous
Orti		Λ Λ	DMA controller
		/ / /	/
	V V V V V V V		Watchdog timer
	3 output,		(Time) SCI
port	output :: :		A/D converter
	ITU output Port outp		ITU output
	110 daipat Port daip	: \	ITU output output or
			output?
	ggle output Set for port output with compare output upon compare	Set for toggle outpupon compare	put
	compare output upon compare n the TIOR match in the TIOR	match in the TIO	Related Manuals
(timer I/O c	ontrol register) (timer I/O control register) (timer I/O control register) (timer I/O control register)	timer I/O control reg	Manual Title
	4.043.04		
	Figure 2.11 ITU Output and Por	t Outnut (O)	
	rigure 2.11 The Output und For	t Output (Q)	
			Other Technical
			Documentation
			Documentation
			Documentation
			Documentation
			Document Name
			Documentation
			Document Name Related Microcomputer
			Document Name Related Microcomputer Technical Q&A
			Document Name Related Microcomputer Technical Q&A
			Document Name Related Microcomputer Technical Q&A
			Document Name Related Microcomputer Technical Q&A
eference	3		Document Name Related Microcomputer Technical Q&A
eference	3		Document Name Related Microcomputer Technical Q&A

Product	Common	Q&A No.	QA300H-120-2
Topic	ITU Output and Port Output		
Answer			

- 1. When port output is changed to ITU output, the value from before the change is output.
- 2. When a compare match signal is generated at the point when the port output is to be changed to ITU output, the value changes. (See figure 2.12.)

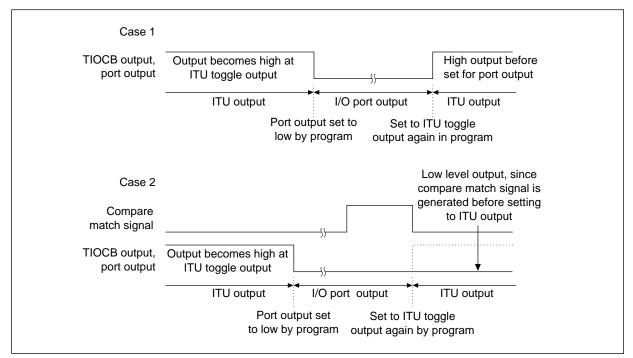


Figure 2.12 ITU Output and Port Output (A)

References

- 1. When the ITU was started after a reset, the TIOCn output is low until the first compare match occurs.
- 2. When set to input capture and output is disabled, the output level changes when an input capture occurs.

Product	Common	Q&A No.	QA:	300H-121-1
Торіс	ITU Settings			
Question				Classification—H8/300H
Dlagga avi	alain in datail the nules width	cycle cettings and registe		Software
_	plain in detail the pulse width, or ITU pulse output as well as			Registers
clock.	II II O puise output as well as	the relationship to the mic	71141	Bus controller
CIOCK.				Interrupts
				Resets
				Power-down mode
				Instructions
				Miscellaneous
				DMA controller
			0	ITU
				Watchdog timer
				SCI
				A/D converter
				I/O ports
Answer			Re	elated Manuals
]		Ma	anual Title
the follow	eputting pulses in the PWM maying equation.	ode, the duty can be found	from	
•	y = n + 1 / N + 1 y = 0 GPA = n (set the counter $y = 0$)	ala commonanding to the I		
	the GRA = n (set the counter value $h - 1$), and	alue corresponding to the 1		ther Technical
	B = N (set the counter value co	orresponding to the cycle –	_	ther Technical ocumentation
OND	- 14 (set the counter value of	mesponding to the eyele	1/	ocument Name
Example:	When the operating frequen for the count is $\phi/2$ and GRI (with an N of 9):	-	clock	
(n +	1)/(9+1) = 0.5		R ₆	elated Microcomputer
GRA mus	st be set to 4. The exact timing	g is shown in figures 2.13 t	to 2.16. Te	echnical Q&A
References	<u> </u>		111	tle

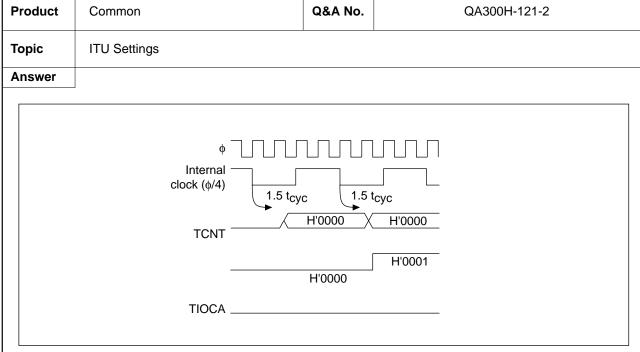


Figure 2.13 ITU Settings (1)

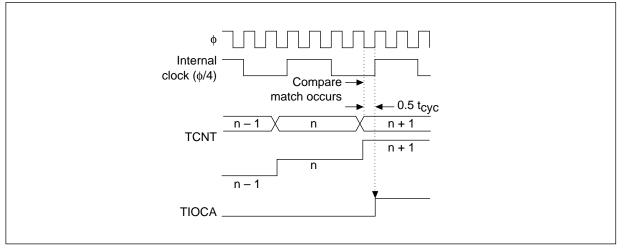


Figure 2.14 ITU Settings (2)

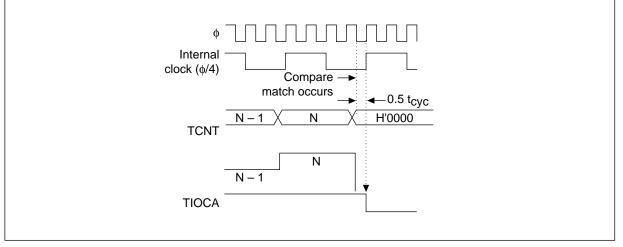


Figure 2.15 ITU Settings (3)

Product	Common	Q&A No.	QA300H-121-3
Topic	ITU Settings		
Answer			

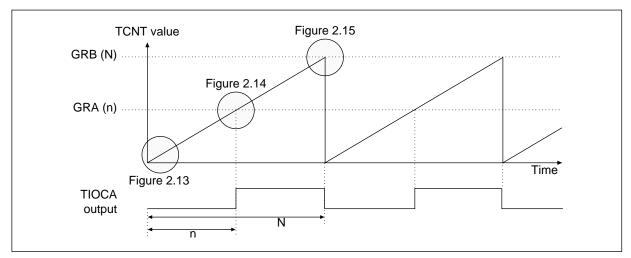


Figure 2.16 ITU Settings (4)

Product	Common	Q&A No.		QA	300H-122
Topic	Independent Operation of TCNT4 Usin	ng Reset-Syr	chronized PWI	М Мо	de
Question				С	Classification—H8/300H
The menu	al states that "TCNT4 mine independen	11.11 m.h.a	va a t		Software
	al states that "TCNT4 runs independent zed PWM mode is used. Do this mean	-			Registers
purposes?		it can be use	d for other		Bus controller
purposes.					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
				0	ITU
					Watchdog timer
					SCI
					A/D converter
					I/O ports
_				-	
Answer					lated Manuals nual Title
only coun GRB4. Th	chronized PWM mode uses channel 3 ters and registers it uses are TCNT3, Chis allows TCNT4 to be used independent or run it as an interval timer using countries.	GRA3, GRA4 ently. One w	I, GRB3 and ay to use it		
					ner Technical cumentation
					cument Name
				Re Tec	lated Microcomputer chnical Q&A
				Titl	le
References	s			1	

Product	Common	Q&A No.		QA30	0H-123
Торіс	Halting the WDT's System Clock				
Question				Cla	ssification—H8/300H
When the	system clock is halted, does the WDT	(watchdog t	imer) detect		Software
abnormali		(wateriasg t	anier) detect		Registers
				E	Bus controller
				I	nterrupts
				F	Resets
				F	Power-down mode
				I	nstructions
				ı	Miscellaneous
					DMA controller
				I	TU
					Vatchdog timer
					SCI
					VD converter
					/O ports
Answer				Relat	ed Manuals
	system clock of the entire LSI is halted				ıal Title
				Docu	r Technical mentation ment Name
				Relat Techi Title	ed Microcomputer nical Q&A
References	S				

Product	Common	Q&A No.		QA	300H-124
Topic	Using the RDR and TDR When the SC	CI Is Not Beir	ng Used		
Question				C	Classification—H8/300H
When the	SCI is not being used:				Software
when the	SCI is not being used:				Registers
1. Can	the RDR (receive data register) be used	as a data re	gister?		Bus controller
					Interrupts
2. Can	the TDR (transmit data register)?				Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
				0	SCI
					A/D converter
					I/O ports
Answer					lated Manuals
Yes and N	lo.			Ма	nual Title
	RDR cannot be used as a data register b	because it is	a read-only		
regis	ter.				
2. The	ΓDR can be used as a data register.				
	12 10 cm oc docu no m cmm 10g.scom				ner Technical cumentation
					cument Name
				Re	lated Microcomputer
					chnical Q&A
			_	Tit	le
References	•				
Kererences	5				

Product	Common	Q&A No.		QA	300H-125
Торіс	I/O Settings of Clock Pins for the SCI				
Question				(Classification—H8/300H
When the	SCI is being used, does the DDR (date	direction re	gistor) of		Software
	SCI is being used, does the DDR (data or the SCK (serial clock) pin set the I/O				Registers
pin?	of the SCK (serial clock) pin set the 1/O	specificano	ni ioi tilat		Bus controller
piii.					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
				0	SCI
					A/D converter
					I/O ports
Answer				Re	lated Manuals
mode regi	by the C/A bit (communications mode) ster) and the CKE1 and CKE0 (clock entrol register). Setting the DDR of the p	nable) bits o	of the SCR	Do Do	her Technical cumentation cument Name
References	6				

Product	Common	Q&A No.		QA	300H-126
Topic	Serial I/O Pin State				
Question				С	classification—H8/300H
A ft an wain	a the dual function nine that can be use	d og I/O mor	to (TVD		Software
	g the dual-function pins that can be use SCK) as SCI pins. I reset them as I/O r	_			Registers
RXD and SCK) as SCI pins, I reset them as I/O ports with the SCR (serial control register) and SMR (serial mode register). What happens to					Bus controller
	of the DDR (data direction register) pi	-			Interrupts
the variety	of the BBR (data direction register) pr	ns when this	у парреня.		Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
				0	SCI
					A/D converter
					I/O ports
Answer				Rel	lated Manuals
This mean	tion does not affect the contents of the as that in the case described above the I being set as an SCI pin.		_	Ма	nual Title
					ner Technical cumentation
				Do	cument Name
				Rel Tec	lated Microcomputer chnical Q&A
				Titl	e
References	3				

Product	Common	Q&A No.		QA	300H-127
Торіс	Simultaneous Transmission and Rece	ption with the	e SCI		
Question				С	Classification—H8/300H
VVIa a sa 41a a	CCI is being used our transmission us	!			Software
	SCI is being used, can transmission usignition using the state of the	-			Registers
occui siiii	untaneous with reception on the externa	i clock (of v	rice versa):		Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
				0	SCI
					A/D converter
					I/O ports
Answer					lated Manuals nual Title
prevents s	ock source can be selected as the SCI tr imultaneous transmission and reception multaneous transmission/reception usin	n using 2 typ	oes of		
					ner Technical cumentation
				Do	cument Name
				Re Tec	lated Microcomputer chnical Q&A
				Tit	le
References	3				

Product	Common	Q&A No.		QA	300H-128
Topic	RDRF				
Question				C	Classification—H8/300H
XX71 . 1	······································	1 .	. C 11) CI		Software
	pens if, when clearing the RDRF (recei	_	_		Registers
	R (serial status register) to 0 during SCl ly without first reading a 1?	reception, i	t is cleared		Bus controller
10 0 direct	Ty without first reading a 1?				Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
				0	SCI
					A/D converter
					I/O ports
					, o posto
Answer				Re	lated Manuals
					nual Title
	be cleared. When the BCLR instruction				
	in byte units, then the bit that correspor		-		
	0 and a write occurs, again in byte unit				
	(RXI interrupt processing routine), the	BCLR instr	ruction thus		
cannot cie	ar the RDRF flag.			Otl	her Technical
					cumentation
				Do	cument Name
				Re Te	lated Microcomputer chnical Q&A
				Tit	le
References	8				

Product	Common	Q&A No.		QA3	00H-129-1
Горіс	Setting for Asynchronous Trans	smission			
Question				С	lassification—H8/300
A l	and the CCI	Ham de Leet it to	1		Software
Asynchronous transmission uses the SCI. How do I set it to do a transfer by software (i.e., using the data empty interrupt (TXI) but not the					Registers
DMAC)?			t tile		Bus controller
				Interrupts	
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
				0	SCI
					A/D converter
					I/O ports
					·
Answer				Re	ated Manuals
When the	TDRE = 1, the data empty inter	runt is always gans	rated and	Ma	nual Title
	set to 1. There are thus 2 metho		raicu anu		
112 13	sector. There are thus 2 metho	. as			
	ng the first byte with an interrup	t processing routing	e:		
	- 0 (transfer counter)				
	1 (transfer enable)				ner Technical
TIE :	= 1 (empty interrupt enable)				cumentation
2. Setti	ng the first byte with the initializ	zation:		Do	cument Name
	- 1 (transfer counter)	zation.			
	1 (transfer enable)				
	byte set to TDR				
	E cleared (transfer starts, TDRE	$E = 1$ after TDR \rightarrow	TSR		
	= 1 (empty interrupt enable)				lated Microcomputer chnical Q&A
				Titl	
	ase, the TXI interrupt processin	g routine is as shov	n in the		
figure 2.1	1.				
References	<u> </u>				
zeierence					

Product	Common	Q&A No.	QA300H-129-2				
Topic	Setting for Asynchronous Transmission						
Answer							

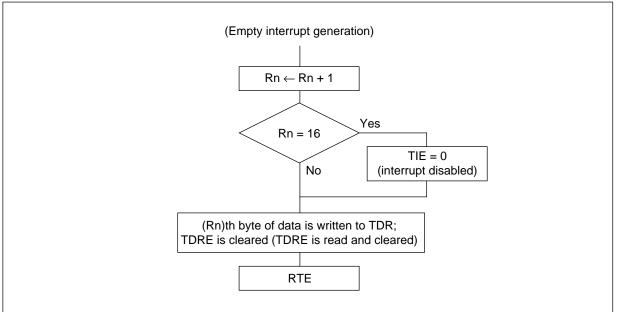


Figure 2.17 TXI Interrupt Processing Routine

	rconnical gacs		AIIG AIIS	WCI 3		
Product	Common	Q&A No.		QA300H-130-1		
Topic	How Data Is Transferred to the TDR					
Question				Classification—H8/300H		
Are there space to the figure 2.18	sfer using software? he DMAC? H8/3003 SCI	DRAM	as shown in	Software Registers Bus controller Interrupts Resets Power-down mode Instructions Miscellaneous DMA controller ITU Watchdog timer o SCI A/D converter I/O ports		
	Figure 2.18 Transferring Data to	the TDR				
A m a a w				Related Manuals		
Answer				Manual Title		
1. 16-bit bus spaces can be accessed in byte units. Read transfer data on the DRAM <u>1 byte at a time</u> and transfer it to the SCI's TDR. To transfer data stored in the transfer buffer, do as shown in figure 2.19.						
	10000			Other Technical Documentation		
	10010			Document Name		
No	ote: Start address of transfer buffer 10000 s	stored in ER().	Related Microcomputer Technical Q&A		
	Figure 2.19 Transfer Buffe	er		Title		
References	3					

Product	Common			Q&A No.	QA300H-130-2			
Торіс	How Data Is	Transferred to	the TDR					
Answer								
LOOP:		#12,R2L for interrupt R2L	Can be p Copy the R3L and	laced in the				
	BNE	LOOP	Continue	e until the tra	ransfer			
TxI Interrupt: MOV.B @ER0+,R3L		Transfer the transfer data to the SCI's TDR						
	MOV.B BCLR BNE	R3L,@TDR #7,@SSR LOOP	Clear TD		counter by 1			

2. Using the DMAC: Start up the DMAC with the SCI's TXI interrupt and transfer the transfer data on DRAM 1 byte at a time to the SCI's TDR. Byte needs to be specified as the size in the DMAC. (Word size transfers are impossible, since they start up the DMAC at every transmission of a byte.)

References

The bus controller function can be used to enable word-sized transfers as shown in figure 2.20. For each read cycle (16-bit data), 2 consecutive write cycles of 8-bit data are necessary.

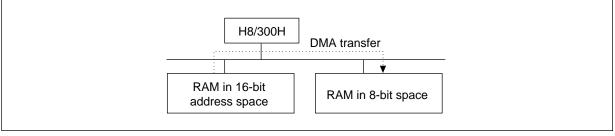


Figure 2.20 Using the Bus Controller Function to Enable Word-Sized Transfers

Product Common Q&A No.				QA300H-131A-1		
Topic	Timing of Setting RDRF					
Question				Classification—H8/300H		
				Software		
	1. When data reception ends, the RDRF (receive data register full) flag		Registers			
	e SSR (serial status register) is set to 1.	At what poi	int in the	Bus controller		
asyno	chronous mode is the RDRF set?			Interrupts		
2. When	n is it set in clock-synchronous mode?			Resets		
2. ***	is it set in clock synemonous mode.			Power-down mode		
				Instructions		
				Miscellaneous		
				DMA controller		
				ITU Watch days Gaves		
				Watchdog timer		
				o SCI		
				A/D converter		
				I/O ports		
Answer			Related Manuals			
1. The l	RDRF flag is set after the MSB data is	received and	d the data	Manual Title		
	ling clock falls. (See figure 2.21.)					
•						
Basic	clock 1 2 3 4 5 6 7 8 9 10111213141516 1 2 3 4	5	13141516			
Dasic		וטטטטטטטט !!	JUUUL	Other Technical		
				Documentation		
Danaha				Document Name		
Receive	data D7 Stop		<u> </u>			
Data same	ation a	П				
Data sam	piing	<u>\</u>				
	DRF	→		Related Microcomputer Technical Q&A		
	DIT			Title		
				Title		
	When SCK clock source is the internal clock					
,	states. When SCK clock source is an exterr	iai ciock, 3-4	siales.			
	Figure 2.21 8-Bit Data, 1 Sto	p Bit				
Doforonos						
References						

Product	Common	Q&A No.	QA300H-131A-2
Topic	Timing of Setting RDRF		
Answer			

2. The RDRF flag is set after the MSB data is received and synchronization clock rises. (See figure 2.22.)

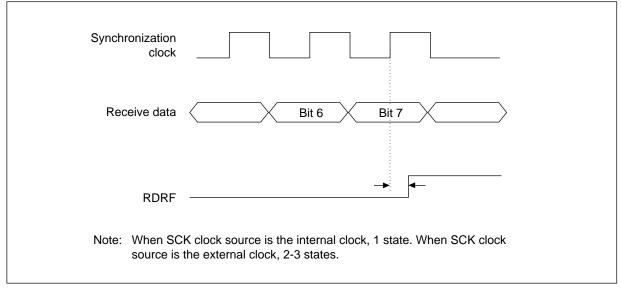


Figure 2.22 8-Bit Data

		I	ı			
Product	Common	Q&A No.	(QA300H-132A-1		
Topic	Timing of Setting TDRE					
Question				Classification—H8/300H		
4 ****		SE (:		Software		
	n 8-bit data transmission ends, the TDI	•	•	Registers		
_	y) flag of the SSR (serial status registe		. At what	Bus controller		
point	in the asynchronous mode is the TDR	E set?		Interrupts		
2. Whe	n is it set in clock-synchronous mode?			Resets		
				Power-down mode		
				Instructions		
				Miscellaneous		
				DMA controller		
				ITU		
				Watchdog timer		
				o SCI		
				A/D converter		
				I/O ports		
Answer				Related Manuals		
Th. TDD		•	Control days to	Manual Title		
	E flag is set at different times when the		ission data in			
the ISK (transmit shift register) and when there	is not.				
1. Asyr	chronous mode. (See figure 2.23.)					
,	` ' '					
				Other Technical		
	1 2 3 4 5 6 7 8 9 101112131415161 2 3 4 9	5 6 7 8 9 10111213	141516 ППП	Documentation		
Basic			JUUL	Document Name		
_		6				
Transm	it data _ Stop bit	Start bit				
	TDD5					
	TDRE When SCK clock	source is the ir	nternal	Related Microcomputer		
	clock, 4 state. When SCK clock source is the external			Technical Q&A		
	clock, 4–5 state.	Source is the e	Atemai	Title		
I	Figure 2.23 Transmit data in TSR (Asyr	ichronous m	ode)			
References				L		

Product	Common	Q&A No.	QA300H-132A-2
Topic	Timing of Setting TDRE		
Answer			

The start of transmission according to the setting of the TE (transmit enable) bit also follows this timing. (See figure 2.24.)

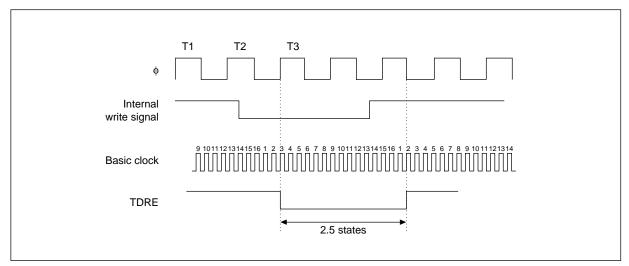


Figure 2.24 No transmit data in TSR (Asynchronous mode)

2. Clock-synchronous mode (See figures 2.25 and 2.26.)

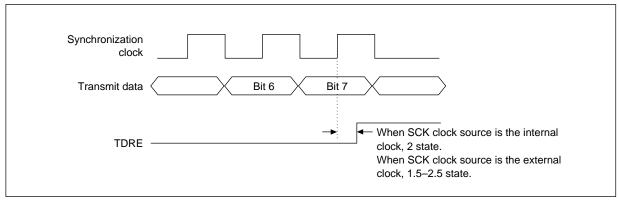


Figure 2.25 Transmit data in TSR (Clock-synchronous mode)

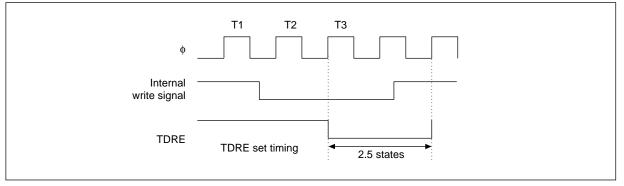


Figure 2.26 No transmit data in TSR (Clock-synchronous mode)

Product	Common	Q&A No.		QA	300H-133
Торіс	SCI Reception Errors				
Question				C	Classification—H8/300H
Dry motum	ing to the main routing during a receive	arrar intarr	unt routing		Software
By returning to the main routine during a receive error interrupt routine without clearing the reception error flags of the SSR (serial status register), is a receive error interrupt generated again?					Registers
					Bus controller
register), i	register), is a receive error interrupt generated again:				Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
				0	SCI
					A/D converter
					I/O ports
Answer				Re	lated Manuals
main rout	ve error flag is not automatically cleare ine (after executing the RTE instruction will be generated again.		-	Otl	her Technical
					cumentation
					cument Name
				Tec	chnical Q&A
				Tit	le
References	S				

Product	duct Common Q&A No. QA300H-134				300H-134	
Topic	Operating the SCI in External Clock M	ode				
Question				С	lassification—H8/300H	
XX/1	COL:		1 1		Software	
when the	SCI is operated in clock-synchronous	external cloc	ck mode:		Registers	
1. Does	the SCI start the next transmit operation if, after the				Bus controller	
	pletion of 1 byte of data transmission, the				Interrupts	
appli	applied to the SCK pin before the H8/300H CPU writes to the TDR				Resets	
(transmit data register)?				Power-down mode		
					Instructions	
2. What	t happens after reception?				Miscellaneous	
					DMA controller	
					ITU	
					Watchdog timer	
				0	SCI	
					A/D converter	
					I/O ports	
					•	
Answer				Re	lated Manuals	
	2.11			Ma	nual Title	
The result	s are as follows:					
1. Trans	smission does not start. The next transn	nission will	not start			
	the TDRE (transmit data register empty					
	s register) is cleared to 0.	, ,	`			
	-			Oth	ner Technical	
	otion starts, however, an overrun error will occur unless the			Documentation		
	F (receive data register full) of the SSR	k is cleared	before the	Do	cument Name	
next	data is completely received.					
				Re	lated Microcomputer chnical Q&A	
				Titl		
				- 110		
References						
iveletetice:	2					

Product	Common	Q&A No.		QA	300H-135
Topic	System Clocks and SCK Phases				
Question				C	Classification—H8/300H
	I				Software
	(serial transfer clock) output synchron	em clock (\$)		Registers	
rise or fall	1?				Bus controller
					Interrupts
					Resets
					Power-down mode
					Instructions
					Miscellaneous
					DMA controller
					ITU
					Watchdog timer
				0	SCI
					A/D converter
					I/O ports
Answer					lated Manuals nual Title
				Otl Do	ner Technical cumentation
					lated Microcomputer chnical Q&A
References	S				

Product		Common	Q&A No.	QA300H-136			
Topi	С	Changing the A/D Mode and Channel	Changing the A/D Mode and Channel During A/D Conversion				
Que	stion				С	lassification—H8/300H	
1	TT	1. I'	1 A /D		Software		
1.	How	do I switch the A/D conversion mode	during A/D	conversion?	Registers		
2.	How	do I change the selected channel during	g A/D conve	ersion?		Bus controller	
					Interrupts		
						Resets	
						Power-down mode	
						Instructions	
						Miscellaneous	
						DMA controller	
						ITU	
						Watchdog timer	
						SCI	
					0	A/D converter	
						I/O ports	
Ans	wer					ated Manuals	
1.	Swite	thing the A/D conversion mode during	A/D conver	rsion will	Mai	nual Title	
		ase conversion accuracy. We advise ag					
2.		ging the selected channel during A/D o					
		problem as switching the conversion n	node. Agaın	, we advise			
	again	St it.				er Technical cumentation	
						cument Name	
					Rel	ated Microcomputer	
					Tec	hnical Q&A	
					Titl	e	
Refe	rences	;					

Before switching the A/D conversion mode or changing the selected channel, check the ADF (A/D end flag) in the ADCSR (A/D control/status register).

	Common		Q&A No.		QA300H-137			
оріс	Using General-Purpose Ports							
Question				Classification—H8/300H				
Can instructions that manipulate bits be used on I/O ports when a bit of					Software			
the port is designated an output port?					Registers			
					Bus controller			
						Interrupts		
						Resets		
						Power-down mode		
						Instructions		
						Miscellaneous		
						DMA controller		
						ITU		
						Watchdog timer		
						SCI		
						A/D converter		
					0	I/O ports		
nswer					Rela	ated Manuals		
	J					ual Title		
Yes. When a port set as an output port is read by the CPU, the contents of the port data register (DR) are read, regardless of the pin state. When an input port is read, the pin state is read. This means there are no problems in using instructions that manipulate bits. When there are pins in the port that have been designated input ports, however, the DR values of the input ports will become undefined (pin state). (See figure 2.27.)					Other Technical Documentation			
	been designated in	put ports, however, t			Doc	umentation		
	been designated in s will become und	oput ports, however, the fined (pin state). (See Settings Settings			Doc	_		
	been designated in s will become und	Output Input settings settings			Doc	umentation		
	been designated in s will become und DDR contents Pin status	Output Input settings settings 1 1 1 1 0 0 1 1 0 0			Doc	umentation ument Name		
	been designated in s will become und DDR contents Pin status DR contents	Output Input settings Settings Settings 1 1 1 1 1 0 0 0 0 0 1 1 0 1 0 1 0 1 0			Doc	umentation		
input port	been designated in s will become und DDR contents Pin status	Output Input settings settings 1 1 1 1 0 0 1 1 0 0		7.) to U s with	Doc	umentation ument Name ated Microcomputer		

The BSET, BCLR, BNOT, BST and BIST instructions manipulate bits.

Product	Common	Q&A No.		QA300H-138		
Topic	Processing Ports When Not in Use					
Question How shou	lld I process ports that are not in use?		Classification—H8/300H Software			
				Registers Bus controller Interrupts Resets		
				Power-down mode Instructions Miscellaneous		
				DMA controller ITU Watchdog timer		
				SCI A/D converter		
				o I/O ports		
Answer				Related Manuals Manual Title		
1. Clear the DDR (data direction register) of I/O ports to 0 to put them in input state and pull each pin up or down with a resistance of about 10 kΩ.						
2. Hand	lle input-only ports the same way.			Other Technical Documentation		
				Document Name		
			_	Related Microcomputer Technical Q&A Title		
References	S		1			