CML Semiconductor Products

PRODUCT INFORMATION

FX439 FFSK Modem

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Provisional Issue

Features/Applications

- 1200 Baud FFSK Modem
- Meets Cellular and Trunked Radio Specifications
- Full-Duplex 1200 Baud
- On-Chip Rx and Tx Bandpass Filters
- Clock Recovery and Carrier Detect Facilities
- Pin Selectable Xtal/Clock Frequencies (1.008MHz or 4.032MHz Input)
- Mobile and Cellular Radio Data Signalling
- NMT 450/900
- Band III
- Radiocom 2000
- ZVEI
- Personal Radio
- Portable Data Terminals
- General Purpose Applications

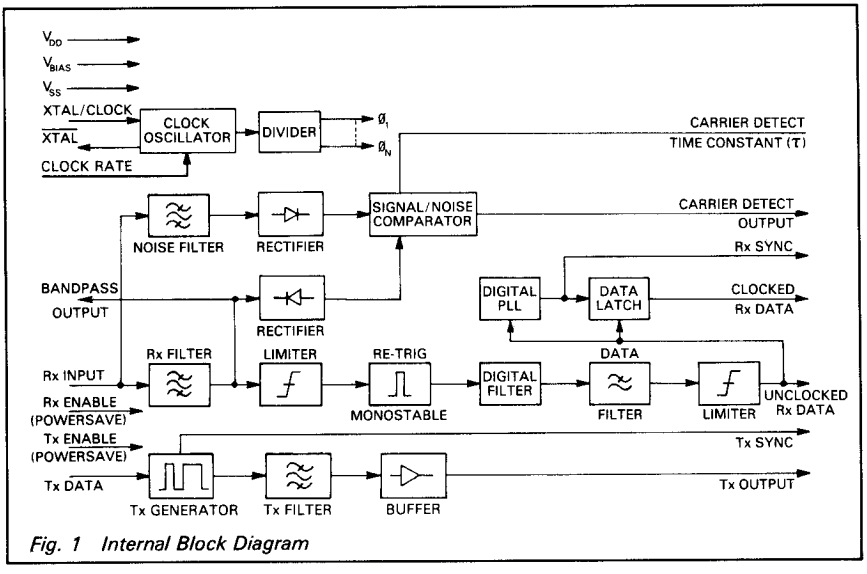


Fig. 1 Internal Block Diagram

FX439

Brief Description

The FX439 is a single-chip CMOS LSI circuit which operates as a 1200 baud FFSK modem. The mark and space frequencies are 1200Hz and 1800Hz phase continuous and the frequency transitions occur at the zero crossing point. The transmitter and receiver will work independently, thus providing full-duplex operation at 1200 baud. The baud rate, transmit mark and space frequencies, Tx and Rx synchronization are all derived from a highly stable Xtal oscillator. The on-chip oscillator is capable of working at one of two input frequencies, from a 1.008MHz or 4.032MHz external Xtal/clock input, frequency being pin selectable with the 'Clock Rate' logic input. The device includes circuitry for carrier detect and facility for the Rx clock recovery. An on-board switched capacitor 900Hz – 2100Hz bandpass filter provides optimum carrier filtering. The use of switched capacitor analogue filters and digital signal processing results in excellent dynamic performance with few external components, the CMOS process and current saving techniques offer low standby supply current for portable battery powered applications.

Pin Number Function

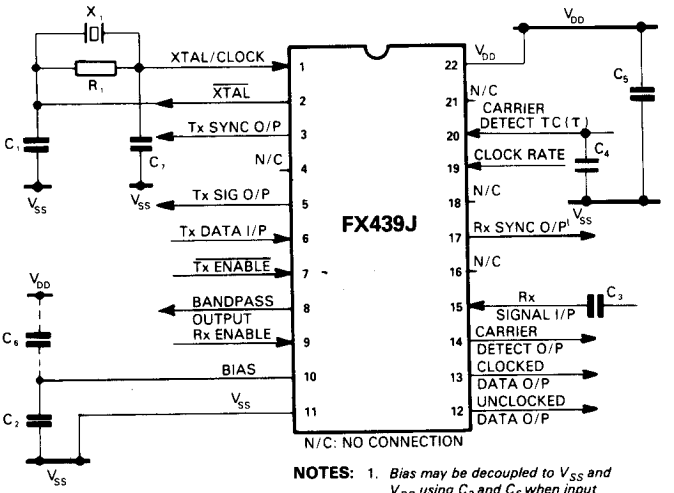
FX439 DW	FX439 J	FX439 LG/LS	Function
1	1	1	**Xtal/Clock:** The input to the on-chip inverter, for use with either a 1.008MHz or a 4.032MHz Xtal or external clock. Clock frequency selection is by the "Clock Rate" input pin.
2	2	2	**$\overline{\text{Xtal}}$:** Output of the on-chip inverter (See Figure 2).
3	3	3	**Tx Sync O/P:** A 1200Hz squarewave used to synchronize the input of logic data and transmission of the FFSK signal (See Figure 5).
4	5	5	**Tx Signal O/P:** When the transmitter is enabled, this pin outputs the 1200/1800Hz (140-step pseudo sinewave) FFSK signal (See Figure 5). With the transmitter disabled, this output is set to a high-impedance state.
5	6	7	**Tx Data I/P:** Serial logic data to be transmitted is input to this pin.
6	7	8	**$\overline{\text{Tx Enable}}$:** A logic '0' will enable the transmitter (See Figure 5). A logic '1' at this input will put the transmitter into powersave whilst forcing the "Tx Sync O/P" to a logic '1' and "Tx Signal O/P" to a high-impedance state. This pin is internally pulled to V_{DD}.
	8	9	**Bandpass O/P:** The output of the Rx 900Hz-2100Hz bandpass filter. This output impedance is typically 10kΩ and may require buffering prior to use.
8	9	10	**Rx Enable:** The control of the Rx function. The control of other outputs is given below.

Rx Enable	=	Rx Function	Clock Data O/P	Carrier Detect	Rx Sync Out
"1"	=	Enabled	Enabled	Enabled	Enabled
"0"	=	Powersave	"0"	"0"	1" or "0"

When both Tx and Rx functions are disabled, the bias voltage is switched internally to V_{SS} (via ≈25kΩ). Bias line R_{OUT} ≈12.5kΩ. With the Bias line decoupled by a 1.0µF capacitor (C_2) the FX439 may take approximately 25 milli-seconds to establish correct operation when enabling the Rx facility. This period may be minimized by either: reducing the value of C_2, lowering the bias line impedance externally or adopting a different powersaving strategy (such as using C_2 and C_6 and supplying V_{DD} via a series switch). This pin is internally pulled to V_{DD}.

9	10	11	**Bias:** The output of the on-chip analogue bias circuitry. Held internally at $V_{DD}/2$, this pin should be decoupled to V_{SS} by a capacitor (C_2). (See Figure 2 and *Rx Enable* notes).
10	11	12	**V_{SS}:** Negative supply rail (GND).
11	12	13	**Unclocked Data O/P:** The recovered asynchronous serial data output from the receiver.
12	13	14	**Clocked Data O/P:** The recovered synchronous serial data output from the receiver. Data is latched out by the recovered clock, available at the "Rx Sync O/P," (See Figure 6).
13	14	15	**Carrier Detect O/P:** When an FFSK signal is being received this output is a logic '1.'
	15	16	**Rx Signal I/P:** The FFSK signal input for the receiver. This input should be coupled via a capacitor, C_3.
15	17	18	**Rx Sync O/P:** A flywheel 1200Hz squarewave output. This clock will synchronize to incoming Rx FFSK data (See Figure 6).
18	19	21	**Clock Rate:** A logic input to select and allow the use of either a 1.008MHz or 4.032MHz Xtal/clock. Logic '1' = 4.032MHz, logic '0' = 1.008MHz. This input has an internal pulldown resistor (1.008MHz).
19	20	22	**Carrier Detect Time Constant (τ):** Part of the carrier detect integration function. The value of C_4 connected to this pin will affect the carrier detect response time and hence noise performance (See Figure 2, Note 3).
20	22	24	**V_{DD}:** Positive supply rail. A single 5-volt supply is required.
16, 17	4, 16,18, 21	4, 6, 17,19, 20, 23	No Internal Connection, do not use.

Note: Output Loading. Large capacitive loads would cause the output pins of this device to oscillate. If capacitive loads in excess of 200pF are unavoidable, a resistor of typically 100Ω put in series with the load should minimise this effect.



NOTES:

1. *Bias may be decoupled to V_{SS} and V_{DD} using C_2 and C_6 when input signals are referenced to the bias pin. For input signals referenced to V_{SS}, decouple Bias to V_{SS} using C_2 only.*
2. *Use C_5 when input signals are referenced to V_{SS}, to decouple V_{DD}.*

Component References

Component	Unit Value	Tolerance %
R_1	1M	±10
C_1	33p	
C_2	1.0µ	±20
C_3	0.1µ	
C_4	0.1µ	±10
C_5	1.0µ	±20
C_6	1.0µ	
C_7	33p	
X_1	1.008MHz or 4.032MHz	See 'Clock Rate' Pin

3. *The value of C_4 determines the carrier detect time constant. A long time constant results in improved noise immunity but increased response time. C_4 may be varied to trade-off response time for noise immunity.*
4. *The value of C_7 reduces xtal voltage overshoot. Refer to CML Xtal Oscillator application note D/XT/1 APRIL 1986.*
5. *X_1 can be either a 1.008MHz or 4.032MHz Xtal, dependant upon the 'Clock Rate' setting.*

Fig. 2 External Component Connections

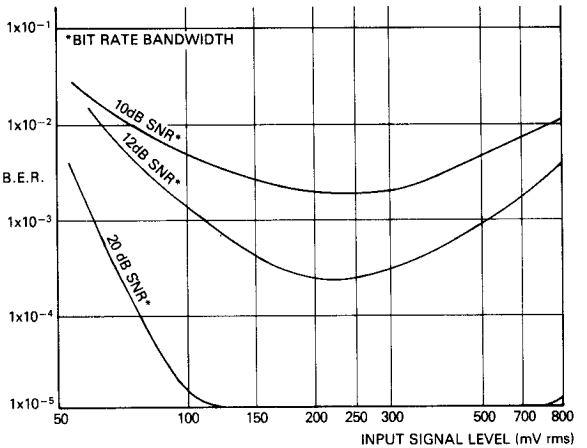


Fig. 3 Typical Variation of 'B.E.R.' with Input Signal Level

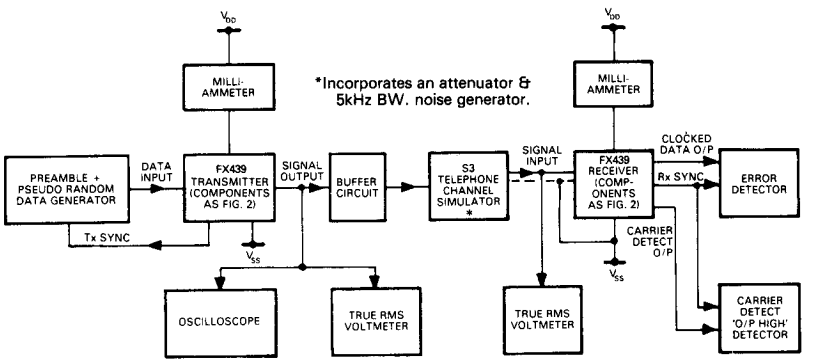


Fig. 4 FX439 Test set-up.

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	−0.3V to 7.0V
Input voltage at any pin (ref V_{SS} = OV)	−0.3V to (V_{DD} + 0.3V)
Output sink/source current (total)	20mA
Operating temperature range: FX439J	-30°C to +85°C (cerdip)
FX439DW/LG/LS	-30°C to +70°C (plastic)
Storage temperature range: FX439J	-55°C to +125°C (cerdip)
FX439DW/LG/LS	-40°C to +85°C (plastic)
Total device dissipation @ T_{AMB} 25°C	800mW Max.
Derating	10mW/°C

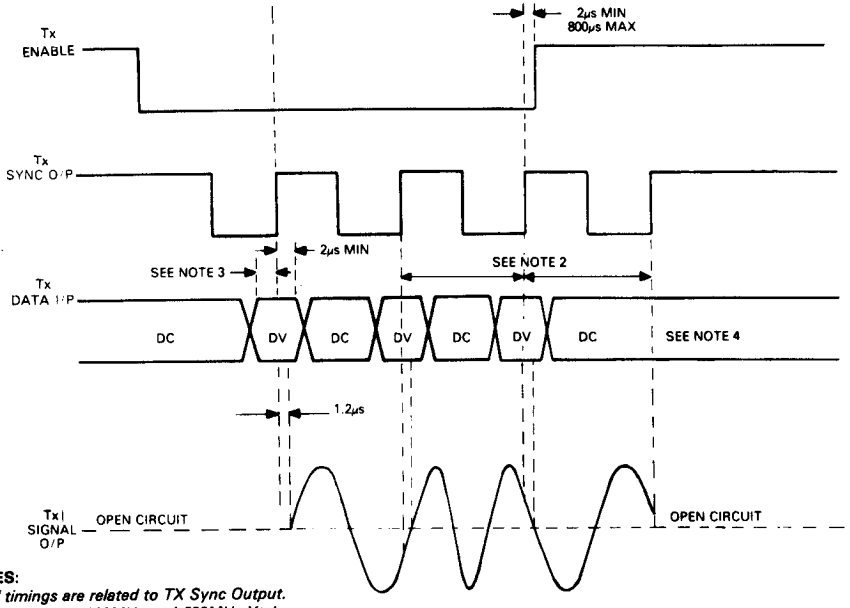
Operating Limits

All characteristics measured using the standard test circuit *(Figure 4)* with the following test parameters and is valid for all tests unless otherwise stated:
V_{DD} = +5V, T_{amb} = 25°C, Xtal (X_1) Frequency: 1.008MHz

0dB reference	300mV rms
Noise	(band limited 5kHz gaussian white noise)
SNR ratio measured in bit rate bandwidth (1200Hz)	

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Characteristics					
Supply Volts		4.5	5.0	5.5	V
Supply Current: Rx (Enabled) Tx (Disabled)		—	3.6	—	mA
Rx (Enabled) Tx (Enabled)		—	4.5	—	mA
Rx (Disabled) Tx (Disabled)		—	650	—	μA
Logic '1' level		80%V_{DD}	—	—	V
Logic '0' level		—	—	20%V_{DD}	V
Digital Output Impedance		—	4	—	kΩ
Analogue and Digital Input Impedance		100	—	—	kΩ
Tx Output Impedance		—	10	—	kΩ
On-Chip Crystal Oscillator:					
R_{in}		10	—	—	MΩ
R_{out}		5	—	15	kΩ
Inverter Gain		10	—	20	dB
Gain Bandwidth Product		3×10^6	—	—	
Crystal Frequency	1	—	1.008	—	MHz
Crystal Frequency	1	—	4.032	—	MHz
Dynamic Characteristics					
Receiver:					
Signal Input: Dynamic Range (50dB SNR)	2, 3	100	230	1000	mV rms
Bit Error Rate: 12dB SNR	3	—	7.0	—	10^{-4}
20dB SNR	3	—	1.0	—	10^{-8}
Receiver Synchronization 12dB SNR:	6				
Probability of Bit 8 being correct			0.99		
Probability of Bit 16 being correct			0.995		
Carrier Detect	4				
Sensitivity	6, 7	—	—	150	mV rms
Probability of Carrier Detect being high:					
12dB SNR after Bit 8	4, 8	—	0.98	—	
12dB SNR after Bit 16	4, 8	—	0.995	—	
0dB Noise (No Signal)	8	—	0.05	—	
Transmitter Output					
Tx Output Level		—	775	—	mV rms
Output Level Variation 1200/1800Hz		0	—	±1.00	dB
Output Distortion		—	3	5	%
3rd Harmonic Distortion		—	2	3	%
Logic '1' Carrier Frequency	5	—	1200	—	Hz
Logic '0' Carrier Frequency	5	—	1800	—	Hz
Isochronous Distortion					
1200Hz – 1800Hz		—	25	40	μs
1800Hz – 1200Hz		—	20	40	μs

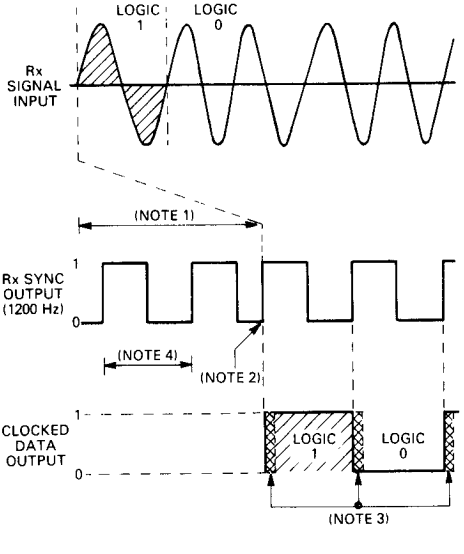
Notes: *1. Crystal frequency, type and tolerance depends on system requirements.*
2. See Figure 3.
3. SNR (Bit Rate Bandwidth).
4. See Figure 2 Note 3.
5. Depending on crystal tolerance.
6. 10101010101 . . . pattern.
7. Measured with 150mV rms signal (No noise).
8. 0dB level for CD probability measurements is 230mV rms.



NOTES:

1. *All timings are related to TX Sync Output.*
2. *0.833ms for 1.008MHz or 4.032MHz Xtal.*
3. *2µs Min + Crystal tolerance.*
4. *DC = Don't Care. DV = Data Valid.*

Fig. 5 Transmitter Timing Diagram



NOTES:

1. *Internal Delay-typ 1.5ms.*
2. *From freely running to Sync in 8 data bits (See spec).*
3. *Undetermined state—2µs max.*
4. *Min. 800µs—Max. 865µs.*

Fig. 6 Receiver Timing Diagram

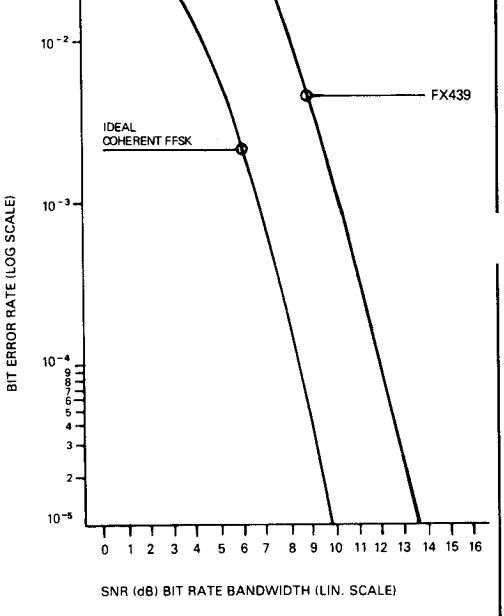
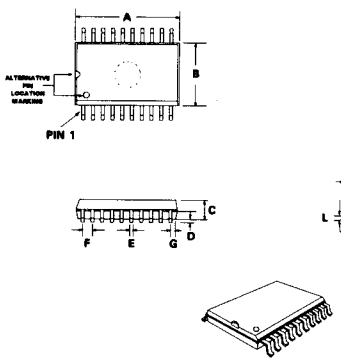


Fig. 7 Receiver B.E.R. Vs SNR

Package Outlines

The FX439DW, the S.O.I.C. package is shown in Figure 8, the 'J' version in Figure 9, the 'LG' version in Figure 10 and the 'LS' version in Figure 11.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top (indent side).

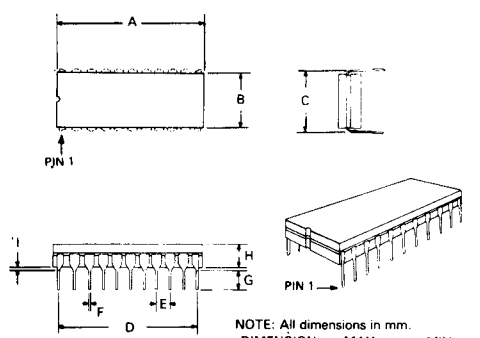
Fig.8 **FX439DW** *S.O.I.C. Package*



All dimensions in mm. Angles in degrees

DIMENSION	MAX.	TYP.	MIN.	DIMENSION	MAX.	TYP.	MIN.
A	12.85		12.62	G		0.66	
B	7.59		7.39	H	10.51		10.11
C	2.67		2.21	J		0.63	
D		0.20		K		45°	
E		0.40		L		5°	
F		1.27		M		0.25	
				N		0.76	

Fig.9 **FX439J** *Package*



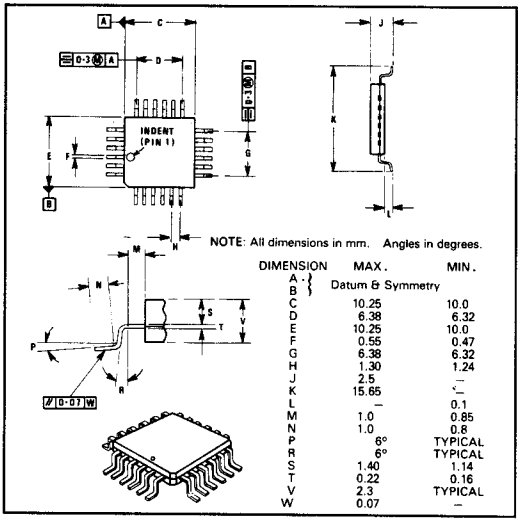
NOTE: All dimensions in mm.

DIMENSION	MAX.	MIN.
A	27.38	26.98
B	9.75	9.55
C	10.60	10.40
D	25.50	25.30
E	2.54	TYPICAL
F	0.46	DIMENSION
G	4.30	4.10
H	4.27	3.99
I	1.4	TYPICAL

Handling Precautions

The FX439 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

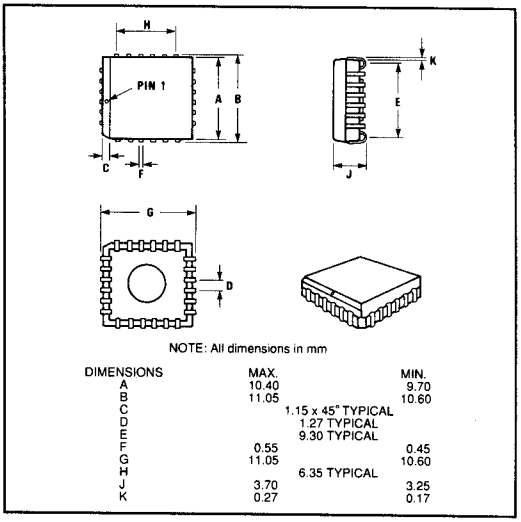
Fig.10 ***FX439LG*** *Package*



NOTE: All dimensions in mm. Angles in degrees.

DIMENSION	MAX.	MIN.
A, B	Datum & Symmetry	
C	10.25	10.0
D	6.38	6.32
E	10.25	10.0
F	0.55	0.47
G	6.38	6.32
H	1.30	1.24
J	2.5	–
K	15.65	–
L	–	0.1
M	1.0	0.85
N	1.0	0.8
P	6°	TYPICAL
R	6°	TYPICAL
S	1.40	1.14
T	0.22	0.16
V	2.3	TYPICAL
W	0.07	–

Fig.11 ***FX439LS*** *Package*



NOTE: All dimensions in mm

DIMENSIONS	MAX.	MIN.
A	10.40	9.70
B	11.05	10.60
C	1.15 x 45° TYPICAL	
D	1.27 TYPICAL	
E	9.30 TYPICAL	
F	0.55	0.45
G	11.05	10.60
H	6.35 TYPICAL	
J	3.70	3.25
K	0.27	0.17

Ordering Information

FX439DW	20-pin surface mount S.O.I.C.
FX439J	22-pin cerdip DIL
FX439LG	24-pin quad plastic encapsulated, bent and cropped
FX439LS	24-lead plastic leaded chip carrier