CML Semiconductor Products

PRODUCT INFORMATION

FX365C Low-Voltage CTCSS Encoder/ Decoder

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Features

- **Low-Voltage (3-Volt) Supply**
- **39 Programmable Sub-Audio Tones + NOTONE**
- **Meets MPT1306 and EIA - 220 B**
- **High Voiceband/CTCSS Isolation**
- **Separate Sub-Audio and Rx/Tx Audio Paths and Filtering**

Applications

- **Mobile Radio Systems**
- **Community Base Stations**
- **“Sports Radio” (Japan)**
- **Sub-Audio Signalling and Selective Calling**
- **Status and Alarm Systems**
- **Amateur Radio**

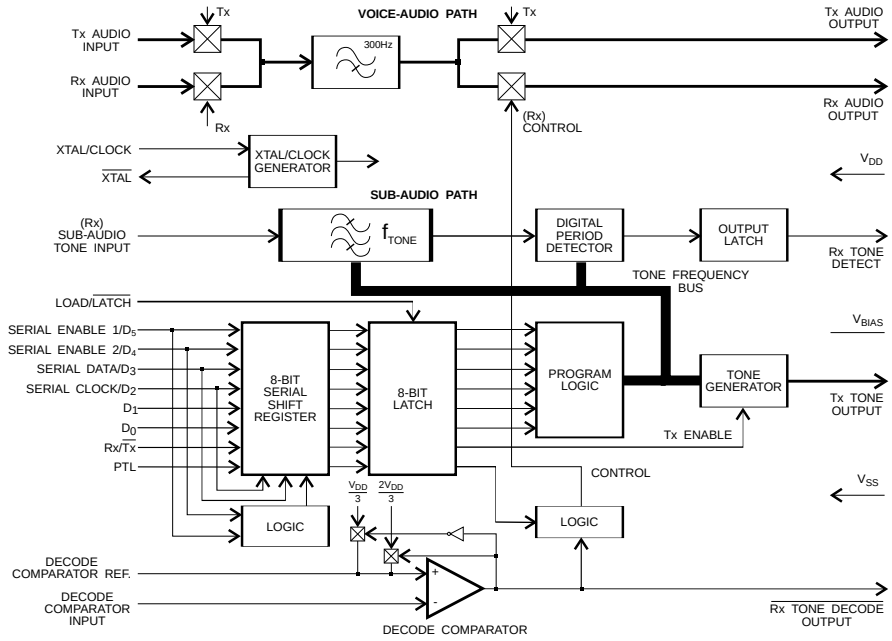


Fig.1 Functional Block Diagram

FX365C

Brief Description

The FX365C is a 3-volt, half-duplex predictive Continuous Tone Controlled Squelch System (CTCSS) encoder/decoder microcircuit. The FX365C has integral voice-band filtering for prefiltering of Tx audio and the rejection of the CTCSS tone in receive.

Under µProcessor control, the FX365C will encode and decode any one of 39 sub-audio frequencies (+NOTONE) in the range 67.0Hz to 250.3Hz. Tone frequencies and all functional commands can be loaded to the device in either pin-selectable 8-bit parallel or serial format.

A separate, Rx/Tx voice-audio path is available with a highpass (sub-audio reject) filter automatically placed in the relevant Rx or Tx voice line.

The Rx sub-audio (CTCSS) path contains a (selected tone frequency) bandpass filter and period detector providing a logic level output (Rx Tone Detect) to indicate a successful decode operation.

Rx “Press to Listen” (PTL) and Tx “Squelch-Tail Elimination” functions are available in both command loading modes. The squelch-tail elimination function will provide (Tx tone) phase-reversal to minimise the annoying audio outputs that occur at the receiver on completion of a transmission.

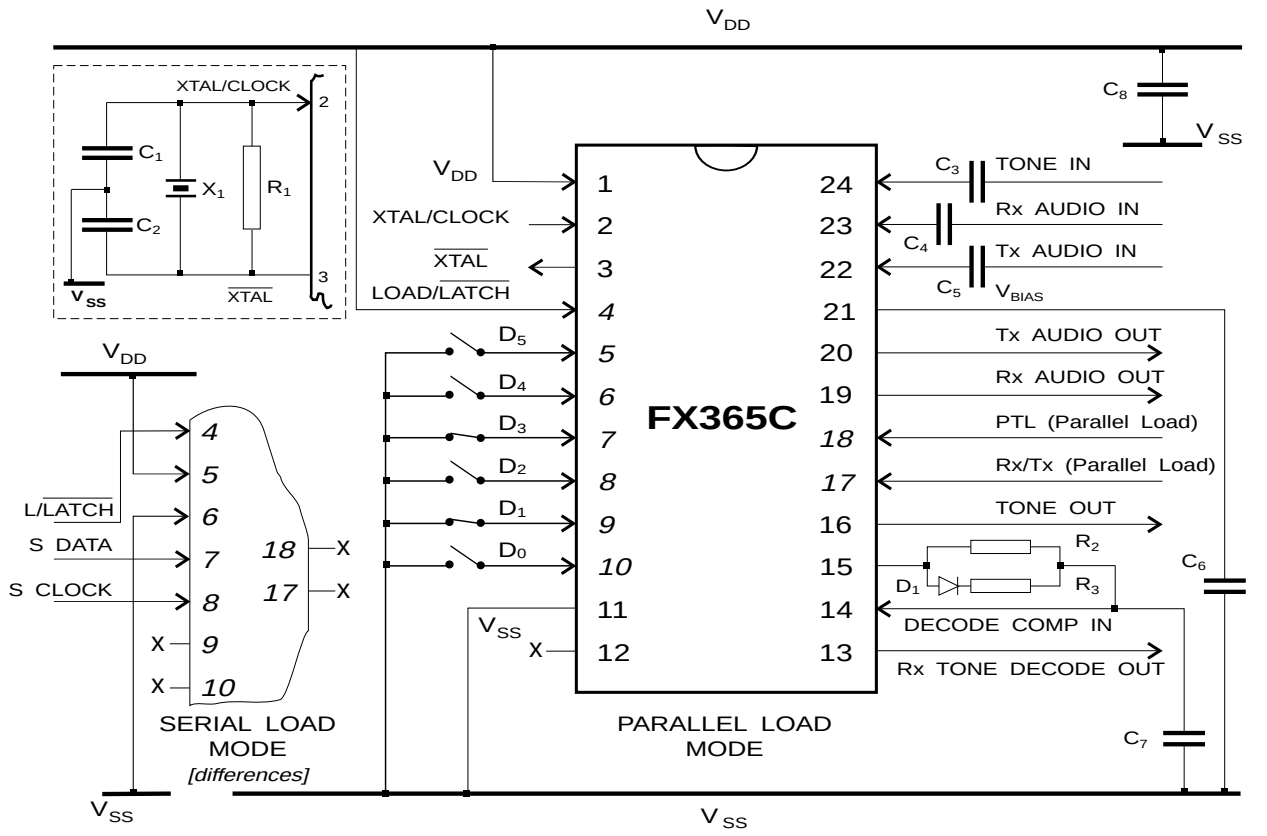
Tone frequencies and filter accuracies are maintained by an on-chip 1.0MHz clock oscillator employing an external crystal or clock pulse input.

The FX365C, which exhibits high audio and sub-audio performance with low falsing, is available in 24-pin DIL and small outline SMD packages.

Pin Number	Function
FX365C	DW and J package styles.
1	**V_{DD}:** Positive supply rail. A single stable supply is required; levels and voltages within the FX365C are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor located close to the pin.
2	**Xtal/Clock:** Input to the on-chip inverter; used with a 1.0MHz Xtal or external clock source.
3	**$\overline{\text{Xtal}}$:** Output of the on-chip clock oscillator inverter.
4	**Load/$\overline{\text{Latch}}$:** Controls 8 on-chip latches and is used to latch Rx/Tx, PTL, D_0 - D_5. This pin is internally pulled to V_{DD}. A logic '1' applied to this input places the 8 latches into a 'transparent' mode. A logic '0' applied to this input places the 8 latches into the 'latched' mode. In parallel mode data is loaded and latched by a logic '1' to '0' transition (see Figure 4a). In serial mode data is loaded and latched by a '0' to '1' to '0' strobe pulse on this pin (see Figure 4b).
5	**D_5/Serial Enable 1:** Data input D_5 (Parallel Mode); Serial Enable 1 (Serial Mode). A logic 'l' applied to this input, together with a logic '0' applied to D_4/Serial Enable 2, will put the device into 'Serial Mode' (see Figure 4b). This pin is internally pulled to V_{DD}.
6	**D_4/Serial Enable 2:** Data input D_4 (Parallel Mode); Serial Enable 2 (Serial Mode). A logic '0' applied to this input, together with a logic '1' applied to D_5/Serial Enable 1, will place the device into 'Serial Mode' (see Figure 4b). This pin internally pulled to V_{DD}.
7	**D_3/Serial Data:** Data input D_3 (Parallel Mode); Serial Data Input (Serial Mode). In Serial Mode this pin becomes the serial data input for D_5 - D_0, Rx/Tx, PTL (see Figure 4b). D_5 is clocked-in first and PTL last. This pin internally pulled to V_{DD}.
8	**D_2/Serial Clock:** Data input D_2 (Parallel Mode); Serial Clock Input (Serial Mode). In Serial Mode this pin becomes the Serial Clock input. Data is clocked on the positive-going edge (see Figure 4b). This pin is internally pulled to V_{DD}.
9	**D_1:** Data input D_1 (Parallel Mode); Not Used (Serial Mode). This pin is internally pulled to V_{DD}.
10	**D_0:** Data input D_0 (Parallel Mode); Not Used (Serial Mode). This pin is internally pulled to V_{DD}.
11	**V_{SS}:** Negative supply (GND).
12	**Decode Comparator Ref.** (I/P)**:** Internally biased to $V_{DD}/3$ or $2V_{DD}/3$ via 1.0MΩ resistors depending on the logical state of the Tone Decode Output pin, this input provides the decode comparator reference voltage; switching of bias voltages provides hysteresis to reduce 'chatter' under marginal conditions. Tone Decode Output = logic '1' will place this input to $2V_{DD}/3$ bias, a logic '0' will bias this input to $V_{DD}/3$.

Pin Number	Function
FX365C	DW and J package styles.
13	**$\overline{\text{Rx Tone Decoder}}$** (O/P)**:** The gated output of the on-chip Decode Comparator. This output is used to gate the Rx Audio path. A logic '0' output on this pin indicates a successful decode and indicates that the 'Decode Comparator Input' pin is more positive than the 'Decode Comparator Ref' input (see Table 1).
14	**Decode Comparator Input:** The inverting input of the Decode Comparator. This pin is to be connected to the Rx Tone Detect pin via external integrating components as shown in Figure 2.
15	**Rx Tone Detect** (O/P)**:** In the Rx mode this output will go to a logic '1' during a successful decode (Table 1). This pin is to be connected to the Decode Comparator Input via the external integrating circuitry as shown in Figure 2.
16	**Tx Tone Output:** A low-impedance emitter-follower source, under the control of the Rx/Tx pin, of the CTCSS sinewave. This output, when not transmitting a sub-audio tone, may be set to a V_{DD}/(2-0.7)V bias or open-circuit as described in Table 1.
17	**Rx/$\overline{\text{Tx}}$:** This input (Parallel Mode) selects Rx or Tx modes (see Figure 2). Logic '1' = Rx; logic '0' = Tx. In Serial Mode this (Rx or Tx) function is serially loaded via pin 7 (Serial Data) and this pin not used. This pin is internally pulled to V_{DD} via a 1MΩ resistor (Rx operaion).
18	**PTL:** A dual-function input. In the parallel load mode, Rx operation: A logic '1' provides a "Press To Listen" function by overriding the tone-squelch and enabling the audio path. In the parallel load mode, Tx operation: A logic '1' provides a "Squelch Tail Elimination" function by reversing the phase of the transmitting sub-audio tone; the phase reversal function should be applied by a suitable timing circuit. In the serial load mode (Rx and Tx) these functions are loaded via the serial data word at pin 7.
19	**Rx Audio Output:** The high-pass filtered 'Received Audio' output. This pin outputs audio when Rx Tone Decode = '0', or PTL = '1' or 'Notone' is programmed (Table 2). In Tx Mode this pin is biased to V_{DD}/2.
20	**Tx Audio Output:** The high-pass filtered 'Transmit Audio' output. In Tx mode this pin outputs audio present at the Tx Audio Input by opening the Tx audio path. In Rx mode this pin is biased to V_{DD}/2.
21	**V_{BIAS}:** The output of the on-chip analogue bias circuitry. Held internally at V_{DD}/2, this pin should be externally decoupled to V_{SS}.
22	**Tx Audio Input:** The Tx Audio Input pin. Tx voice-band audio may be prefiitered, using the Voice Audio Path, thus helping to avoid talk-off due to the intermodulation of speech frequencies with the transmitted CTCSS tone. The Tx Audio Path may also be used to pre-filter speech when employing 'scramblers' which could introduce noise into the low frequency band. This pin is internally biased to V_{DD}/2.
23	**Rx Audio Input:** The input to the Voice Audio high-pass filter in the Rx Mode. This pin is internally biased to V_{DD}/2.
24	**Tone Input:** The input to the CTCSS tone detector and is internally biased to V_{DD}/2.

Application Information



External Components

Component	Value	Tolerance	Component	Value	Tolerance
R_1	1.0MΩ	±10%	C_4	0.1µF	±20%
R_2	820kΩ	±10%	C_5	0.1µF	±20%
R_3	330kΩ	±10%	C_6	1.0µF	±20%
			C_7	0.1µF	±20%
C_1	68.0pF	±20%	C_8	1.0µF	±20%
C_2	33pF	±20%	D_1	small signal type	
C_3	0.1µF	±20%	X_1	1.0MHz	

Fig.2 Recommended External Components

Input Pin Condition				*Output Pin Condition*		*Result and/or Function*					
D_0 to D_5	Rx/$\overline{Tx}$	PTL	Decode Comp. Input	Rx Tone Detect	$\overline{\text{Rx Tone Decode}}$	Tone Tx Enabled	Tx Tone Phase Reversed	Tx Audio Path Enabled	Tone Decoder Enabled	Rx Audio Path Enabled	Notes
TONE	0	0	x	0	1	YES	NO	YES	NO	NO (BIAS)	1A
TONE	0	1	x	0	1	YES	YES	YES	NO	NO (BIAS)	1B
NOTONE	0	x	x	0	1	NO (BIAS)	x	YES	NO	NO (BIAS)	2
TONE	1	0	0	0	1	No(o/c)	x	NO	YES	YES	3A
TONE	1	1	0	0	1	No (o/c)	x	NO	YES	YES	3B
TONE	1	x	1	1	0	No (o/c)	x	NO	YES	YES	4
NOTONE	1	x	x	x	0	No (o/c)	x	NO	YES	YES	5

NOTES

1A Normal tone transmit condition.
1B Tone Tx with phase reversed.
2 NOTONE programmed in Tx mode; tone transmit output set to $V_{DD}/2$ -(0.7v). Tx audio path enabled.
3A Normal decode standby.
3B Normal decode standby with PTL used to enable audio.
4 Normal 'decode of correct CTCSS tone' condition; PTL has no effect.
5 NOTONE programmed in Rx mode; tone transmit output (o/c). Rx audio path enabled.

Table 1 Combinations of Input/Output Conditions *x = don't care*

Application Information .....

Nominal Freq (Hz)	FX365C Freq. (Hz)	Δfo %	D_0	D_1	D_2	D_3	D_4	D_5
67.0	67.05	+0.7	1	1	1	1	1	1
69.3	69.32	+0.03	1	0	0	1	1	1
71.9	71.90	0.0	1	1	1	1	1	0
74.4	74.35	-0.07	0	1	1	1	1	1
77.0	76.96	-0.05	1	1	1	1	0	0
79.7	79.77	+0.09	1	0	1	1	1	1
82.5	82.59	+0.10	0	1	1	1	1	0
85.4	85.38	-0.02	0	0	1	1	1	1
88.5	88.61	+0.13	0	1	1	1	0	0
91.5	91.58	+0.09	1	1	0	1	1	1
94.8	94.76	-0.04	1	0	1	1	1	0
97.4	97.29	-0.11	0	1	0	1	1	1
100.0	99.96	-0.04	1	0	1	1	0	0
103.5	103.43	-0.07	0	0	1	1	1	0
107.2	107.15	-0.05	0	0	1	1	0	0
110.9	110.77	-0.12	1	1	0	1	1	0
114.8	114.64	-0.14	1	1	0	1	0	0
118.8	118.80	0.0	0	1	0	1	1	0
123.0	122.80	-0.17	0	1	0	1	0	0
127.3	127.08	-0.17	1	0	0	1	1	0
131.8	131.67	-0.10	1	0	0	1	0	0
136.5	136.61	+0.08	0	0	0	1	1	0
141.3	141.32	+0.02	0	0	0	1	0	0
146.2	146.37	+0.12	1	1	1	0	1	0
151.4	151.09	-0.20	1	1	1	0	0	0
156.7	156.88	+0.11	0	1	1	0	1	0
162.2	162.31	+0.07	0	1	1	0	0	0
167.9	168.14	+0.14	1	0	1	0	1	0
173.8	173.48	-0.19	1	0	1	0	0	0
179.9	180.15	+0.14	0	0	1	0	1	0
186.2	186.29	+0.05	0	0	1	0	0	0
192.8	192.86	+0.03	1	1	0	0	1	0
203.5	203.65	+0.07	1	1	0	0	0	0
210.7	210.17	-0.25	0	1	0	0	1	0
218.1	218.58	+0.22	0	1	0	0	0	0
225.7	226.12	+0.18	1	0	0	0	1	0
233.6	234.19	+0.25	1	0	0	0	0	0
241.8	241.08	-0.30	0	0	0	0	1	0
250.3	250.28	-0.01	0	0	0	0	0	0
NOTONE	NOTONE		0	0	0	0	1	1
Serial Input Mode			x	x	Clock	Data	0	1

Table 2 Tone Programming Information

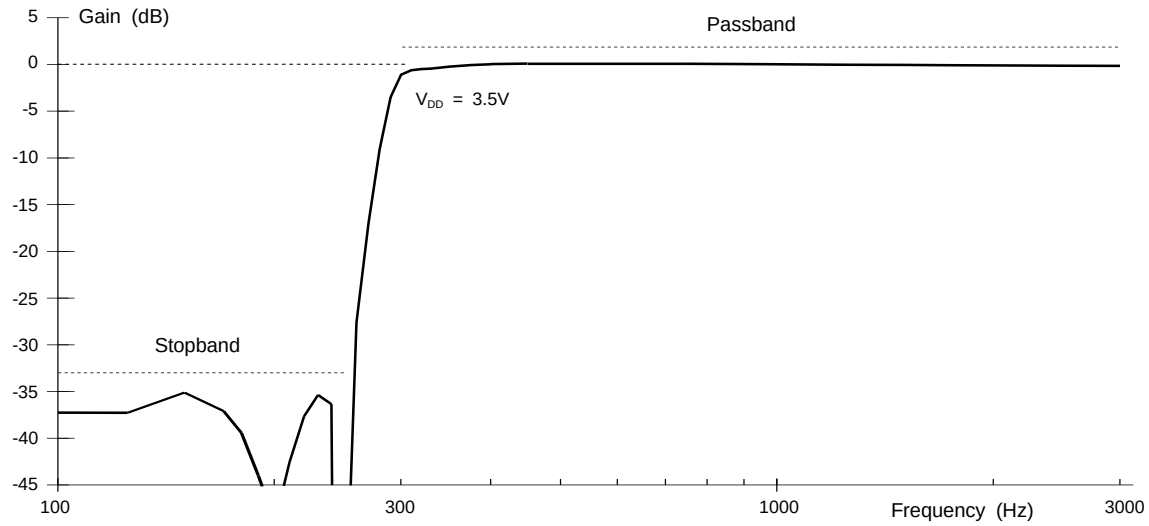


Fig.3 Voiceband Filter Response

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)		+/- 30mA
(other pins)		+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX365C J**	-40°C to +85°C (cerdip)
	FX365C DW	-40°C to +85°C (plastic)
Storage temperature range:	**FX365C J**	-55°C to +125°C (cerdip)
	FX365C DW	-40°C to +85°C (plastic)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:
V_{DD} = 3.3V. T_{AMB} = 25°C. Xtal/Clock f_0 = 1.0MHz. Signal 0dB ref: = 180mVrms.
Composite Signal = 1.0kHz Audio Tone at 0dB, Noise at –12.0dB (gaussian white noise, band-limited to 6.0kHz), Programmed CTCSS Tone at -20dB.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Characteristics					
Supply Voltage (V_{DD})		3.0	3.3	5.5	V
Supply Current					
(Tx)		-	1.5	-	mA
(Rx)		-	1.5	-	mA
Sub-Audio Tone Input Impedance		-	1.0	-	MΩ
Tx Tone Output Impedance		-	4.0	-	kΩ
Voice-Audio Input Impedance		-	1.0	-	MΩ
Voice-Audio Output Impedance		-	1.0	-	kΩ
Digital Input Impedance	1	-	1.0	-	MΩ
Input Logic '1'	1	70.0	-	-	%V_{DD}
Input Logic '0'	1	-	-	30.0	%V_{DD}
Output Logic '1', source = 0.1mA	2	80.0	-	-	%V_{DD}
Output Logic '0', sink = 0.1 mA	2	-	-	20.0	%V_{DD}
Dynamic Characteristics					
Tone Decoder					
Decode Input Signal Level	3	-20.0	-	-	dB
Decode Response Time	3, 6	-	-	250	ms
De-Response Time	3, 6	-	-	250	ms
Decode Selectivity	3	±0.5	-	±3.0	%f_O
Tone Encoder					
Tx Tone Output Level		-	627	-	mVrms
Tx Tone Frequency Accuracy (f_O error)		-0.3	-	+0.3	%f_O
Risetime to 90% (nominal output)					
f_O > 100Hz	4	-	55.0	-	ms
f_O < 100Hz	4	-	70.0	-	ms
Tone Output Load Current		-	-	5.0	mA
Total Harmonic Distortion		-	2.0	5.0	%
Output Level Variation Between Tones		-	0.1	-	dB
Spurious Emissions		-	-	-48.0	dB
Voice-Audio Filter and Path					
Passband Frequencies		300		3000	Hz
Passband Gain					
at 1.0kHz		-	0	-	dB
w.r.t. 1.0kHz		-2.0	-	0.5	dB
Total Harmonic Distortion	5	-	2.0	5.0	%
Stopband Frequencies		-	-	250	Hz
Stopband Attenuation		33.0	36.0	-	dB
Output Noise Level (Input a.c. Short Cct)	7	-	-54.0	-48.0	dB
SINAD	8	36.0	40.0	-	dB
Audio Switch Isolation	5	-	60.0	-	dB

Specification .....

Characteristics	See Note	Min.	Typ.	Max.	Unit
Serial/Parallel Inputs					
Parallel Set-Up Time (t_{SP})		400	-	-	ns
Load/Latch Pulse Width (t_L)		400	-	-	ns
Serial Clock Pulse Width (t_C)		400	-	-	ns
Serial Set-Up Time (t_{SS})		400	-	-	ns
Serial Enable Time (t_1)		400	-	-	ns
Serial Load/Latch Set-Up Time (t_2)		400	-	-	ns
Serial Clock Frequency		-	1.0	-	MHz

Notes

1. Refers to Rx/Tx, PTL, Decode Comparator Input, D_0, D_1, D_2, D_3, D_4, D_5 inputs.
2. All logic outputs.
3. Composite Signal test condition.
4. Any programme tone and RL = 600Ω. CL = 15pF. Includes response to a phase-reversal instruction.
5. 1kHz reference = 0dB.
6. f_O > 100Hz, (for 100Hz >f_O >67Hz: t = (100/f_O Hz) x 250ms).
7. Measured in a 30kHz bandwidth.
8. For an input level of 180mVrms at 1.0kHz, in a 30kHz measurement bandwidth.

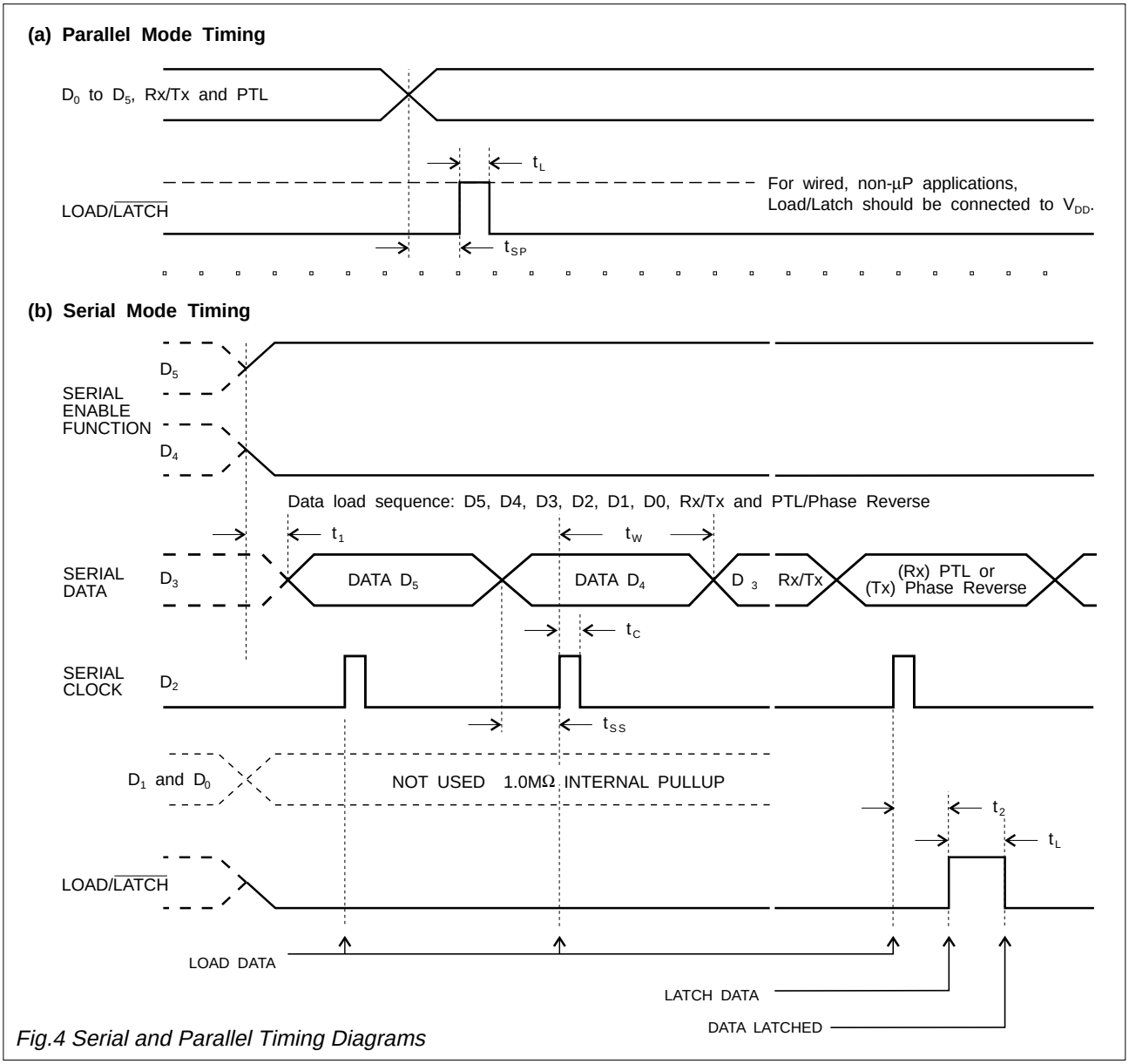


Fig.4 Serial and Parallel Timing Diagrams

Package Outlines

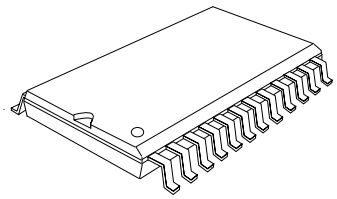
The FX365C is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX365C is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX365C DW 24-pin plastic S.O.I.C (D2)

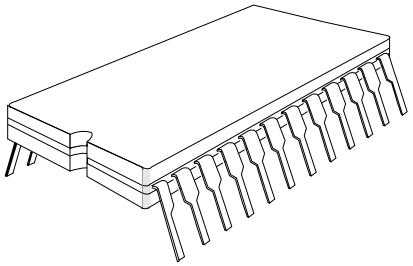
NOT TO SCALE



Max. Body Length 15.57mm
Max. Body Width 7.59mm

FX365C J 24-pin cerdip DIL (J4)

NOT TO SCALE



Max. Body Length 32.00mm
Max. Body Width 13.36mm

Ordering Information

FX365C DW 24-pin plastic S.O.I.C. (D2)

FX365C J 24-pin cerdip DIL (J4)