CML Semiconductor Products

PRODUCT INFORMATION

FX029 Dual Digitally Controlled Amplifier Array

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Provisional Issue

Features

- 2 Digitally Controlled Amplifiers
- Gain/Attenuation Range of ±48dB + Output Mute, in 2dB Steps
- Gain/Attenuation Levels Set by Serial Interface
- Separate Fixed-Gain Uncommitted Amplifier
- 5 Volt Low-Power Operation

Applications

- Cellular and PMR Communications Systems
- Automatic and Manual Test Equipment
- Remote Gain Adjustments
- Telephone Audio Settings
- Medical Equipment
- Audio and Data Gain Setting Applications

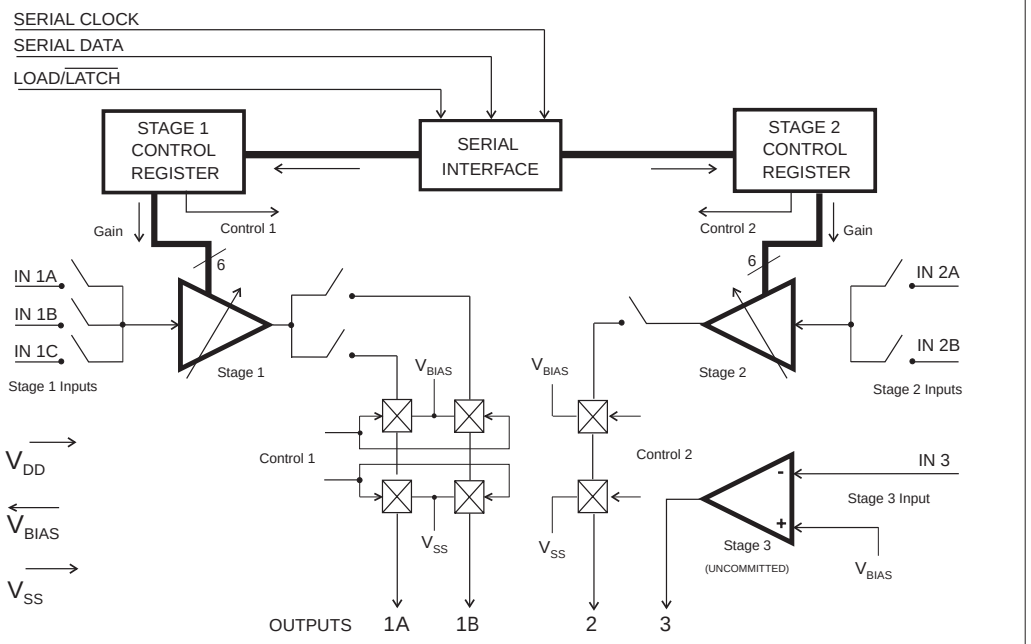


Fig.1 Functional Block Diagram

FX029

Brief Description

The FX029 single-chip Dual Digitally Controlled Amplifier Array can replace manual audio-level controls in most electronic applications including radio and line communications systems.

The FX029 comprises two digitally controlled gain and attenuation stages, with each stage having 48 distinct gain steps (range; between -48dB and +48dB in 2dB steps) plus a MUTE state to powersave the addressed section. Minimum current drain results from muting both sections.

Both gain stages have selectable inputs. This switching allows for selection of three different input signals to stage 1 and two to stage 2.

Stage 1 also provides output switching.

In addition to the two digitally controlled gain stages, there is a general purpose, uncommitted inverting amplifier; the gain of this particular amplifier is component controlled externally using negative feedback.

Control of each gain stage section is accomplished through the serial interface. All switching is accomplished using controlled rise and fall times, thereby ensuring no annoying transients (clicks or pops).

The FX029 requires a single 5 volt supply and is available in compact cerdip and small outline packages.

Pin Number		Function
FX029 DW/J	FX029 D5	
1	1	**Serial Clock:** This external clock input is used to “clock in” the control data. See Figure 4 for timing information. This input has an internal 1MΩ pullup resistor.
2	4	**Serial Data:** Operation of the two amplifier stages (1 and 2) is controlled by the data entered serially at this pin. The data is entered (bit 13 to bit 0) on the rising edge of the external Serial Clock. The data format is described in Tables 1-3 and Figure 4. This input has an internal 1MΩ pullup resistor.
3	5	**Load/$\overline{\text{Latch}}$:** Governs the loading and execution of the serial control data. During serial data loading this input should be kept at a logical “1” to ensure that data rippling past the latches has no effect. When all 14 bits have been loaded this input should be strobed “1” to “0” to “1” to latch the new data in. Data is executed on the rising edge of this strobe.
4	6	**IN 1A** (Stage 1 Input 1)**:** Analogue Input.
5	7	**IN 1B** (Stage 1 Input 2)**:** Analogue Input.
6	8	**IN 2A** (Stage 2 Input 1)**:** Analogue Input.
7	9	**IN 2B** (Stage 2 Input 2)**:** Analogue Input.
8	12	**V_{SS}:** Negative supply rail (GND).
9	13	**V_{BIAS}:** The output of the on-chip bias circuitry, held at $V_{DD}/2$.
10	16	**IN 1C** (Stage 1 Input 3)**:** Analogue Input. Normally used for FSK data.
11	17	**OUT 2** (Stage 2 Output)**:** Analogue Output.
12	18	**OUT 1B** (Stage 1 Output 2)**:** Analogue Output.
13	20	**OUT 1A** (Stage 1 Output 1)**:** Analogue Output.
14	21	**OUT 3** (Uncommitted Amplifier Output)**:** Output from the general purpose uncommitted amplifier.
15	23	**IN 3** (Uncommitted Amplifier Input)**:** Inverting input to general purpose uncommitted amplifier.
16	24	**V_{DD}:** Positive supply rail. A single +5-volt power supply is required.

Application Information

External Components

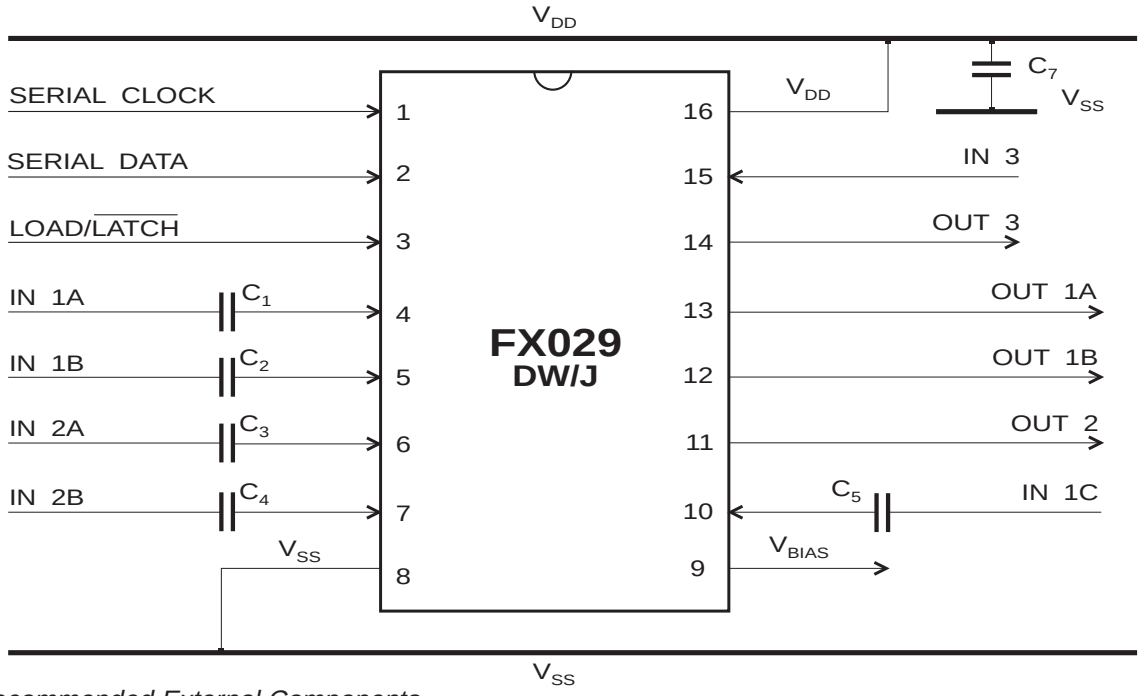


Fig.2 Recommended External Components

Component Recommendations

Component	Value
C_1	0.1µF
C_2	0.1µF
C_3	0.1µF
C_4	0.1µF
C_5	0.1µF
C_6	Not Used
C_7	1.0µF

Tolerances 20%

Input capacitors C_1 to C_5 are only required for ac input signals; dc input signals do not require these components.

The gain of the uncommitted stage (3) is set by external components employed around the input and output pins (see Specification page).

Application Recommendations

To avoid noise and instability the following practices are recommended:

(a) Use a clean, well-regulated power supply.

(b) Keep tracks short.

(c) Inputs and outputs should be shielded wherever possible.

(d) Analogue tracks should not run parallel to digital tracks.

(e) A "Ground Plane" connected to V_{SS} will assist in eliminating external pick-up on the channel input and output pins.

(f) Avoid running high level outputs adjacent to low level inputs.

(g) The serial clock should not be running consecutively when not in the process of actually loading data.

Serial Interface Timing

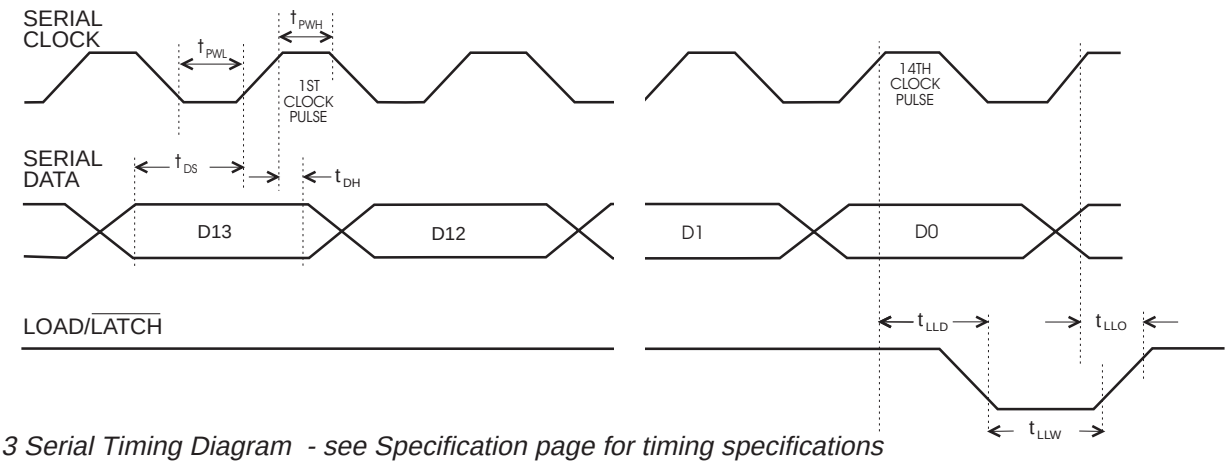


Fig.3 Serial Timing Diagram - see Specification page for timing specifications

Control Data and Timing

The gain and I/O signal path for each section (Channels 1 and 2) is set individually by a 14-bit data word (D0 to D13). Data is loaded on the rising edge of the Serial Clock. Loaded data is executed on the rising edge of the Load/ Latch pulse.The 14-bit word consists of 1 channel address bit (D7) for selection of the channel to be programmed, 6 bits for setting the amplification/attenuation level (D8-D13), 3 bits for input selection (D4 and D6), and 4 bits for output settings (D0-D3). This format is illustrated below in Figure 4.
Tables 1-3 show how the data word is used to control channel selection, amplification/attenuation, input selection and output settings, respectively.

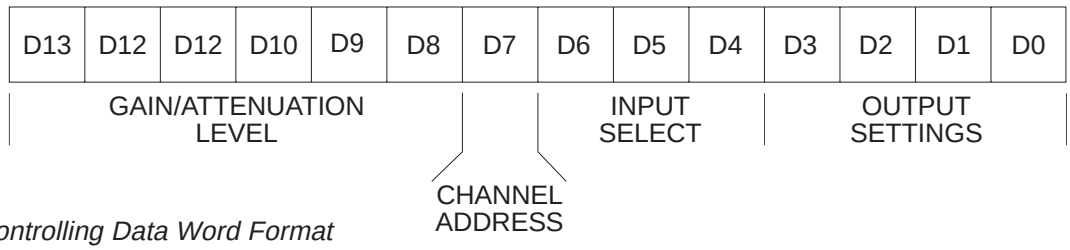


Fig.4 Level-Controlling Data Word Format

D13	D12	D11	D10	D9	D8	Gain Set (dB)	D13	D12	D11	D10	D9	D8	Gain Set (dB)
0	*0*	*0*	*0*	*0*	*0*	*MUTE*	*0*	*1*	*1*	*0*	*0*	*1*	*0*
0	0	0	0	0	1	-48	0	1	1	0	1	0	2
0	0	0	0	1	0	-46	0	1	1	0	1	1	4
0	0	0	0	1	1	-44	0	1	1	1	0	0	6
0	0	0	1	0	0	-42	0	1	1	1	0	1	8
0	0	0	1	0	1	-40	0	1	1	1	1	0	10
0	0	0	1	1	0	-38	0	1	1	1	1	1	12
0	0	0	1	1	1	-36	1	0	0	0	0	0	14
0	0	1	0	0	0	-34	1	0	0	0	0	1	16
0	0	1	0	0	1	-32	1	0	0	0	1	0	18
0	0	1	0	1	0	-30	1	0	0	0	1	1	20
0	0	1	0	1	1	-28	1	0	0	1	0	0	22
0	0	1	1	0	0	-26	1	0	0	1	0	1	24
0	0	1	1	0	1	-24	1	0	0	1	1	0	26
0	0	1	1	1	0	-22	1	0	0	1	1	1	28
0	0	1	1	1	1	-20	1	0	1	0	0	0	30
0	1	0	0	0	0	-18	1	0	1	0	0	1	32
0	1	0	0	0	1	-16	1	0	1	0	1	0	34
0	1	0	0	1	0	-14	1	0	1	0	1	1	36
0	1	0	0	1	1	-12	1	0	1	1	0	0	38
0	1	0	1	0	0	-10	1	0	1	1	0	1	40
0	1	0	1	0	1	-8	1	0	1	1	1	0	42
0	1	0	1	1	0	-6	1	0	1	1	1	1	44
0	1	0	1	1	1	-4	1	1	0	0	0	0	46
0	1	1	0	0	0	-2	1	1	0	0	0	1	48
0	*1*	*1*	*0*	*0*	*1*	*0*	1	1	0	0	1	0	48
							1	1	0	0	1	1	48

Table 1 - Amplification/Attenuation Level

D7	Stage Selected	D6	D5	D4	Inputs Selected
0	1	0	0	0	none
1	2	0	0	1	1
		0	1	0	2
		0	1	1	1 and 2
		1	0	0	3
		1	0	1	1 and 3
		1	1	0	2 and 3
		1	1	1	1, 2 and 3

Table 2 Stage and Input Selection

D3	D2	Output 1B	D1	D0	Outputs 1A & 2
0	0	high Z	0	0	high Z
0	1	enabled	0	1	enabled
1	0	V_{SS}	1	0	V_{SS}
1	1	V_{BIAS}	1	1	V_{BIAS}

Table 3 Stage Output Selection

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref. V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)		+/- 30mA
(other pins)		+/- 20mA
Total device dissipation (DW/J) @ T_{AMB} 25°C		800mW Max.
(D5) @ T_{AMB} 25°C		550mW Max.
Derating (DW/J)		10mW/°C
(D5)		9mW/°C
Operating temperature range:	**FX029DW/D5/J**	-40°C to +85°C
Storage temperature range:	**FX029D5**	-40°C to +85°C
	FX029DW/J	-55°C to +125°C

Operating Characteristics

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V, T_{AMB} = 25°C. External components as Figure 2. Audio 0dB ref. = 775mVrms

Characteristics	See Note	Min.	Typ.	Max.	Unit
Supply Voltage		4.5	5.0	5.5	V
Current (All Stages Mute)		-	0.10	-	mA
(All Stages Operating)		-	3.0	-	mA
Digital Inputs	4				
Input Logic “1”		3.5	-	-	V
Input Logic “0”		-	-	1.5	V
Digital Input Impedances		0.5	1.0	-	MΩ
Gain Control Amplifier Stages (Stages 1 and 2)					
Bandwidth (-3dB)	1	3.3	-	-	kHz
Output Impedance		-	1.0	2.0	kΩ
Total Harmonic Distortion	2, 5	-	0.35	0.5	%
Interstage Isolation		-	60.0	-	dB
Gain		46.0	48.0	-	dB
Attenuation		46.0	48.0	-	dB
Gain/Attenuation Step Size		-	2.0	-	dB/step
Step Error		-	-	0.4	dB
Input Impedance		50.0	-	-	kΩ
Input Referred Offset Voltage (V_{IOS})		-	10.0	-	mV
Uncommitted Amplifier (Stage 3)					
Bandwidth (-3dB)	3	10.0	-	-	kHz
Output Impedance		-	1.0	2.0	kΩ
Total Harmonic Distortion	3	-	0.35	0.5	%
Open Loop DC Gain		-	60	-	dB
Timing (See Figure 3)					
Serial Clock “High” Pulse Width (t_{PWH})		250	-	-	ns
Serial Clock “Low” Pulse Width (t_{PWL})		250	-	-	ns
Data Set-up Time (t_{DS})		150	-	-	ns
Data Hold Time (t_{DH})		50.0	-	-	ns
Load/Latch Delay (t_{LLD})		200	-	-	ns
Load/Latch Over-Time (t_{LLO})		-	-	0	ns
Load/Latch Pulse Width (t_{LLW})		150	-	-	ns
Serial Data Clock Frequency		-	-	2.0	MHz

Notes

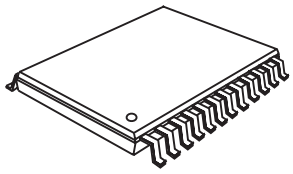
1. Gain set to maximum (+48.0dB).
2. Gain Set 0dB. Input Level 1.0kHz, -3.0dB (549mVrms).
3. Gain externally set to 10.0dB.
4. Serial Clock, Serial Data and Load/Latch inputs.
5. With a 100kΩ load on the relevant output.

Package Outlines

The FX029 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of the Data Book.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

FX029D5 24-Pin Plastic S.S.O.P.

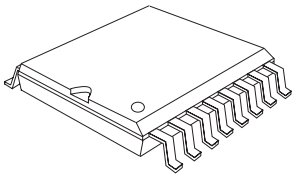
NOT TO SCALE



Max. Body Length	8.33mm
Max. Body Width	5.38mm

FX029DW 16-pin plastic S.O.I.C. (D4)

NOT TO SCALE



Max. Body Length	10.49mm
Max. Body Width	7.59mm

FX029J 16-pin cerdip DIL (J2)

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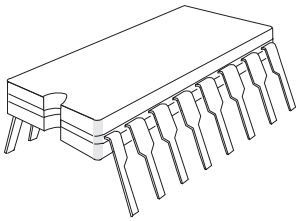

Max. Body Length	19.48mm
Max. Body Width	7.39mm

Handling Precautions

The FX029 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

Ordering Information

FX029D5 24-pin plastic S.S.O.P.
FX029DW 16-pin plastic S.O.I.C. (D4)
FX029J 16-pin cerdip (J2)