CIRRUS LOGIC ®

FEATURES

- **ARM720T processor**
  - ARM7TDMI CPU
  - 8 K-bytes of four-way set-associative cache
  - MMU with 64-entry TLB (transition look-aside buffer)
  - Write Buffer
  - Windows® CE enabled
  - Thumb code support enabled
- **Dynamically programmable clock speeds of 18, 36, 49, and 74 MHz at 2.5 V**
- **Performance matching 100-MHz Intel® Pentium-based PC**
- **Ultra low power**
  - Designed for applications that require long battery life while using standard AA/AAA batteries or rechargeable cells
  - Typical Power Numbers
    - 90 mW at 74 MHz in the Operating State
    - 30 mW at 18 MHz in the Operating State
    - 10 mW in the Idle State (clock to the CPU stopped, everything else running)
    - <1 mW in the Standby State (realtime clock 'on', everything else stopped)
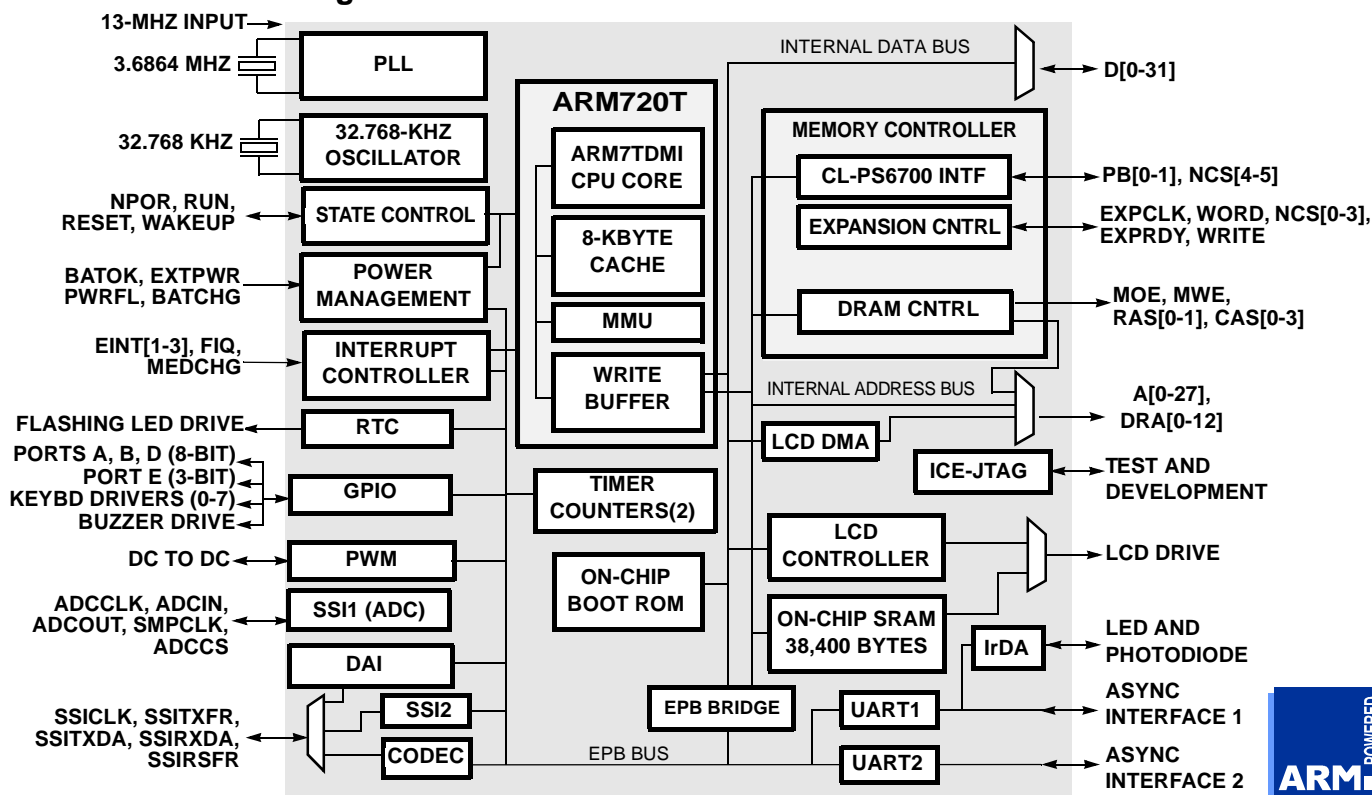
(cont.)

High-Performance, Low-Power System-on-Chip with LCD Controller and Digital Audio Interface (DAI)

OVERVIEW

The EP7212 is designed for ultra-low-power applications such as organizers / PDAs, two-way pagers, smart cellular phones or any vertical PDA device that features the added capability of digital audio decompression. The core-logic functionality of the device is built around an ARM720T processor with 8 K-bytes of four-way set-associative unified cache and a write buffer. Incorporated into the ARM720T is an enhanced memory management unit (MMU) which allows for support of sophisticated operating systems like Microsoft Windows CE.

(cont.)

Functional Block Diagram

DS474PB2
FEB 00

FEATURES *(cont.)*

■ **Advanced audio decoder / decompression capability**
— Allows for support of multiple audio decompression algorithms
— Supports MPEG 1, 2, & 2.5 layer 3 audio decoding, including ISO compliant MPEG 1 & 2 layer 3 support for all standard sample rates and bit rates
— Supports bit streams with adaptive bit rates
— DAI (Digital Audio Interface) providing glueless interface to low-power DACs, ADCs, and Codecs

■ **LCD controller**
— Interfaces directly to a single-scan panel monochrome LCD
— Panel width size is programmable from 32 to 1024 pixels in 16-pixel increments
— Video frame buffer size programmable up to 128 kbytes
— Bits per pixel of 1, 2, or 4 bits

■ **DRAM controller**
— Supports both 16- and 32-bit-wide DRAMs
— EDO support (Fast Page Mode support for 13 MHz and 18 MHz operation only)

■ **Memory controller**
— Decodes up to 6 separate memory segments of up to 256 Mbytes each
— Each segment can be configured as 8, 16, or 32 bits wide and supports page-mode access
— Programmable access time for conventional ROM / SRAM / FLASH memory
— Supports Removable FLASH card interface
— Enables connection to removable FLASH card for addition of expansion FLASH memory modules

■ **38,400 bytes (0x9600) of on-chip SRAM for fast program execution and / or as a frame buffer**

■ **Synchronous serial interface**
— ADC (SSI) Interface: Master mode only; SPI® and Microwire1®-compatible (128 kbps operation)

■ **On-chip ROM; for manufacturing support**

■ **27-bits of general-purpose I/O**
— Three 8-bit and one 3-bit GPIO port
— Supports scanning keyboard matrix

■ **Two UARTs (16550 type)**
— Supports bit rates up to 115.2 kbps
— Contains two 16-byte FIFOs for TX and RX
— UART1 supports modem control signals

■ **SIR (up to 115.2 kbps) infrared encoder / decoder**
— IrDA (Infrared Data Association) SIR protocol encoder / decoder

■ **DC-to-DC converter interface (PWM)**
— Provides two 96-kHz clock outputs with programmable duty ratio (from 1-in-16 to 15-in-16) that can be used to drive a DC to DC converter

■ **Two timer counters**

■ **208-pin LQFP or new 256-ball PBGA packages**

■ **Evaluation kit available with BOM, schematics, sample code, and design database**

■ **Support for up to two ultra-low-power CL-PS6700 PC Card controllers**

■ **Dedicated LED flasher pin from RTC**

■ **Full JTAG boundary scan and Embedded ICE® support**

■ **Commercial operating temperature range**

OVERVIEW *(cont.)*

The EP7212 also includes a 32-bit Y2K-compliant realtime clock and comparator.

Power Management

The EP7212 is designed for ultra-low-power operation. Its core operates at only 2.5 V, while its I/O has an operation range of 2.5 V–3.3 V. The device has three basic power states:

Operating — This state is the full performance state. All the clocks and peripheral logic are enabled.

Idle — This state is the same as the Operating State, except the CPU clock is halted while waiting for an event such as a key press.

Standby — This state is equivalent to the computer being switched off (no display), and the main oscillator shut down. An event such as a key press can wake-up the processor.

Memory Interfaces

There are two main external memory interfaces.

The first one is the ROM / SRAM / FLASH-style interface that has programmable wait-state timings and includes burst-mode capability, with eight chip selects decoding six 256-Mbyte sections of addressable space. For maximum flexibility, each bank can be specified to be 8, 16, or 32 bits wide. This allows the use of 8-bit-wide boot ROM options to minimize over-

OVERVIEW *(cont.)*

all system cost. The on-chip boot ROM can be used in product manufacturing to serially download system code into system FLASH memory. To further minimize system memory requirements and cost, the ARM Thumb® instruction set is supported, providing for the use of high-speed 32-bit operations in 16-bit op-codes and yielding industry-leading code density.

The second is the programmable 16- or 32-bit-wide DRAM interface that allows direct connection of up to two banks of DRAM, each bank containing up to 256 Mbytes. To assure the lowest possible power consumption, the EP7212 supports self-refresh DRAMs, which are placed in a low-power state by the device when it enters the low-power Standby State. EDO and Fast Page DRAM are supported.

A DMA address generator is also provided that fetches video display data for the LCD controller from main DRAM memory. The display frame buffer start address is programmable. In addition, the built-in LCD controller can utilize external or internal SRAM for memory, thus eliminating the need for DRAMs.

Digital Audio Capability

The EP7212 uses its powerful 32-bit RISC processing engine to implement audio decompression algorithms in software. The nature of the on-board RISC processor and the availability of efficient C-compilers and other software development tools, ensures that a wide range of audio decompression algorithms can easily be ported to and run on the EP7212.

Serial Interfaces

The EP7212 includes two 16550-type UARTs for RS-232 serial communications, both of which have two 16-byte FIFOs for receiving and transmitting data. The UARTs support bit rates up to 115.2 kbps. An IrDA SIR protocol encoder / decoder can be optionally switched into the RX / TX signals to / from one of the UARTs to enable these signals to drive an infrared communication interface directly.

Digital Audio Interface (DAI)

The EP7212 integrates an interface to enable a direct connection to many low cost, low power, high quality audio converters. In particular, the DAI can directly interface with the Crystal® CS43L41 / 42 / 43 low-power audio DACs and the Crystal® CS53L32 low-power ADC. Some of these devices feature digital bass and treble boost, digital volume control and compressor-limiter functions.

Packaging

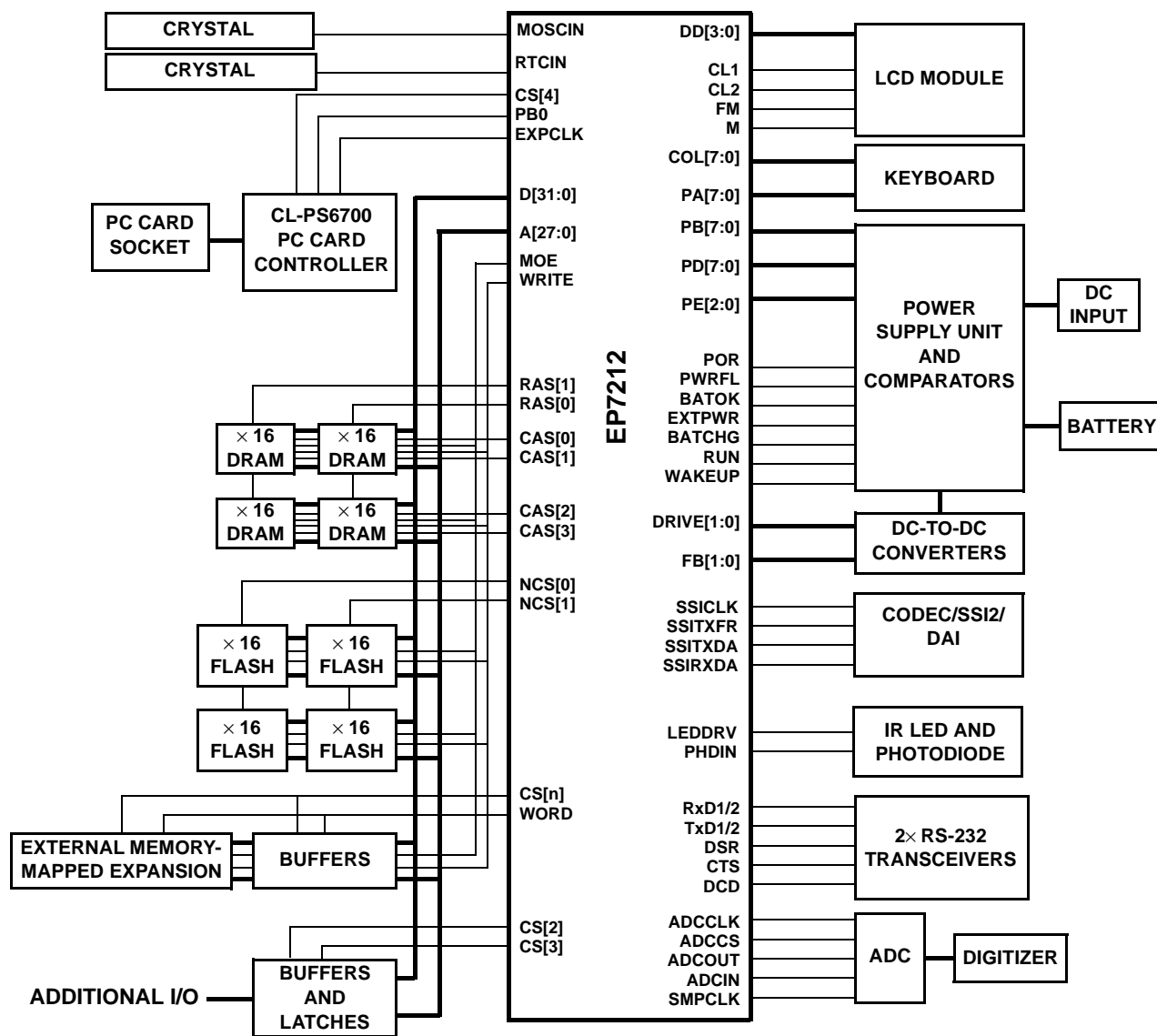The EP7212 is available in a 208-pin LQFP package and a 256-ball PBGA package.

System Design

As shown in system block diagram, simply adding desired memory and peripherals to the highly integrated EP7212 completes a low-power system solution. All necessary interface logic is integrated on-chip.

Contacting Cirrus Logic Support
For a complete listing of Direct Sales, Distributor, and Sales Representative contacts, visit the Cirrus Logic web site at:
http://www.cirrus.com/corporate/contacts/

CIRRUS LOGIC

A EP7212–Based System