

EMP-B50P12

Programmable Isolated IPM

PI-IPM™ Features:

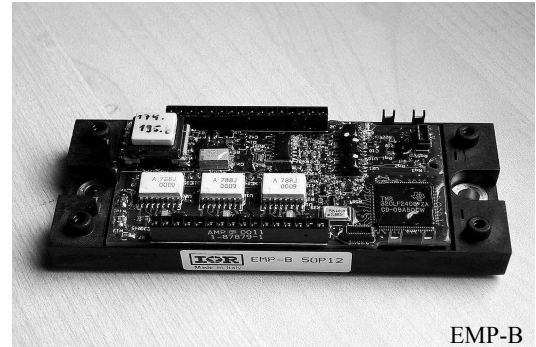
■ Power Module:

- NPT IGBTs 50A, 1200V
- 10us Short Circuit capability
 - Square RBSOA
 - Low $V_{ce(on)}$ (2.15Vtyp @ 50A, 25°C)
 - Positive $V_{ce(on)}$ temperature coefficient
- Gen III HexFred Technology
 - Low diode V_F (1.78Vtyp @ 50A, 25°C)
 - Soft reverse recovery
- 2mΩ sensing resistors on all phase outputs
 - T/C < 50ppm/°C

■ Embedded driving board

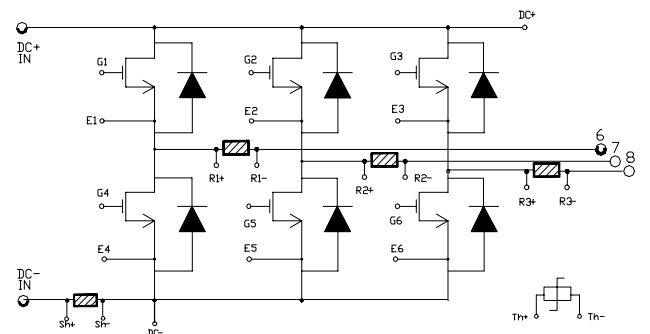
- Programmable 40 Mips DSP
- Current sensing feedback from all phases
- Full protection from ground and line to line faults
- UVLO, OVLO on DCbus voltage
- Embedded flyback smps for floating stages (single 15Vdc @ 300mA input required)
- Asynchronous isolated 2Mbps serial port for DSP communication and programming
- IEEE standard 1149.1 (JTAG port interface) for program downloading and debugging
- Separated turn on / turn off outputs for IGBTs di/dt control
- Isolated serial port input with strobe signal for quadrature encoders

Package:



EMP-B
(EMP™ – Inverter)
(EconoPack 2 outline compatible)

Power Module schematic:



Three phase inverter with current sensing resistors on all output phases

Description

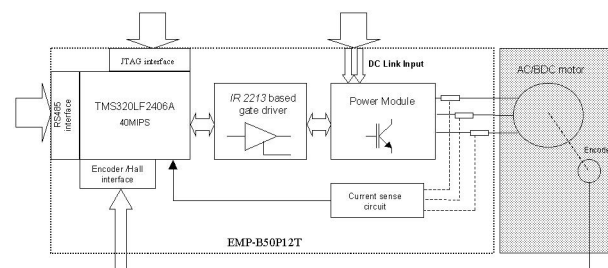
The EMP-B50P12 is a fully integrated Intelligent Power Module for high performances Servo Motor Driver applications.

The device core is a state of the art DSP, the TMS320LF2406A* at 40 Mips, interfaced with a full set of peripheral designed to handle all analog feedback and control signals needed to correctly manage the power section of the device.

The PI-IPM™ has been designed and tailored to implement internally all functions needed to close the current loop of a high performances servo motor driver, a basic software is already installed in the DSP and the JTAG connector allows the user to easily develop and download its own proprietary algorithm.

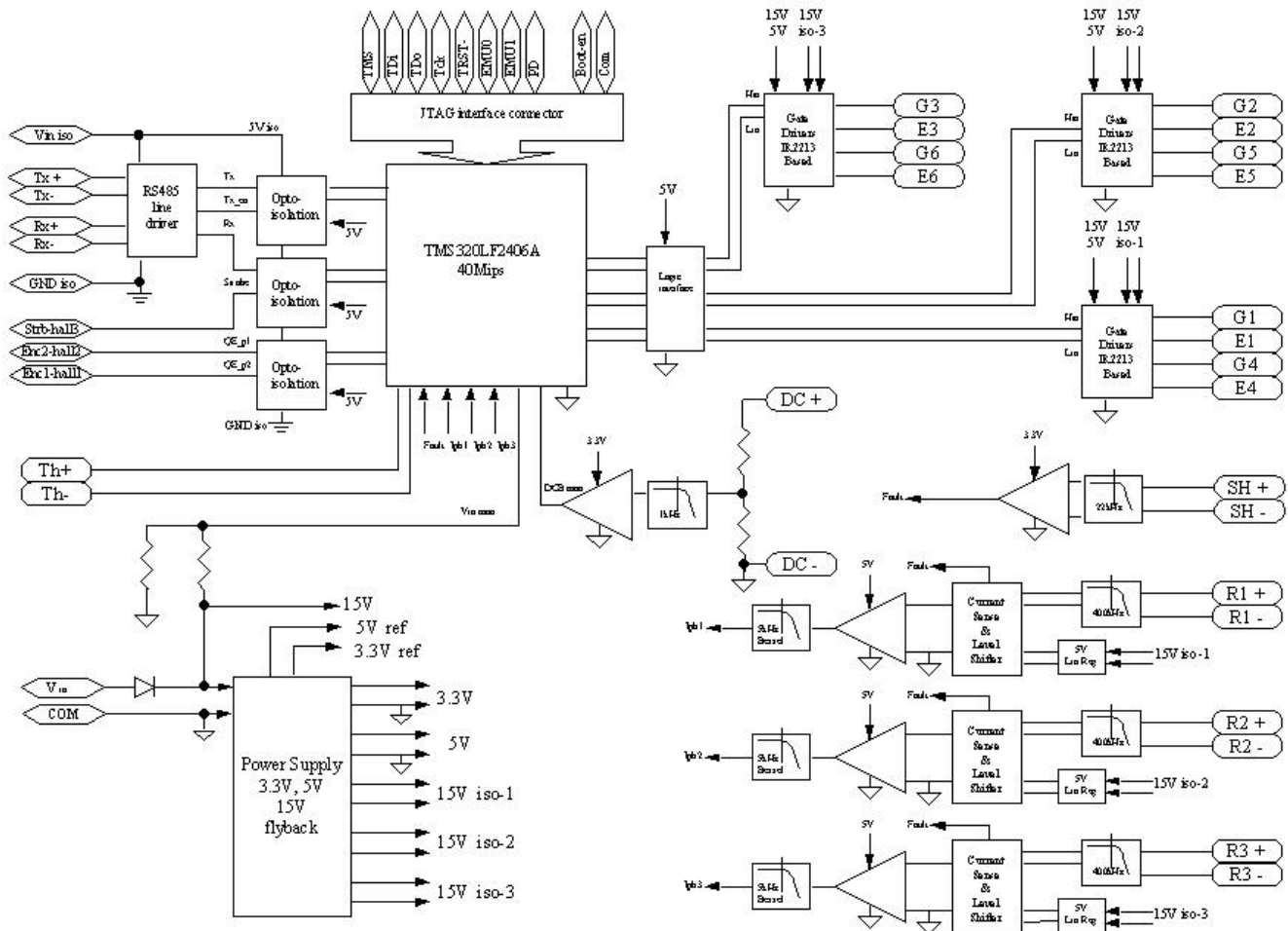
The device comes in the EMP™ package, fully compatible in length, width and height with the popular EconoPack 2 outline.

Control Board Block Schematic:



* First samples come with the TMS320LF2406 at 30Mips, please refer to TI datasheet for further information about performances.

Detailed Block Diagram



Signal pins on RS485 serial port

Symbol	Lead Description	Pin number	
Vin iso	External 5V supply voltage for opto-couplers and line driver supply	6	RS485 serial port
GND iso	External 5V supply ground reference for opto-couplers and line driver supply	7	
Tx+	RS485 Transmitter Non inverting Driver Output	1	
Tx-	RS485 Transmitter Inverting Driver Output	2	
Rx+	RS485 Receiver Non inverting Driver Input	4	
Rx-	RS485 Receiver Inverting Driver Input	3	
Enc1 – Hall1	Incremental Encoder Input 1 / Position hall effect sensor input 1 (GND iso referenced)	5	
Enc2 – Hall2	Incremental Encoder Input 2 / Position hall effect sensor input 2 (GND iso referenced)	9	
Strb – Hall3	Incremental Encoder Strobe Input / Position hall effect sensor input 3 (GND iso ref)	10	
Vin	External 15V supply voltage. Internally referred to DC bus minus pin (DC -)	17-18	
COM	External 15V supply ground reference. This pin is directly connected to DC -	19-20	

Signal pins on IEEE1149.1 JTAG connector

Symbol	Lead Description	State	Pin number	
TMS	JTAG test mode select	Input	12	IEEE1149.1 JTAG
TDI	JTAG test data input	Input	14	
TDO	JTAG test data output	Output	13	
TCK	JTAG test clock. TCK is a 10MHz clock source from the emulation pod. This signal can be used to drive the system test clock.	Input	15	
TRST-	JTAG test reset	Input	11	
EMU0	Emulation pin 0	I/O	9-10	
EMU1	Emulation pin 1	I/O	7-8	
PD	Presence detect. Indicates that the emulation cable is connected and that the PI-IPM logic is powered up. PD is tied to the DSP 3.3V supply through a 1k resistor.	Output	1	
TCK_RET	JTAG test clock return. Test clock input to the emulator. Internally short circuited to TCK.	Output	16	
Boot-En	Boot ROM enable. This pin is sampled during DSP reset, pulling it low enables DSP boot ROM (Only in Flash versions). 47k internal pull up.	Input	17	
COM	External 15V supply ground reference. This pin is directly connected to DC -	N/A	20	

Following pins are intended for signal communication between driving board and power module only ,
though here described for completeness, they are on purpose not available to the user.

DC +	DC Bus plus input signal	Lateral connectors on embedded driving board
DC -	DC Bus minus input signal (internally connected to COM)	
Th +	Thermal sensor positive input	
Th -	Thermal sensor negative input (internally connected to COM)	
Sh +	DC Bus minus series shunt positive input (Kelvin point)	
Sh -	DC Bus minus series shunt negative input (internally connected to COM, Kelvin point)	
G1/2/3	Gate connections for high side IGBTs	
E1/2/3	Emitter connections for high side IGBTs (Kelvin points)	
R1/2/3 +	Output current sensing resistor positive input (IGBTs emitters 1/2/3 side, Kelvin points)	
R1/2/3 -	Output current sensing resistor negative input (Motor side, Kelvin points)	
G4/5/6	Gate connections for low side IGBTs	
E4/5/6	Emitter connections for low side IGBTs (Kelvin points)	

Absolute Maximum Ratings ($T_C=25^{\circ}\text{C}$)

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{DC-} , all currents are defined positive into any lead. Thermal Resistance and Power Dissipation ratings are measured at still air conditions.

	Symbol	Parameter Definition	Min.	Max.	Units
Inverter	V_{DC}	DC Bus Voltage	0	1000	V
	V_{CES}	Collector Emitter Voltage	0	1200	
	$I_C @ 100^{\circ}\text{C}$	IGBTs continuous collector current ($T_C = 100^{\circ}\text{C}$)		50	A
	$I_C @ 25^{\circ}\text{C}$	IGBTs continuous collector current		100	
	I_{CM}	Pulsed Collector Current (Fig.3, Fig. CT.5)		200	
	I_F	Diode Continuous Forward Current ($T_C = 100^{\circ}\text{C}$)		50	
	I_{FM}	Diode Maximum Forward Current		200	
	V_{GE}	Gate to Emitter Voltage	-20	+20	V
	$P_D @ 25^{\circ}\text{C}$	Power Dissipation (One transistor)		600	W
	$P_D @ 100^{\circ}\text{C}$	Power Dissipation (One transistor, $T_C = 100^{\circ}\text{C}$)		250	
Driving Board	V_{in}	Non isolated supply voltage (DC- referenced)	-20	20	V
	V_{in-iso}	Isolated supply voltage (GND iso referenced)	0	5.5	
	R_X	RS485 Receiver input voltage (GND iso referenced)	- 7	12	
Power Module	MT	Mounting Torque		3.5	Nm
	T_J	Operating Junction Temperature	-40	+150	$^{\circ}\text{C}$
	T_{STG}	Storage Temperature Range	-40	+150	
	V_{C-iso}	Isolation Voltage to Base Copper Plate	-2500	+2500	V

Electrical Characteristics: Inverter

For proper operation the device should be used within the recommended conditions.

$T_J = 25^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter Definition	Min.	Typ.	Max.	Units	Test Conditions	Fig.
$V_{(BR)CES}$	Collector To Emitter Breakdown Voltage	1200			V	$V_{GE} = 0V, I_C = 250\mu A$	
$\Delta V_{(BR)CES} /$	Temperature Coeff. of Breakdown Voltage		+1.2		$V/^{\circ}\text{C}$	$V_{GE} = 0V, I_C = 1mA (25 - 125^{\circ}\text{C})$	
$V_{CE(on)}$	Collector To Emitter Saturation Voltage		2.15	2.34	V	$I_C = 50A, V_{GE} = 15V$	5, 6
			3.24	3.78		$I_C = 100A, V_{GE} = 15V$	7,9
			2.6V	3.0		$I_C = 50A, V_{GE} = 15V, T_J = 125^{\circ}\text{C}$	10,11
$V_{GE(th)}$	Gate Threshold Voltage	4.4	4.7	5.5	V	$V_{CE} = V_{GE}, I_C = 250\mu A$	9,10
$\Delta V_{GE(th)} / \Delta T_J$	Temp. Coeff. of Threshold Voltage		-1.2		$mV/^{\circ}\text{C}$	$V_{CE} = V_{GE}, I_C = 1mA (25 - 125^{\circ}\text{C})$	11,12
g_{fe}	Forward Transconductance	29	33	38	S	$V_{CE} = 50V, I_C = 50A, PW = 80\mu s$	
I_{CES}	Zero Gate Voltage Collector Current			500	μA	$V_{GE} = 0V, V_{CE} = 1200V$	
			650	1350		$V_{GE} = 0V, V_{CE} = 1200V, T_J = 125^{\circ}\text{C}$	
				4000		$V_{GE} = 0V, V_{CE} = 1200V, T_J = 150^{\circ}\text{C}$	
V_{FM}	Diode Forward Voltage Drop		1.78	2.1	V	$I_C = 50A$	8
			1.90	2.22		$I_C = 50A, T_J = 125^{\circ}\text{C}$	8
I_{RM}	Diode Reverse Leakage Current			20	μA	$V_R = 1200V, T_J = 25^{\circ}\text{C}$	
I_{GES}	Gate To Emitter Leakage Current			± 200	nA	$V_{GE} = 20V$	

Electrical Characteristics: Inverter (continued)

R1/2/3	Sensing Resistors	1.9	2	2.1	mΩ		
Rsh	DC bus minus series shunt resistor	4.75	5	5.25			

Switching Characteristics: Inverter

For proper operation the device should be used within the recommended conditions.

T_J = 25°C (unless otherwise specified)

Symbol	Parameter Definition	Min	Typ	Max	Units	Test Conditions	Fig.
Q _g	Total Gate Charge (turn on)		338	508	nC	I _C = 50A	23 CT1
Q _{ge}	Gate – Emitter Charge (turn on)		38	58		V _{DC} = 600V	
Q _{gc}	Gate – Collector Charge (turn on)		164	246		V _{GE} = 15V	
E _{on}	Turn on Switching Loss		2345	2750	μJ	I _C = 50A, V _{DC} = 600V, T _J = 25 °C	CT1
E _{off}	Turn off Switching Loss		3284	3960		V _{GE} = 15V, R _G = 10Ω, L = 200μH	WF1
E _{tot}	Total Switching Loss		5630	6710		Tail and Diode Rev. Recovery included	WF2
E _{on}	Turn on Switching Loss		3652	4083	μJ	I _C = 50A, V _{DC} = 600V, T _J = 125 °C	13, 15 CT1 WF1 WF2
E _{off}	Turn off Switching Loss		4660	5676		V _{GE} = 15V, R _G = 10Ω, L = 200μH	
E _{tot}	Total Switching Loss		8312	9759		Tail and Diode Rev. Recovery included	
t _d (on)	Turn on delay time		50	65	ns	I _C = 50A, V _{DC} = 600V, T _J = 125 °C	14,16 CT1 WF1 WF2
t _r	Rise time		50	70			
t _d (off)	Turn off delay time		300	400			
t _f	Fall time		30	45			
C _{ies}	Input Capacitance		4400		pF	V _{DC} = 30V	22
C _{oes}	Output Capacitance		420			V _{GE} = 0V	
C _{res}	Reverse Transfer Capacitance		170			f = 1MHz	
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				T _J = 150 °C, I _C = 250A, V _{GE} = 15V to 0V V _{CC} = 1000V, V _p = 1200V, R _G = 5Ω	4 CT2
SCSOA	Short Circuit Safe Operating Area	10			μs	T _J = 150 °C, V _{GE} = 15V to 0V V _{CC} = 900V, V _p = 1200V, R _G = 5Ω	CT3 WF4
E _{rec}	Diode reverse recovery energy		3200	4300	μJ	T _J = 125 °C	17,18 19,20 21 CT4 WF3
t _{rr}	Diode reverse recovery time		150		ns	I _C = 50A, V _{DC} = 600V,	
I _{rr}	Peak reverse recovery current		56	72	A	V _{GE} = 15V, R _G = 10Ω, L = 200μH	
R _{thJ-C,T}	Each IGBT to copper plate thermal resistance			0.35	°C/W		
R _{thJ-C,D}	Each Diode to copper plate thermal resistance			0.60	°C/W		
P _{diss}	Total Dissipated Power		65		W	I _C = 7A, V _{DC} = 515V, f _{sw} = 4kHz	PD1
			180			I _C = 7A, V _{DC} = 515V, f _{sw} = 16kHz	
			155			I _C = 20A, V _{DC} = 515V, f _{sw} = 2kHz	PD3
			210			I _C = 20A, V _{DC} = 515V, f _{sw} = 4kHz	

Electrical Characteristics: Embedded Driving Board (EDB) communication ports

For proper operation the device should be used within the recommended conditions.

V_{in} = 15V, V_{in-iso} = 5V, T_C = T_{MIN} to T_{MAX} (unless otherwise specified)

Symbol	Parameter Definition	Min.	Typ.	Max.	Units	Test Conditions	Conn.
V _{in}	EDB Input supply Voltage	12	15	18	V		RS485 port
I _{supp}	EDB Input Supply Current	180		250	mA	V _{DC} = 600V, f _{PWM} = 16kHz	
V _{in iso}	EDB isolated supply voltage	4.5	5	5.5	V		
I _{q. iso}	EDB isolated quiescent supply current		9	15	mA	Rx+ =Vin iso, Rx- =GND iso Hall1/2/3 = open, Tx enabled by DSP	
I _{supp. iso}	EDB isolated supply current	30	40	50	mA	Hall1/2/3 low, Tx enabled. Rx+ =GND iso, Rx- =Vin iso	
V _{DO-TX}	Differential Driver Output Voltage	2			V	Rload = 120 Ω	RS485 port
V _{CO-TX}	Driver Common mode output voltage			3	V		
V _{DI-RX}	Receiver Input Differential Threshold Voltage	- 0.2		0.2	V	- 7V ≤ V _{CM} ≤ +12V	
R _{IN-RX}	Receiver Input Resistance		120		Ω		
f _{MAX}	RS485 maximum data rate	2			Mbps		
V _{enc-high} / V _{hall-high}	Logic High Input Voltage	3.6			V	Enc1 / Hall1 Enc2 / Hall2 Strb / Hall3 input pins	RS485 port
V _{enc-low} / V _{hall-low}	Logic Low Input Voltage			2	V		
I _{enc-low} / I _{hall-low}	Logic Low Input Current	- 5.2			mA		
TMS TDI TDO TCK TRST- EMU0 EMU1 PD	JTAG interface pins	Please see TMS320LF2406A datasheet from Texas Instruments and V _{PD} specifications				Directly connected from DSP to connector pins. EMU0 and EMU1 with 4.7k internal pull up.	JTAG
V _{PD}	Presence detect voltage	3.2	3.3	3.4	V	I _{PD} =-100μA	JTAG
V _{Boot En}	Boot ROM enable input voltage			0.5	V	Active low	JTAG
I _{Boot-En}	Boot ROM enable input current			- 100	μA		

AC Electrical Characteristics: Embedded Driving Board (EDB)

DSP pins mapping

For proper operation the device should be used within the recommended conditions.

V_{in} = 15V, V_{in-iso} = 5V, T_C = T_{MIN} to T_{MAX} (unless otherwise specified)

Symbol	Parameter Definition	Min.	Typ.	Max.	Units	Test Conditions	DSP pin
V _{DCgain}	DC bus voltage feedback partition coefficient	3.40	3.47	3.54	mV/V		72
V _{DCpole}	DC bus voltage feedback filter pole	680	720	760	Hz		
V _{THgain}	Thermal sensor feedback value at 25 °C ¹	2.150	2.268	2.382	V		70
V _{in-gain}	Input voltage feedback partition coefficient	125	128	131	mV/V		69
V _{in-pole}	Input voltage feedback filter pole	1600	1700	1800	Hz		
I _{ph-GAIN}	Current feedback gain	16.3	16.5	16.7	mV/A	all phases	ph1: 79 ph2: 77 ph3: 74
I _{ph-pole}	Current feedback filter pole ³	4.3	5.0	5.7	kHz		
I _{ph-LAT}	Current feedback signal delay			12	μs		
I _{ph-Zero}	Zero current input voltage level ²	1.63	1.65	1.67	V		
I _{SC}	Short Circuit Threshold Current	110	128	146	A	all phases	6
I _{SC-DEL}	Short Circuit detection delay time		3	6	μs	all phases	
DC _{OC}	DC bus minus over-current level	55	60	65	A	DC bus minus	6
DC _{OC-pole}	DC bus minus over-current filter pole		400		kHz	DC bus minus	
WD	External watchdog timeout (see also RS~ signal)	0.9	1.6	2.5	Sec		85
PDPINTB	Power Down Protection Interrupt B		3.3		V	4.7k pull up	95
COM	DSP Ground	2, 3, 5, 7, 11, 12, 13, 14, 15, 19, 21, 22, 23, 24, 26, 27, 29, 32, 34, 38, 41, 43, 45, 46, 48, 49, 50, 53, 56, 58, 60, 63, 65, 66, 67, 68, 71, 73, 75, 76, 78, 80, 81, 84, 90, 97					
3.3V	DSP 3.3V supply	4, 10, 20, 30, 35, 47, 54, 59, 64, 91, 98					

¹ For sensing voltage vs. temperature complete characteristic see also figure

² This offset is then internally corrected through a DSP software routine.

³ First samples have been assembled with a 20kHz filter pole

Other DSP pins mapping

Symbol	Signal Definition	DSP pin	Comments
PWM1	Phase 1 high side IGBT gate drive signal	39	DSP Event Manager A output
PWM2	Phase 1 low side IGBT gate drive signal	37	DSP Event Manager A output
PWM3	Phase 2 high side IGBT gate drive signal	36	DSP Event Manager A output
PWM4	Phase 2 low side IGBT gate drive signal	33	DSP Event Manager A output
PWM5	Phase 3 high side IGBT gate drive signal	31	DSP Event Manager A output
PWM6	Phase 3 low side IGBT gate drive signal	28	DSP Event Manager A output
Enc1 - Hall1	Incremental Encoder input 1	57	Optically isolated input
Enc2 - Hall2	Incremental Encoder input 2	55	Optically isolated input
Strb - Hall3	Incremental Encoder Strobe signal	52	Optically isolated input
Ref3.3V	3.3V reference voltage	82, 83	3.3V reference voltage for ADC converter
5V supp.	Flash programming voltage pin	40	Supplied by the embedded flyback regulator
Boot En~	Boot ROM enable signal	86	See also EDB electrical characteristics
Tx	SCI transmit data	17	Drives Tx+ and Tx- through an opto-isolator and a line driver
Rx	SCI receive data	18	Driven by Rx+ and Rx- through an opto-isolator and a line driver
Tx-En	SCI transmit enable	16	Transmit enable for SCI line driver
LFAULT	System general fault input (latched)	92	Activated by short circuits on output phases and DC bus minus
LFAULT reset	System general fault output reset signal	89	LFAULT Reset signal, to be activated via software after a fault or system boot
FAULT~	System general fault input (not latched)	6	Activated by short circuits on output phases and DC bus minus
RS~	DSP reset input signal (see also WD signal)	93	Forces a DSP reset if WD signal holds too long (see also EDB electrical char.)
Xtal1	PLL oscillator input pin	87	A 10Mhz oscillator at 100ppm frequency stability feeds this pin.
PLL1	PLL filter input 1	9	PLL filter for 40Mhz DSP clock frequency
PLL2	PLL filter input 2	8	PLL filter for 40Mhz DSP clock frequency

~ indicates active low signals

Fig.1 - Maximum DC Collector Current vs. Case Temperature

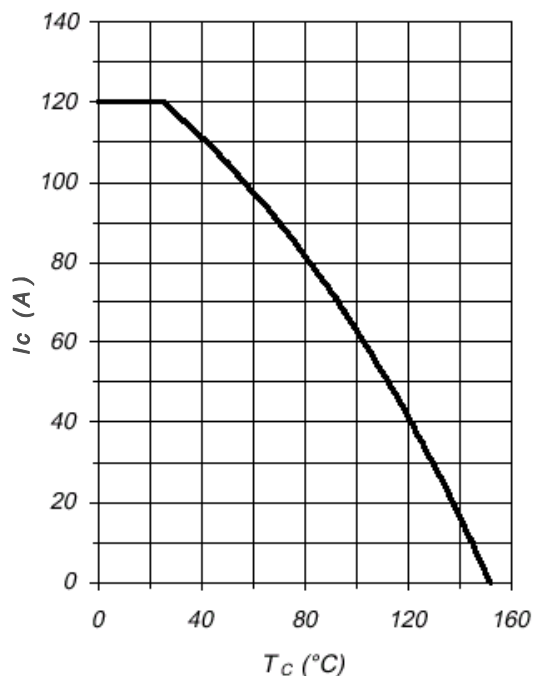


Fig.2 - Power Dissipation vs. Case Temperature

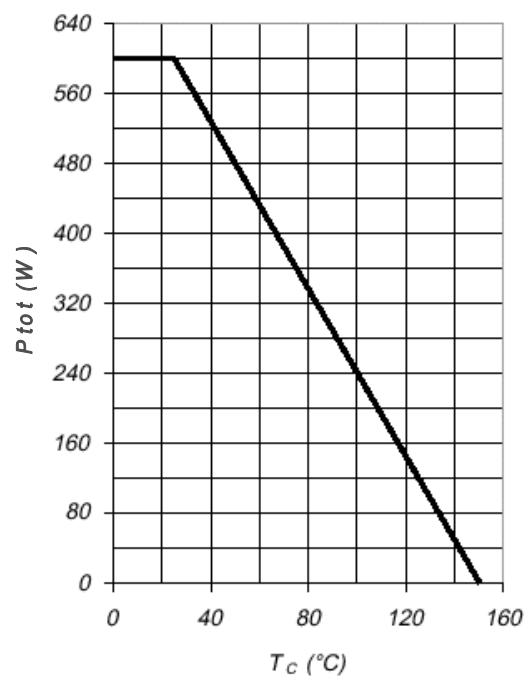


Fig.3 - Forward SOA
 $T_C=25^\circ\text{C}$; $T_J \leq 150^\circ\text{C}$

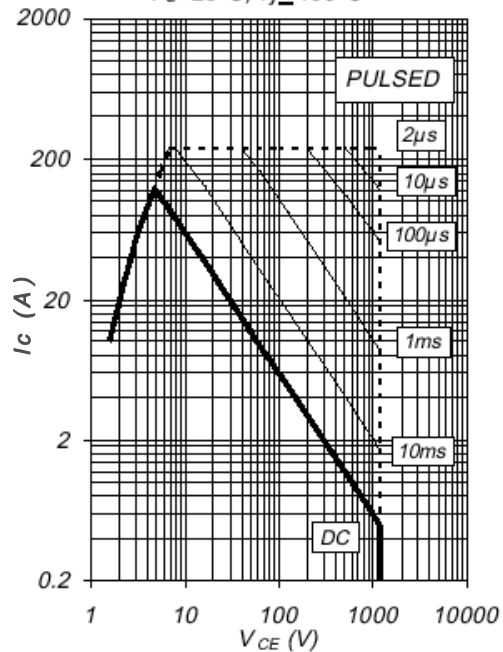


Fig.4 - Reverse Bias SOA
 $T_J = 150^\circ\text{C}$, $V_{GE} = 15\text{V}$

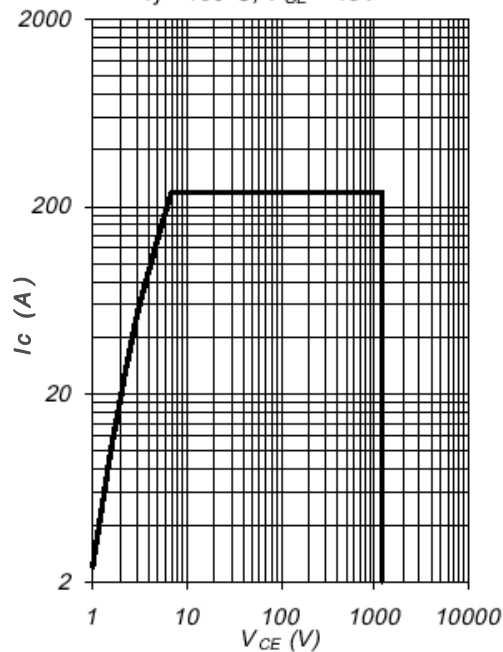


Fig.5 - Typical IGBT Output
Characteristics
 $T_j = -40^\circ\text{C}$; $t_p = 300\mu\text{s}$

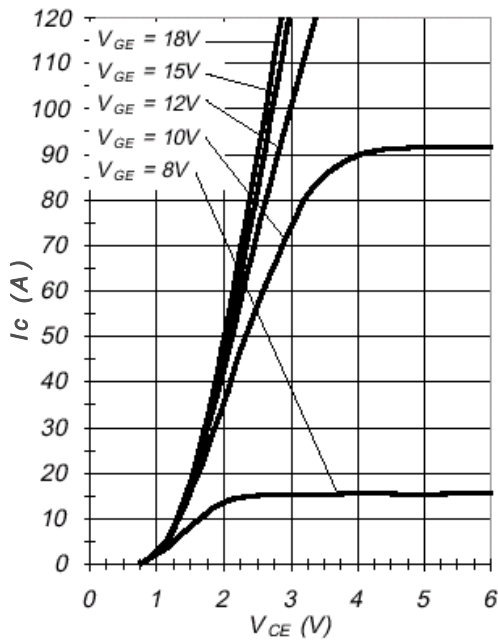


Fig.6 - Typical IGBT Output
Characteristics
 $T_j = 25^\circ\text{C}$; $t_p = 300\mu\text{s}$

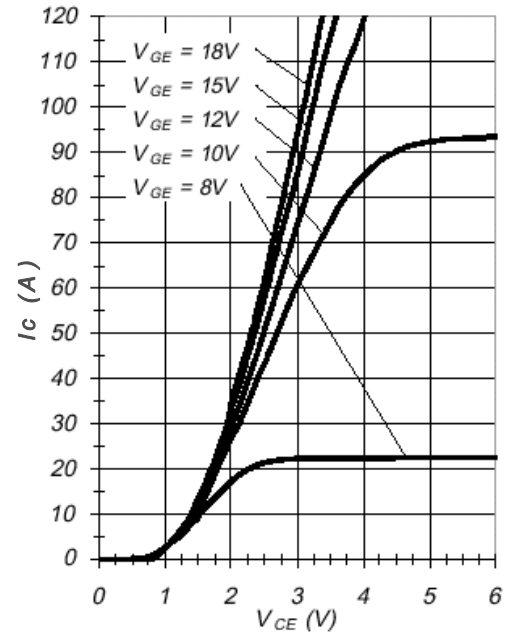


Fig.7 - Typical IGBT Output
Characteristics
 $T_j = 125^\circ\text{C}$; $t_p = 300\mu\text{s}$

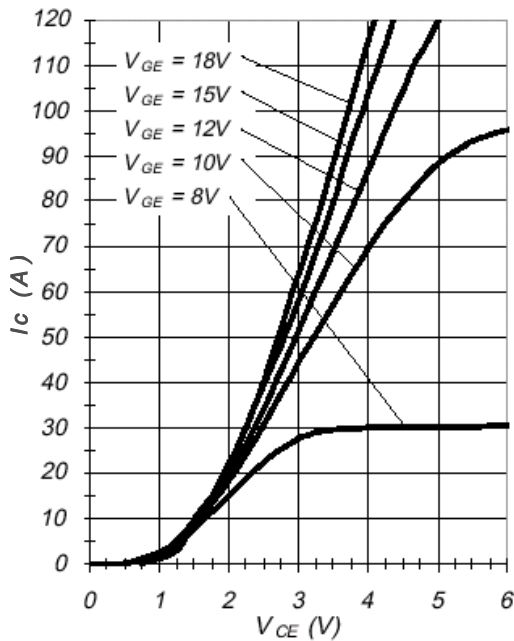


Fig.8 - Typical Diode Forward
Characteristic
 $t_p = 300\mu\text{s}$

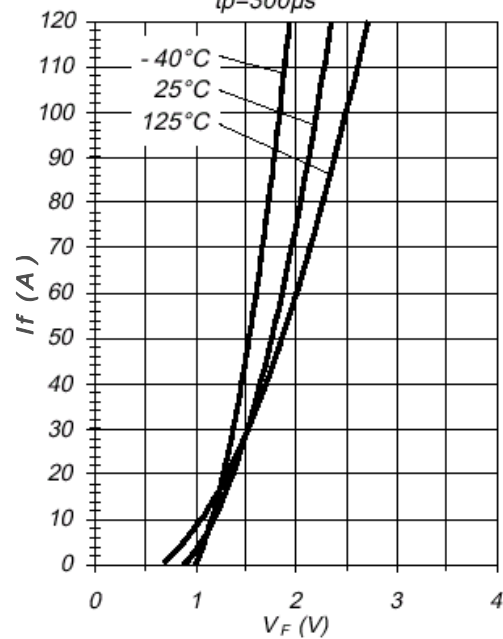


Fig.9 - Typical V_{CE} vs V_{GE}
 $T_j = -40^\circ\text{C}$

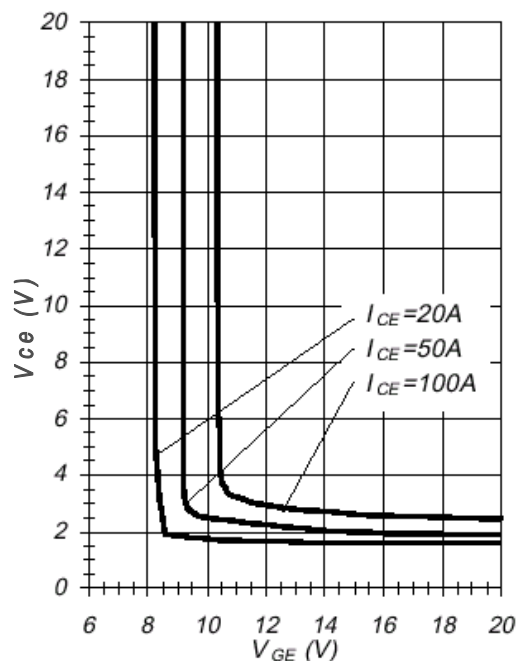


Fig.10 - Typical V_{CE} vs V_{GE}
 $T_j = 25^\circ\text{C}$

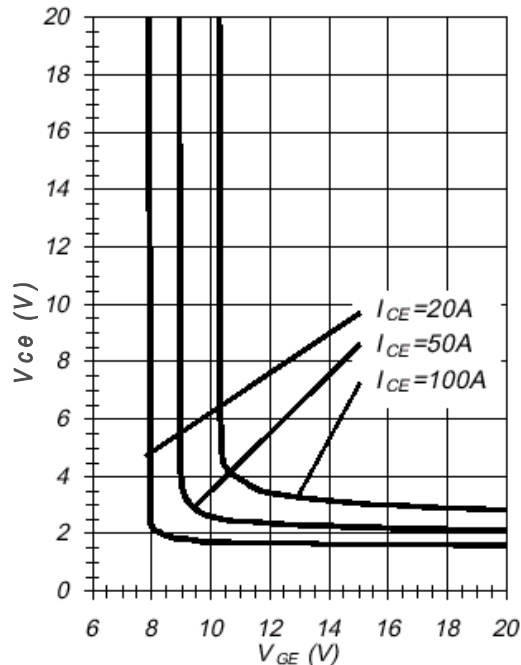


Fig.11 - Typical V_{CE} vs V_{GE}
 $T_j = 125^\circ\text{C}$

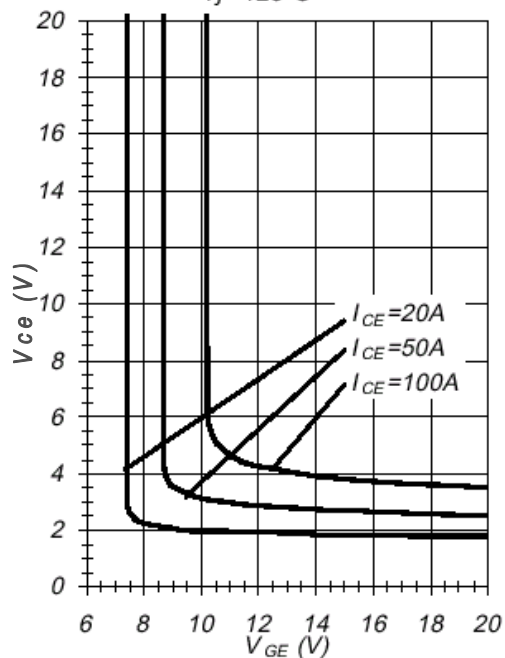


Fig.12 - Typ. Transfer Characteristics
 $V_{CE} = 20\text{V}$; $t_p = 20\mu\text{s}$

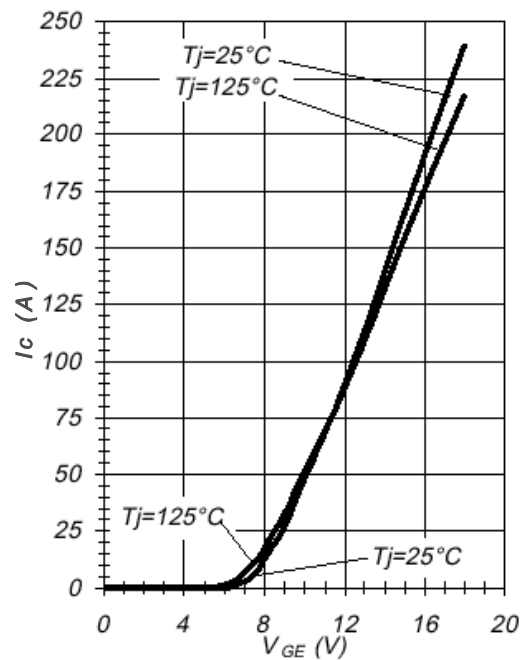


Fig.13 - Typical Energy Loss vs I_C
 $T_j=125^\circ\text{C}$; $L=200\mu\text{H}$; $V_{CE}=600\text{V}$;
 $R_g=10\Omega$; $V_{GE}=15\text{V}$

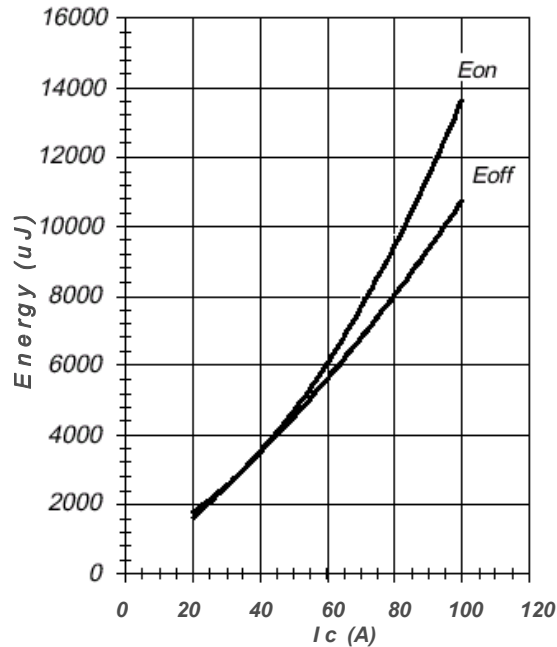


Fig.14 - Typical Switching Time vs I_C
 $T_j=125^\circ\text{C}$; $L=200\mu\text{H}$; $V_{CE}=600\text{V}$;
 $R_g=10\Omega$; $V_{GE}=15\text{V}$

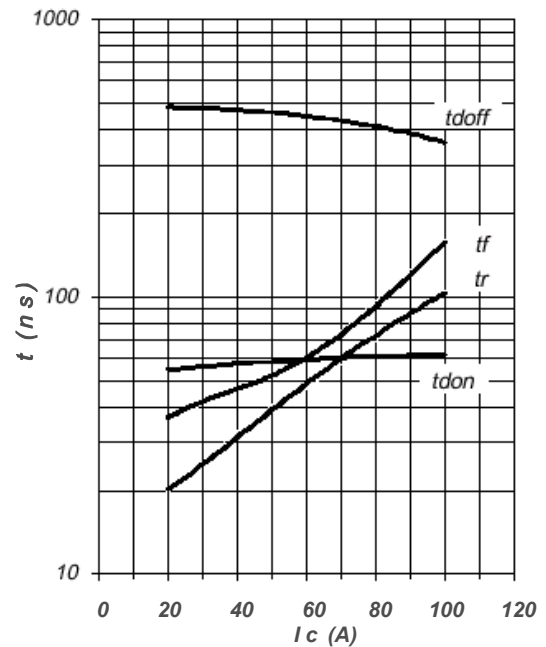


Fig.15 - Typical Energy Loss vs R_g
 $T_j=125^\circ\text{C}$; $L=200\mu\text{H}$; $V_{CE}=600\text{V}$;
 $I_{CE}=50\text{A}$; $V_{GE}=15\text{V}$

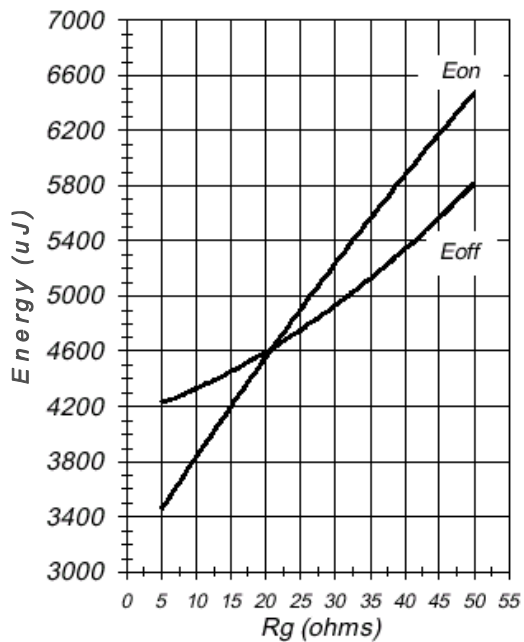


Fig.16 - Typical Switching Time vs R_g
 $T_j=125^\circ\text{C}$; $L=200\mu\text{H}$; $V_{CE}=600\text{V}$;
 $I_{CE}=50\text{A}$; $V_{GE}=15\text{V}$

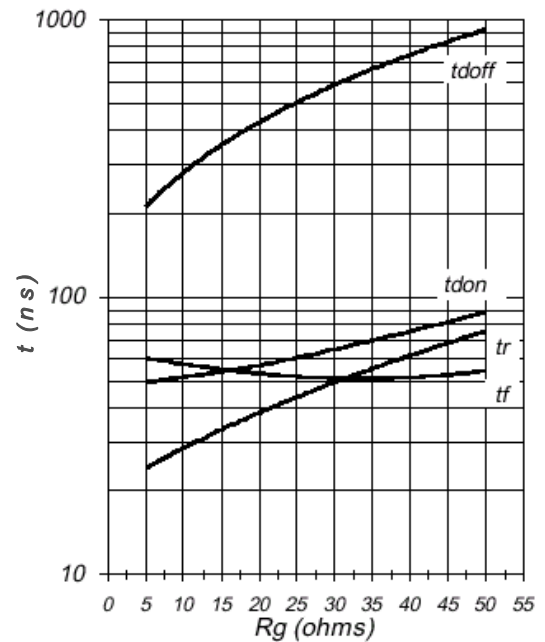


Fig.17 - Typical Diode I_{RR} vs I_F
 $T_j=125^\circ\text{C}$

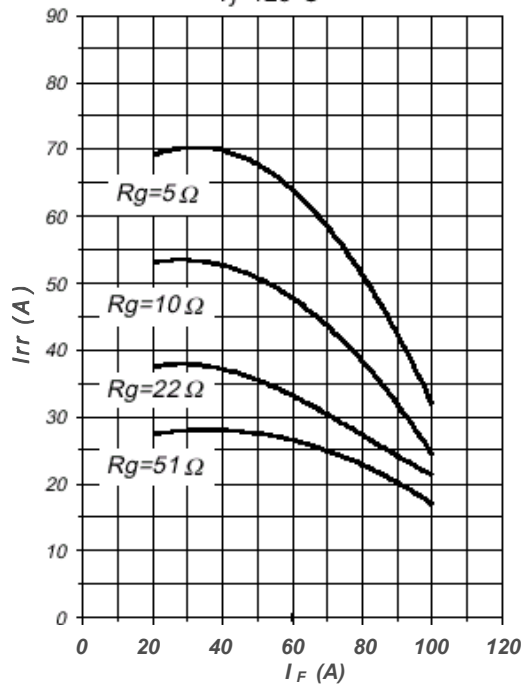


Fig.18 - Typical Diode I_{RR} vs R_g
 $T_j=125^\circ\text{C}; I_F=50\text{A}$

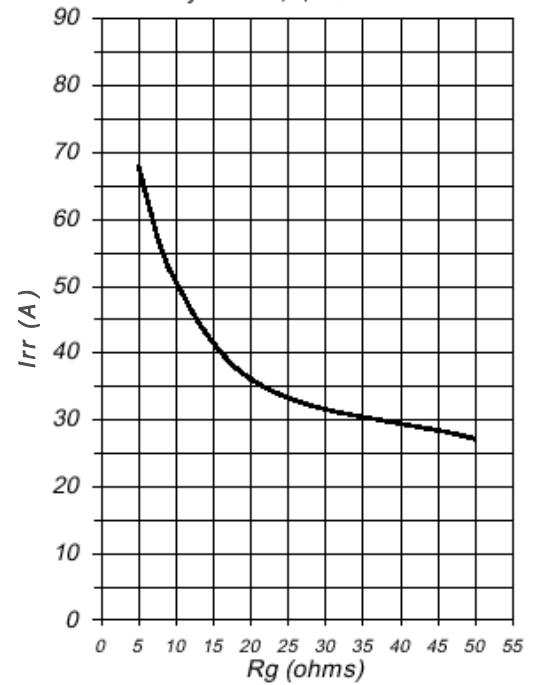


Fig.19 - Typical Diode I_{RR} vs di_F/dt
 $V_{CC}=600\text{V}; V_{GE}=15\text{V}$
 $I_F=50\text{A}; T_j=125^\circ\text{C}$

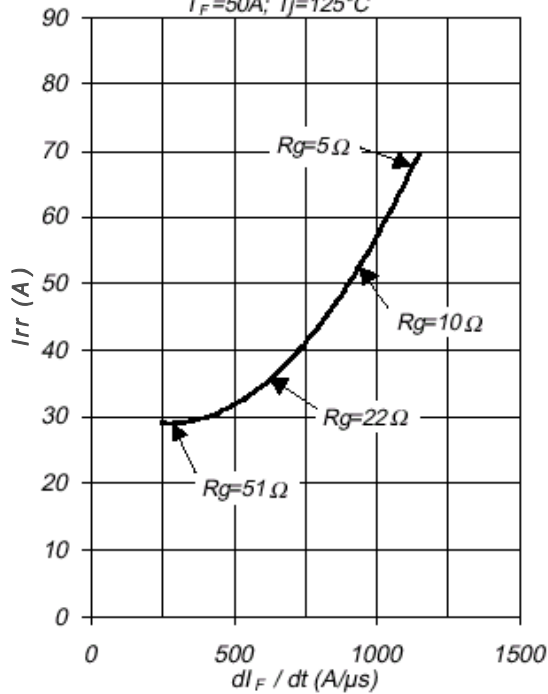


Fig.20 - Typical Diode Q_{RR}
 $V_{CC}=600\text{V}; V_{GE}=15\text{V}; T_j=125^\circ\text{C}$

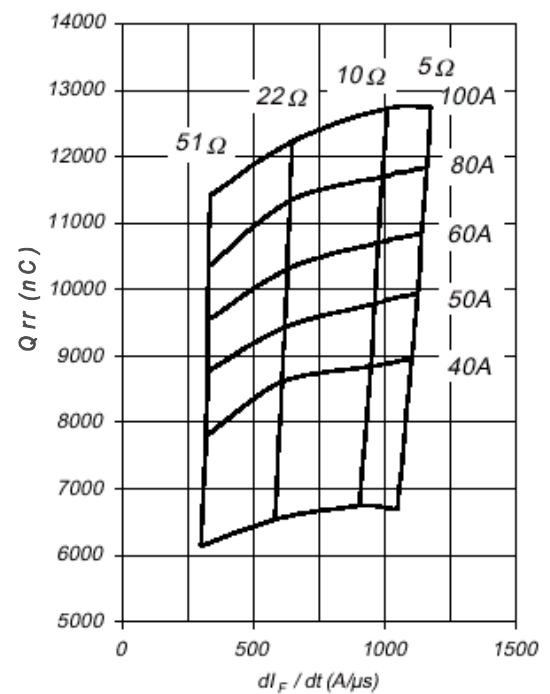


Fig.21 - Typ. Diode E_{rec} vs. I_F
 $T_J=125^\circ\text{C}$

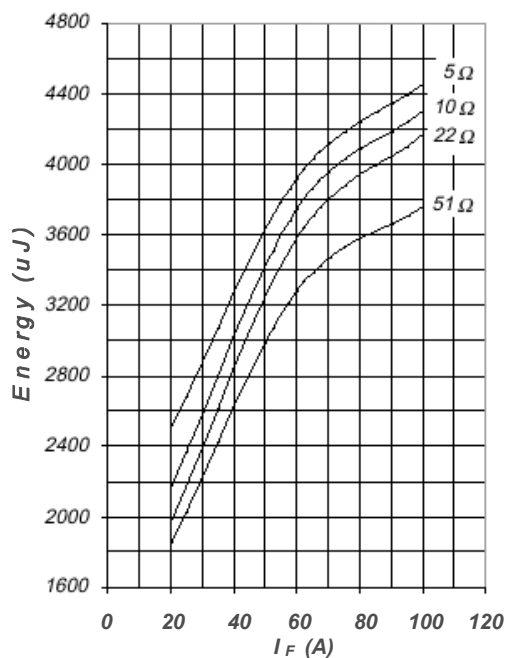


Fig.22 - Typical Capacitance vs V_{CE}
 $V_{GE}=0\text{V}$; $f=1\text{MHz}$

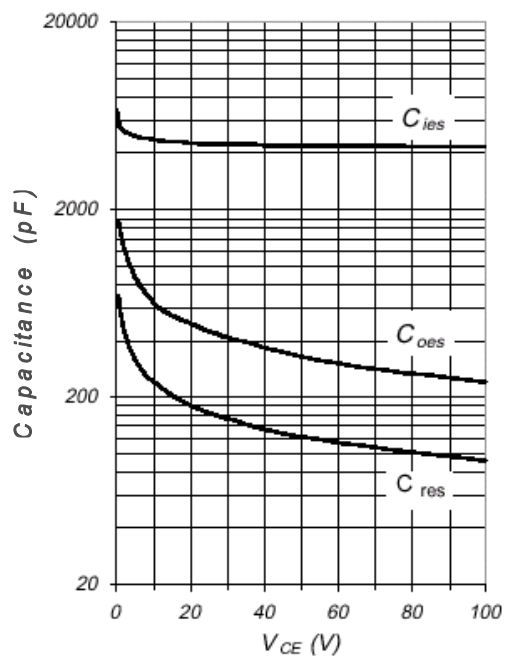


Fig.23 - Typ. Gate Charge vs. V_{GE}
 $I_C=25\text{A}$; $L=600\mu\text{H}$

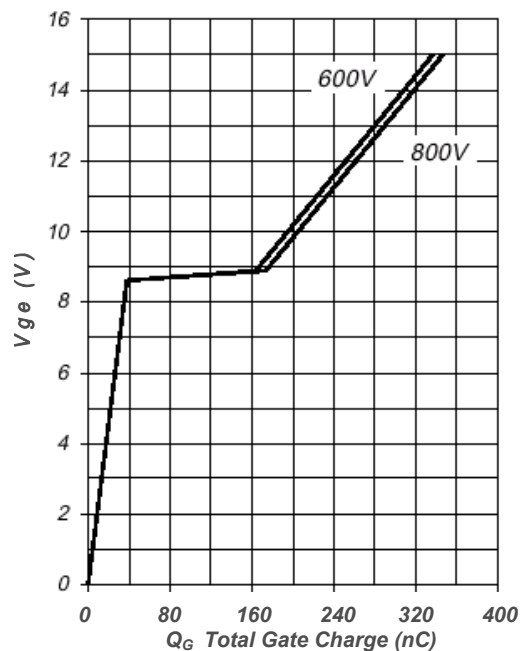


Fig. CT.1 - Gate Charge Circuit (turn-off)

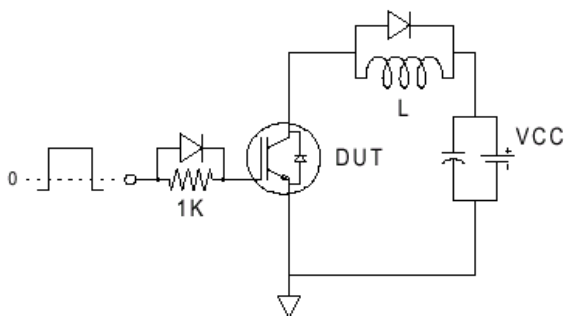


Fig. CT.2 - RBSOA Circuit

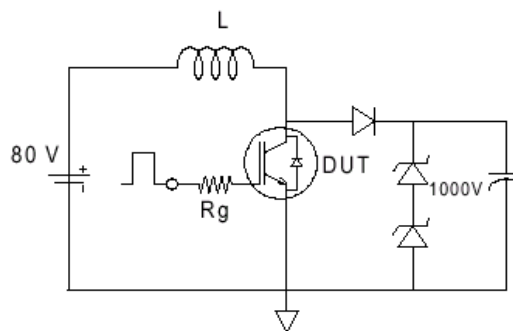


Fig. CT.3 - S.C. SOA Circuit

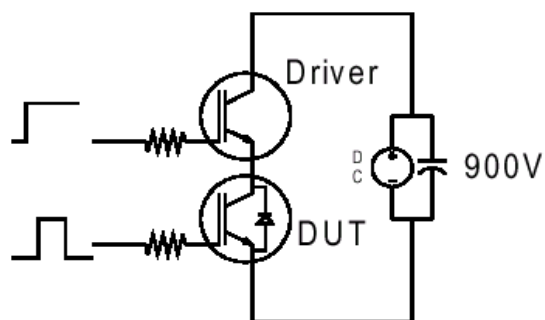


Fig. CT.4 - Switching Loss Circuit

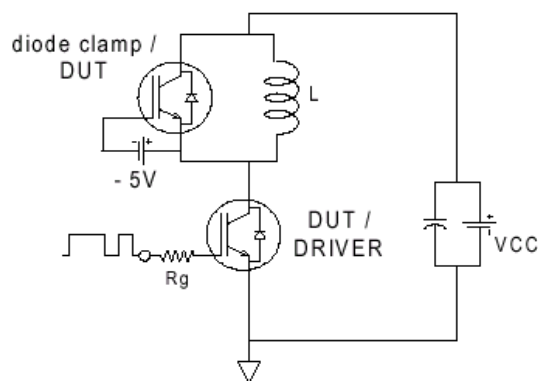


Fig. CT.5 - Resistive Load Circuit

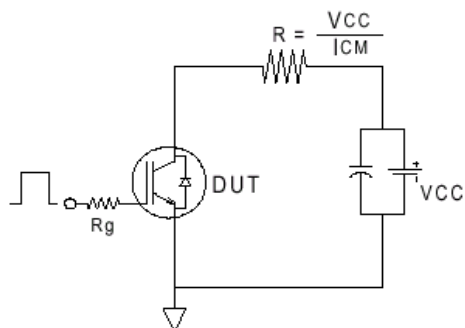


Fig. WF.1 - Typ. Turn-off Loss Waveform
@ $T_j=125^\circ\text{C}$ using Fig. CT.4

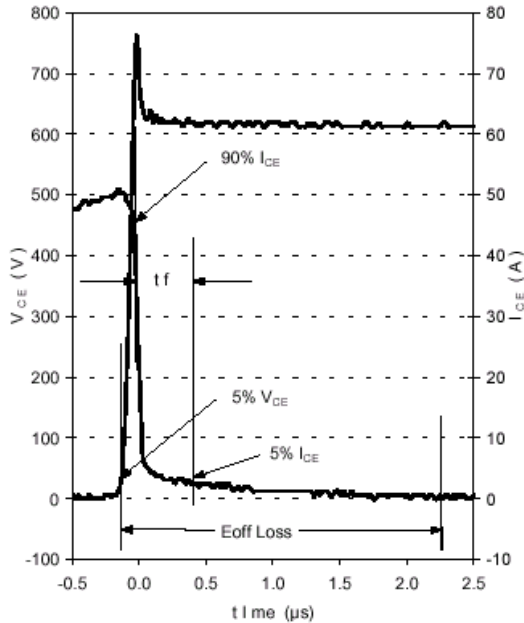


Fig. WF.2 - Typ. Turn-on Loss Waveform
@ $T_j=125^\circ\text{C}$ using Fig. CT.4

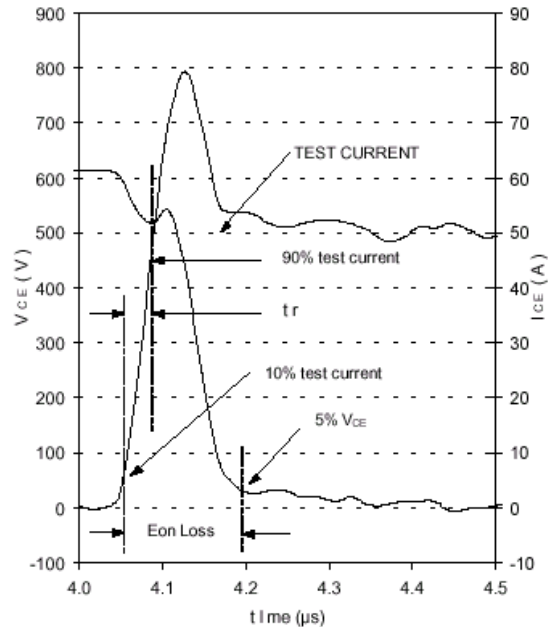


Fig. WF.3 - Typ. Diode Recovery Waveform
@ $T_j=125^\circ\text{C}$ using Fig. CT.4

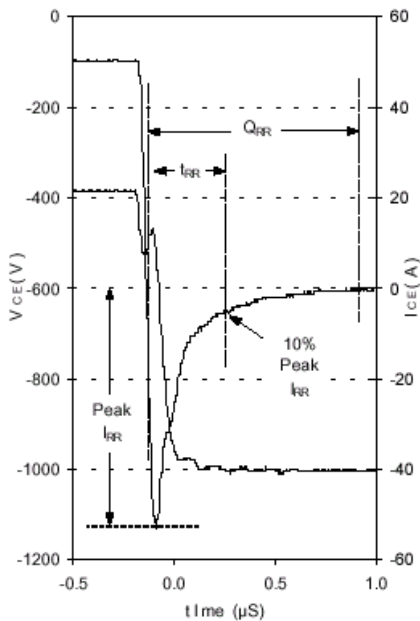
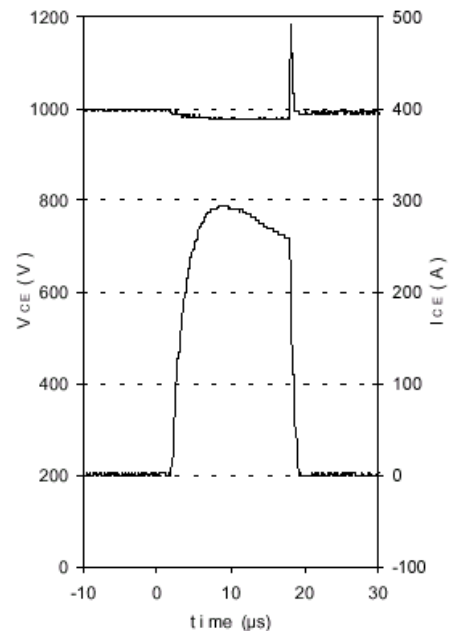
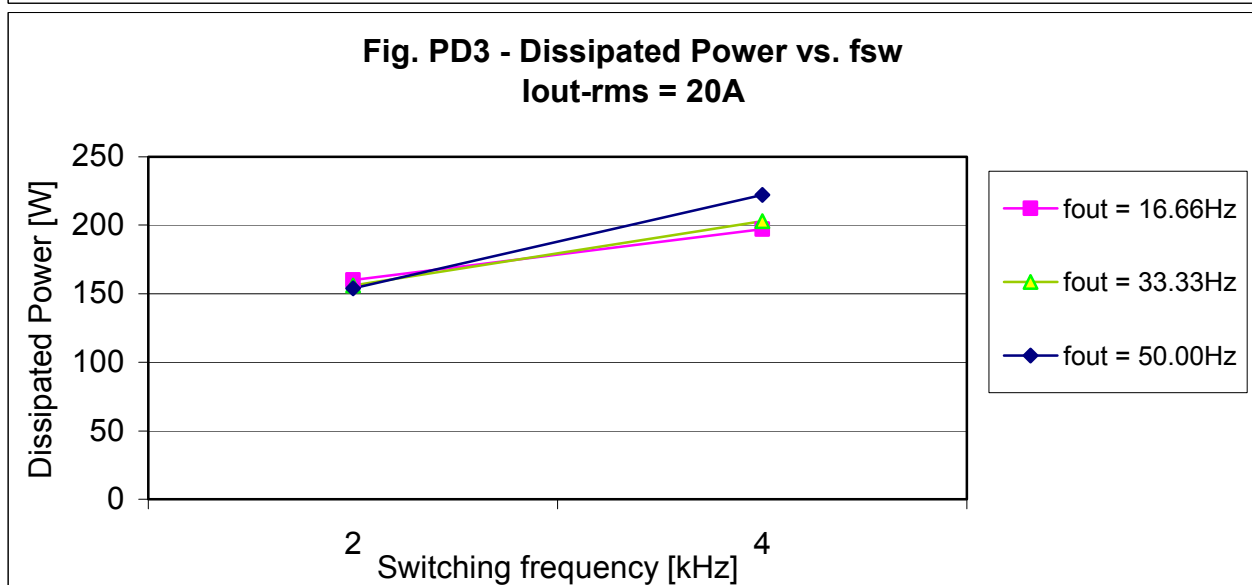
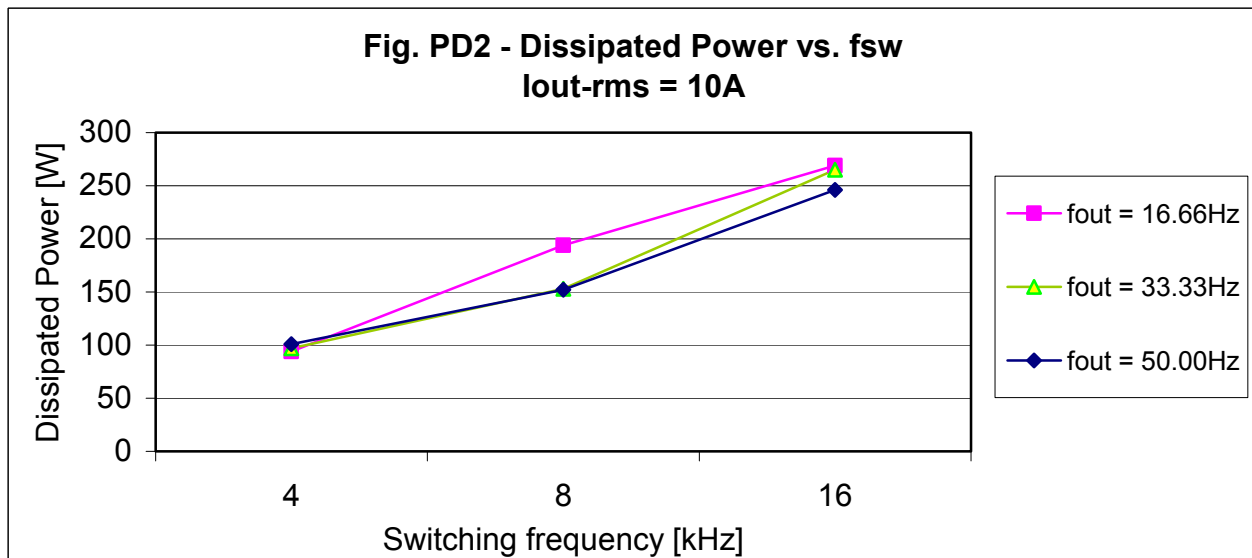
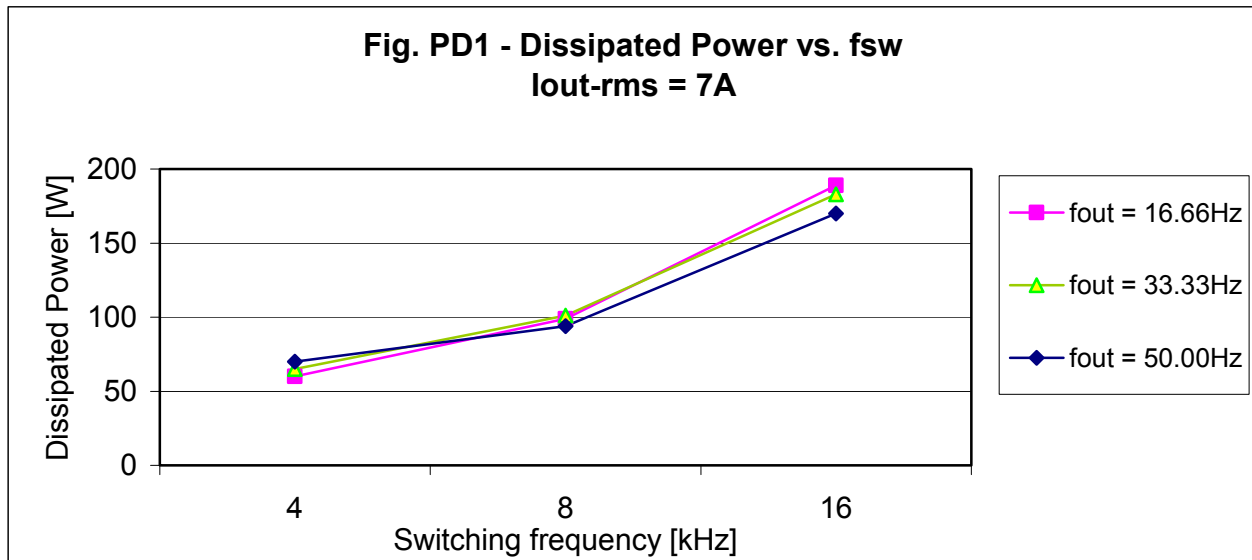
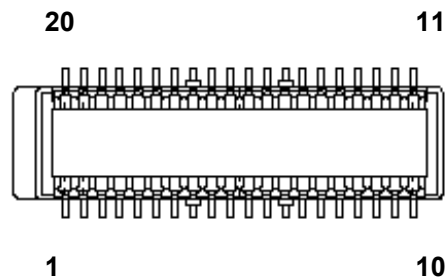


Fig. WF.4 - Typ. S.C. Waveform
@ $T_C=150^\circ\text{C}$ using Fig. CT.3

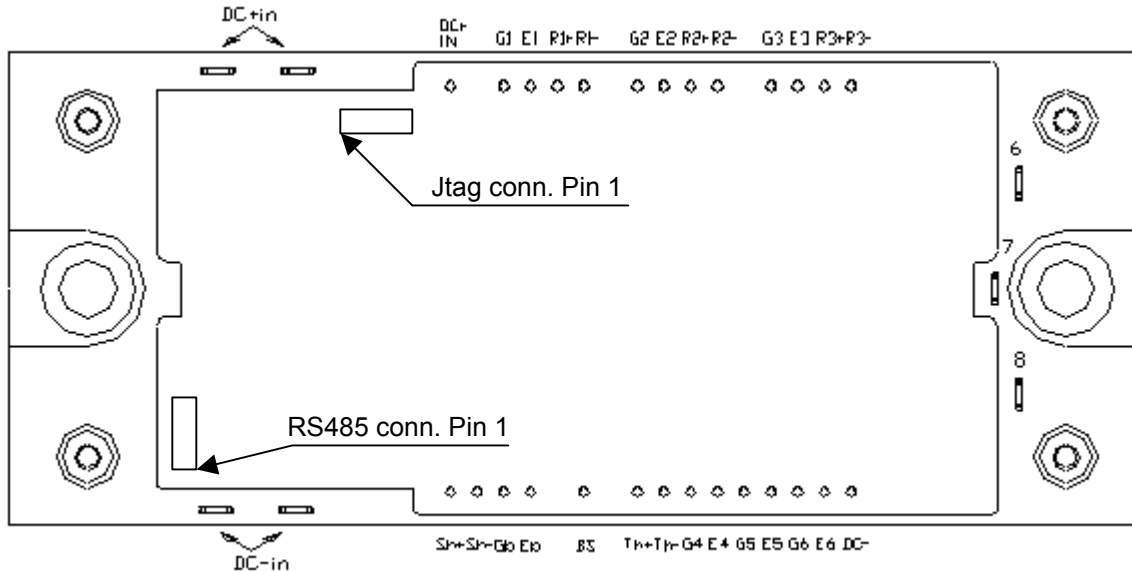




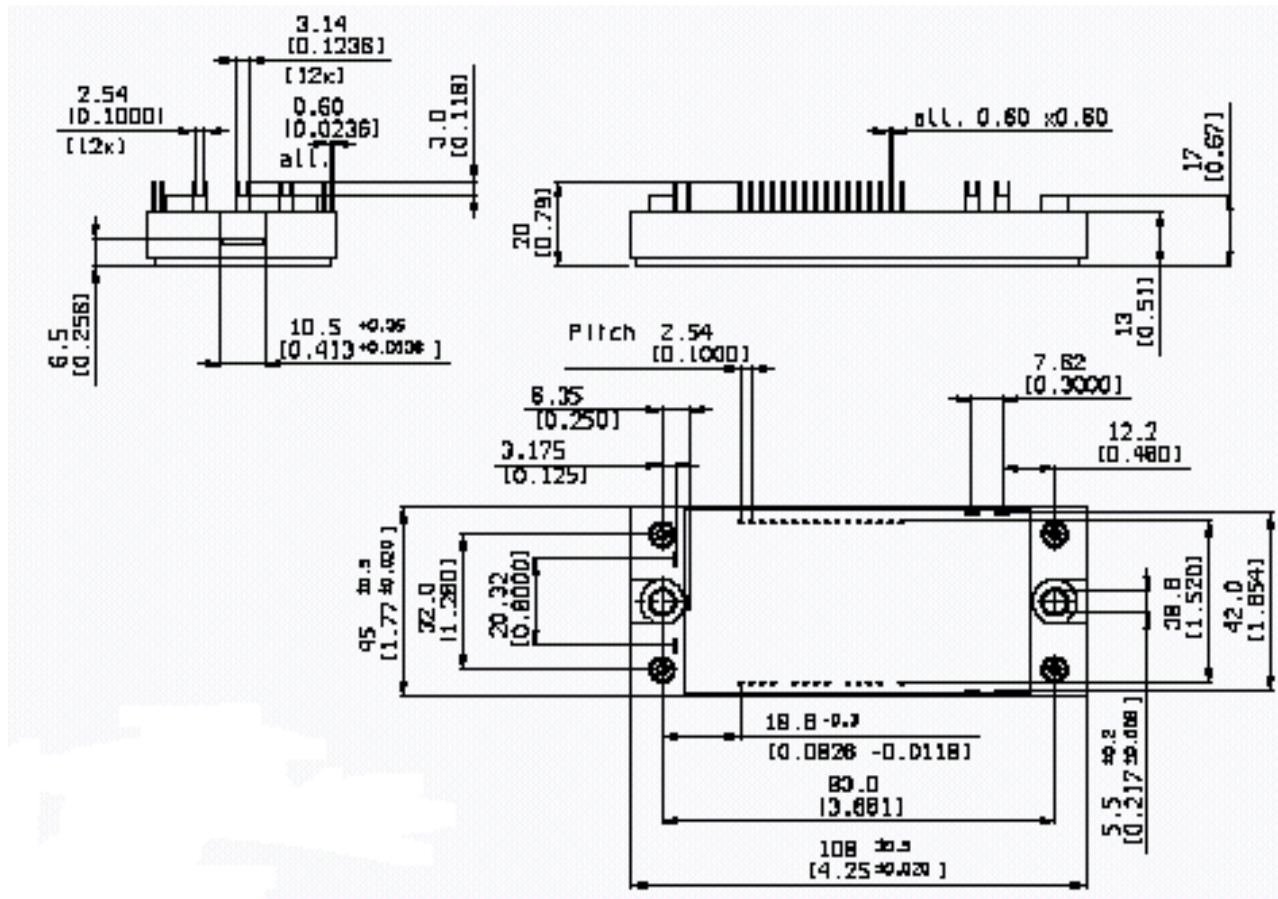
JTAG and RS485 on-board connectors are Molex 53916-0204 mates with 54167-0208 or 52991-0208



EMP-B pin out



EMP-B Case outline and Dimensions



International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
 EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
 IR CANADA: 13325 Centreville Creek Road, Bolton, Ontario Tel: (905) 475 1897
 IR GERMANY: Frankfurter Strasse 227, 63263 Neu-Isenburg Tel: ++49 6102-884 400
 IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
 IR FAR EAST: Sunshine 60, 51F, 3-1-1 Higashi-Ikebukuro Toshima-ku, Tokyo 170-6051 Tel: ++ 81 3 3983 0086
 IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 838 4630
<http://www.irf.com>

Sales Offices, Agents and Distributors in Major Cities Throughout the World.

Data and specifications subject to change without notice.

© 2001 International Rectifier - Printed in Italy 8-01 - Rev. 1.2