CS5531/32/33/34

16-Bit and 24-Bit ADCs with Ultra Low Noise PGIA

Features

- Chopper Stabilized PGIA (Programmable Gain Instrumentation Amplifier, 1x to 64x)
  - 6 nV/√Hz @ 0.1 Hz (No 1/f noise)
  - 500 pA Input Current with Gains >1
- Delta-Sigma Analog-to-Digital Converter
  - Linearity Error: 0.0007% FS
  - Noise Free Resolution: Up to 23 bits
- Two or Four Channel Differential MUX
- Scalable Input Span via Calibration
  - 5 mV to 5 V
- Scalable V_{REF} Input: Up to Analog Supply
- On-chip Guard Drive Output Buffer
- Simple three-wire serial interface
  - SPI® and Microwire™ Compatible
  - Schmitt Trigger on Serial Clock (SCLK)
- R/W Calibration Registers Per Channel
- Selectable Word Rates: 7.5 Hz to 3,840 Hz
- Power Supply Configurations
  - VA+ = +5 V; VA- = 0 V; VD+ = +3 V to +5 V
  - VA+ = +2.5 V; VA- = -2.5 V; VD+ = +3 V to +5 V
  - VA+ = +3 V; VA- = -3 V; VD+ = +3 V

General Description

The CS5531/32/33/34 are highly integrated ΔΣ Analog-to-Digital Converters (ADCs) which use charge-balance techniques to achieve 16-bit (CS5531/33) and 24-bit (CS5532/34) performance. The ADCs are optimized for measuring low-level unipolar or bipolar signals in weigh scale, process control, scientific, and medical applications.

To accommodate these applications, the ADCs come as either two-channel (CS5531/32) or four-channel (CS5533/34) devices and include a very low noise chopper-stabilized instrumentation amplifier (6 nV/√Hz @ 0.1 Hz) with selectable gains of 1×, 2×, 4×, 8×, 16×, 32×, and 64×. These ADCs also include a fourth order ΔΣ modulator followed by a digital filter which provides ten selectable output word rates of 7.5 Hz, 15 Hz, 30 Hz, 60 Hz, 120 Hz, 240 Hz, 480 Hz, 960 Hz, 1.92 kHz, and 3.84 kHz (MCLK = 4.9152 MHz).

To ease communication between the ADCs and a microcontroller, the converters include a simple three-wire serial interface which is SPI and Microwire compatible with a Schmitt Trigger input on the serial clock (SCLK).

High dynamic range, programmable output rates, and flexible power supply options makes these ADCs ideal solutions for weigh scale and process control applications.

ORDERING INFORMATION

See page 43

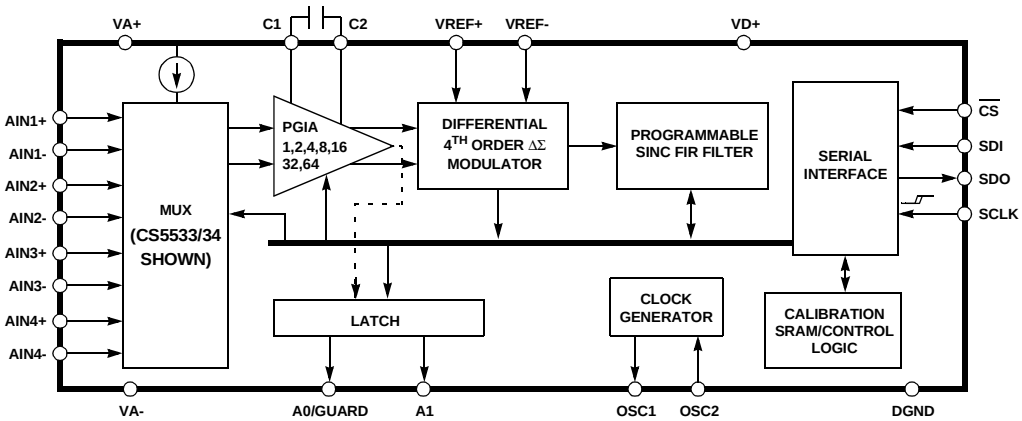

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TABLE OF CONTENTS

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LIST OF FIGURES

LIST OF TABLES

1. CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS (T_A = 25 °C; VA+, VD+ = 5 V ±5%; VREF+ = 5 V; VA-, VREF-, DGND = 0 V; MCLK = 4.9152 MHz; OWR (Output Word Rate) = 60 Hz; Bipolar Mode; Gain = 32; (See Notes 1 and 2.)

Parameter			CS5531-AS/CS5533-AS			Unit
			Min	Typ	Max	
Accuracy						
Linearity Error			-	±0.0015	±0.003	%FS
No Missing Codes			16	-	-	Bits
Bipolar Offset		(Note 3)	-	±1	±2	LSB_{16}
Unipolar Offset		(Note 3)	-	±2	±4	LSB_{16}
Offset Drift	Gain = 1	(Notes 3 and 4)	-	TBD	-	nV/°C
	Gain = 2, 4, 8, 16, 32, 64		-	DRIFT	-	nV/°C
Offset Drift	/1000 Hours.		-	TBD	-	ppm
Bipolar Full Scale Error			-	±8	±31	ppm
Unipolar Full Scale Error			-	±16	±62	ppm
Full Scale Drift		(Note 4)	-	1	3	ppm/°C
Full Scale Drift	/1000 Hours.		-	TBD	-	ppm

Parameter			CS5532-AS/CS5534-AS			CS5532-BS/CS5534-BS			Unit
			Min	Typ	Max	Min	Typ	Max	
Accuracy									
Linearity Error			-	±0.0015	±0.003	-	±0.0007	±0.0015	%FS
No Missing Codes			24	-	-	24	-	-	Bits
Bipolar Offset		(Note 3)	-	±16	±32	-	±16	±32	LSB_{24}
Unipolar Offset		(Note 3)	-	±32	±64	-	±32	±64	LSB_{24}
Offset Drift	Gain = 1	(Notes 3 and 4)	-	TBD	-	-	TBD	-	nV/°C
	Gain = 2, 4, 8, 16, 32, 64		-	DRIFT	-	-	DRIFT	-	nV/°C
Offset Drift	/1000 Hours.		-	TBD	-	-	TBD	-	ppm
Bipolar Full Scale Error			-	±8	±31	-	±8	±31	ppm
Unipolar Full Scale Error			-	±16	±62	-	±16	±62	ppm
Full Scale Drift		(Note 4)	-	1	3	-	1	3	ppm/°C
Full Scale Drift	/1000 Hours.		-	TBD	-	-	TBD	-	ppm

Notes:
1. Applies after system calibration at any temperature within -40 °C ~ +85 °C.
2. Specifications guaranteed by design, characterization, and/or test. LSB is 16 bits for the CS5531/33 and LSB is 24 bits for the CS5532/34.
3. The offset drift is dictated by the gain setting. The offset drift, DRIFT, is (TBD nV/°C)/G, where G is the gain of the amplifier. Further note, the specification applies to the device only and does not include any effects by external parasitic thermocouples.
4. Drift over specified temperature range after calibration at power-up at 25 °C.

ANALOG CHARACTERISTICS (Continued) (See Notes 1 and 2.)

Parameter			Min	Typ	Max	Unit
Analog Input						
Common Mode + Signal on AIN+ or AIN-	Bipolar/Unipolar Mode					
	Gain = 1		VA-	-	VA+	V
	Gain = 2, 4, 8, 16, 32, 64		VA- + 0.7	-	VA+ - 1.7	V
CVF Current on AIN+ or AIN-	Gain = 1	(Note 5)	-	100	-	nA
	Gain = 2, 4, 8, 16, 32, 64		-	500	-	pA
Input Current Drift			-	TBD	-	pA/°C
Input Leakage for Mux when Off			-	TBD	-	pA
Open Circuit Detect Current			100	300	-	nA
Common Mode Rejection	dc		-	120	-	dB
	50, 60 Hz		-	120	-	dB
Input Capacitance			-	60	-	pF
Guard Drive Output			-	TBD	-	µA
Voltage Reference Input						
Range	(VREF+) - (VREF-)		1	2.5	(VA+)-(VA-)	V
CVF Current		(Note 5)	-	100	-	nA
Common Mode Rejection	dc		-	120	-	dB
	50, 60 Hz		-	120	-	dB
Input Capacitance			11	-	22	pF
System Calibration Specifications						
Full Scale Calibration Range	Bipolar/Unipolar Mode		-	TBD	-	%FS
Offset Calibration Range	Bipolar/Unipolar Mode		-	TBD	-	%FS

Parameter			CS5531/32/33/34-AS			CS5532/34-BS			Unit
			Min	Typ	Max	Min	Typ	Max	
Power Supplies									
DC Power Supply Currents (Normal Mode)		I_{A+}	-	TBD	TBD	-	TBD	6.5	mA
		I_{D+}	-	TBD	TBD	-	TBD	1.5	mA
Power Consumption	Normal Mode	(Note 6)	-	TBD	30	-	TBD	40	mW
	Standby		-	TBD	-	-	TBD	-	mW
	Sleep		-	TBD	-	-	TBD	-	µW
Power Supply Rejection	dc Positive Supplies		-	120	-	-	120	-	dB
	dc Negative Supply		-	120	-	-	120	-	dB

Notes: 5. See the section of the data sheet which discusses input models.

6. All outputs unloaded. All input CMOS levels.

TYPICAL RMS NOISE (nV), CS5531/32/33/34-AS (See notes 7 and 8)

Output Word Rate (Hz)	-3 dB Filter Frequency (Hz)	Instrumentation Amplifier Gain						
		x64	x32	x16	x8	x4	x2	x1
7.5	1.94	17	17	19	26	42	79	155
15	3.88	24	25	27	36	59	111	218
30	7.75	34	35	39	51	84	157	308
60	15.5	48	49	54	72	118	222	436
120	31	68	70	77	102	167	314	616
240	62	115	160	276	527	1040	2070	4150
480	122	163	230	392	748	1480	2950	5890
960	230	229	321	554	1060	2090	4170	8340
1,920	390	344	523	946	1840	3650	7290	14600
3,840	780	1390	2710	5390	10800	21500	43000	86100

Notes: 7. Wideband noise aliased into the baseband. Referred to the input. Typical values shown for 25 °C.

8. For Peak-to-Peak Noise multiply by 6.6 for all ranges and output rates.

TYPICAL NOISE FREE RESOLUTION(BITS), CS5532/34-AS (See Note 9)

Output Word Rate (Hz)	-3 dB Filter Frequency (Hz)	Instrumentation Amplifier Gain						
		x64	x32	x16	x8	x4	x2	x1
7.5	1.94	19	20	21	22	22	22	22
15	3.88	19	20	21	21	21	22	22
30	7.75	18	19	20	21	21	21	21
60	15.5	18	19	20	20	20	21	21
120	31	17	18	19	20	20	20	20
240	62	16	17	17	17	17	17	17
480	122	16	17	17	17	17	17	17
960	230	15	16	16	16	16	16	16
1,920	390	15	15	15	15	15	15	15
3,840	780	13	13	13	13	13	13	13

9. Noise Free Resolution is LOG((2xInput Span)/(6.6xRMS Noise))/LOG(2) rounded to the nearest bit. The input span is calculated in the analog input span section of the data sheet.

Specifications are subject to change without notice.

TYPICAL RMS NOISE (nV), CS5532/34-BS (See notes 10 and 11)

Output Word Rate (Hz)	-3 dB Filter Frequency (Hz)	Instrumentation Amplifier Gain						
		x64	x32	x16	x8	x4	x2	x1
7.5	1.94	8.5	9	10	15	26	50	99
15	3.88	12	13	15	21	37	70	139
30	7.75	17	18	21	30	52	99	196
60	15.5	24	25	29	42	73	140	277
120	31	34	36	42	59	103	198	392
240	62	80	136	260	514	1020	2050	4090
480	122	113	194	369	730	1450	2900	5810
960	230	159	274	523	1030	2060	4110	8230
1,920	390	260	470	912	1810	3620	7230	14500
3,840	780	1360	2690	5380	10800	21500	43000	86000

Notes: 10. Wideband noise aliased into the baseband. Referred to the input. Typical values shown for 25 °C.

11. For Peak-to-Peak Noise multiply by 6.6 for all ranges and output rates.

TYPICAL NOISE FREE RESOLUTION(BITS), CS5532/34-BS (See Notes 12 and 13)

Output Word Rate (Hz)	-3 dB Filter Frequency (Hz)	Instrumentation Amplifier Gain						
		x64	x32	x16	x8	x4	x2	x1
7.5	1.94	20	21	22	23	23	23	23
15	3.88	20	21	22	22	22	22	22
30	7.75	19	20	21	22	22	22	22
60	15.5	19	20	21	21	21	21	21
120	31	18	19	20	21	21	21	21
240	62	17	17	18	18	18	18	18
480	122	17	17	17	17	17	17	17
960	230	16	16	17	17	17	17	17
1,920	390	16	16	16	16	16	16	16
3,840	780	13	13	13	13	13	13	13

12. Noise Free Resolution is LOG((2xInput Span)/(6.6xRMS Noise))/LOG(2) rounded to the nearest bit. The input span is calculated in the analog input span section of the data sheet.

13. Note that the -B devices provide the best noise specifications.

Specifications are subject to change without notice.

5 V DIGITAL CHARACTERISTICS (T_A = 25 °C; VA+, VD+ = 5 V ±5%; VA-, DGND = 0 V; See Notes 2 and 14.)

Parameter		Symbol	Min	Typ	Max	Unit
High-Level Input Voltage		V_{IH}	0.6 VD+	-	VD+	V
Low-Level Input Voltage		V_{IL}	0.0	-	0.8	V
High-Level Output Voltage	I_{out} = -5.0 mA	V_{OH}	(VD+) - 1.0	-	-	V
Low-Level Output Voltage	I_{out} = 5.0 mA	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	±1	±10	µA
3-State Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

3 V DIGITAL CHARACTERISTICS (T_A = 25 °C; VA+ = 5V ±5%; VD+ = 3.0V±10%; VA-, DGND = 0V; See Notes 2 and 14.)

Parameter		Symbol	Min	Typ	Max	Unit
High-Level Input Voltage		V_{IH}	0.6 VD+	-	VD+	V
Low-Level Input Voltage		V_{IL}	0.0	-	0.8	V
High-Level Output Voltage	I_{out} = -5.0 mA	V_{OH}	(VD+) - 1.0	-	-	V
Low-Level Output Voltage	I_{out} = 5.0 mA	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	±1	±10	µA
3-State Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

14. All measurements performed under static conditions.

DYNAMIC CHARACTERISTICS

Parameter	Symbol	Ratio	Unit
Modulator Sampling Frequency	f_s	MCLK/16	Hz
Filter Settling Time to 1/2 LSB (Full Scale Step Input)			
Single conversion mode (See notes 15, 16, 17)	t_s	1/OWR	s
Multiple conversions mode, OWR < 3840 Hz	t_s	3/OWR	s
Multiple conversions mode, OWR = 3840 Hz	t_s	5/OWR	s

15. The ADCs use a $Sinc^5$ filter for the 3840 Hz output word rate (OWR) and a $Sinc^3$ filter for the other OWRs. This implies that the filter's settling time with a full scale step input is dictated by the OWR.
16. The single conversion mode only outputs fully settled output conversions. This implies that the effective throughput in the single conversion mode is reduced by 3 times with an OWR of less than 3840 Hz and it is reduced by 5 times with an OWR of 3840 Hz.
17. The multiple conversions mode outputs every conversion. This implies that the filter's settling time with a full scale step input in the multiple conversions mode is dictated by the OWR.

ABSOLUTE MAXIMUM RATINGS (DGND = 0 V; See Note 18.)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	(Notes 19 and 20)					
	Positive Digital	VD+	-0.3	-	+6.0	V
	Positive Analog	VA+	-0.3	-	+6.0	V
	Negative Analog	VA-	+0.3	-	-3.75	V
Input Current, Any Pin Except Supplies	(Notes 21 and 22)	I_{IN}	-	-	±10	mA
Output Current		I_{OUT}	-	-	±25	mA
Power Dissipation	(Note 23)	PDN	-	-	500	mW
Analog Input Voltage	VREF pins	V_{INR}	-0.3	-	(VA+) + 0.3	V
	AIN Pins	V_{INA}	-0.3	-	(VA+) + 0.3	V
Digital Input Voltage		V_{IND}	-0.3	-	(VD+) + 0.3	V
Ambient Operating Temperature		T_A	-40	-	85	°C
Storage Temperature		T_{stg}	-65	-	150	°C

Notes: 18. All voltages with respect to ground.

19. VA+ and VA- must satisfy {(VA+) - (VA-)} ≤ +6.6 V.

20. VD+ and VA- must satisfy {(VD+) - (VA-)} ≤ +7.5 V.

21. Applies to all pins including continuous overvoltage conditions at the analog input (AIN) pins.

22. Transient current of up to 100 mA will not cause SCR latch-up. Maximum input current for a power supply pin is ±50 mA.

23. Total power dissipation, including all input currents and output currents.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS (T_A = 25 °C; VA+ = 2.5 V or 5 V ±5%; VA- = -2.5V±5% or 0 V; VD+ = 3.0 V ±10% or 5 V ±5%;DGND = 0 V; Levels: Logic 0 = 0 V, Logic 1 = VD+; C_L = 50 pF; See Figures 1 and 2.)

Parameter	Symbol	Min	Typ	Max	Unit
Master Clock Frequency (Note 24) External Clock or Internal Oscillator	MCLK	1	4.9152	5	MHz
Master Clock Duty Cycle		40	-	60	%
Rise Times (Note 25) Any Digital Input Except SCLK SCLK Any Digital Output	t_{rise}	 - - -	 - - 50	 1.0 100 -	 µs µs ns
Fall Times (Note 25) Any Digital Input Except SCLK SCLK Any Digital Output	t_{fall}	 - - -	 - - 50	 1.0 100 -	 µs µs ns
Start-up					
Oscillator Start-up Time XTAL = 4.9152MHz (Note 26)	t_{ost}	-	20	-	ms
Serial Port Timing					
Serial Clock Frequency	SCLK	0	-	2	MHz
Serial Clock Pulse Width High Pulse Width Low	t_1 t_2	250 250	- -	- -	ns ns
SDI Write Timing					
$\overline{CS}$ Enable to Valid Latch Clock	t_3	50	-	-	ns
Data Set-up Time prior to SCLK rising	t_4	50	-	-	ns
Data Hold Time After SCLK Rising	t_5	100	-	-	ns
SCLK Falling Prior to $\overline{CS}$ Disable	t_6	100	-	-	ns
SDO Read Timing					
$\overline{CS}$ to Data Valid	t_7	-	-	150	ns
SCLK Falling to New Data Bit	t_8	-	-	150	ns
$\overline{CS}$ Rising to SDO Hi-Z	t_9	-	-	150	ns

Notes: 24. Device parameters are specified with a 4.9125 MHz clock.

25. Specified using 10% and 90% points on waveform of interest. Output loaded with 50 pF.

26. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.

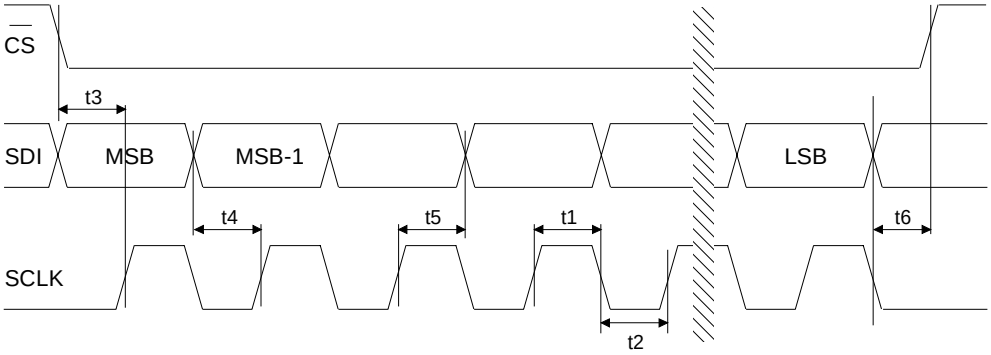


Figure 1. SDI Write Timing (Not to Scale).

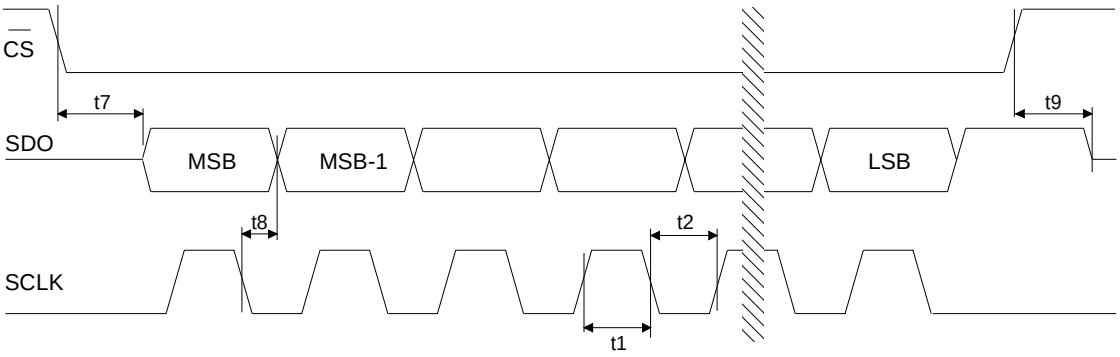


Figure 2. SDO Read Timing (Not to Scale).

2. GENERAL DESCRIPTION

The CS5531/32/33/34 are highly integrated ΔΣ Analog-to-Digital Converters (ADCs) which use charge-balance techniques to achieve 16-bit (CS5531/33) and 24-bit (CS5532/34) performance. The ADCs are optimized for measuring low-level unipolar or bipolar signals in weigh scale, process control, scientific, and medical applications.

To accommodate these applications, the ADCs come as either two-channel (CS5531/32) or four-channel (CS5533/34) devices and include a very low noise chopper-stabilized programmable gain instrumentation amplifier (PGIA, 6 nV/√Hz @ 0.1 Hz) with selectable gains of 1×, 2×, 4×, 8×, 16×, 32×, and 64×. These ADCs also include a fourth order ΔΣ modulator followed by a digital filter which provides ten selectable output word rates of 7.5 Hz, 15 Hz, 30 Hz, 60 Hz, 120 Hz, 240 Hz, 480 Hz, 960 Hz, 1.92 kHz, and 3.84 kHz (MCLK = 4.9152 MHz).

To ease communication between the ADCs and a micro-controller, the converters include a simple three-wire serial interface which is SPI and Microwire compatible with a Schmitt Trigger input on the serial clock (SCLK).

2.1. Analog Input

Figure 3 illustrates a block diagram of the CS5531/32/33/34. The front end consists of a multiplexer, a unity gain coarse/fine charge input buffer, and a programmable gain chopper-stabilized instrumentation amplifier. The unity gain buffer is activated any time conversions are performed with a gain of one and the instrumentation amplifier is activated any time conversions are performed with gain settings greater than one.

The unity gain buffer is designed to accommodate rail to rail input signals. The common-mode plus signal range for the unity gain buffer amplifier is VA- to VA+. Typical CVF (sampling) current for the unity gain buffer amplifier is about 100 nA (MCLK = 4.9152 MHz, see Figure 4).

The instrumentation amplifier is chopper-stabilized and operates with a chop clock frequency of MCLK/128. The CVF (sampling) current into the instrumentation amplifier is less than TBD pA over

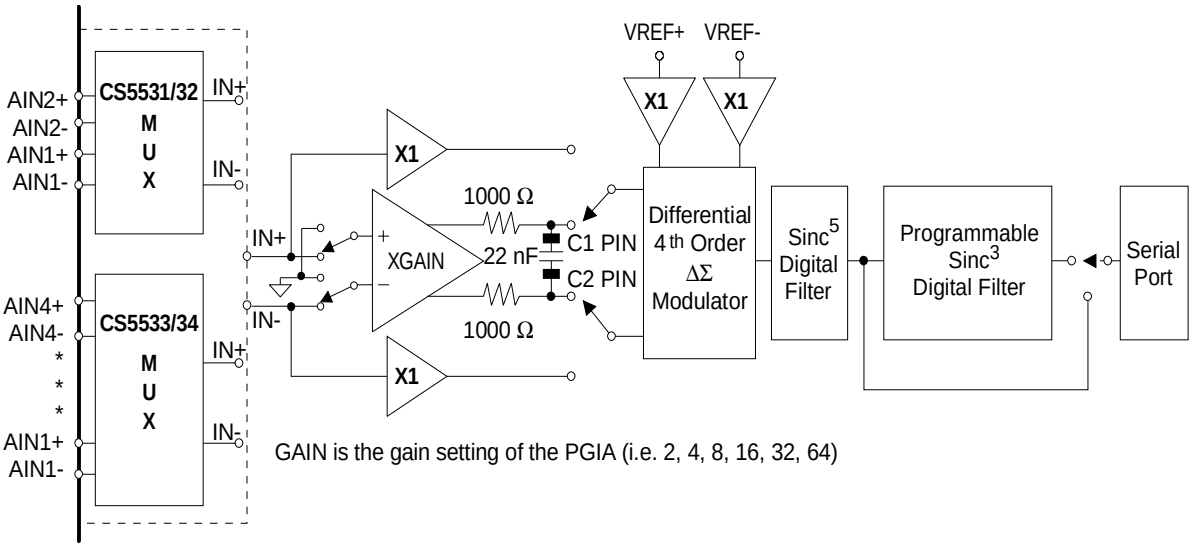


Figure 3. Multiplexer Configuration.

-40°C to +85°C (MCLK=4.9152 MHz). The common-mode plus signal range of the instrumentation amplifier is (VA-) + 0.7 V to (VA+) - 1.7 V.

Figure 4 illustrates the input models for the amplifiers. The dynamic input current for each of the pins can be determined from the models shown.

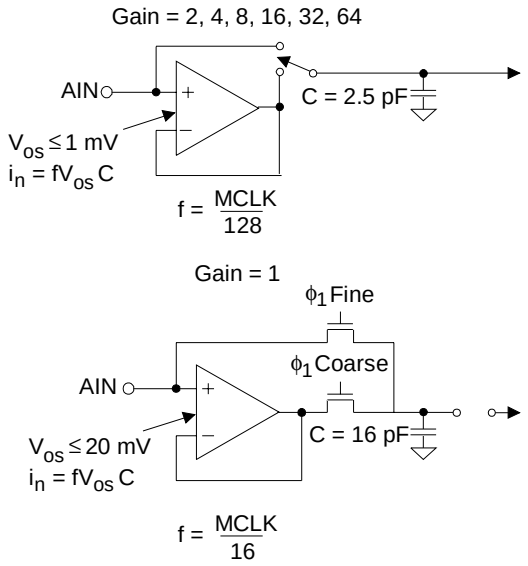


Figure 4. Input models for AIN+ and AIN- pins.

Note: The C=2.5pF and C = 16pF capacitors are for input current modeling only. For physical input capacitance see 'Input Capacitance' specification under *Analog Characteristics*.

2.1.1. Analog Input Span

The full scale input signal that the converter can digitize is a function of the gain setting and the reference voltage connected between the VREF+ and VREF- pins. The full scale input span of the converter is ((VREF+) - (VREF-))/(GxA), where G is the gain of the amplifier and A is 2 for VRS = 0, or A is 1 for VRS = 1.

After reset, the unity gain buffer is engaged. With a 2.5V reference this would make the full scale input range default to 2.5 V. By activating the instrumentation amplifier (i.e. a gain setting other than 1) and using a gain setting of 32, the full scale input range can quickly be set to 2.5/32 or about 78mV. Note that these input ranges assume the calibration registers are set to their default values (i.e. Gain = 1.0 and Offset = 0.0).

2.1.2. Multiplexed Settling Limitations

The settling performance of the CS5531/32/33/34 in multiplexed applications is affected by the single-pole low-pass filter which follows the instrumentation amplifier (see Figure 3). To achieve data sheet settling and linearity specifications, it is recommended that a 22 nF C0G capacitor be used. Capacitors as low as 10 nF can be used with some noise degradation.

2.1.3. Voltage Noise Density Performance

Figure 5 illustrates the voltage noise density versus frequency from 0.01 Hz to 10 Hz of a CS5532-BS. The device was powered with ±2.5 V supplies, 120 Hz OWR, the 64x gain range, bipolar mode, and with the input short bits enabled.

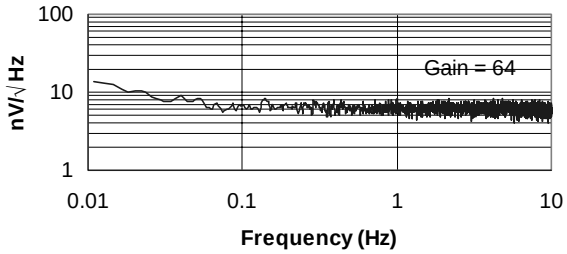


Figure 5. Measured Voltage Noise Density.

2.1.4. No Offset DAC

An offset DAC was not included in the CS553x family because the high dynamic range of the converter eliminates the need for one. The offset register can be manipulated by the user to mimic the function of a DAC if desired.

2.2. Overview of ADC Register Structure and Operating Modes

The CS5531/32/33/34 ADCs have an on-chip controller, which includes a number of user-accessible registers. The registers are used to hold offset and gain calibration results, configure the chip's operating modes, hold conversion instructions, and to store conversion data words. Figure 6 depicts a block diagram of the on-chip controller's internal registers.

Each of the converters has 32-bit registers to function as offset and gain calibration registers for each channel. The converters with two channels have two offset and two gain calibration registers, the converters with four channels have four offset and four gain calibration registers. These register hold calibration results. The contents of these registers can be read or written by the user. This allows calibration data to be off-loaded into an external EEPROM. The user can also manipulate the contents of these registers to modify the offset or the gain slope of the converter.

The converters include a 32-bit configuration register of which 10 of the bits are used for setting options such as the operating power options, resetting the converter, shorting the analog inputs, and enabling diagnostic test bits like the guard signal.

A group of registers, called Channel Setup Registers, are also included in the converters. These registers can be used to hold pre-loaded conversion instructions. Each channel setup register is 32 bits long but holds two 16-bit conversion instructions referred to as Setups. Upon power up, these registers can be initialized by the users' microcontroller with conversion instructions. The user can then instruct the converter to perform single or multiple conversions or calibrations with the converter in the mode defined by the Setup referenced.

Using the single conversion mode, an 8-bit command word can be written into the serial port. The

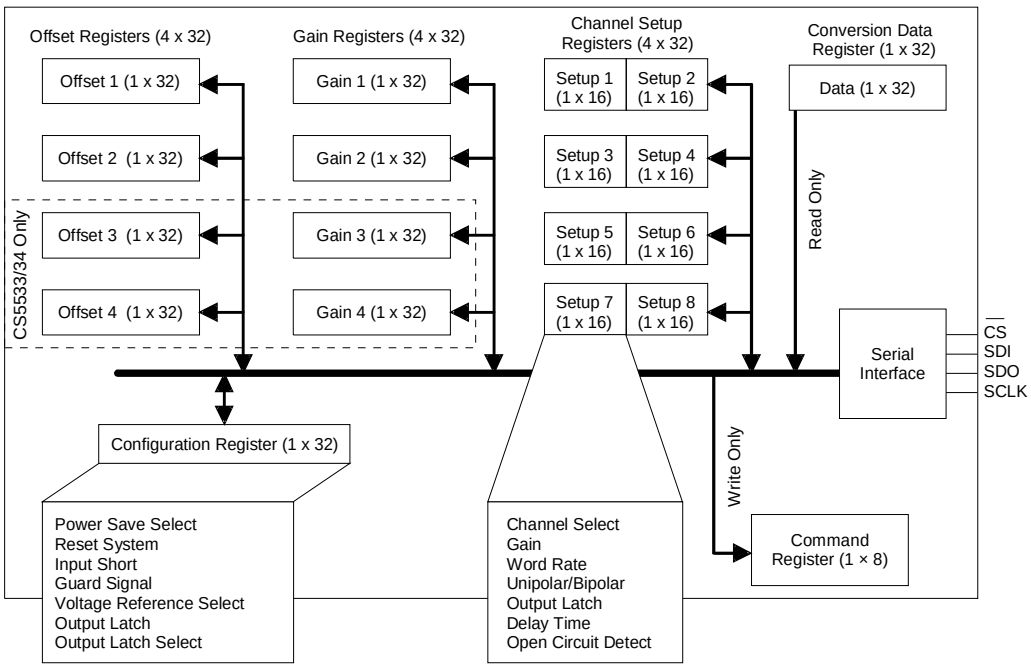


Figure 6. CS5531/32/33/34 Register Diagram.

command includes pointer bits which 'point' to a 16-bit command in one of the Channel Setup Registers which is to be executed. The 16-bit Setups can be programmed to perform a conversion on any of the input channels of the converter. More than one of the 16-bit Setups can be used for the same analog input channel. This allows the user to convert on the same signal with either a different conversion speed, a different gain range, or any of the other options, which are in the channel setup registers. Alternatively, the user can set up the registers to perform different conversion conditions on each of the input channels.

The ADCs also include multiple conversions capability. User bits in the configuration register of the ADCs can be configured to continuously convert one 16-bit command Setup, performing a conversion according to the content of each 16-bit Setup. In the multiple conversions mode, the conversion data words are loaded into a the data conversion register. The converter issues a flag on the SDO pin when a conversion cycle is completed so the user can read the conversion register. More details will follow.

The following pages document how to initialize the converter, perform offset and gain calibrations, and how to configure the converter for the various conversion modes. Each of the bits of the configuration register and of the Channel Setup Registers is described. A list of examples follows the description section. Also the *Command Register Quick Reference* can be used to decode all valid commands (the first 8-bits into the serial port).

2.2.1. System Initialization

The CS5531/32/33/34 provide no power-on-reset function. To initialize the ADCs, the user must perform a software reset by resetting the ADC's serial port with the Serial Port Initialization sequence. This sequence resets the serial port to the command mode and is accomplished by transmitting 15 SYNC1 command bytes (0xFF hexadecimal), followed by one SYNC0 command (0xFE hexadecimal). Note that this sequence can be initiated at anytime to reinitialize the serial port. To complete the system initialization sequence, the user must also perform a system reset by setting the Reset System (RS) bit in the configuration register. A system reset can also be initiated at any time by writing a logic 1 to the RS bit in the configuration register. After a system reset cycle is complete, the RS bit is automatically returned to logic 0, and the on-chip registers are initialized to the following states:

Configuration Register:	00000000(H)
Offset Registers:	00000000(H)
Gain Registers:	01000000(H)
Channel Setup Registers:	00000000(H)

After a system initialization or reset, the on-chip controller is initialized into command mode where it waits for a valid command (the first 8-bits transmitted into the serial port are transmitted into the command register). Once a valid command is received and decoded, the byte instructs the converter to either acquire data from or transfer data to an internal register(s), or perform a conversion or a calibration. The *Command Register Descriptions* section can be used to decode all valid commands.

2.2.2. Command Register Quick Reference

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	ARA	CS1	CS0	R/$\overline{W}$	RSB2	RSB1	RSB0

BIT	NAME	VALUE	FUNCTION
D7	Command Bit, C	0	Must be logic 0 for these commands.
		1	These commands are invalid if this bit is logic 1.
D6	Access Registers as Arrays, ARA	0	Ignore this function.
		1	Access the respective registers, offset, gain, or channel-setup, as an array of registers. The particular registers accessed are determined by the RS bits. The registers are accessed MSB first with physical channel 0 accessed first followed by physical channel 1 next and so forth.
D5-D4	Channel Select Bits, CS1-CS0	00	CS1-CS0 provide the address of one of the two (four for CS5533/34) physical input channels. These bits are also used to access the calibration registers associated with the respective physical input channel. Note that these bits are ignored when reading data register.
		01	
		10	
		11	
D3	Read/$\overline{Write}$, R/$\overline{W}$	0	Write to selected register.
		1	Read from selected register.
D2-D0	Register Select Bit, RSB3-RSB0	000	Reserved
		001	Offset Register
		010	Gain Register
		011	Configuration Register
		100	Conversion Data Register (Read Only)
		101	Channel-Setup Registers
		110	Reserved
		111	Reserved

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	MC	CSRP2	CSRP1	CSRP0	CC2	CC1	CC0

BIT	NAME	VALUE	FUNCTION
D7	Command Bit, C	0	These commands are invalid if this bit is logic 0.
		1	Must be logic 1 for these commands.
D6	Multiple Conversions, MC	0	Perform fully settled single conversions.
		1	Perform conversions continuously.
D5-D3	Channel-Setup Register Pointer Bits, CSRP	000	These bits are used as pointers to the Channel-Setup registers. Either a single conversion or continuous conversions are performed on the channel setup register pointed to by these bits.
		...	
		111	
D2-D0	Conversion/Calibration Bits, CC2-CC0	000	Normal Conversion
		001	Self-Offset Calibration
		010	Self-Gain Calibration
		011	Reserved
		100	Reserved
		101	System-Offset Calibration
		110	System-Gain Calibration
		111	Reserved

2.2.3. Command Register Descriptions

READ/$\overline{\text{WRITE}}$ ALL OFFSET CALIBRATION REGISTERS

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	R/$\overline{W}$	0	0	1

Function: *These commands are used to access the offset registers as arrays.*

R/$\overline{W}$ (Read/$\overline{Write}$)

0 Write to selected register.

1 Read from selected register.

READ/$\overline{\text{WRITE}}$ ALL GAIN CALIBRATION REGISTERS

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	R/$\overline{W}$	0	1	0

Function: *These commands are used to access the gain registers as arrays.*

R/$\overline{W}$ (Read/$\overline{Write}$)

0 Write to selected register.

1 Read from selected register.

READ/$\overline{\text{WRITE}}$ ALL CHANNEL-SETUP REGISTERS

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	R/$\overline{W}$	1	0	1

Function: *These commands are used to access the channel-setup registers as arrays.*

R/$\overline{W}$ (Read/$\overline{Write}$)

0 Write to selected register.

1 Read from selected register.

READ/$\overline{\text{WRITE}}$ INDIVIDUAL OFFSET REGISTER

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	0	CS1	CS0	R/$\overline{W}$	0	0	1

Function: *These commands are used to access each offset register separately. CS1 - CS0 decode the registers accessed.*

R/$\overline{W}$ (Read/$\overline{Write}$)

0 Write to selected register.

1 Read from selected register.

CS[1:0] (Channel Select Bits)

00 Offset Register 1 (All devices)

01 Offset Register 2 (All devices)

10 Offset Register 3 (CS5533/34 only)

11 Offset Register 4 (CS5533/34 only)

READ/$\overline{\text{WRITE}}$ INDIVIDUAL GAIN REGISTER

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	0	CS1	CS0	R/$\overline{\text{W}}$	0	1	0

Function: *These commands are used to access each gain register separately. CS1 - CS0 decode the registers accessed.*

R/$\overline{\text{W}}$ (Read/$\overline{\text{Write}}$)

0 Write to selected register.

1 Read from selected register.

CS[1:0] (Channel Select Bits)

00 Gain Register 1 (All devices)

01 Gain Register 2 (All devices)

10 Gain Register 3 (CS5533/34 only)

11 Gain Register 4 (CS5533/34 only)

READ/$\overline{\text{WRITE}}$ INDIVIDUAL CHANNEL-SETUP REGISTER

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	0	CS1	CS0	R/$\overline{\text{W}}$	1	0	1

Function: *These commands are used to access each channel-setup register separately. CS1 - CS0 decode the registers accessed.*

R/$\overline{\text{W}}$ (Read/$\overline{\text{Write}}$)

0 Write to selected register.

1 Read from selected register.

CS[1:0] (Channel Select Bits)

00 Channel-Setup Register 1 (All devices)

01 Channel-Setup Register 2 (All devices)

10 Channel-Setup Register 3 (All devices)

11 Channel-Setup Register 4 (All devices)

READ/$\overline{\text{WRITE}}$ CONFIGURATION REGISTER

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	R/$\overline{\text{W}}$	0	1	1

Function: *These commands are used to read from or write to the configuration register.*

R/$\overline{\text{W}}$ (Read/$\overline{\text{Write}}$)

0 Write to selected register.

1 Read from selected register.

PERFORM CONVERSION

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	MC	CSRP2	CSRP1	CSRP0	0	0	0

Function: *These commands instruct the ADC to perform either a single conversion or continuous conversions on the physical input channel pointed to by the pointer bits (CSRP2 - CRSP0) in the channel-setup register.*

MC (Multiple Conversions)

0 Perform fully settled single conversions.

1 Perform conversions continuously.

CSRP [2:0] (Channel Setup Register Pointer Bits)

000 Setup 1 (All devices)

001 Setup 2 (All devices)

010 Setup 3 (All devices)

011 Setup 4 (All devices)

100 Setup 5 (All devices)

101 Setup 6 (All devices)

110 Setup 7 (All devices)

111 Setup 8 (All devices)

READ CONVERSION DATA REGISTER

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	0

Function: *This command is used to read from the conversion data register.*

PERFORM CALIBRATION

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	0	CSRP2	CSRP1	CSRP0	CC2	CC1	CC0

Function: *These commands instruct the ADC to perform a calibration on the physical input channel selected by the setup register which is chosen by the command byte pointer bits (CSRP2 - CSRP0).*

CSRP [2:0] (Channel Setup Register Pointer Bits)

000 Setup 1 (All devices)
001 Setup 2 (All devices)
010 Setup 3 (All devices)
011 Setup 4 (All devices)
100 Setup 5 (All devices)
101 Setup 6 (All devices)
110 Setup 7 (All devices)
111 Setup 8 (All devices)

CC [2:0] (Calibration Control Bits)

000 Reserved
001 Self-Offset Calibration
010 Self-Gain Calibration
011 Reserved
100 Reserved
101 System-Offset Calibration
110 System-Gain Calibration
111 Reserved

SYNC1

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Function: *Part of the serial port re-initialization sequence.*

SYNC0

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	0

Function: *End of the serial port re-initialization sequence.*

NULL

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

Function: *This command is used to clear a port flag and keep the converter in the continuous conversion mode.*

2.2.4. Serial Port Interface

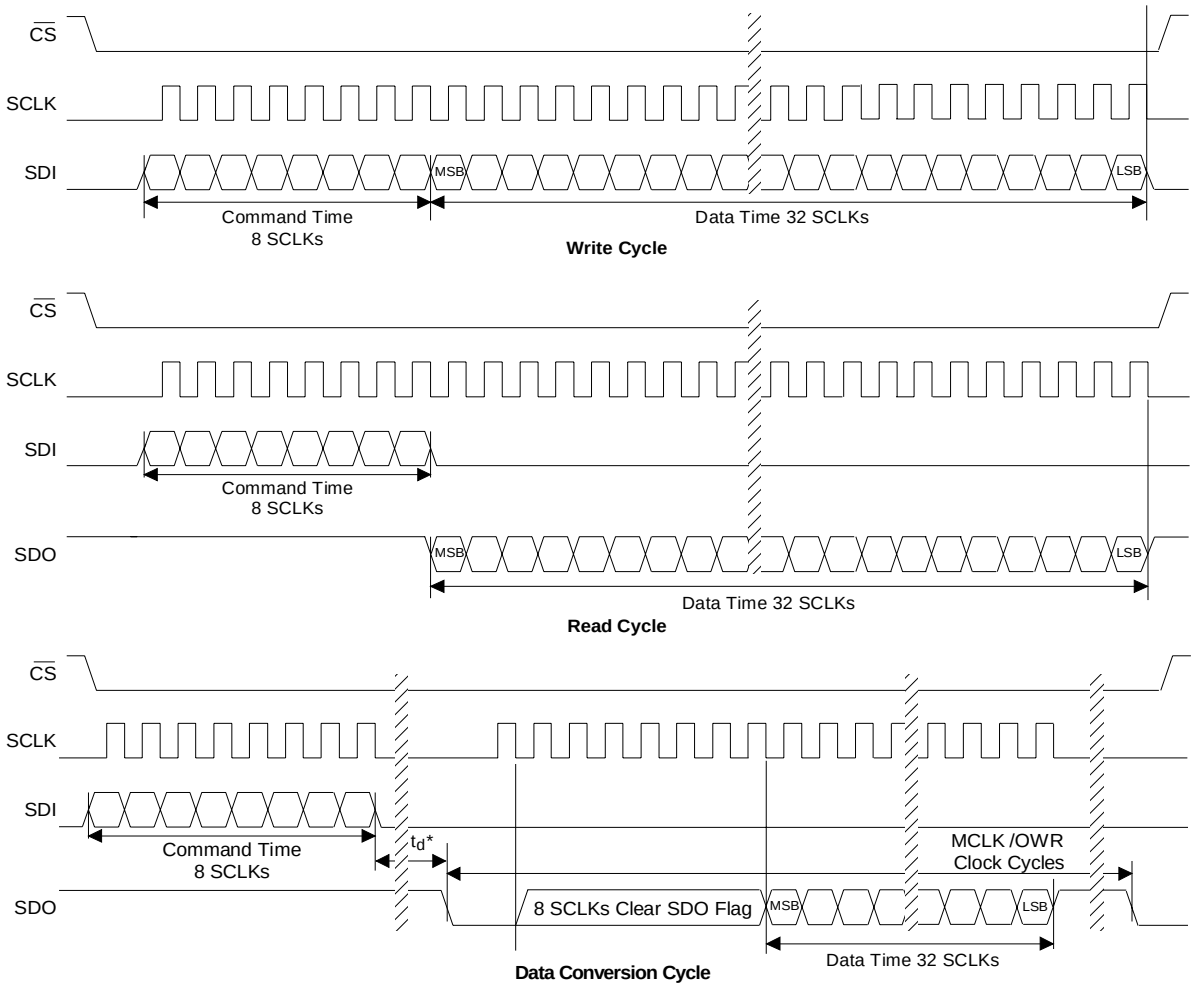
The CS5531/32/33/34's serial interface consists of four control lines: $\overline{CS}$, SDI, SDO, SCLK. Figure 7 details the command and data word timing.

$\overline{CS}$, Chip Select, is the control line which enables access to the serial port. If the $\overline{CS}$ pin is tied low, the port can function as a three wire interface.

SDI, Serial Data In, is the data signal used to transfer data to the converters.

SDO, Serial Data Out, is the data signal used to transfer output data from the converters. The SDO output will be held at high impedance any time $\overline{CS}$ is at logic 1.

SCLK, Serial Clock, is the serial bit-clock which controls the shifting of data to or from the ADC's serial port. The $\overline{CS}$ pin must be held low (logic 0) before SCLK transitions can be recognized by the port logic. To accommodate optoisolators SCLK is designed with a Schmitt-trigger input to allow an optoisolator with slower rise and fall times to directly drive the pin. Additionally, SDO is capable of sinking or sourcing up to 5 mA to directly drive an optoisolator LED. SDO will have less than a 400 mV loss in the drive voltage when sinking or sourcing 5 mA.



* td = MCLK/OWR clock cycles for each conversion except the first conversion which will take MCLK/OWR + 7 clock cycles

Figure 7. Command and Data Word Timing.

2.2.5. Reading/Writing On-Chip Registers

The CS5531/32/33/34's offset, gain, configuration, and channel-setup registers are readable and writable while the conversion data register is read only.

As shown in Figure 7, to write to a particular register the user must transmit the appropriate write command and then follow that command by 32 bits of data. For example, to write 0x80000000 (hexadecimal) to physical channel one's gain register, the user would first transmit the command byte 0x02 (hexadecimal) followed by the data 0x80000000 (hexadecimal). Similarly, to read a particular register the user must transmit the appropriate read command and then acquire the 32 bits of data. Once a register is written to or read from, the serial port returns to the command mode.

In addition to accessing the internal registers one at a time, the gain and offset registers as well as the channel-setup registers, can be accessed as arrays (i.e. the entire register set can be accessed with one command). For example, to write 0x80000000 (hexadecimal) to all four gain registers, the user would transmit the command 0x42 (hexadecimal) followed by four iterations of 0x80000000 (hexadecimal), (i.e. 0x42 followed by 0x80000000, 0x80000000, 0x80000000, 0x80000000). The registers are written to or read from in sequential order (i.e, 1, followed by 2, then 3, then 4). Once the registers are written to or read from, the serial port returns to the command mode.

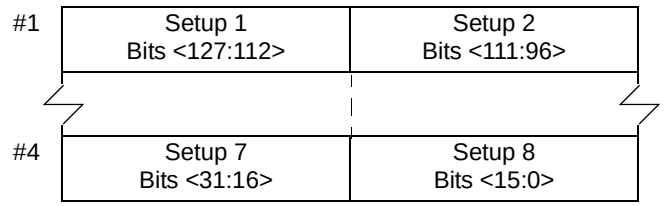
2.2.6. Setting up the CSRs for a Measurement

The CS5531/32/33/34 have four Channel-Setup Registers (CSRs). Each CSR contains two 16-bit Setups which are programmed by the user to contain data conversion information such as: 1) which physical channel will be converted, 2) at what gain will the channel be converted, 3) at what word rate will the channel be converted, 4) will the output conversion be unipolar or bipolar, 5) what will be the state of the output latch during the conversion, 6) will the converter delay the start of a conversion to allow time for the output latch to settle before the conversion is begun, and 7) will the open circuit detect current source be activated for that Setup. Note that a particular physical input channel can be represented in more than one Setup with different output rates, gain ranges, etc. (i.e. each Setup is independently defined). Refer to the *Channel-Setup Register Descriptions* section for more details.

Each 32-bit CSR is individually accessible and contains two 16-bit Setups. As an example, to configure Setup 1 in the CS5531/32/33/34 with the write individual channel-setup register command (0x05 hexadecimal), bits 31 to 16 of CSR 1 contains the information for Setup 1 and bits 15 to 0 contain the information for Setup 2. Note that while reading/writing CSRs, two Setups are accessed in pairs as a single 32-bit CSR register. Even if one of the Setups isn't used, it must be written to or read. Examples detailing the power of the CSRs are provided in the *Use of Pointers in the Command Byte* section.

2.2.7. Channel-Setup Register Descriptions

CSR



D31(MSB)	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
CS1	CS0	G2	G1	G0	WR3	WR2	WR1	WR0	U/B	OL1	OL0	DT	OCD	NU	NU
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
CS1	CS0	G2	G1	G0	WR3	WR2	WR1	WR0	U/B	OL1	OL0	DT	OCD	NU	NU

CS1-CS0 (Channel Select Bits) [31:30] [15:14]

00 Select physical channel 1 (All devices)

01 Select physical channel 2 (All devices)

10 Select physical channel 3 (CS5533/34 only)

11 Select physical channel 4 (CS5533/34 only)

G2-G0 (Gain Bits) [29:27] [13:11]

000 Gain = 1, (Input Span = [(VREF+)-(VREF-)]/1 for unipolar).

001 Gain = 2, (Input Span = [(VREF+)-(VREF-)]/2 for unipolar).

010 Gain = 4, (Input Span = [(VREF+)-(VREF-)]/4 for unipolar).

011 Gain = 8, (Input Span = [(VREF+)-(VREF-)]/8 for unipolar).

100 Gain = 16, (Input Span = [(VREF+)-(VREF-)]/16 for unipolar).

101 Gain = 32, (Input Span = [(VREF+)-(VREF-)]/32 for unipolar).

110 Gain = 64, (Input Span = [(VREF+)-(VREF-)]/64 for unipolar).

WR3-WR0 (Word Rate) [26:23] [10:7]

Word Rates apply to continuous conversion mode. In single conversion mode, an output will take three conversions to settle. Only the third output will be provided to the serial port.

Bit	WR (4.9152 MHz)	WR (4.096 MHz)	Clock Cycles
0000	120 Hz	100 Hz	(40960 MCLK cycles)
0001	60 Hz	50 Hz	(81920 MCLK cycles)
0010	30 Hz	25 Hz	(163840 MCLK cycles)
0011	15 Hz	12.5 Hz	(327680 MCLK cycles)
0100	7.5 Hz	6.25 Hz	(655360 MCLK cycles)
1000	3840 Hz	3200 Hz	(1280 MCLK cycles)
1001	1920 Hz	1600 Hz	(2560 MCLK cycles)
1010	960 Hz	800 Hz	(5120 MCLK cycles)
1011	480 Hz	400 Hz	(10240 MCLK cycles)
1100	240 Hz	200 Hz	(20480 MCLK cycles)

All other combinations are not used.

U/$\overline{B}$ (Unipolar / $\overline{Bipolar}$) [22] [6]

0 Select Bipolar mode.

1 Select Unipolar mode.

OL1-OL0 (Output Latch Bits) [21:20] [5:4]

The latch bits will be set to the logic state of these bits upon command word execution when the output latch select bit (OLS) in the configuration register is logic 0. Note that the logic outputs on the chip are powered from VA+ and VA-.

00 A0 = 0, A1 = 0

01 A0 = 0, A1 = 1

10 A0 = 1, A1 = 0

11 A0 = 1, A1 = 1

DT (Delay Time Bit) [19] [3]

When set, the converter will wait for a delay time before starting a conversion. This allows settling time for A0 and A1outputs before a conversion begins. The delay time will be 1280 MCLK cycles.

0 Normal mode.

1 Wait 1280 MCLK cycles before starting conversion.

OCD (Open Circuit Detect Bit) [18] [2]

When set, this bit activates a 300 nA current source on the input channel (AIN+) selected by the channel select bits. Note that the 300nA current source is rated at 25°C. At -55°C, the current source doubles to approximately 600nA. This feature is particularly useful in thermocouple applications when the user wants to drive a suspected open thermocouple lead to a supply rail.

0 Normal mode.

1 Activate current source.

NU (Not Used) [17:16] [1:0]

These bits are reserved for future upgrade.

2.3. Configuration Register

To ease the architectural design, the configuration register is thirty-two bits long, however, only ten of the thirty two bits are used. The following sections detail the bits in the configuration register.

2.3.1. Power Consumption

The CS5531/32/33/34 accommodate three power consumption modes: normal, standby, and sleep. The normal mode, the default mode, is entered after power is applied. In this mode, the CS5531/32/33/34-AS versions typically consume 30 mW. The CS5532/34-BS versions typically consume 40 mW. The last two modes are referred to as the power save modes. They power down most of the analog portion of the chip and stop filter convolutions. The power save modes are entered whenever the power down (PDW) bit of the configuration register is set to logic 1. The particular power save mode entered depends on state of the PSS (Power Save Select) bit. If PSS is logic 0, the converter enters the standby mode reducing the power consumption to TBD mW. The standby mode leaves the oscillator and the on-chip bias generator for the analog portion of the chip active. This allows the converter to quickly return to the normal mode once PDW is set back to a logic 1. If PSS and PDW are both set to logic 1, the sleep mode is entered reducing the consumed power to around TBD µW. Since this sleep mode disables the oscillator, approximately a 20 ms oscillator start-up delay period is required before returning to the normal mode. If an external clock is used no delay is necessary. Further note that when the chips are used in the Gain = 1 mode, the PGIA is powered down. In this mode, the power consumed in the normal power mode is reduced to TBD mW. The sleep and standby modes are not affected.

2.3.2. Reset System

The reset system (RS) bit permits the user to perform a system reset. A system reset can be initiated at any time by writing a logic 1 to the RS bit in the configuration register. After a system reset cycle is complete, the reset valid (RV) bit is set indicating that the internal logic was properly reset. The RV bit is cleared after the configuration register is read. Note that the on-chip registers are initialized to the following states.

Configuration Register:	00000000(H)
Offset Registers:	00000000(H)
Gain Registers:	01000000(H)
Channel Setup Registers:	00000000(H)

Further note that after reset the RS bit automatically returns to logic 0 and the ADCs return to the command mode where they wait for a valid command. Also, the RS bit is the only bit in the configuration register that can be set when initiating a reset.

2.3.3. Input Short

The input short bit allows the user to internally ground all the inputs of the multiplexer. This is a useful function because it allows the user to easily test the grounded input performance of the ADC and eliminate the noise effects due to the external system.

2.3.4. Guard Signal

The guard signal bit is a bit that modifies the function of A0. When set, this bit outputs the common mode voltage of the instrumentation amplifier on A0. This feature is useful when the user wants to connect an external shield to the common mode potential of the instrumentation amplifier to protect against leakage. Figure 8 illustrates a typical connection diagram for the guard signal.

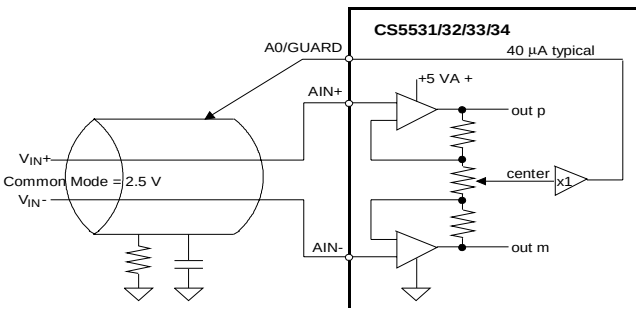


Figure 8. Guard Signal Shielding Scheme.

2.3.5. Voltage Reference Select

The voltage reference select (VRS) bit selects the size of the sampling capacitor used to sample the voltage reference. The bit should be set based upon the magnitude of the reference voltage to achieve optimal performance. Figures 9 and 10 model the effects on the reference's input impedance and input current for each VRS setting. As the models show, the reference includes a coarse/fine charge buffer which reduces the dynamic current demand of the external reference.

The reference's input buffer is designed to accommodate rail-to-rail (common-mode plus signal) input voltages. The differential voltage between the VREF+ and VREF- can be any voltage from 1.0 V up to the analog supply (depending on how VRS is configured), however, the VREF+ cannot go above VA+ and the VREF- pin can not go below VA-. For a single-ended reference voltage, the reference voltage is input into the VREF+ pin of the converter and the VREF- pin is grounded. Note that if ±3 V supplies are used, the supplies must be established before the reference voltage.

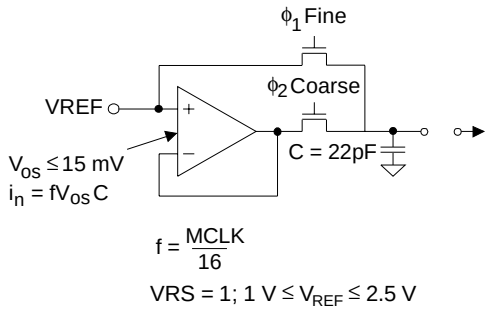


Figure 9. Input Reference Model when VRS = 1.

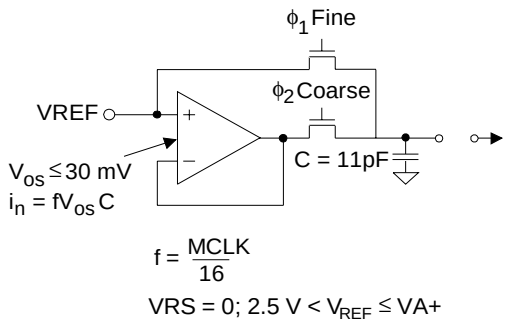


Figure 10. Input Reference Model when VRS = 0.

2.3.6. Output Latch Pins

The A1-A0 pins of the ADCs mimic the D21-D20/D5-D4 bits of the channel-setup registers if the output latch select bit is logic 0 (default). If the output latch select bit is logic 1 then A1-A0 mimic the output latch bit setting in the configuration register. These two options give the user a choice of allowing the latch outputs to change anytime a different CSR is selected for a conversion; or to allow the latch bits to remain latched to a fixed state (determined by the configuration register bit) for all CSR selections. In either case, A1-A0 can be used to control external multiplexers and other logic functions outside the converter. The A1-A0 outputs can sink or source at least 1 mA, but it is recommended to limit drive currents to less than 20 μA to reduce self-heating of the chip. These outputs are powered from VA+ and VA-. Their output voltage will be limited to the VA+ voltage for a logic 1 and VA- for a logic 0.

2.3.7. Configuration Register Descriptions

D31(MSB)	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
PSS	PDW	RS	RV	IS	GB	VRS	A1	A0	OLS	NU	NU	NU	NU	NU	NU
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
NU	NU	NU	NU	NU	NU	NU	NU	NU	NU	NU	NU	NU	NU	NU	NU

PSS (Power Save Select)[31]

0 Standby Mode (Oscillator active, allows quick power-up).

1 Sleep Mode (Oscillator inactive).

PDW (Power Down Mode)[30]

0 Normal Mode

1 Activate the power save select mode.

RS (Reset System)[29]

0 Normal Operation.

1 Activate a Reset cycle. Bit automatically returns to logic 0 after reset.

RV (Reset Valid)[28]

0 Normal Operation

1 System got reset. This bit is read only. Bit is cleared to logic zero after the configuration register is read.

IS (Input Short)[27]

0 Normal Input

1 All signal input pairs for each channel are shorted internally.

GB (Guard Signal Bit)[26]

0 Normal Operation of A0 as an output latch.

1 A0's output is modified to output the common mode output voltage of the instrumentation amplifier (typically 2.5 V). The output latch select bit is ignored when the guard buffer is activated.

VRS (Voltage Reference Select)[25]

0 $2.5\ V < V_{REF} \leq VA+$

1 $1\ V \leq V_{REF} \leq 2.5V$

A1-A0 (Output Latch bits)[24:23]

The latch bits (A0 and A1) will be set to the logic state of these bits upon command word execution if the output latch select bit (OLS) is set. Note that these logic outputs are powered from VA+ and VA-.

00 A0 = 0, A1 = 0

01 A0 = 0, A1 = 1

10 A0 = 1, A1 = 0

11 A0 = 1, A1 = 1

Output Latch Select, OLS[22]

0 When low, uses the Channel-Setup Register as the source of A1 and A0.

1 When set, uses the Configuration Register as the source of A1 and A0.

NU (Not Used)[21:0]

0 Must always be logic 0. Reserved for future upgrades.

2.4. Calibration

Calibration is used to set the zero and gain slope of the ADC's transfer function. The CS5531/32/33/34 offer both self calibration and system calibration.

Note: 1) After the ADCs are reset, they are functional and can perform measurements without being calibrated (remember that the VRS bit in the configuration register must be configured). In this case, the converter will utilize the initialized values of the on-chip registers (Gain = 1.0, Offset = 0.0) to calculate output words. Any initial offset and gain errors in the internal circuitry of the chip will remain. 2) Calibrations steps each take one conversion cycle to complete. At the end of the calibration step, SDO falls low to indicate that a calibration is complete. 3) Offset calibration must be performed before gain calibration because the gain slope is referenced from the offset calibrations.

2.4.1. Calibration Registers

The CS5531/32/33/34 converters have an individual offset and gain register for each channel input. The gain and offset registers, which are used during both self and system calibration, are used to set the zero and gain slope of the converter's transfer function. As shown in *Offset Register* section, one LSB in the offset register is 2^{-24} proportion of the input span (bipolar span is 2 times the unipolar span). The MSB in the offset register determines if the offset to be trimmed is positive or negative (0 positive, 1 negative). Note that the magnitude of the offset that is trimmed from the input is mapped through the gain register. The converter can typically trim ±100 percent of the input span. As shown in the *Gain Register* section, the gain register spans from 0 to $(32 - 2^{-22})$. The decimal equivalent meaning of the gain register is

$$D = b_{D28}2^4 + (b_{D27}2^3 + b_{D26}2^2 + \ldots + b_N2^{-N}) = b_{D28}2^4 + \sum_{i=0}^{N} b_i2^{-i}$$

where the binary numbers have a value of either zero or one (b_{D28} corresponds to bit D28).

2.4.2. Gain Register

MSB	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
NU	NU	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**LSB**
2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{22}	2^{-23}	2^{-24}
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The gain register span is from 0 to ($32-2^{-24}$). After Reset D24 is 1, all other bits are ‘0’.

2.4.3. Offset Register

MSB	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Sign	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**LSB**
2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	NU	NU	NU	NU	NU	NU	NU	NU
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

One LSB represents 2^{-24} proportion of the input span (bipolar span is 2 times unipolar span).
Offset and data word bits align by MSB. After reset, all bits are ‘0’.

2.4.4. Performing Calibrations

To perform a calibration the user must send a command byte with its MSB=1, its pointer bits (CSRP2-CSRP0) set to address the desired Setup to calibrate, and the appropriate calibration bits (CC2-CC0) set to choose the type of calibration to be performed. Note that calibration assumes that the CSRs have been previously initialized because the information concerning the physical channel, its filter rate, gain range, and polarity, comes from the channel-setup register being addressed by the pointer bits in the command byte. Once the CSRs are initialized, a calibration can be performed with one command byte.

Once a calibration cycle is complete, SDO falls and the results are stored in either the gain or offset register for the physical channel being calibrated. Note that if additional calibrations are performed on the same physical channel referenced by a different Setups with different filter rates, gain ranges, or conversion modes, the last calibration results will replace the effects from the previous calibration as only one offset and gain register is available per physical channel. Further note that only one calibration is performed with each command byte. To calibrate all the channels additional calibration commands are necessary.

2.4.5. Self Calibration

The CS5531/32/33/34 offer both self offset and self gain calibrations. For the self-calibration of offset, the converters internally tie the inputs of the amplifier together and routes them to the AIN- pin as shown in Figure 11. For proper self-calibration of offset to occur, the AIN pins must be at the proper common-mode-voltage as specified in the *Analog Characteristics* section.

For self-calibration of gain, the differential inputs of the modulator are connected to VREF+ and VREF- as shown in Figure 12. Self-calibration of gain is performed in the GAIN = 1x mode without regard to the setup register's gain setting. Gain errors in the PGIA gain steps 2x to 64x are not calibrated as this would require an accurate low voltage source other than the reference voltage. A system calibration of gain should be performed if accurate gains are to be achieved on the 2x and up ranges.

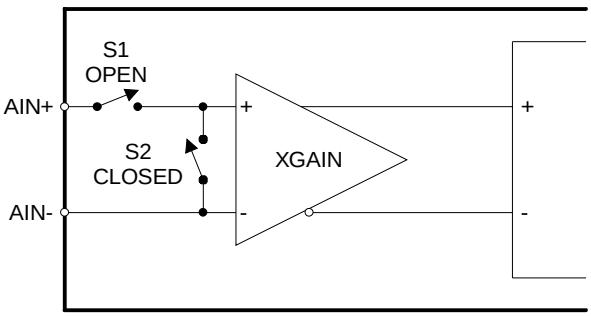


Figure 11. Self Calibration of Offset.

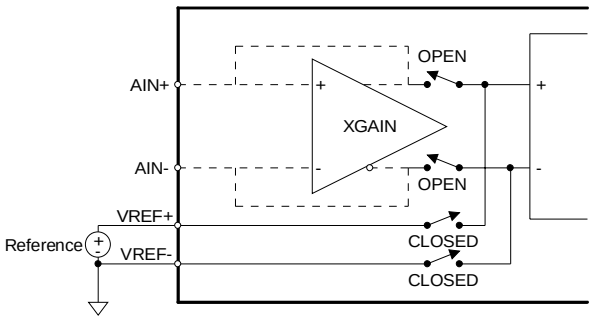


Figure 12. Self Calibration of Gain.

2.4.6. System Calibration

For the system calibration functions, the user must supply the converters calibration signals which represent ground and full scale. When a system offset calibration is performed, a ground reference signal must be applied to the converters. Figure 13 illustrates system offset calibration.

As shown in Figure 14, the user must input a signal representing the positive full scale point to perform a system gain calibration. In either case, the calibration signals must be within the specified calibration limits for each specific calibration step (refer to the *System Calibration Specifications*).

2.4.7. Calibration Tips

Calibration steps are performed at the output word rate selected by the WR2-WR0 bits of the channel setup registers. Since higher word rates result in conversion words with more peak-to-peak noise, calibration should be performed at lower output word rates. Also, to minimize digital noise near the device, the user should wait for each calibration step to be completed before reading or writing to the serial port.

For maximum accuracy, calibrations should be performed for both offset and gain (selected by changing the G2-G0 bits of the channel-setup registers). Note that only one gain range can be calibrated per physical channel. And if factory calibration of the user's system is performed using the system calibration capabilities of the CS5531/32/33/34, the offset and gain register contents can be read by the system microcontroller and recorded in EEPROM. These same calibration words can then be uploaded into the offset and gain registers of the converter when power is first applied to the system, or when the gain range is changed.

Note that if a user wants to use uncalibrated conversions, the uncalibrated gain accuracy is ±1 percent. Further note that the gain tracking from range to range is not affected by calibration. Gain tracking from range to range is 0.1 percent.

Note that the gain from the offset register to the output is approximately 1.8 decimal, not 1. If a user wants to calculate the calibration coefficients externally, they will need to divide the content of the offset register by the scale factor 01D5C315 hexadecimal while in the bipolar mode (for unipolar mode divide by two).

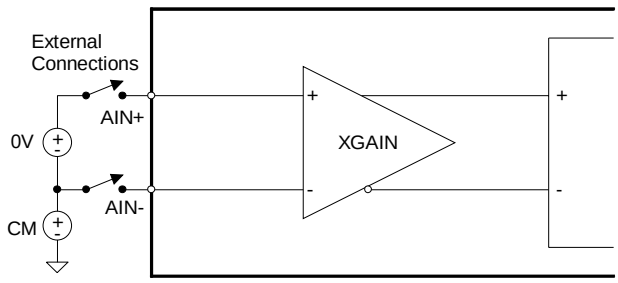


Figure 13. System Calibration of Offset.

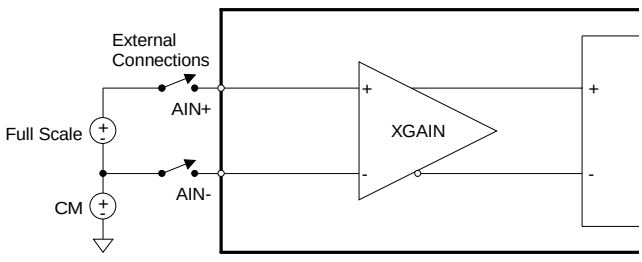


Figure 14. System Calibration of Gain.

2.4.8. Limitations in Calibration Range

System calibration can be limited by signal headroom in the analog signal path inside the chip as discussed under the *Analog Input* section of this data sheet. For gain calibration, the full scale input signal can be reduced to the point in which the gain register reaches its upper limit of ($32\text{-}2^{-64}$ decimal). Under nominal conditions, this occurs with a full scale input signal equal to about 1/32 the nominal full scale. With the converter's intrinsic gain error, this full scale input signal may be higher or lower. In defining the minimum Full Scale Calibration Range (FSCR) under *Analog Characteristics*, margin is retained to accommodate the intrinsic gain error. Alternatively the input full scale signal can be increased to a point in which the modulator reaches its 1's density limit of 90 percent, which under nominal condition occurs when the full scale input signal is 1.1 times the nominal full scale. With the chip's intrinsic gain error, this input full scale input signal maybe higher or lower. In defining the maximum FSCR, margin is again incorporated to accommodate the intrinsic gain error.

2.5. Performing Conversions

The CS5531/32/33/34 offers two modes of performing conversions. The three sections that follow detail the differences and provide examples illustrating how to use the conversion modes with the channel-setup registers.

2.5.1. Single Conversion Mode (MC = 0)

Based on the information provided in the channel-setup registers (CSRs), a single conversion is performed after the user transmits the single conversion command. The command byte includes a pointer address to the Setup register to be used during the conversion. Once transmitted, the serial port enters data mode where it waits until a conversion is complete. After the conversion is done, SDO falls to logic 0. Forty SCLKs are then needed to read the conversion. The first 8 SCLKs are used to clear the SDO flag. During the first 8 SCLKs, SDI must be logic 0. The last 32 SCLKs are needed to read the conversion result. Note that the user is forced to read the conversion in single conversion mode as SDO will remain low (i.e. the serial port is in data mode) until SCLK transitions 40 times. After reading the data, the serial port returns to the command mode, where it waits for a new command to be issued.

Note: In single conversion mode only fully settled data conversions are output to the data conversion register. Since the converter uses a $Sinc^5$ filter for the 3840 Hz word rate, the effective word rate in the single conversion mode will be 1/5 the normal rate (3840/5 which is 768 Hz, MCLK = 4.9152 MHz). Since the converter uses a $Sinc^3$ filter for all other rates, their effective rates will be cut by 1/3 as three conversion are required to fully settle the $Sinc^3$ filter.

2.5.2. Multiple Conversions Mode (MC = 1)

Based on the information provided in the channel-setup registers (CSRs), continuous conversions are repeatedly performed using the Setup register contents pointed to by the conversion command. The command byte includes a pointer address to the Setup register to be used during the conversion. Once transmitted, the serial port enters data mode where it waits until a conversion is complete. After the conversion is done, SDO falls to logic 0. Forty SCLKs are then needed to read the conversion. The first 8 SCLKs are used to clear the SDO flag. The last 32 SCLKs are needed to read the conversion result. If '00000000' is provided to SDI during the first 8 SCLKs when the SDO flag is cleared, the converter remains in this conversion mode and continues to convert the selected channel using the same CSR Setup. While in this mode, not every conversion word needs to be read. The user needs only to read the conversion words required for the application as SDO rises and falls to indicate the availability of a new conversion. Note that if a conversion is not read it will be lost and replaced by a new conversion. To exit this conversion mode the

user must provide '11111111' to the SDI pin during the first 8 SCLKs. If the user decides to exit, 32 SCLKs are required to clock out the last conversion before the converter will return to the command mode.

Note: If a calibration or a single conversion is performed before a multiple conversions command is given, the user must ignore the first three (for OWRs less than 3840 Hz, MCLK = 4.9152 MHz) or first five (for OWR equal to 3840 Hz) conversions in multiple conversions mode as residual filter coefficients must be flushed from the filter before accurate conversion are performed.

2.5.3. Examples of Using CSRs to Perform Conversions and Calibrations

Any time a calibration or conversion command is issued (C, MC, and CC2-CC0 bits must be properly set), the CSRP2-CSRP0 bits in the command byte are used as pointers to address one of the Setups in the channel-setup registers (CSRs). Table 1 details the address decoding of the pointer the bits.

(CSRP2-CSRP0)	CSR Location	Setup
000	CSR #1	1
001	CSR #1	2
010	CSR #2	3
011	CSR #2	4
100	CSR #3	5
101	CSR #3	6
110	CSR#4	7
111	CSR #4	8

Table 1. Command Byte Pointer Table.

The examples that follow detail situations that a user might encounter when acquiring a conversion or calibrating the converter. These examples assume that the CSRs are programmed with the following physical channel order: 4, 1, 1, 2, 4, 3, 4, 4.

A physical channel is defined as the actual input channel (AIN1 to AIN4) to which an external signal is connected.

Example 1: single conversion with Setup 1. The command issued is '10000000'. These settings instruct the converter to perform a single conversion with Setup 1's settings as CSRP2 - CSRP0 = '000' (which happens to be physical channel 4 in this example). After the command is received and decoded the ADC performs a conversion on physical channel 4 and then SDO falls to indicate that the conversion is complete. To read the conversion, 40 SCLKs are then required. Once acquired, the serial port returns to the command mode.

Example 2: continuous conversion with Setup 3. The command issued is '11010000'. These settings instruct the converter to perform continuous conversions with Setup 3's settings as CSRP2 - CSRP0 = '010' (which happens to be physical channel 1 in this example). After the command is received and decoded the ADC performs a conversion on physical channel 1 and then SDO falls to indicate that the conversion is complete. The user now has three options. The user can acquire the conversion and remain in this mode, acquire the conversion and exit this mode, or ignore the conversion and wait for a new conversion at the next update interval.

Example 3: calibration with Setup 4. The command issued is '10011001'. These settings instruct the converter to perform a self offset calibration with Setup 4's settings as CSRP2 - CSRP0 = '011' (which happens to be physical channel 2 in this example). After the command is received and decoded the ADC performs a self offset calibration on physical channel 2 and then SDO falls to indicate that the calibration is complete. To perform additional calibrations, more commands have to be issued.

Note: The CSRs need not be written. If they are not initialized, all the Setups point to their default settings irrespective of the single conversion, multiple single conversion, or calibration mode (i.e conversion can be performed, but only physical channel 1 will be converted). Further note that filter convolutions are reset (i.e. flushed) if consecutive conversions are

performed on two different physical channels. If consecutive conversions are performed on the same physical channel, the filter is not reset. This allows the ADCs to more quickly settle full scale step inputs.

2.6. Conversion Output Coding

The CS5531/32/33/34 output 16-bit (CS5531/33) and 24-bit (CS5532/34) data conversion words. To read a conversion word the user must read the conversion data register. The conversion data register is 32 bits long and outputs the conversions MSB first. The last byte of the conversion data register contains data monitoring flags. The channel indicator (CI) bits keep track of which physical channel was converted and the overrange flag (OF) monitors to determine if a valid conversion was performed. Refer to the *Conversion Data Register Descriptions* section for more details.

The CS5531/32/33/34 output data conversions in binary format when operating in unipolar mode and in two's complement when operating in bipolar mode. Refer to the *Output Coding* section for more details.

2.6.1. Conversion Data Register Descriptions

CS5531/33 (16-BIT CONVERSIONS)

D31(MSB)	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	0	0	0	0	0	OF	CI1	CI0

CS5532/34 (24-BIT CONVERSIONS)

D31(MSB)	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
MSB	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
7	6	5	4	3	2	1	LSB	0	0	0	0	0	OF	CI1	CI0

Conversion Data Bits [31:16 for CS5531/33; 31:8 for CS5532/34]

These bits depict the latest output conversion.

NU (Not Used) [15:3 for CS5531/33; 7:3 for CS5532/34]

These bits are masked logic zero.

OF (Over-range Flag Bit) [2]

0 Bit is clear when over-range condition has not occurred (read only).

1 Bit is set when input signal is more positive than the positive full scale, more negative than zero (unipolar mode) or when the input is more negative than the negative full scale (bipolar mode).

CI (Channel Indicator Bits) [1:0]

These bits indicate which physical input channel was converted.

00 Physical Channel 1

01 Physical Channel 2

10 Physical Channel 3

11 Physical Channel 4

2.6.2. Output Coding

CS5531/33 16-Bit Output Coding

Unipolar Input Voltage	Offset Binary	Bipolar Input Voltage	Two's Complement
>(VFS-1.5 LSB)	FFFF	>(VFS-1.5 LSB)	7FFF
VFS-1.5 LSB	FFFF ------ FFFE	VFS-1.5 LSB	7FFF ------ 7FFE
VFS/2-0.5 LSB	8000 ------ 7FFF	-0.5 LSB	0000 ------ FFFF
+0.5 LSB	0001 ------ 0000	-VFS+0.5 LSB	8001 ------ 8000
<(+0.5 LSB)	0000	<(-VFS+0.5 LSB)	8000

CS5532/34 24-Bit Output Coding

Unipolar Input Voltage	Offset Binary	Bipolar Input Voltage	Two's Complement
>(VFS-1.5 LSB)	FFFFFF	>(VFS-1.5 LSB)	7FFFFF
VFS-1.5 LSB	FFFFFF ------ FFFFFE	VFS-1.5 LSB	7FFFFF ------ 7FFFFE
VFS/2-0.5 LSB	800000 ------ 7FFFFF	-0.5 LSB	000000 ------ FFFFFF
+0.5 LSB	000001 ------ 000000	-VFS+0.5 LSB	800001 ------ 800000
<(+0.5 LSB)	000000	<(-VFS+0.5 LSB)	800000

Note: VFS in the table equals the voltage between ground and full scale for any of the unipolar gain ranges, or the voltage between ± full scale for any of the bipolar gain ranges. See text about error flags under overrange conditions.

Table 2. Output Coding for 16-bit CS5531/33 and 24-bit CS5532/34.

2.7. Digital Filter

The CS5531/32/33/34 have linear phase digital filters which are programmed to achieve a range of output word rates (OWRs) as stated in the *Channel-Setup Register Descriptions* section. The ADCs use a $Sinc^5$ digital filter to output word rates at 3840 Hz (MCLK = 4.9152 MHz). Other output word rates are achieved by using a $Sinc^3$ filter with a programmable decimation (see Figure 15). The $Sinc^3$ is active for all output word rates except for the 3840 Hz (MCLK = 4.9152 MHz) rate.

The converter's digital filters scale with MCLK. For example, with an output word rate of 120 Hz, the filter's corner frequency is typically 31 Hz. If MCLK is increased to 5.0 MHz, the OWR increases by 1.0175 percent and the filter's corner frequency moves to 31.54 Hz. Note that the converter isn't specified to run at MCLK clock frequencies greater than 5 MHz.

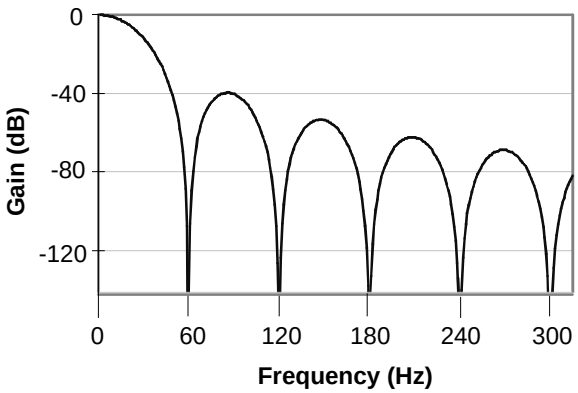


Figure 15. Digital Filter Response (Word Rate = 60 Hz).

Frequency (Hz)	Notch Depth (dB)	Frequency (Hz)	Minimum Attenuation (dB)
50 (MCLK = 4.096MHz)	TBD	TBD	TBD
60 (MCLK = 4.9152MHz)	TBD	TBD	TBD

Table 3. Filter Notch Attenuation.

2.8. Clock Generator

The CS5531/32/33/34 include an on-chip inverting amplifier which can be connected with an external crystal to provide the master clock for the chip. The chips are designed to operate using a 4.9152 MHz crystal; however, other crystal with frequencies between 1 MHz to 5 MHz can be used. One lead of the crystal should be connected to OSC1 and the other to OSC2. Lead lengths should be minimized to reduce stray capacitance. Note that while using the on chip oscillator, neither OSC1 or OSC2 is capable of directly driving any off chip logic. When the on chip oscillator is used, the voltage on OSC2 is typically 1/2 V peak-to-peak. This signal is not compatible with external logic unless additional external circuitry is added. The OSC2 output should be used if the crystal output is used to drive other logic.

The designer can use an external CMOS compatible oscillator to drive OSC2 with a 1 MHz to 5 MHz clock for the ADC. In this scheme, OSC1 is left unconnected.

2.9. Power Supply Arrangements

The CS5531/32/33/34 are designed to operate from single or dual analog supplies and a single digital supply. The following power supply connections are possible:

VA+ = +5 V; VA- = 0 V; VD+ = +3 V to +5 V

VA+ = +2.5 V; VA- = -2.5 V; VD+ = +3 V to +5 V

VA+ = +3 V; VA- = -3 V; VD+ = +3 V

Figure 16 illustrates the CS5532 connected with a single +5.0 V supply to measure differential inputs relative to a common mode of 2.5 V. Figure 17 illustrates the CS5532 connected with ±2.5 V bipolar analog supplies and a +3 V to +5 V digital supply to measure ground referenced bipolar signals. Figure 18 illustrates the CS5532 connected with ±3 V analog supplies and a +3 V digital supply to measure ground referenced bipolar signals.

Figure 19 illustrates alternate bridge configurations which can be measured with the converter. Voltage V1 can be measured with the PGIA gain set to 1x as the input amplifier on this gain setting can go rail-to-rail. Voltage V2 should be measured with the PGIA gain set at 2x or higher as the instrumentation amplifier used on these gain ranges achieves lower noise.

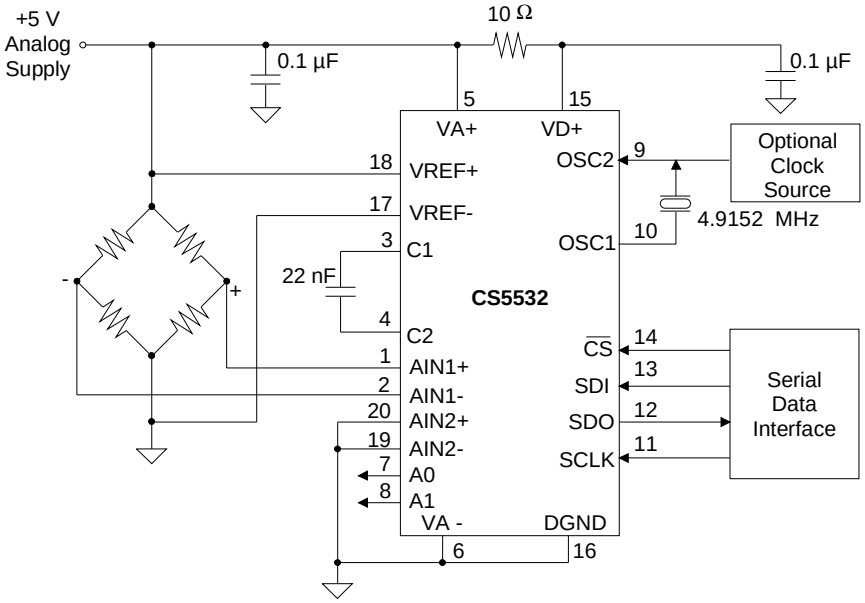


Figure 16. CS5532 Configured with a Single +5 V Supply.

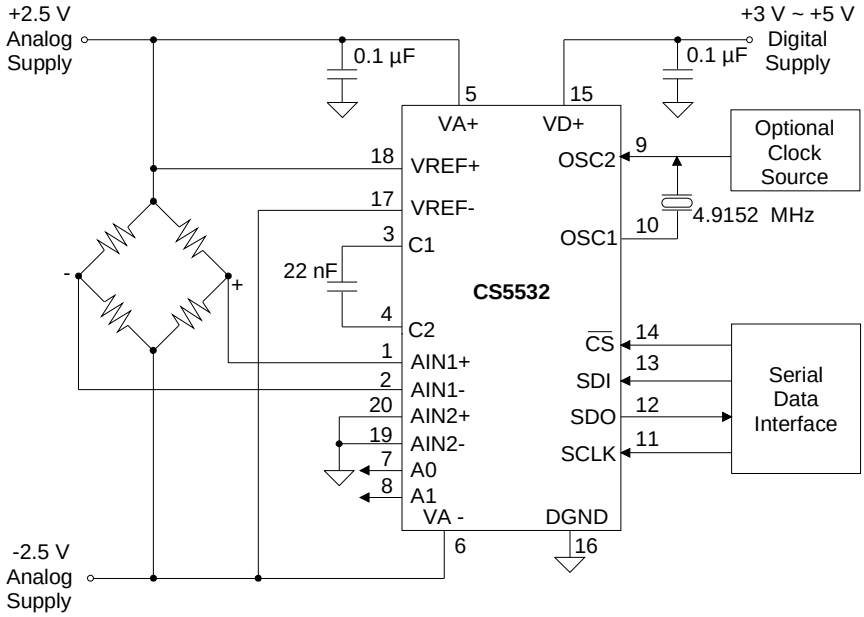


Figure 17. CS5532 Configured with ±2.5 V Analog Supplies.

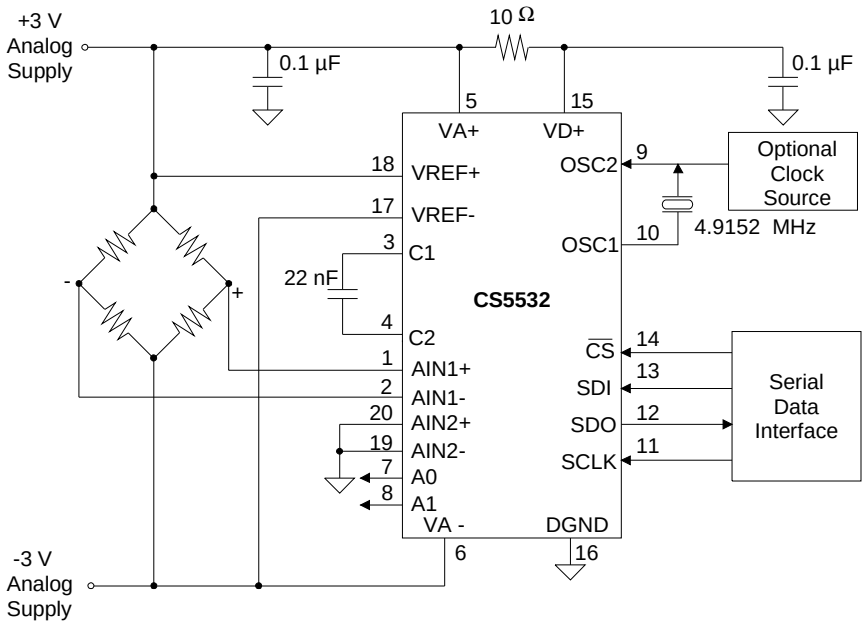


Figure 18. CS5532 Configured with ±3 V Analog Supplies.

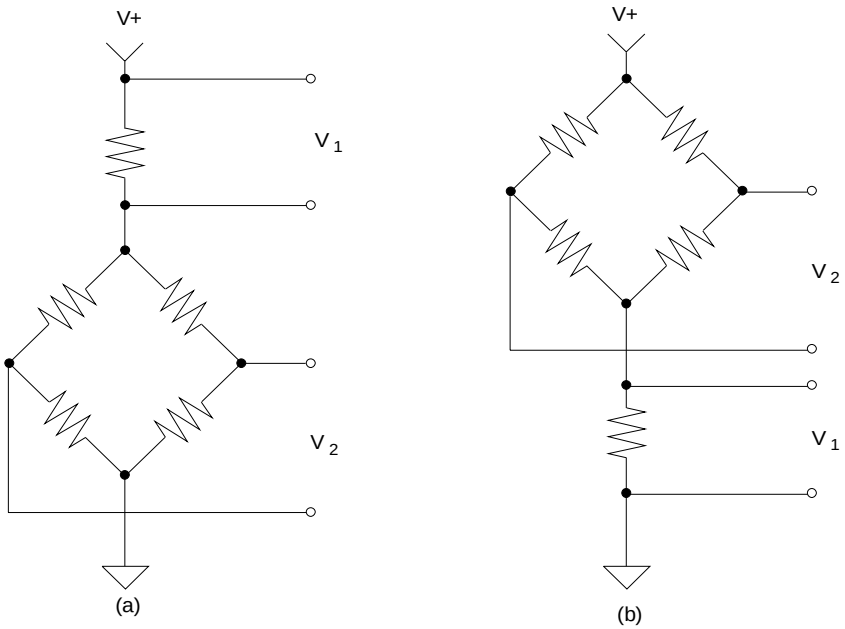


Figure 19. Bridge with Series Resistors.

2.10. Getting Started

This part has several features. From a software programmer's prospective, what should be done first? To begin, a 4.9152 MHz or 4.096 MHz crystal takes approximately 20 ms to start. To accommodate for this, it is recommended that a software delay of approximately 20 ms start the processor's ADC initialization code. Next, since the CS5531/32/33/34 do not provide a power-on-reset function, the user must first initialize the ADC to a known state. This is accomplished by resetting the ADC's serial port with the Serial Port Initialization sequence. This sequence resets the serial port to the command mode and is accomplished by transmitting 15 SYNC1 command bytes (0xFF hexadecimal), followed by one SYNC0 command (0xFE hexadecimal). Once the ADC is in a known state (in this case the command mode), the user must reset all the internal logic by performing a system reset. This is accomplished by setting the Reset System (RS) bit in the configuration register. After a system reset cycle is complete, the RS bit is automatically returned to logic 0, all on-chip logic is initialized to its proper state, and the ADC is returned to the command mode where it waits for the next valid command to execute. The next action is to initialize the voltage reference mode. The voltage reference select (VRS) bit in the configuration register must be set based upon the magnitude of the reference voltage between the VREF+ and the VREF- pins.

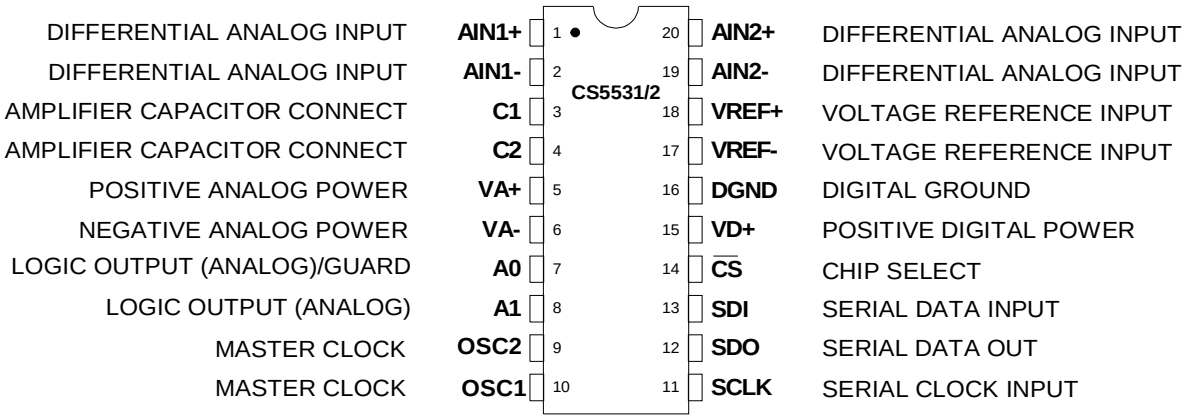
After this, initialize the channel-setup registers (CSRs) as these registers determine how calibrations and conversions will be performed. Once the CSRs are initialized, the user has three options in calibrating the ADC: 1) don't calibrate and use the default settings; 2) perform self or system calibrations; or 3) upload previously saved calibration results to the offset and gain registers. Once calibrated, the ADC is ready to perform conversions.

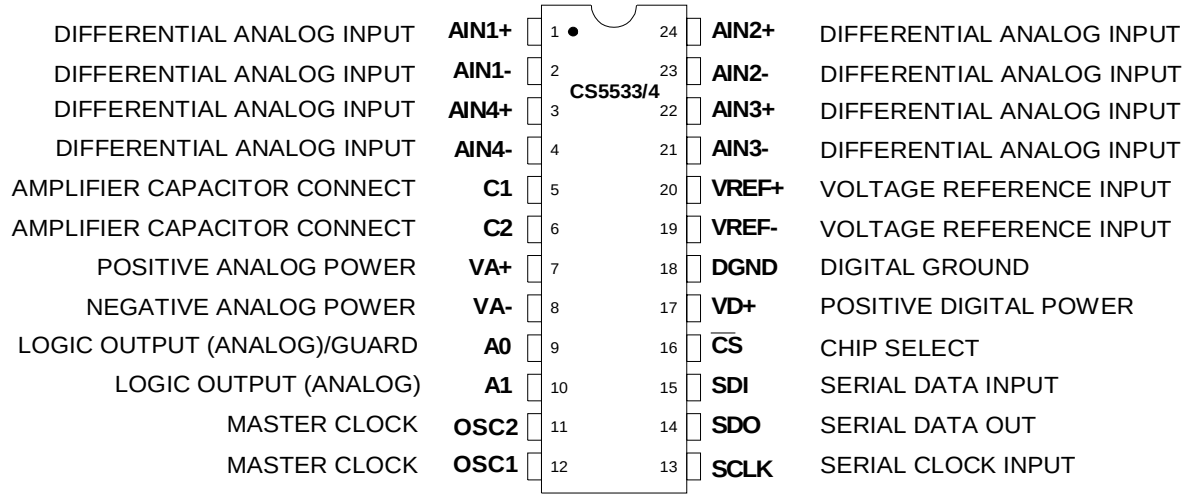
2.11. PCB Layout

The CS5531/32/33/34 should be placed entirely over an analog ground plane. Place the analog-digital plane split immediately adjacent to the digital portion of the chip.

Note: See the CDB5531/32/33/34 data sheet for suggested layout details and Applications Note 18 for more detailed layout guidelines. Before layout, please call for our Free Schematic Review Service.

3. PIN DESCRIPTIONS





Clock Generator

OSC1; OSC2 - Master Clock.

An inverting amplifier inside the chip is connected between these pins and can be used with a crystal to provide the master clock for the device. Alternatively, an external (CMOS compatible) clock (powered relative to VD+) can be supplied into the OSC2 pin to provide the master clock for the device.

Control Pins and Serial Data I/O

$\overline{\text{CS}}$ - Chip Select.

When active low, the port will recognize SCLK. When high the SDO pin will output a high impedance state. $\overline{\text{CS}}$ should be changed when SCLK = 0.

SDI - Serial Data Input.

SDI is the input pin of the serial input port. Data will be input at a rate determined by SCLK.

SDO - Serial Data Output.

SDO is the serial data output. It will output a high impedance state if $\overline{CS}$ = 1.

SCLK - Serial Clock Input.

A clock signal on this pin determines the input/output rate of the data for the SDI/SDO pins respectively. This input is a Schmitt trigger to allow for slow rise time signals. The SCLK pin will recognize clocks only when $\overline{CS}$ is low.

A0 - Logic Output (Analog)/Guard, A1 - Logic Output (Analog).

The logic states of A0-A1 mimic the states of the D22/D10-D23/D11 bits of the channel-setup register. Logic Output 0 = VA-, and Logic Output 1 = VA+. A0 can be used as a guard drive for the instrumentation amplifier with proper setting of the GB bit in the Configuration Register.

Measurement and Reference Inputs

AIN1+, AIN1-, AIN2+, AIN2- AIN3+, AIN3-, AIN4+, AIN4- - Differential Analog Input.

Differential input pins into the CS5531.

VREF+, VREF- - Voltage Reference Input.

Fully differential inputs which establish the voltage reference for the on-chip modulator.

C1, C2 - Amplifier Capacitor Inputs.

Connections for the instrumentation amplifier's capacitor.

Power Supply Connections

VA+ - Positive Analog Power.

Positive analog supply voltage.

VD+ - Positive Digital Power.

Positive digital supply voltage (nominally +3.0 V or +5 V).

VA- - Negative Analog Power.

Negative analog supply voltage.

DGND - Digital Ground.

Digital Ground.

4. SPECIFICATION DEFINITIONS

Linearity Error

The deviation of a code from a straight line which connects the two endpoints of the ADC transfer function. One endpoint is located 1/2 LSB below the first code transition and the other endpoint is located 1/2 LSB beyond the code transition to all ones. Units in percent of full-scale.

Differential Nonlinearity

The deviation of a code's width from the ideal width. Units in LSBs.

Full Scale Error

The deviation of the last code transition from the ideal [{(VREF+) - (VREF-)} - 3/2 LSB]. Units are in LSBs.

Unipolar Offset

The deviation of the first code transition from the ideal (1/2 LSB above the voltage on the AIN- pin.). When in unipolar mode (U/$\overline{B}$ bit = 1). Units are in LSBs.

Bipolar Offset

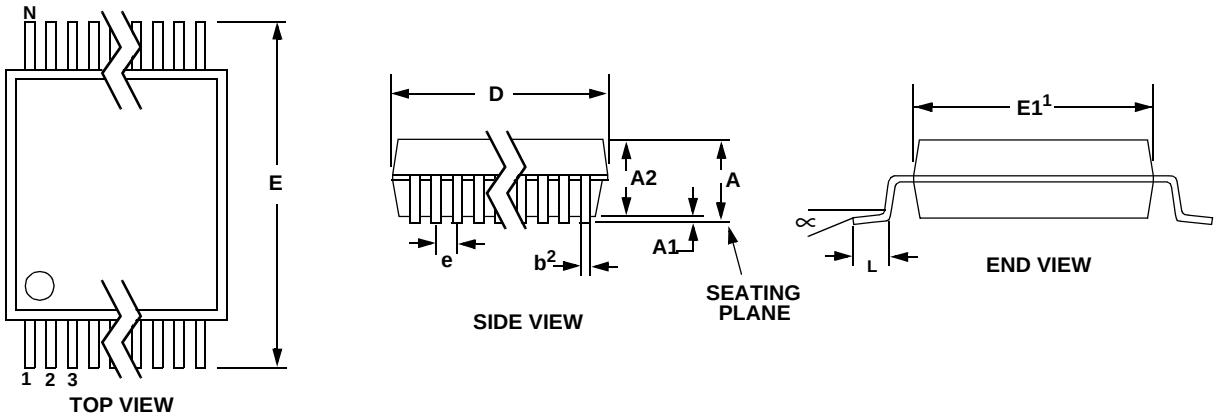
The deviation of the mid-scale transition (111...111 to 000...000) from the ideal (1/2 LSB below the voltage on the AIN- pin). When in bipolar mode (U/$\overline{B}$ bit = 0). Units are in LSBs.

5. ORDERING GUIDE

Model Number	Bits	Channels	Linearity Error (Max)	Temperature Range	Package
CS5531-AS	16	2	±0.003%	-40°C to +85°C	20-pin 0.2" Plastic SSOP
CS5533-AS	16	4	±0.003%	-40°C to +85°C	24-pin 0.2" Plastic SSOP
CS5532-AS	24	2	±0.003%	-40°C to +85°C	20-pin 0.2" Plastic SSOP
CS5532-BS	24	2	±0.0015%	-40°C to +85°C	20-pin 0.2" Plastic SSOP
CS5534-AS	24	4	±0.003%	-40°C to +85°C	24-pin 0.2" Plastic SSOP
CS5534-BS	24	4	±0.0015%	-40°C to +85°C	24-pin 0.2" Plastic SSOP

6. PACKAGE DRAWINGS

20 PIN SSOP PACKAGE DRAWING



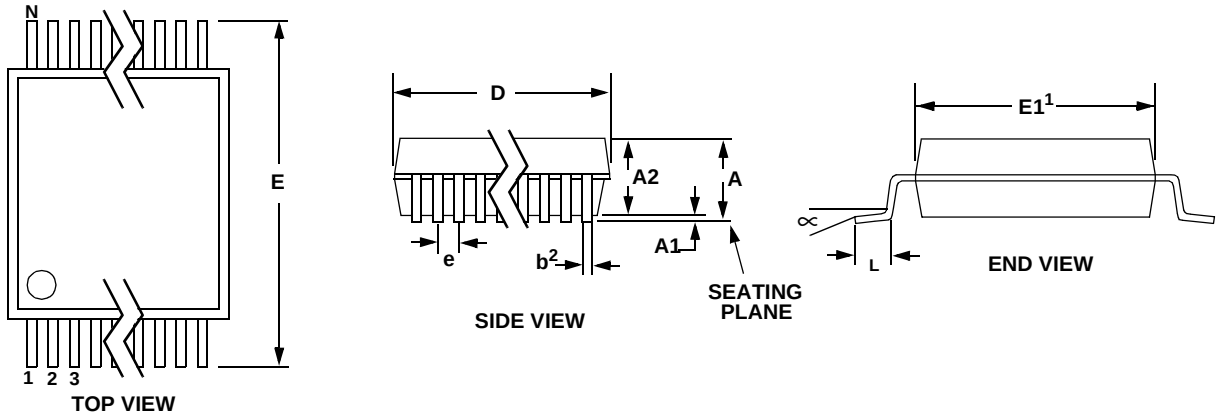
	INCHES		MILLIMETERS		NOTE
DIM	MIN	MAX	MIN	MAX	
A	--	0.084	--	2.13	
A1	0.002	0.010	0.05	0.25	
A2	0.064	0.074	1.62	1.88	
b	0.009	0.015	0.22	0.38	2,3
D	0.272	0.295	6.90	7.50	1
E	0.291	0.323	7.40	8.20	
E1	0.197	0.220	5.00	5.60	1
e	0.024	0.027	0.61	0.69	
L	0.025	0.040	0.63	1.03	
∝	0°	8°	0°	8°	

Notes: 1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

24 PIN SSOP PACKAGE DRAWING



	INCHES		MILLIMETERS		NOTE
DIM	MIN	MAX	MIN	MAX	
A	--	0.084	--	2.13	
A1	0.002	0.010	0.05	0.25	
A2	0.064	0.074	1.62	1.88	
b	0.009	0.015	0.22	0.38	2,3
D	0.311	0.335	7.90	8.50	1
E	0.291	0.323	7.40	8.20	
E1	0.197	0.220	5.00	5.60	1
e	0.024	0.027	0.61	0.69	
L	0.025	0.040	0.63	1.03	
∝	0°	8°	0°	8°	

Notes: 1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

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