CS5460

Single Phase Bi-Directional Power/Energy IC

Features

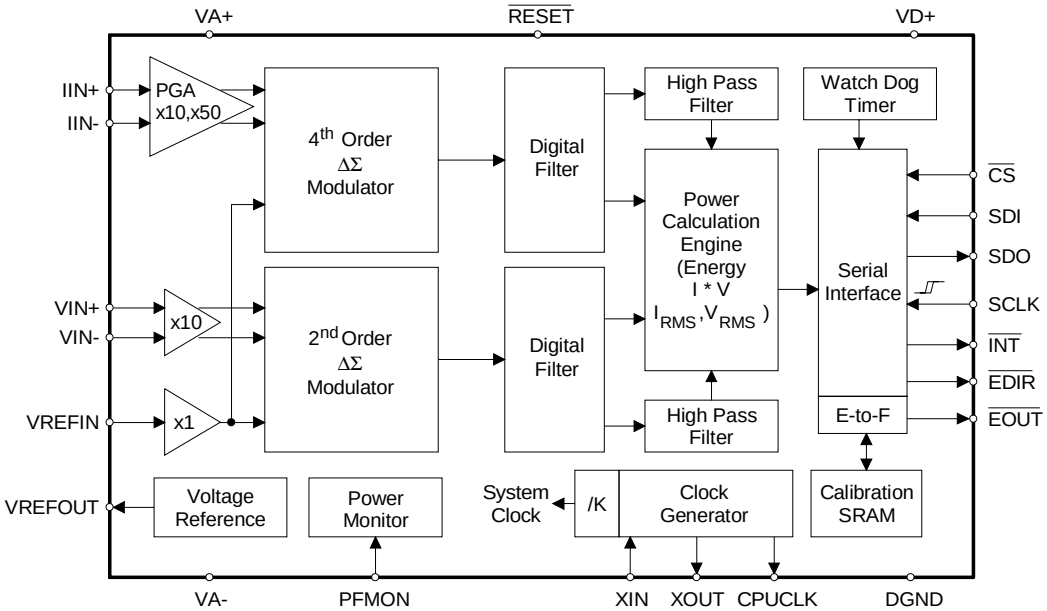
- Energy Data Linearity: 0.1% of Reading over 1000:1 Dynamic Range
- On-Chip Functions: Energy, I ∗ V, I_{RMS} and V_{RMS}, Energy to Pulse-Rate Conversion
- Complies with IEC 687/1036, JIS
- Power Consumption <12 mW
- Interface Optimized for Shunt Sensor
- Phase Compensation
- Ground-Referenced Signals with Single Supply
- System Calibration
- On-chip 2.5 V Reference (60 ppm/°C drift)
- Simple Three-wire Serial Interface
- Watch Dog Timer
- Power Supply Monitor
- Power Supply Configurations
  - VA+ = +5 V; VA- = 0V; VD+ = +3 V to +5 V
  - VA+ = +2.5 V; VA- = -2.5 V; VD+ = +3 V

Description

The CS5460 is a highly integrated ΔΣ Analog-to-Digital Converter (ADC) which combines two ΔΣ ADCs, high speed power calculation functions, and a serial interface on a single chip. It is designed to accurately measure and calculate: Energy, Instantaneous Power, I_{RMS}, and V_{RMS} for single phase 2 or 3-wire power meter applications. The CS5460 interfaces to a low cost shunt or transformer to measure current, and resistive divider or transformer to measure voltage. The CS5460 features a bi-directional serial interface for communication with a micro-controller and a fixed-width programmable frequency output that is proportional to energy. The product is initialized and fully functional upon power-up, and includes facilities for system-level calibration under control of the user program.

ORDERING INFORMATION:

CS5460-BS	-40°C to +85°C	24-pin SSOP



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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1. CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS (T_A = -40 °C to +85 °C; VA+, VD+ = +5 V ±10%; VREFIN = 2.5 V; VA- = AGND; MCLK = 4.096 MHz, K = 1; N = 4000, OWR = 4.0 kHz.)(See Notes 1, 2, and 3)

Parameter		Symbol	Min	Typ	Max	Unit
Accuracy (Both Channels)						
Total Harmonic Distortion		THD	74	-	-	dB
Common Mode Rejection	(DC, 50, 60 Hz)	CMRR	80	-	-	dB
Offset Drift (Without the High Pass Filter)			-	5	-	nV/°C
Full Scale DC Calibration Range	(Note 4)	FSCR	25	-	100	%F.S.
Input Sampling Rate	DCLK = MCLK/K		-	DCLK/4	-	Hz
Analog Inputs (Current Channel)						
Differential Input Voltage Range {(IIN+) - (IIN-)}	(Gain = 10) (Gain = 50)	IIN	- -	150 30	- -	mV_{rms} mV_{rms}
Common Mode + Signal on IIN+ or IIN-	(Gain = 10 or 50)		-0.25	-	VA+	V
Crosstalk with Voltage Channel at Full Scale	(50, 60 Hz)		-	-	-115	dB
Input Capacitance	(Gain = 10) (Gain = 50)	IC	- -	5 25	- -	pF pF
Effective Input Impedance	(Note 5) (Gain = 10) (Gain = 50)	EII	 30 30	 - -	 - -	 kΩ kΩ
Noise (Referred to Input)	(Gain = 10) (Gain = 50)		- -	- -	20 4	μV_{rms} μV_{rms}
Accuracy (Current Channel)						
Bipolar Offset Error	(Note 1)	VOS	-	-	±0.001	%F.S.
Full-Scale Error	(Note 1)	FSE	-	-	±0.001	%F.S.
Analog Inputs (Voltage Channel)						
Differential Input Voltage Range	{(VIN+) - (VIN-)}	VIN	-	150	-	mV_{rms}
Common Mode + Signal on VIN+ or VIN-			-0.25	-	VA+	V
Crosstalk with Current Channel at Full Scale	(50, 60 Hz)		-	-	-70	dB
Input Capacitance		IC	-	0.2	-	pF
Effective Input Impedance	(Note 5)	EII	5	-	-	MΩ
Noise (Referred to Input)			-	-	250	μV_{rms}
Accuracy (Voltage Channel)						
Bipolar Offset Error	(Note 1)	VOS	-	-	±0.01	%F.S.
Full-Scale Error	(Note 1)	FSE	-	-	±0.01	%F.S.

Notes:
1. Applies after system calibration
2. Specifications guaranteed by design, characterization, and/or test.
3. Analog signals are relative to VA- and digital signals to DGND unless otherwise noted.
4. The minimum FSCR is limited by the maximum allowed gain register value.
5. Effective Input Impedance (EII) varies with clock frequency (DCLK) and Input Capacitance (IC) EII = 1/(IC*DCLK/4)

ANALOG CHARACTERISTICS (Continued)

Parameter		Symbol	Min	Typ	Max	Unit
Dynamic Characteristics						
Phase Compensation	(Voltage Channel at 60 Hz)		-2.4	-	+2.5	°
High Rate Filter Output Word Rate	(Both Channels)	OWR	-	DCLK/1024	-	Hz
High Pass Filter Pole Frequency	-3 dB		-	0.5	-	Hz
Reference Output						
Output Voltage		REFOUT	2.4	-	2.6	V
Temperature Coefficient			-	25	60	ppm/°C
Load Regulation	(Output Current 1 µA Source or Sink)	ΔV_R	-	6	10	mV
Output Noise Voltage	(0.1 Hz to 512 kHz)	eN	-	100	-	μV_{rms}
Reference Input						
Input Voltage Range		VREFIN	2.4	2.5	2.6	V
Input Capacitance			-	4	-	pF
Input CVF Current			-	25	-	nA
Power Supplies						
Power Supply Currents (Normal Mode)	I_{A+}	PSCA	-	1.3	-	mA
	I_{D+} (VD+ = 5 V)	PSCD	-	2.9	-	mA
	I_{D+} (VD+ = 3 V)	PSCD	-	1.7	-	mA
Power Consumption	Normal Mode (VD+ = 5 V)	PC	-	21	25	mW
(Note 6)	Normal Mode (VD+ = 3 V)		-	11.6	-	mW
	Standby		-	6.75	-	mW
	Sleep		-	10	-	µW
Power Supply Rejection	(50, 60 Hz)			-	-	
	(Gain = 10)	PSRR	56			dB
	(Gain = 50)	PSRR	70			dB
Power Monitor Thresholds		PM	2.3		2.7	V

Notes: 6. All outputs unloaded. All inputs CMOS level.

5 V DIGITAL CHARACTERISTICS (T_A = -40 °C to +85 °C; VA+, VD+ = 5 V ±10% VA-, DGND = 0 V) (See Notes 2 and 7)

Parameter		Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	All Pins Except XIN and SCLK	V_{IH}	0.6 VD+	-	-	V
	XIN		(VD+) - 0.5	-	-	V
	SCLK		0.8 VD+	-	-	V
Low-Level Input Voltage	All Pins Except XIN and SCLK	V_{IL}	-	-	0.8	V
	XIN		-	-	1.5	
	SCLK		-	-	0.2 VD+	
High-Level Output Voltage	I_{out} = +5 mA	V_{OH}	(VD+) - 1.0	-	-	V
Low-Level Output Voltage	I_{out} = -5 mA	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	±1	±10	µA
3-State Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	5	-	pF

3 V DIGITAL CHARACTERISTICS (T_A = -40 °C to +85 °C; VA+ = 5 V ±10%, VD+ = 3 V ±10%; VA-, DGND = 0 V) (See Notes 2 and 7)

Parameter		Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	All Pins Except XIN and SCLK	V_{IH}	0.6 VD+	-	-	V
	XIN		(VD+) - 0.5	-	-	V
	SCLK		0.8 VD+	-	-	V
Low-Level Input Voltage	All Pins Except XIN and SCLK	V_{IL}	-	-	0.48	V
	XIN		-	-	0.3	
	SCLK		-	-	0.2 VD+	
High-Level Output Voltage	I_{out} = +5 mA	V_{OH}	(VD+) - 1.0	-	-	V
Low-Level Output Voltage	I_{out} = -5 mA	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	±1	±10	µA
3-State Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	5	-	pF

Notes: 7. All measurements performed under static conditions.

ABSOLUTE MAXIMUM RATINGS (DGND = 0 V; See Note 8)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	(Notes 9 and 10)					
	Positive Digital	VD+	-0.3	-	+6.0	V
	Positive Analog	VA+	-0.3	-	+6.0	V
	Negative Analog	VA-	+0.3	-	-6.0	V
Input Current, Any Pin Except Supplies	(Note 11 and 12)	I_{IN}	-	-	±10	mA
Output Current		I_{OUT}	-	-	±25	mA
Power Dissipation	(Note 13)	PDN	-	-	500	mW
Analog Input Voltage	All Analog Pins	V_{INA}	- 0.3	-	(VA+) + 0.3	V
Digital Input Voltage	All Digital Pins	V_{IND}	-0.3	-	(VD+) + 0.3	V
Ambient Operating Temperature		T_A	-40	-	85	°C
Storage Temperature		T_{stg}	-65	-	150	°C

Notes: 8. All voltages with respect to ground.

9. VA+ and VA- must satisfy {(VA+) - (VA-)} < +6.0 V.

10. VD+ and VA- must satisfy {(VD+) - (VA-)} < +6.0 V.

11. Applies to all pins including continuous over-voltage conditions at the analog input (AIN) pins.

12. Transient current of up to 100 mA will not cause SCR latch-up. Maximum input current for a power supply pin is ±50 mA.

13. Total power dissipation, including all input currents and output currents.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS (T_A = -40 °C to +85 °C; VA+ = 5.0 V ±10%; VD+ = 3.0 V ±10% or 5.0 V ±10%; VA- = 0.0 V; Logic Levels: Logic 0 = 0.0 V, Logic 1 = VD+; CL = 50pF))

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Frequency	Internal Gate Oscillator (Note 14)	MCLK	2.5	4.096	20	MHz
Master Clock Duty Cycle			40	-	60	%
CPUCLK Duty Cycle	(Note 15)		40		60	%
Rise Times	Any Digital Input Except SCLK (Note 16)	t_{rise}	-	-	1.0	µs
	SCLK		-	-	100	µs
	Any Digital Output		-	50	-	ns
Fall Times	Any Digital Input Except SCLK (Note 16)	t_{fall}	-	-	1.0	µs
	SCLK		-	-	100	µs
	Any Digital Output		-	50	-	ns
Start-up						
Oscillator Start-up Time	XTAL = 4.096 MHz (Note 17)	t_{ost}	-	60	-	ms
Serial Port Timing						
Serial Clock Frequency		SCLK	-	-	2	MHz
Serial Clock	Pulse Width High	t_1	200	-	-	ns
	Pulse Width Low	t_2	200	-	-	ns
SDI Write Timing						
$\overline{CS}$ Enable to Valid Latch Clock		t_3	50	-	-	ns
Data Set-up Time Prior to SCLK Rising		t_4	50	-	-	ns
Data Hold Time After SCLK Rising		t_5	100	-	-	ns
SCLK Falling Prior to CS Disable		t_6	100	-	-	ns
SDO Read Timing						
$\overline{CS}$ Enable to Valid Latch Clock		t_7	-	-	150	ns
SCLK Falling to New Data Bit		t_8	-	-	150	ns
CS Rising to SDO Hi-Z		t_9	-	-	150	ns

Notes: 14. Device parameters are specified with a 4.096 MHz clock, however, clocks between 3MHz to 20 MHz can be used.

15. If external MCLK is used, then its duty cycle must be between 45% and 55% to maintain this spec.

16. Specified using 10% and 90% points on wave-form of interest. Output loaded with 50 pF.

17. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.

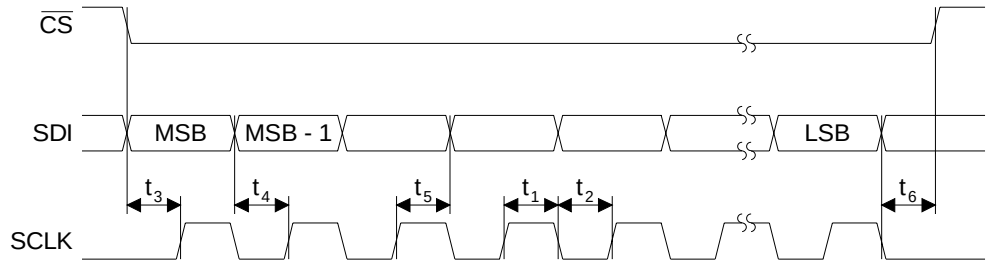


Figure 1. SDI Write Timing (Not to Scale)

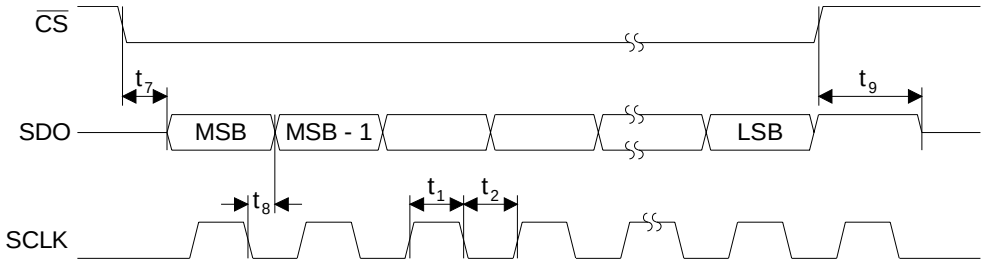


Figure 2. SDO Read Timing (Not to Scale)

2. GENERAL DESCRIPTION

The CS5460 is a CMOS monolithic power measurement device with an energy computation engine. The CS5460 combines a programmable gain amplifier, two ΔΣ modulators, two high rate filters, system calibration, and power calculation functions to compute Energy, V_{RMS}, I_{RMS}, and Instantaneous Power.

The CS5460 is designed for power meter applications and is optimized to interface to shunts or current transformers to measure current, and a resistive divider or transformer to measure voltage. To accommodate various input voltage levels due to shunts, the current channel includes a programmable gain amplifier (PGA) which allows the user to measure either $150mV_{RMS}$ or $30mV_{RMS}$ signals.

The CS5460 includes two high-rate digital filters which output data at a (MCLK/K)/1024 output word rate (OWR). A high-pass filter in both channels can be enabled to remove the DC content from the input signal before the energy calculations are made.

To ease communication between the CS5460 and a micro-controller, the converter includes a simple three-wire serial interface which is SPI™ and Microwire™ compatible. The serial port also contains a Schmitt Trigger input on its serial clock (SCLK) to allow for slow rise time signals.

2.1 Theory of Operation

The CS5460 is designed to operate from a single +5 V supply or dual ±2.5 V supplies, to provide a $30mV_{RMS}$ or $150mV_{RMS}$ range for the current channel and to provide a $150mV_{RMS}$ range for the voltage channel. With single supply, the CS5460 is designed to accommodate common mode signals of -0.25V to VA+.

Figure 3 illustrates the CS5460 connected to a service to measure power in a single-phase 2-wire system while operating in a single supply configuration. Figure 4 illustrates the CS5460 configured to measure power in a single-phase 3-wire system.

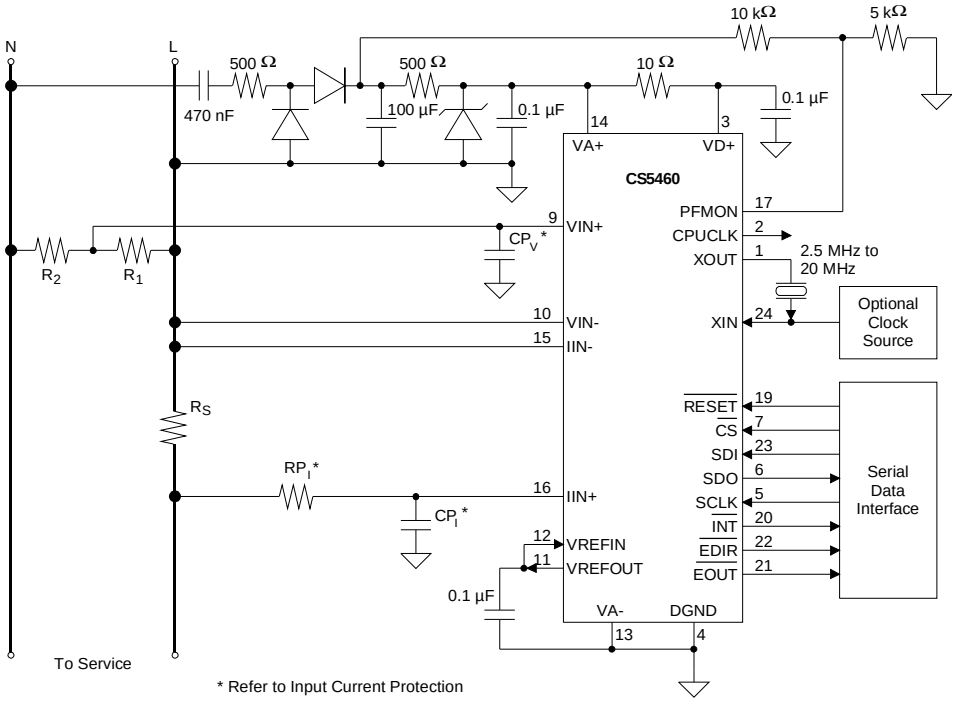


Figure 3. Typical Connection Diagram (One-Phase 2-Wire)

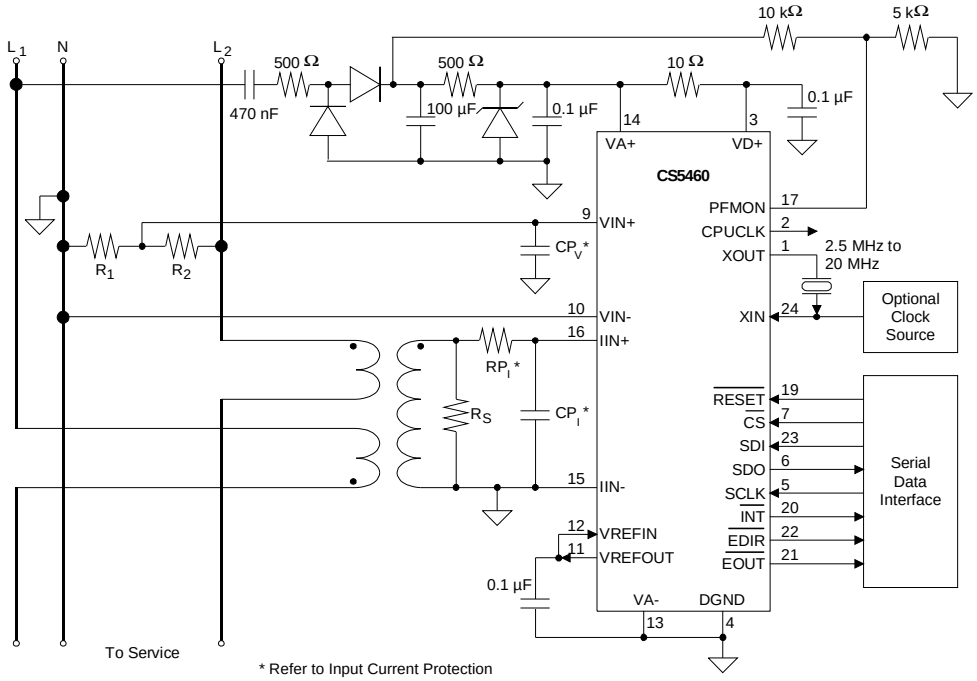


Figure 4. Typical Connection Diagram (One-Phase 3-Wire)

2.2 Performing Measurements

The CS5460 performs measurements of instantaneous current, instantaneous voltage, instantaneous power, energy, RMS current, and RMS voltage. These measurements are output as 24-bit signed and unsigned data formats as a percentage of full scale. The flow of data to perform these calculations is shown in Figure 5. All of these measurements begin when a start conversion command is given. The energy and RMS registers are then updated every N conversions (or 1 computation cycle) where N is the content of the Cycle Count register. After the computation cycle has finished, the DRDY bit in the Status and Mask register is set. The $\overline{INT}$ pin will also become active if the DRDY bit is unmasked.

Table 1 provides an example detailing the output linearity. A computation cycle is derived from the master clock and its frequency is (MCLK/K)/(1024*N). Instantaneous calculations are performed at a 4000 Hz rate where as, I_{RMS}, V_{RMS}, and energy, are performed at a 1 Hz rate. Also, DRDY is set only after computation cycles are complete (i.e. there is no indicator flag to indicate when the instantaneous conversions are read; however, if the Cycle Count register were set to 1, all output calculations would be instantaneous and DRDY would indicate when instantaneous calculations were finished).

	Energy	Vrms	Irms
Range	1000:1	2:1	500:1
Max Input	See *Analog Characteristics*		
Linearity (After Calibration)	0.1% of reading	0.1% of reading	0.1% of reading
Output word	24-bits		

Table 1. Specification with MCLK = 4.096 MHz, K = 1, and N = 4000.

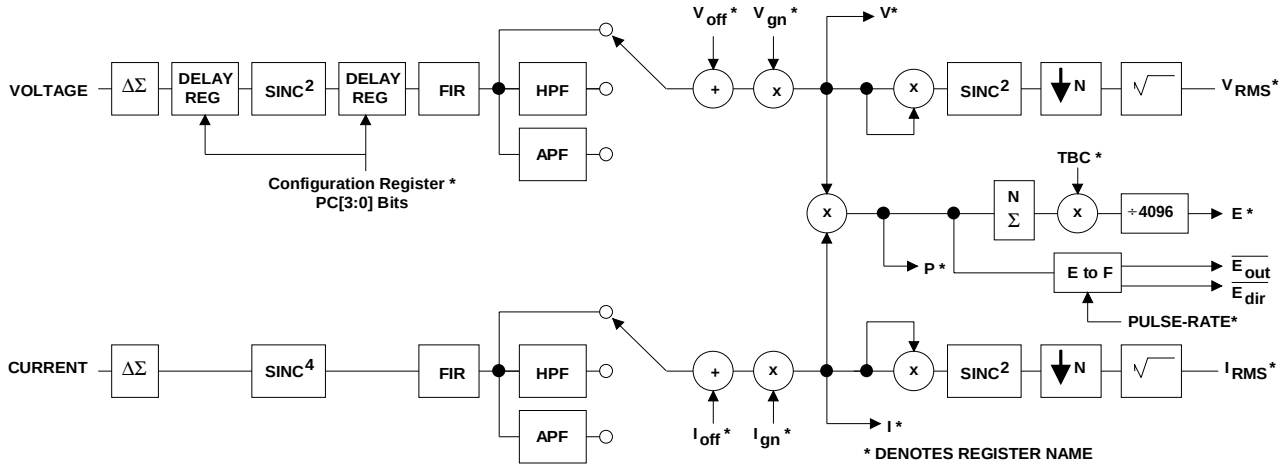


Figure 5. Data Flow.

2.2.1 Single Computation Cycle (C = 0)

Based on the information provided in the Cycle Count register, a single computation cycle is performed after the user transmits the single conversion cycle command. After the computations are complete, DRDY is set. Thirty-two SCLKs are then needed to acquire a calculation result. The first 8 SCLKs are used to clock in the command to determine which result register is to be read. The last 24 SCLKs are needed to read the desired calculation result register. After reading the data, the serial port returns to the command mode, where it waits for a new command to be issued.

2.2.2 Multiple Computation Cycles (C = 1)

Based on the information provided in the Cycle Count register, continuous computation cycles are repeatedly performed on the voltage and current cycles. Computation cycles cannot be started/stopped on a per channel basis. After each computation cycle is completed, DRDY is set. Thirty-two SCLKs are then needed to read a register. The first 8 SCLKs are used to clock in the command to determine which results register is to be read. The last 24 SCLKs are needed to read the calculation result. While in this mode, the user may choose to acquire only the calculations required for the application as DRDY rises and falls to indicate the availability of a new data.

The RMS calculations require a $Sinc^2$ operation prior to their square root operation. Therefore, the first output for each channel will be invalid (i.e. all RMS calculations are invalid in the single computation cycle routine and the first RMS calculations will be invalid in the continuous computation cycle). All energy calculations will be valid since energy calculations don't require this $Sinc^2$ operation.

2.3 High Rate Digital Filters

The high rate filter on the voltage channel is implemented as a fixed $sinc^2$ filter, compensated by a short length FIR. When the converter is driven with a 4.096 MHz clock (K=1), the filter has a magnitude response similar to that shown in Figure 6. Note that the filter's response scales with MCLK frequency and K.

The current channel contains a $sinc^4$ filter, compensated by a short length FIR. When the converter is driven with a 4.096 MHz clock (K=1) the composite filter response is given in Figure 7.

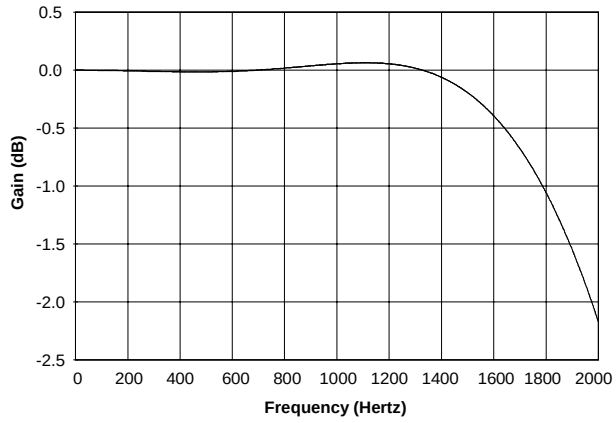


Figure 6. Voltage Input Filter Roll-off

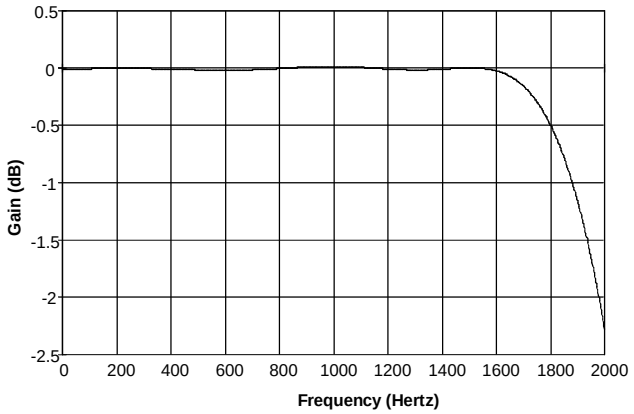


Figure 7. Current Input Filter Roll-off

2.4 Pulse-Rate Output

As an alternative to reading the energy through the serial port, the $\overline{EOUT}$ and $\overline{EDIR}$ pins provide a simple interface with which signed energy can be accumulated. Each $\overline{EOUT}$ pulse represents a predetermined magnitude of energy. The accompanying $\overline{EDIR}$ level represents the sign of the energy. With MCLK = 4.096 MHz, K = 1, and both ADC inputs at their maximum DC values, the pulses will have a frequency equal to that in the pulse rate register.

The following example illustrates how to calculate the pulse-rate register contents for a given meter design. Suppose that a single two-phase power meter (Figure 3) is required to generate 500 impulses/KWH at $I_b = 20\ A_{RMS}$ and $V = 230\ V_{RMS}$. Assume that the maximum current is $I_{max} = 100\ A_{RMS}$ and the maximum voltage is $V_{max} = 300\ V_{RMS}$. To utilize the full dynamic range of the CS5460, the sensor gains can be calculated as:

$$k_v = \frac{150mV_{RMS}}{V_{max}} = \frac{1}{2000}$$

$$k_i = \frac{30mV_{RMS}}{I_{max}} = 300\ \mu\Omega$$

where k_v and k_i are the sensor gains for the voltage and current, respectively. The CS5460 is assumed to be in the 30 mV_{RMS} range to allow for the use of a shunt resistor.

The average Impulse Rate, IR, at the rated inputs is:

$$R = \left(\frac{500\ impulses}{KWH}\right)(I_b V)\left(\frac{1KW}{1000W}\right)\left(\frac{1H}{3600s}\right) \cong \frac{0.639\ impulses}{s}$$

Since the pulse-rate register is defined in terms of full-scale DC (0.25 V for the voltage channel and 0.05 V for the current channel in this case), IR will need to be scaled before being placed in the pulse-rate register. Define a voltage ratio, R_v, and a current ratio, R_i, as:

$$R_v = \frac{0.25\ Volt}{k_v V\ Volt}$$

$$R_i = \frac{0.05\ Volt}{k_i I_b\ Amp}$$

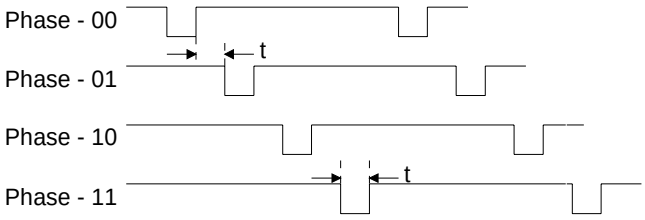
Therefore, the pulse rate register is programmed to be :

$$PR = IR \times R_v \times R_i \cong 11.574 \text{ Hz} = 370 \text{ or } 0x172$$

To improve the accuracy, either gain register can be programmed to correct for the round-off error in PR. This value would be calculated as

$$\text{Ign or Vgn} = \frac{PR}{370 \times 2^{-5}} \cong 1.001 = 0x401067$$

To allow for a simpler interface in a multi-phase system, the $\overline{EOUT}$ and $\overline{EDIR}$ pins can be connected together and used in a wired-or configuration. The parts must be driven with the same clock and programmed with different phases (PH[1:0] in the Configuration register). The pulse width and the pulse separation is an integer multiple of system clocks (approximately equal to 1/8 of the period of the contents of the pulse-rate register). The maximum frequency is therefore MCLK/K/8. A timing diagram for a multi-phase system is shown in Figure 8.



$$t \cong \frac{\textit{Pulse-Rate Register Period}}{8} = \frac{N}{MCLK/K} \quad \textit{for Integer N}$$

Figure 8. Multi-Phase System

3. SERIAL PORT OVERVIEW

The CS5460's serial port incorporates a state machine with transmit/receive buffers. The state machine interprets 8 bit command words on the rising edge of SCLK. Upon decoding of the command word the state machine performs the requested command or prepares for a data transfer of the addressed register. Request for a read requires an internal register transfer to the transmit buffer, while a write waits until the completion of 24 SCLKs before performing a transfer. The internal registers are used to control the ADC's functions. All registers are 24-bits in length. Figure 9 depicts the internal registers available to the user.

After system initialization or reset, the serial port state machine is initialized into command mode where it waits to receive a valid command (the first 8-bits clocked into the serial port). Upon receiving and decoding a valid command word the state machine instructs the converter to either perform a system operation, or transfer data to or from an internal register. The Command Word section can be used to decode all valid commands.

The state machine decodes the command word as it is received. The serial port enters data transfer mode if the MSB of the command word is logic 0 (B7 = 0). In data transfer mode, the internal registers are read from or written to. Command words instructing a register write must be followed by 24 bits of data. For instance, to write the configuration register, the user would transmit the command (0x40) to initiate the write. The ADC would then acquire the serial data input from the (SDI) pin when the user pulses the serial clock (SCLK) 24 times. Once the data is received the state machine would write the data to the configuration register and return to the command mode. Command words instructing a register read may be terminated at 8-bit boundaries (e.g., read transfers may be 8, 16, or 24 bits in length). Also data register reads allow "command chaining". For example, a command word instructs the state machine to read a signed output register. After the user pulses SCLK for 16-bits of data, a write command word (e.g., to clear the status register) may be pulsed on to the SDI line at the same time the remaining 8-bits of data are pulsed from the SDO line.

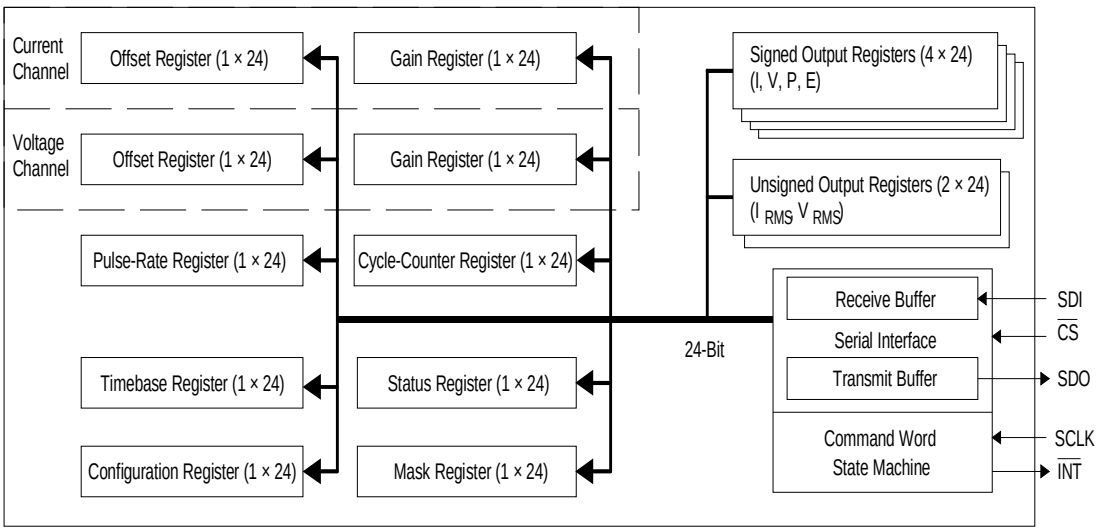


Figure 9. CS5460 Register Diagram

3.1 Command Word (Write Only)

All command words are always 1 byte in length. Commands that write to a register initiate 3 bytes of register data. Commands that read from registers must be followed by 1, 2, or 3 bytes of register read data. Commands that read data can be chained with other commands (e.g., while reading data, a new command can be sent to SDI which can execute before the original read is completed). This allows for “chaining” commands.

3.1.1 Start Conversions

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	0	C	0	0	0

This command indicates to the state machine to begin acquiring measurements and calculating results. The device has two modes of acquisition.

C Modes of measurement
0 = Perform a single computation cycle
1 = Perform continuous computation cycles

3.1.2 SYNC0 Command

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	1	1	1	1	0

This command is the end of the serial port re-initialization sequence. The command can also be used as a NOP command. The serial port is resynchronized to byte boundaries by sending three or more consecutive SYNC1 commands followed by a SYNC0 command.

3.1.3 SYNC1 Command

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	1	1	1	1	1

This command is part of the serial port re-initialization sequence. The command can also serve as a NOP command, but no more than three consecutive bytes should be transmitted.

3.1.4 Power-up/Halt Control

B7	B6	B5	B4	B3	B2	B1	B0
1	0	1	0	0	0	0	0

If the device is powered-down, this command will power-up the device. When powered-on, no computations will be running. If the part is already powered-on, all computations will be halted.

3.1.5 Power-down Control

B7	B6	B5	B4	B3	B2	B1	B0
1	0	0	S1	S0	0	0	0

The device has two power-down modes to conserve power. If the chip is put in stand-by mode all circuitry except the clock generator is turned off.

S1,S0 Power-down mode
00 = Reserved
01 = Halt and enter stand-by power saving mode. This mode allows quick power-on time
10 = Halt and enter sleep power saving mode. This mode requires a slow power-on time
11 = Reserved

3.1.6 Calibration Control

B7	B6	B5	B4	B3	B2	B1	B0
1	1	0	Cv	Ci	0	GC	OC

The device has the capability of performing a system offset and gain calibration. The user must supply the proper inputs to the device before proceeding with the calibration cycle.

Cv,Ci Designates calibration channel
00 = Not allowed
01 = Calibrate the current channel
10 = Calibrate the voltage channel
11 = Calibrate voltage and current channel simultaneously

GC Designates gain calibration
0 = Normal operation
1 = Perform gain calibration

OC Designates offset calibration
0 = Normal operation
1 = Perform offset calibration

3.1.7 Register Read/Write Command

B7	B6	B5	B4	B3	B2	B1	B0
0	W/$\overline{R}$	RA4	RA3	RA2	RA1	RA0	0

This command informs the state machine that a register access is required. On reads the addressed register is loaded into the output buffer and clocked out by SCLK. On writes the data is clocked into the input buffer and transferred to the addressed register on the 24th SCLK.

W/$\overline{R}$ Write/Read control
0 = Read register
1 = Write register

RA[4:0] Register address bits. Binary encoded 0 to 31. All registers are 24 bits in length.

Address	Name	Description
00000	Config	Configuration Register
00001	Ioff	Current offset calibration
00010	Ign	Current gain calibration
00011	Voff	Voltage offset calibration
00100	Vgn	Voltage gain calibration
00101	Cycle Count	Number of conversions to integrate over (N)
00110	Pulse-Rate	Used to calibrate/scale the energy to frequency output
00111	I	Last current value
01000	V	Last voltage value
01001	P	Last Power value
01010	E	Total energy value of last cycle
01011	I_{RMS}	RMS current value of last cycle
01100	V_{RMS}	RMS voltage value of last cycle
01101	TBC	Timebase Calibration
01110	Test	Internal Use only †
01111	Status	Status register
10000	Res	Reserved
.		
.		
10111	Res	Reserved
11000	Test	Internal Use only †
11001	Test	Internal Use Only †
11010	Mask	Interrupt mask register
11011	Test	Internal Use Only †
11100	Res	Reserved
.		
.		
11111	Res	Reserved

† These Registers are for Internal Use only and should not be written to. Accessing these registers will NOT generate an “Invalid Command” ($\overline{IC}$) bit in the Status Register.

3.2 Serial Port Interface

The CS5460's serial interface consists of four control lines: $\overline{CS}$, SDI, SDO, and SCLK.

$\overline{CS}$, Chip Select, is the control line which enables access to the serial port. If the $\overline{CS}$ pin is tied to logic 0, the port can function as a three wire interface. SDI, Serial Data In, is the data signal used to transfer data to the converters.

SDO, Serial Data Out, is the data signal used to transfer output data from the converters. The SDO output will be held at high impedance any time $\overline{CS}$ is at logic 1. Figure 10 illustrates the serial sequence necessary to write to, or read from the serial port's buffers.

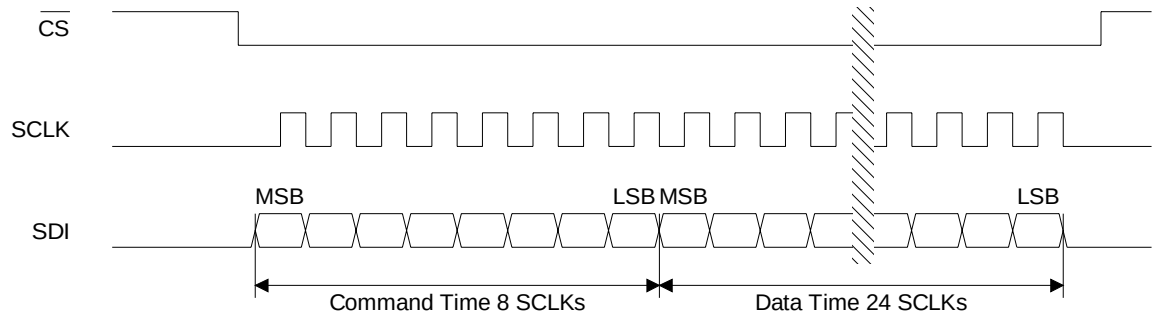
SCLK, Serial Clock, is the serial bit-clock which controls the shifting of data to or from the ADC's serial port. The $\overline{CS}$ pin must be held at logic 0 before SCLK transitions can be recognized by the port logic. To accommodate opto-isolators SCLK is designed with a Schmitt-trigger input to allow an opto-isolator with slower rise and fall times to directly drive the pin. Additionally, SDO is capable of sinking or sourcing up to 5 mA to directly drive an opto-isolator LED. SDO will have less than a 400 mV loss in the drive voltage when sinking or sourcing 5 mA.

As shown in Figure 10 a transfer of data is always initiated by sending the appropriate 8-bit command (MSB first) to the serial port (SDI pin). It is important to note that some commands use information from the cycle-counter and configuration registers to perform the function. For those commands it is important that the correct information is written to those registers first.

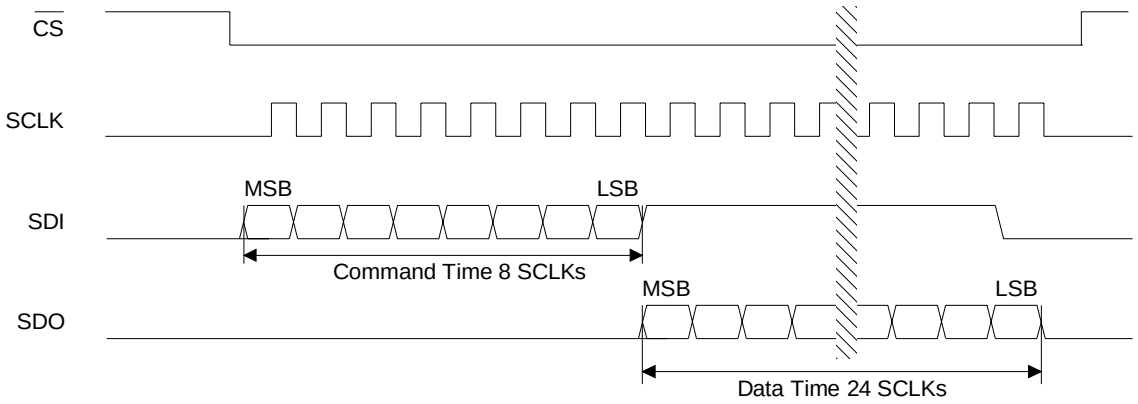
When a command involves a write operation the serial port will continue to clock in the data bits (MSB first) on the SDI pin for the next 24 SCLK cycles. When a read command is initiated the serial port will start transferring register content bit serial (MSB first) on the SDO pin for the next 8, 16, or 24 SCLK cycles depending on the command issued. The micro-controller is allowed to send a new command while reading register data. The new command will be acted upon immediately and could possibly terminate the register read. During the read cycle, the SYNC0 command (NOP) should be strobed on the SDI port while clocking the data from the SDO port.

3.3 Serial Port Initialization

The serial port is initialized to the command mode whenever a reset is performed or when the port initialization sequence is completed. The port initialization sequence involves clocking 3 (or more) SYNC1 command bytes (0xFF) followed by SYNC0 command byte (0xFE). This sequence places the chip in the command mode where it waits until a valid command is received.



Write Cycle



Read Cycle

Figure 10. Command and Data Word Timing

3.4 System Initialization

A software or hardware reset can be initiated at any time. The software reset is initiated by writing a logic 1 to the RS (Reset System) bit in the configuration register, which automatically returns to logic 0 after reset. At the end of the 32nd SCLK (i.e., 8 bit command word and 24 bit data word) internal synchronization delays the loading of the configuration register by 3 or 4 DCLK (MCLK/K). Then the reset circuit initiates the reset routine on the 1st falling edge of MCLK. A hardware reset is initiated when the $\overline{\text{RESET}}$ pin is forced low with a minimum pulse width of 50 ns. The $\overline{\text{RESET}}$ signal is asynchronous requiring no MCLKs for the part to detect and store a reset event. Once the $\overline{\text{RESET}}$ pin is inactive the internal reset circuitry remains active for 5 MCLK cycles to insure resetting the synchronous circuitry in the device. The modulators are held in reset for 12 MCLK cycles after $\overline{\text{RESET}}$ becomes inactive. The internal registers (some of which drive output pins) will be reset to their default values on the first MCLK received after detecting a reset event (see Table 2). After a reset, the on-chip registers are initialized to the following states and the converter is placed in the command mode where it waits for a valid command.

Configuration Register:	0x000001
Offset Register:	0x000000
Gain Registers	0x400000
Pulse-Rate Register:	0x0FA000
Cycle-Counter Register:	0x000FA0
Timebase Register:	0x800000
Status Register:	0x000001
Mask Register	0x000000
Signed Registers	0x000000
Unsigned Registers	0x000000

Table 2. Internal Registers Default Value

4. REGISTER DESCRIPTION

Notes: * "*RA[4:0]*" => register address bits in the Register Read/Write Command word
** "default" => bit status after reset

4.1 Configuration Register

Address: RA[4:0]* = 0x00

23	22	21	20	19	18	17	16
PC3	PC2	PC1	PC0	0	0	0	Gi
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EWA	PH1	PH0	SI1	SI0	EOD	DL1	DL0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RS	VHPF	IHPF	iCPU	K3	K2	K1	K0

Default** = 0x000001

K[3:0] Clock divider. A 4 bit binary number ranging from 0 to 15 used to divide the value of MCLK to generate the internal clock DCLK. The internal clock frequency of DCLK = MCLK/K. Valid values are 1,2, and 4.
0001 = divide by 1 (default)
0010 = divide by 2
0100 = divide by 4

iCPU Inverts the CPUCLK clock. In order to reduce the level of noise present when analog signals are sampled, the logic driven by CPUCLK should not be active during the sample edge.
0 = normal operation (default)
1 = minimize noise when CPUCLK is driving rising edge logic

IHPF Control the use of the High Pass Filter on the Current Channel.
0 = High-pass filter is disabled. If VHPF is set, use all-pass filter. Otherwise, no filter is used. (default)
1 = High-pass filter is enabled.

VHPF Control the use of the High Pass Filter on the voltage Channel.
0 = High-pass filter is disabled. If IHPF is set, use all-pass filter. Otherwise, no filter is used. (default)
1 = High-pass filter enabled

RS Start a chip reset cycle when set 1. The reset cycle lasts for less than 10 XIN cycles. The bit is automatically returned to 0 by the reset cycle.

DL0 When EOD = 1, $\overline{\text{EDIR}}$ becomes a user defined pin. DL0 sets the value of the $\overline{\text{EDIR}}$ pin.
Default = '0'

DL1 When EOD = 1, $\overline{\text{EOUT}}$ becomes a user defined pin. DL1 sets the value of the $\overline{\text{EOUT}}$ pin.
Default = '0'

EOD Allows the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins to be controlled by the DL0 and DL1 bits. $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ can also be accessed using the status register.
0 = Normal operation of the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins. (default)
1 = DL0 and DL1 bits control the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins.

SI[1:0] Soft interrupt configuration. Select the desired pin behavior for indication of an interrupt.
00 = active low level (default)

01 = active high level
10 = falling edge (INT is normally high)
11 = rising edge (INT is normally low)

PH[1:0] Set the phase of the EOUT and EDIR output pin pulse. The EOUT and EDIR pins, on different phases, can be wire-ORed together as a simple way of summing the frequency of different parts.
00 = phase 0 (default)
01 = phase 1
10 = phase 2
11 = phase 3

EWA Allows the output pins of EOUT and EDIR of multiple chips to be connected in a wire-AND, using an external pull-up device.
0 = normal outputs (default)
1 = only the pull-down device of the EOUT and EDIR pins are active

Gi Sets the gain of the current PGA
0 = gain is 10 (default)
1 = gain is 50

Res Reserved. These bits must be set to zero.

PC[3:0] Phase compensation. A 2's complement number used to set the delay in the voltage channel. The bigger the number, the greater the delay in the voltage. The phase adjustment range is about -2.4 to +2.5 degrees at 60Hz. Each step is about 0.34 degrees at 60Hz.
0000 = Zero degrees phase delay (default)

4.2 Current Offset Register and Voltage Offset Register

Address: RA[4:0]* = 0x01 (Current Offset Register)
RA[4:0]* = 0x03 (Voltage Offset Register)

MSB															LSB
SIGN	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	.....	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}

Default** = 0.000

The Offset Registers are initialized to zero on reset, allowing the device to function and perform measurements. The register is loaded after one cycle with the system offset when the proper input is applied and the Calibration Command is received. The register may be read and stored so the register may be restored with the desired system offset compensation. The value is in the range ± ½ full scale.

4.3 Current Gain Register and Voltage Gain Register

Address: RA[4:0]* = 0x02 (Current Gain Register)
RA[4:0]* = 0x04 (Voltage Gain Register)

MSB															LSB
2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	.....	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}

Default** = 1.000

The Gain Registers are initialized to 1.0 on reset, allowing the device to function and perform measurements. The register is loaded after one cycle with the system gain when the proper input is applied and the Calibration Command is received. The register may be read and stored so the register may be restored with the desired system offset compensation. The value is in the range $0.0 \leq \text{Gain} < 4.0$.

4.4 Cycle Count Register

Address: RA[4:0]* = 0x05

MSB															LSB
2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	.....	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Default** = 4000

The Cycle Count Register determines the length of an energy and RMS conversion. A conversion cycle is derived from (MCLK/K)/(1024∗N) where MCLK is master clock, K is clock divider, and N is cycle count. N must be greater than 10 for I_{RMS}, V_{RMS} and energy calculations to be performed.

4.5 Pulse-Rate Register

Address: RA[4:0]* = 0x06

MSB															LSB
2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	.....	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}

Default** = 32000.00Hz

The Pulse-Rate Register determines the frequency of the train of pulses output on the $\overline{EOUT}$ pin. Each $\overline{EOUT}$ pulse represents a predetermined magnitude of energy.The register's smallest valid value is 2^{-4} but can be in 2^{-5} increments.

4.6 I,V,P,E Signed Output Register Results

Address: RA[4:0]* = 0x07 - 0x0A

MSB															LSB
SIGN	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Access: Read Only

The Signed Registers contain the last value of the measured results of I, V, P, and E. The results are in the range of $-1.0 \le I, V, P, E < 1.0$. The value is represented in two's complement notation, with the binary point place to the right of the MSB (which is the sign bit). I, V, P, and E are output results registers which contain signed values.

4.7 I_{RMS}, V_{RMS} Unsigned Output Register Results

Address: RA[4:0]* = 0x0B - 0x0C

MSB															LSB
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	.....	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}

Access: Read Only

The Unsigned Registers contain the last value of the calculated results of I_{RMS} and V_{RMS}. The results are in the range of $0.0 \le I_{RMS}, V_{RMS} < 1.0$. The value is represented in binary notation, with the binary point place to the left of the MSB. I_{RMS} and V_{RMS} are output result registers which contain unsigned values.

4.8 Timebase Calibration

Address: RA[4:0]* = 0x0D

MSB															LSB
2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default** = 1.000

The Timebase Register is initialized to 1.0 on reset, allowing the device to function and perform computations. The register is user loaded with the clock frequency error to compensate for a gain error caused by the crystal/oscillator tolerance. The value is in the range $0.0 \leq TBC < 2.0$.

4.9 Status Register and Mask Register

Address: *RA[4:0]* = 0x0F* (Status Register)
RA[4:0] = 0x1A (Mask Register)*

23	22	21	20	19	18	17	16
DRDY	EOUT	EDIR	Res	MATH	Res	IOR	VOR
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWOR	IROR	VROR	EOR	EOOR	Res	Res	Res
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res	Res	WDT	VOD	IOD	LSD	0	$\overline{IC}$

Default** = 0x000001 (Status Register)

0x000000 (Mask Register)

The Status Register indicates the condition of the chip. In normal operation writing a '1' to a bit will cause the bit to go to the '0' state. Writing a '0' to a bit will maintain the status bit in its current state. With this feature the user can simply write back the status register to clear the bits that have been seen, without concern of clearing any newly set bits. Even if a status bit is masked to prevent the interrupt, the status bit will still be set in the status register so the user can poll the status.

The Mask Register is used to control the activation of the $\overline{INT}$ pin. Placing a logic '1' in the mask register will allow the corresponding bit in the status register to activate the $\overline{INT}$ pin when the status bit becomes active.

$\overline{IC}$ — Invalid Command. Normally logic 1. Set to logic 0 when the part is given an invalid command. Can be deactivated only by sending a port initialization sequence to the serial port. When writing to status register this bit is ignored.

LSD — Low Supply detect. Set when the PFMON pin falls below 2.5 volts with respect to the VA- pin.

IOD — Modulator oscillation detect on the current channel. Set when the modulator oscillates due to an input above Full Scale.

VOD — Modulator oscillation detect on the voltage channel. Set when the modulator oscillates due to an input above Full Scale.

WDT — Watch-Dog Timer. Set when there has been no reading of the Energy register for more than 5 seconds. (MCLK = 4.096 MHz, K = 1) To clear this bit, first read the Energy register, then write to the status register with this bit set to logic '1'.

EOOR — EOUT energy/current summing register went out of range. This can be caused by having an output rate that is too small for the power being measured. The problem can be corrected by specifying a higher frequency in the pulse-rate register.

EOR	Energy Out of Range. Set when the calibrated energy value is too large or too small to fit in the output word.
VROR	RMS Voltage Out of Range. Set when the calibrated RMS voltage value is too large to fit in the output word.
IROR	RMS Current Out of Range. Set when the calibrated RMS current value is too large to fit in the output word.
PWOR	Power Calculation Out of Range.
VOR	Voltage Out of Range. Set when the calibrated voltage value is too large or too small to fit in the output word.
IOR	Current Out of Range. Set when the calibrated current value is too large or too small to fit in the output word.
MATH	General computation error (e.g., divide by 0)
EDIR	Set when sum of energy is less than zero. Set or cleared at the same time as EOUT.
EOUT	Indicates that the energy limit has been reached for the energy to frequency conversion, and a pulse train will be generated on the EOUT pin (if enabled). This bit is cleared automatically when the energy rate drops below the level that produces a 4 KHz EOUT pin rate. The bit can also be cleared by writing to the status register. This status bit is set with a maximum frequency of 4 KHz (when MCLK/K is 4.096 MHz).
DRDY	Data Ready. Set at the end of a calibration or conversion cycle.

5. FUNCTIONAL DESCRIPTION

5.1 Interrupt and Watchdog Timer

5.1.1 Interrupt

The $\overline{\text{INT}}$ pin is used to indicate that an event has taken place in the converter that needs attention. These events inform the system about operation conditions and internal error conditions. The $\overline{\text{INT}}$ signal is created by combining the Status register with the Mask register. Whenever a bit in the Status register becomes active, and the corresponding bit in the Mask register is a logic 1, the $\overline{\text{INT}}$ signal becomes active. The interrupt condition is cleared when the bits of the status register are returned to their inactive state.

5.1.1.1 Clearing the Status Register

Unlike the other registers, the bits in the Status register can only be cleared (set to logic 0). When a word is written to the Status register, any 1s in the word will cause the corresponding bits in the Status register to be cleared. The other bits of the status register remain unchanged. This allows the clearing of particular bits in the register without having to know the state of the other bits. This mechanism is designed to facilitate handshaking and to minimize the risk of losing events that haven't been processed yet.

5.1.1.2 Typical use of the $\overline{\text{INT}}$ pin

The steps below show how interrupts can be handled.

Initialization:

Step I0 - All Status bits are cleared by writing FFFFFF (Hex) into the Status register.

Step I1 - The conditional bits which will be used to generate interrupts are then written to logic 1 in the Mask register.

Step I3 - Enable interrupts.

Interrupt Handler Routine:

Step H0 - Read the Status register.

Step H1 - Disable all interrupts.

Step H2 - Branch to the proper interrupt service routine.

Step H3 - Clear the Status register by writing back the value read in step H0.

Step H4 - Re-enable interrupts.

Step H5 - Return from interrupt service routine.

This handshaking procedure insures that any new interrupts activated between steps H0 and H3 are not lost (cleared) by step H3.

5.1.1.3 $\overline{\text{INT}}$ Active State

The behavior of the $\overline{\text{INT}}$ pin is controlled by the SI1 and SI0 bits of the configuration register. The pin can be active low (default), active high, active on a return to logic 0 (rising edge), or activate on a return to logic 1 (falling edge).

5.1.1.4 Exceptions

The $\overline{\text{IC}}$ (Invalid Command) bit of the Status register can only be cleared by performing the port initialization sequence. This is also the only Status register bit that is active low.

To properly clear the WDT (WatchDog Timer) bit of the Status register, one must first read the Energy register, then clear the bit in the status register.

5.1.2 Watch Dog Timer

The Watch Dog Timer (WDT) is provided as means of alerting the system that there is a potential breakdown in communication with the micro-controller. By allowing the WDT to cause an interrupt, a controller can be brought back, from some unknown code space, into the proper code for processing the data created by the converter. The time-out is preprogrammed to approximately 5 seconds. The countdown restarts each time the Energy register is read. Under typical situations, the Ener-

gy register is read every second. As a result, the WDT will not time out. Other applications, that want to use the watchdog timer, will need to ensure that the Energy register is read at least once in every 5 second span.

5.2 Oscillator Characteristics

XIN and XOUT are the input and output, respectively, of an inverting amplifier to provide oscillation and can be configured as an on-chip oscillator, as shown in Figure 11. The oscillator circuit is designed to work with a quartz crystal or a ceramic resonator. To reduce circuit cost two load capacitors C1 are integrated in the device, one between XIN and DGND, one between XOUT and DGND. Lead lengths should be minimized to reduce stray capacitance. With these load capacitors the oscillator circuit is capable of oscillation up to 20 MHz. To drive the device from an external clock source, XOUT should be left unconnected while XIN is driven by the external circuitry. There is an amplifier between XIN and the digital section which provides CMOS level signals. This amplifier works with sinusoidal inputs so there are no problems with slow edge times.

The CS5460 can be driven by a clock ranging from 2.5 to 20 MHz Table 2 shows the clock divide value K (default = 1) that the CS5460 needs to be programmed with for normal operation.

K	CLK (min) MHz	CLK (max) MHz
1	2.5	5
2	5	10
4	10	20

Table 3. CPU Clock (and K) Restrictions

5.3 Analog Inputs

The CS5460 accommodates a full scale range of 150 mV_{RMS} on both input channels. System calibration can be used to increase or decrease the full scale span of the converter as long as the calibration register values stay within the limits specified. See the *Calibration* section for more details.

The current input channel has an input range of 30 mV_{RMS} when the internal x50 gain stage is enabled. This signal range is designed to handle low level signals from a shunt sensor.

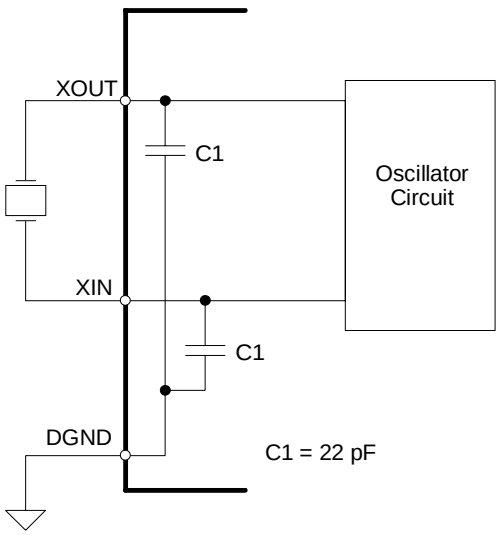


Figure 11. Oscillator Connection

5.4 Voltage Reference

The CS5460 is specified for operation with a +2.5 V reference between the VREFIN and VA- pins. The converter includes an internal 2.5 V reference (60 ppm/°C drift) that can be used by connecting the VREFOUT pin to the VREFIN pin of the device. If higher accuracy/stability is required, an external reference can be used.

5.5 Performing Calibrations

The CS5460 offers two DC calibration modes: system offset and system gain. For system calibration the user must supply the converter calibration signals which represent ground and full scale. The user must provide the positive full scale point to perform a system gain calibration and a ground referenced signal when a system offset is performed. The offset and gain signals must be within the specified calibration limits for each specific calibration step and channel. Since each converter channel has its own offset and gain register associated with it, system offset, or system gain can be performed on either channel without the calibration results from one channel corrupting the other.

The Cycle Count register N, determines the number of conversions averaged to obtain the calibration results. The larger N, the higher the accuracy of the calibration results. Once a calibration cycle is complete, DRDY is set and the results are stored in either the gain or offset register. Note that if additional calibrations are performed, the latest calibration results will replace the effects from the previous calibration. In any event, offset and gain calibration steps take one cycle each to complete.

After the part is reset, the device is functional and can perform measurements without being calibrated. The converters will utilize the initialized values of the on-chip registers (Gain = 1.0, Offset = 0.0) to calculate power information. Although the device can be used without performing an offset or gain calibration, any initial offset and gain errors in the internal circuitry of the chip will remain.

5.5.1 System Calibration

For the system calibration functions, the user must supply the converters calibration signals which represent ground and full scale. When a system offset calibration is performed, a ground reference signal must be applied to the converters. Figure 12 illustrates system offset calibration.

As shown in Figure 13, the user must input a signal representing the positive full scale point to perform a system gain calibration. In either case, the calibration signals must be within the specified calibration limits for each specific calibration step (refer to *Full Scale DC Calibration Range*).

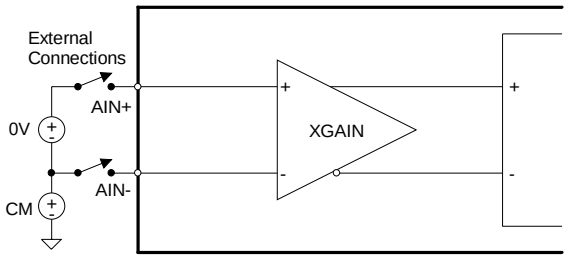


Figure 12. System Calibration of Offset.

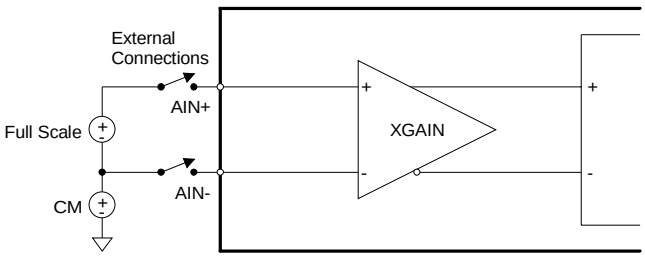


Figure 13. System Calibration of Gain.

5.5.2 Calibration Tips

To minimize digital noise near the device, the user should wait for each calibration step to be completed before reading or writing to the serial port.

After a calibration is performed, the offset and gain register contents can be read by the system micro-controller and recorded in memory. The same calibration words can be uploaded into the offset and gain registers of the converters when power is first applied to the system, or when the gain range on the current channel is changed.

An offset calibration must be performed before a gain calibration. Each gain calibration depends on the zero calibration point obtained from the offset calibration.

The offset and gain calibration steps each take one conversion cycle to complete. At the end of the calibration step, DRDY is set to indicate that the calibration is complete.

5.6 Input Current Protection

In Figure 3 and Figure 4, note the series resistor RP_I which is connected to the IIN+ input pin. This resistor is used to provide current-limit protection for the current-channel input pin in the event of a power surge or lightening surge. The voltage/current-channel inputs have surge-current limits of 100mA. This applies to brief voltage/current spikes (<500 msec). The limit is 10mA for DC input overload situations.

The VIN+ pin does not need a protection resistor for the configurations shown in Figure 3 and Figure 4. This is because a resistive voltage-divider is used as the sensor, and so series resistance is already provided to the VIN+ input pin. (If it was installed, it would be called RP_V). If the negative sides of the CS5460 input channels are not grounded (i.e., if VIN- and IIN- are connected in a differential configuration) then it is appropriate to put protection resistors on these inputs as well.

Capacitors CP_V and CP_I should be included to provide for attenuation of high-frequency noise that may be coupled into the input lines. In differential input configurations, such a capacitor should be added to the VIN- and IIN- pins in addition to the VIN+ and IIN+ pins.

Values for $RP_{V/I}$ and $CP_{V/I}$ must be chosen with the approximate input lowpass cutoff frequency in mind. In general, the cutoff frequency should not be less than 10 times the roll-off frequencies of the internal voltage/current channel filters (see Figure 6 and Figure 7). From these figures we see that the internal voltage channel roll-off is at ~1400Hz while the current channel roll-off is at ~1600Hz. If the cutoff frequency of the external protection is much less than 10x these values (14000Hz and 16000Hz), then some of the harmonic content in the power signal may start to get attenuated by this input filtering, which is undesirable.

The exact values of $RP_{V/I}$ and $CP_{V/I}$ must be calculated for each particular application. *The primary goal is to make sure that the input pins never receive transient input currents greater than 100mA. Also, they should never be exposed to DC currents greater than 10mA.* The user-supplied protection resistors RP_V and RP_I will limit the current that comes into the pins in over-voltage--where the internal protection diodes turn on inside the CS5460. For example, suppose that the value for RP_I (on the current channel input) was chosen to be 500 Ohms. Then we know that the current channel can withstand brief voltage spikes of up to ~50V (referenced to GND) without damage to the part. This is because 50V / 500Ohm = 100mA. We can also say that the pin can withstand a common mode DC voltage of up to 5V.

When computing appropriate values for $RP_{V/I}$, the differential input impedance of the CS5460's voltage channel and current channel should also be considered. This is especially true for the current channel, which has a lower differential input im-

pedance than the voltage channel. These impedance specs are given at the beginning of this data sheet (see the specification titled "Effective Input Impedance" for the voltage and current channels). For example, the differential input impedance in the current channel is spec'd to be 30 kOhm. As the user increases the value of RP_I to provide for more and more common-mode surge protection, the voltage drop across the external protection resistor increases, and it divides the input signal down more and more. This in turn reduces the dynamic range of the signals that are ultimately presented to the CS5460's inputs. As an example, suppose that the user creates a current-sensor configuration that provides a differential voltage of 150mV (RMS) across shunt resistor R_S at maximum line-current level. However, the user has set RP_I to 500 Ohms. This means that when there is 150mV across the shunt resistor (R_S), the voltage across the IIN+ and IIN- inputs is actually 150mV * [30K / (500 + 30K)] = ~148mV (RMS). We see that this has decreased the maximum signal input level. To avoid this voltage division, the user should first consider the input protection that is going to be necessary, and then calculate the sensor gains such that the drop across the protection resistors is taken into account.

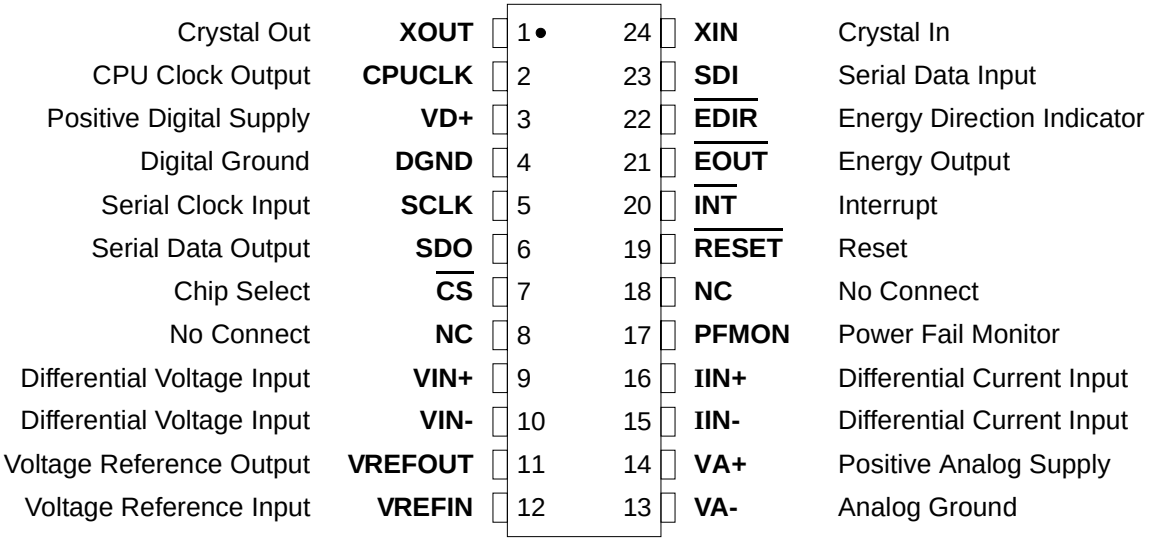
Typical values for these components are RP_I = 500 Ohm, CP_I = 0.02uF, CP_V = 0.002uF and if necessary, RP_V = 5 KOhm.

5.7 PCB Layout

The CS5460 should be placed entirely over an analog ground plane with both the VA- and DGND pins of the device connected to the analog plane. Place the analog-digital plane split immediately adjacent to the digital portion of the chip.

Note: See the CDB5460 data sheet for suggested layout details and Applications Note 18 for more detailed layout guidelines. Before layout, please call for our Free Schematic Review Service.

6. PIN DESCRIPTION



Clock Generator		
Crystal Out **Crystal In**	1,24	**XOUT, XIN** - A gate inside the chip is connected to these pins and can be used with a crystal to provide the system clock for the device. Alternatively, an external (CMOS compatible clock) can be supplied into XIN pin to provide the system clock for the device.
CPU Clock Output	2	**CPUCLK** - Output of on-chip oscillator which can drive one standard CMOS load.
Control Pins and Serial Data I/O		
SCLK	5	**Serial Clock Input -** A clock signal on this pin determines the input and output rate of the data for the SDI and SDO pins respectively. This input is a Schmitt trigger to allow for slow rise time signals. The SCLK pin will recognize clocks only when $\overline{CS}$ is low.
SDO	6	**Serial Data Output -** SDO is the output pin of the serial data port. Its output will be in a high impedance state when $\overline{CS}$ is high.
CS	7	**Chip Select -** When active low, the port will recognize SCLK. An active high on this pins puts the SDO pin in a high impedance state. $\overline{CS}$ should be changed when SCLK is low.
INT	20	**Interrupt -** When $\overline{INT}$ goes low it signals that an enabled event has occurred. $\overline{INT}$ is cleared (logic 1) by writing the appropriate command to the CS5460.
EOUT	21	**Energy Output -** The energy output pin output a fixed-width pulse rate output with a rate (programmable) proportional to energy.
EDIR	22	The energy direction indicator indicates if the measured energy is negative.
SDI	23	**Energy Direction Indicator - Serial Data Input -** SDI is the input pin of the serial data port. Data will be input at a rate determined by SCLK.
Measurement and Reference Input		
Differential Voltage Inputs	9,10	**VIN+, VIN- -** Differential analog input pins for voltage channel.
Voltage Reference Output	11	**VREFOUT -** The on-chip voltage reference is output from this pin. The voltage reference has a nominal magnitude of 2.5 V and is reference to the VA- pin on the converter.
Voltage Reference Input	12	**VREFIN -** The voltage input to this pin establishes the voltage reference for the on-chip modulator.

Differential Current Inputs	15,16	**IIN+, IIN- -** Differential analog input pins for current channel.
Power Supply Connections		
Positive Digital Supply	3	**VD+ -** The positive digital supply is nominally +5 V ±10% relative to DGND.
Digital Ground	4	**DGND -** The digital ground is at the same level as VA-.
Negative Analog Supply	13	**VA- -** The negative analog supply pin must be at the lowest potential.
Positive Analog Supply	14	**VA+ -** The positive analog supply is nominally +5 V ±10% relative to VA-.
Power Fail Monitor	17	**PFMON -** The power fail Monitor pin monitors the analog supply. Typical threshold level is 2.5 V with respect to the VA- pin.
$\overline{\text{RESET}}$	19	**Reset -** When reset is taken low, all internal registers are set to their default states.
Other		
No Connection	8,18	**NC -** No connection. Pins should be left floating.

7. SPECIFICATION DEFINITIONS

Full Scale Error

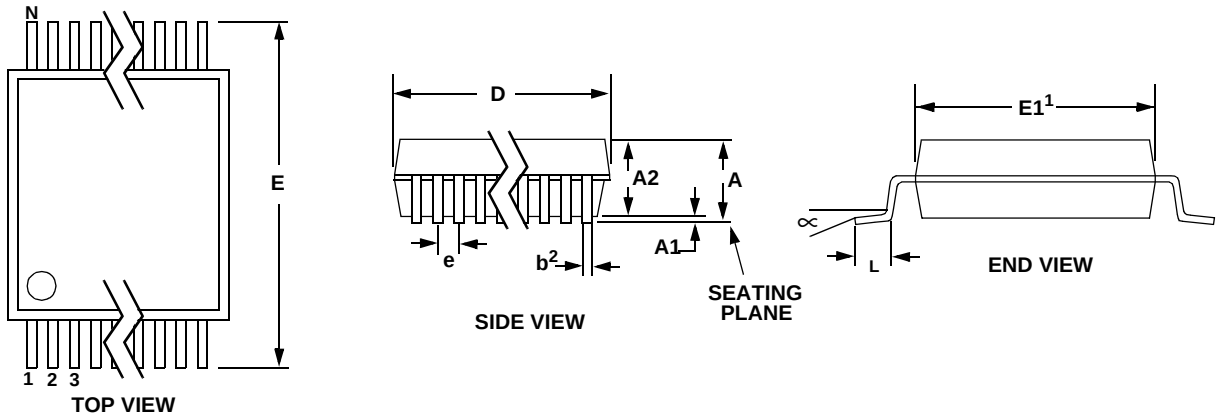
The deviation of the last code transition from the ideal [{(VREFIN) - (VA-)} - 3/2 LSB]. Units are in LSBs.

Bipolar Offset

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal (1/2 LSB below the voltage on the VIN- or IIN- pin). Units are in LSBs.

8. PACKAGE DIMENSIONS

24L SSOP PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.084	--	--	2.13	
A1	0.002	0.006	0.010	0.05	0.13	0.25	
A2	0.064	0.069	0.074	1.62	1.75	1.88	
b	0.009	--	0.015	0.22	--	0.38	2,3
D	0.311	0.323	0.335	7.90	8.20	8.50	1
E	0.291	0.307	0.323	7.40	7.80	8.20	
E1	0.197	0.209	0.220	5.00	5.30	5.60	1
e	0.022	0.026	0.030	0.55	0.65	0.75	
L	0.025	0.0354	0.041	0.63	0.90	1.03	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-150

Notes: 1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.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